



**THE DATASHEET OF
74ALVT162827DGG**





74ALVT162827

20-bit buffer/line driver; non-inverting; with 30 Ω termination resistors; 3-state

Rev. 4 — 25 June 2024

Product data sheet

1. General description

The 74ALVT162827 is a 20-bit buffer/line driver with 30 Ω termination resistors and 3-state outputs.

The device can be used as two 10-bit buffers or one 20-bit buffer. The device features output enable ($\overline{OE}1$ and $\overline{OE}2$) inputs, each controlling 10-bits. A HIGH on either $\overline{OE}1$ or $\overline{OE}2$ causes the outputs to assume a high-impedance OFF-state. Bus hold data inputs eliminate the need for external pull-up resistors to define unused inputs.

2. Features and benefits

- Wide supply voltage range from 2.3 V to 3.6 V
- Overvoltage tolerant inputs to 5.5 V
- BiCMOS high speed and output drive
- Direct interface with TTL levels
- Bus hold on data inputs
- No bus current loading when output is tied to 5 V bus
- Power-up 3-state
- I_{OFF} circuitry provides partial Power-down mode operation
- Latch-up performance exceeds 500 mA per JESD 78 Class II Level B
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to 85 °C

3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|---------------------------------|-------------------|---------|--|--------------------------|
| | Temperature range | Name | Description | Version |
| 74ALVT162827DGG | -40 °C to +85 °C | TSSOP56 | plastic thin shrink small outline package; 56 leads; body width 6.1 mm | SOT364-1 |

4. Functional diagram

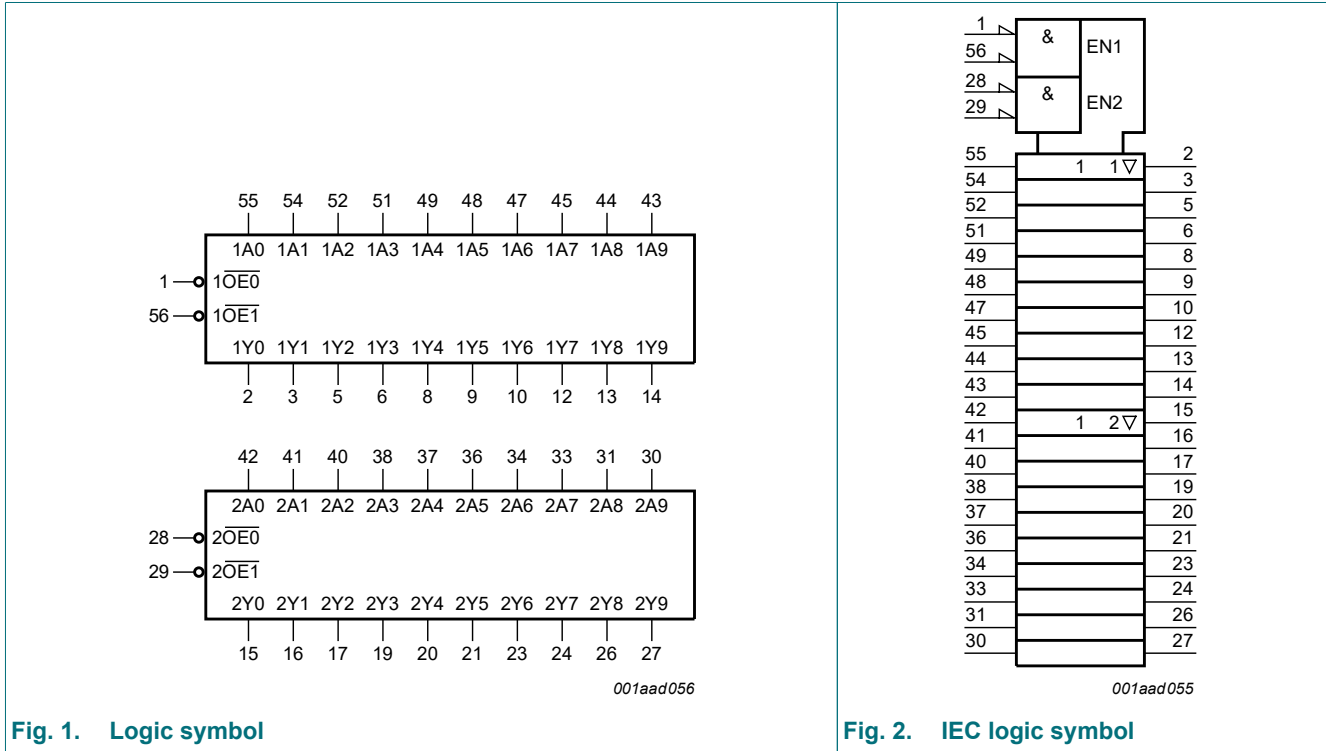


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

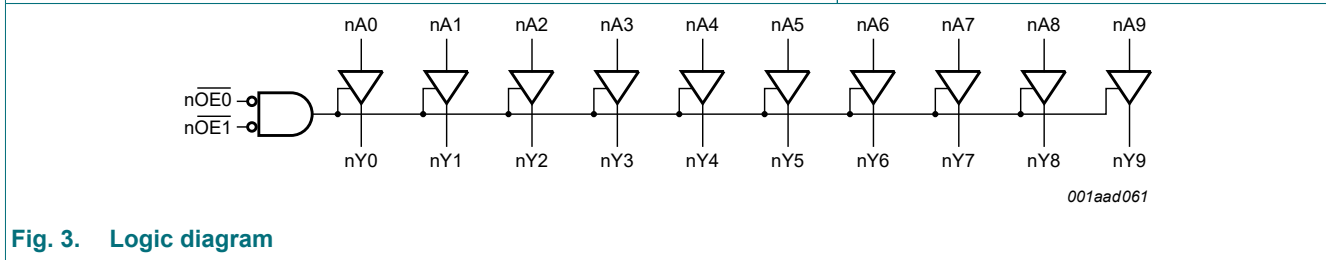


Fig. 3. Logic diagram

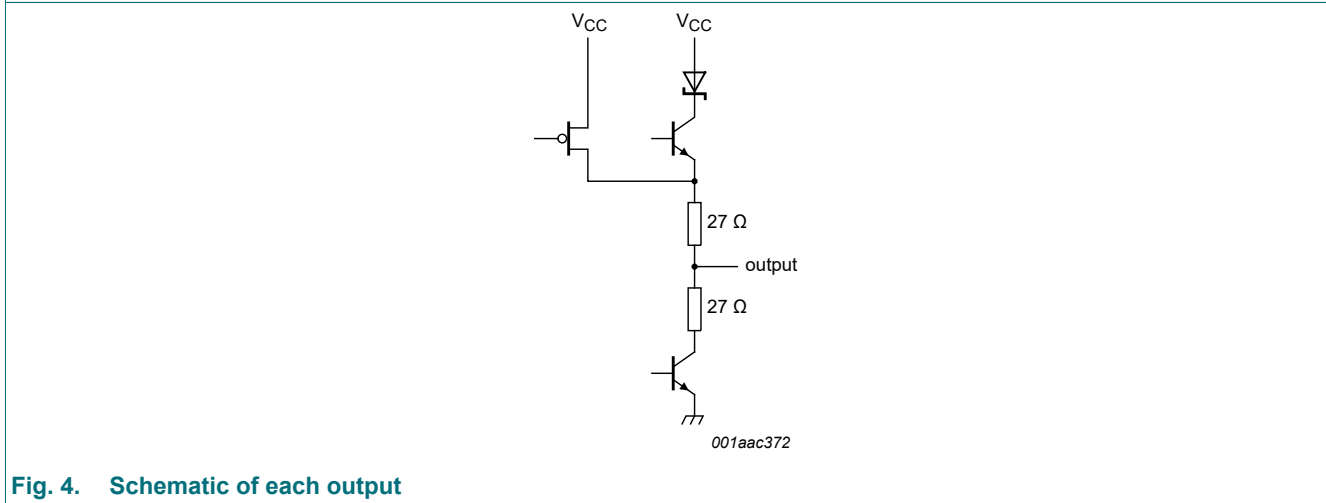
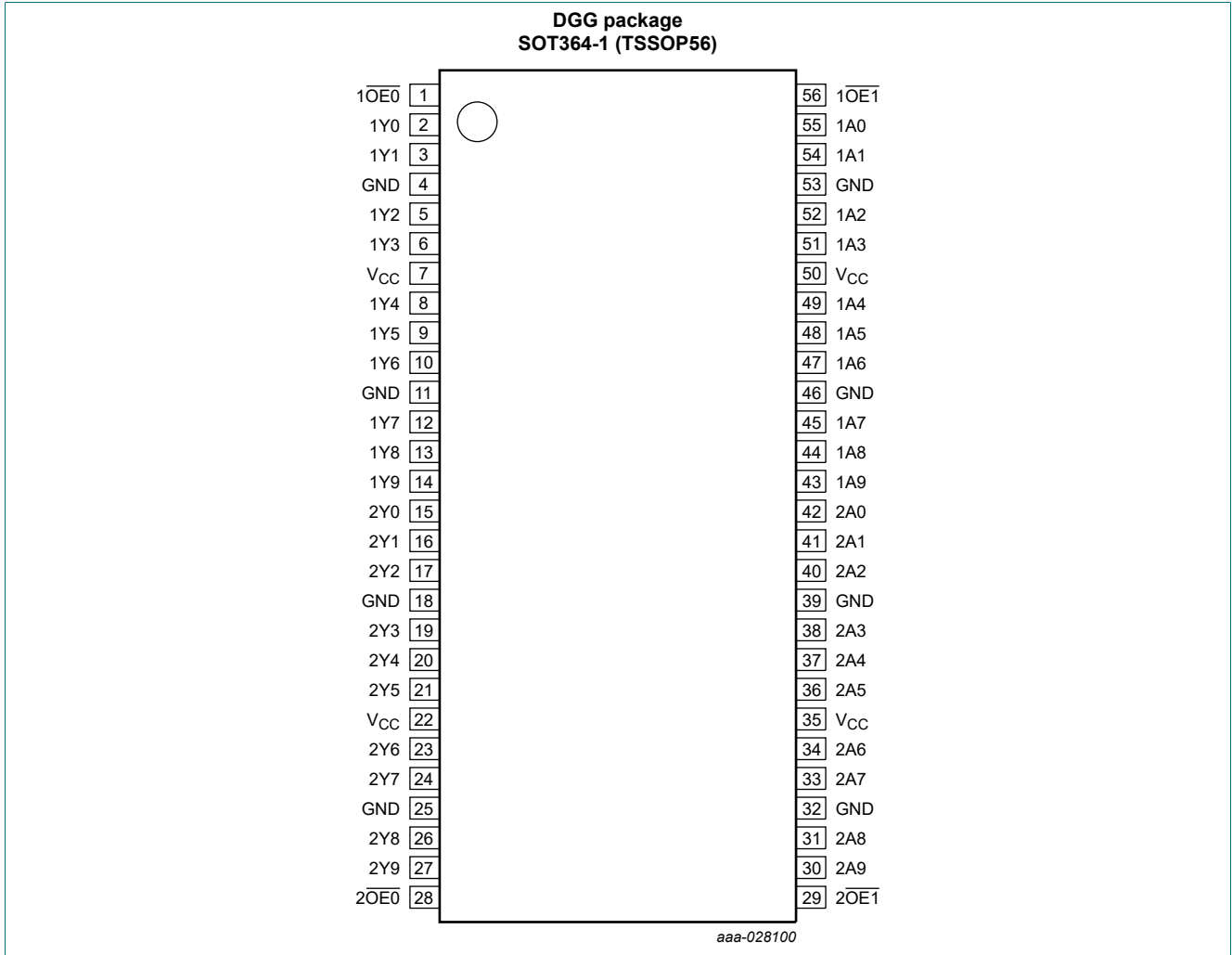


Fig. 4. Schematic of each output

5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|--|--|-----------------------------------|
| 1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7, 1A8, 1A9 | 55, 54, 52, 51, 49, 48, 47, 45, 44, 43 | data input |
| 2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7, 2A8, 2A9 | 42, 41, 40, 38, 37, 36, 34, 33, 31, 30 | data input |
| 1Y0, 1Y1, 1Y2, 1Y3, 1Y4, 1Y5, 1Y6, 1Y7, 1Y8, 1Y9 | 2, 3, 5, 6, 8, 9, 10, 12, 13, 14 | data output |
| 2Y0, 2Y1, 2Y2, 2Y3, 2Y4, 2Y5, 2Y6, 2Y7, 2Y8, 2Y9 | 15, 16, 17, 19, 20, 21, 23, 24, 26, 27 | data output |
| 1OE0, 1OE1, 2OE0, 2OE1 | 1, 56, 28, 29 | output enable inputs (active-LOW) |
| GND | 4, 11, 18, 25, 32, 39, 46, 53 | ground (0 V) |
| V _{CC} | 7, 22, 35, 50 | positive voltage supply |

6. Functional description

Table 3. Function table

X = don't care; Z = High-impedance OFF-state; H = HIGH voltage level; L = LOW voltage level.

| Operating mode | Input | | Output |
|----------------|-------|-----|--------|
| | nOEn | nAn | nYn |
| transparent | L | L | L |
| transparent | L | H | H |
| High-impedance | H | X | Z |

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|------------------|-------------------------|-----------------------------|----------|------|------|
| V _{CC} | supply voltage | | -0.5 | +7.0 | V |
| V _I | input voltage | | [1] -1.2 | +7.0 | V |
| V _O | output voltage | output in OFF or HIGH-state | [1] -0.5 | +5.5 | V |
| I _{IK} | input clamping current | V _I < 0 V | -18 | - | mA |
| I _{OK} | output clamping current | V _O < 0 V | -50 | - | mA |
| I _O | output current | output in LOW-state | - | 128 | mA |
| T _j | junction temperature | | [2] - | +150 | °C |
| T _{stg} | storage temperature | | -65 | +150 | °C |

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

8. Recommended operating conditions

Table 5. Recommended operating conditions

| Symbol | Parameter | Conditions | V _{CC} = 2.5 V ± 0.2 V | | V _{CC} = 3.3 V ± 0.3 V | | Unit |
|------------------|-------------------------------------|-----------------|---------------------------------|-----|---------------------------------|-----|------|
| | | | Min | Max | Min | Max | |
| V _{CC} | supply voltage | | 2.3 | 2.7 | 3.0 | 3.6 | V |
| V _I | input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| I _{OH} | HIGH-level output current | | - | -8 | - | -12 | mA |
| I _{OL} | LOW-level output current | | - | 12 | - | 12 | mA |
| Δt/ΔV | input transition rise and fall rate | outputs enabled | - | 10 | - | 10 | ns/V |
| T _{amb} | ambient temperature | free air | -40 | +85 | -40 | +85 | °C |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; $T_{amb} = -40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$; voltages are referred to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|--|------------------------------------|---|-----|--------|-----------|---------------|
| $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | | | | | |
| V_{IK} | input clamping voltage | $V_{CC} = 2.3\text{ V}$; $I_{IK} = -18\text{ mA}$ | - | -0.85 | -1.2 | V |
| V_{IH} | HIGH-level input voltage | | 1.7 | - | - | V |
| V_{IL} | LOW-level input voltage | | - | - | 0.7 | V |
| V_{OH} | HIGH-level output voltage | $V_{CC} = 2.3\text{ V}$; $I_O = -8\text{ mA}$ | 1.7 | 2.3 | - | V |
| V_{OL} | LOW-level output voltage | $V_{CC} = 2.3\text{ V}$; $I_O = 12\text{ mA}$ | - | 0.5 | 0.7 | V |
| I_I | input leakage current | control pins | | | | |
| | | $V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$ or GND | - | 0.1 | ± 1 | μA |
| | | $V_{CC} = 0\text{ V}$ or 2.7 V ; $V_I = 5.5\text{ V}$ | - | 0.1 | 10 | μA |
| | | data pins [2] | | | | |
| | | $V_{CC} = 2.7\text{ V}$; $V_I = V_{CC}$ | - | 0.1 | 1 | μA |
| | | $V_{CC} = 2.7\text{ V}$; $V_I = 0\text{ V}$ | - | 0.1 | -5 | μA |
| I_{OFF} | power-off leakage current | $V_{CC} = 0\text{ V}$; V_I or $V_O = 0\text{ V}$ to 4.5 V | - | 0.1 | ± 100 | μA |
| I_{BHL} | bus hold LOW current | $V_{CC} = 2.3\text{ V}$; $V_I = 0.7\text{ V}$ [3] | - | 115 | - | μA |
| I_{BHH} | bus hold HIGH current | $V_{CC} = 2.3\text{ V}$; $V_I = 1.7\text{ V}$ [3] | - | -10 | - | μA |
| I_{EX} | external current | output in HIGH-state when $V_O > V_{CC}$; $V_O = 5.5\text{ V}$; $V_{CC} = 2.3\text{ V}$ | - | 10 | 125 | μA |
| $I_{O(pu/pd)}$ | power-up/power-down output current | $V_{CC} \leq 1.2\text{ V}$; $V_O = 0.5\text{ V}$ to V_{CC} ; $V_I = \text{GND}$ or V_{CC} ; $n\overline{OE}n = \text{don't care}$ [4] | - | 1 | 100 | μA |
| I_{OZ} | OFF-state output current | $V_{CC} = 2.7\text{ V}$; $V_I = V_{IL}$ or V_{IH} | | | | |
| | | output HIGH; $V_O = 2.3\text{ V}$ | - | 0.5 | 5 | μA |
| | | output LOW; $V_O = 0.5\text{ V}$ | - | 0.5 | -5 | μA |
| I_{CC} | supply current | $V_{CC} = 2.7\text{ V}$; $V_I = \text{GND}$ or V_{CC} ; $I_O = 0\text{ A}$ | | | | |
| | | outputs HIGH | - | 0.04 | 0.1 | mA |
| | | outputs LOW | - | 3.5 | 5.0 | mA |
| | | outputs disabled [5] | - | 0.04 | 0.1 | mA |
| ΔI_{CC} | additional supply current | per input pin; $V_{CC} = 2.3\text{ V}$ to 2.7 V ; one input at $V_{CC} - 0.6\text{ V}$; other inputs at V_{CC} or GND [6] | - | 0.04 | 0.4 | mA |
| C_I | input capacitance | $V_I = 0\text{ V}$ or V_{CC} | - | 3 | - | pF |
| C_O | output capacitance | $V_O = 0\text{ V}$ or V_{CC} | - | 9 | - | pF |

20-bit buffer/line driver; non-inverting; with 30 Ω termination resistors; 3-state

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|---------------------------------------|------------------------------------|--|------|--------|------|------|
| V_{CC} = 3.3 V ± 0.3 V | | | | | | |
| V _{IK} | input clamping voltage | V _{CC} = 3.0 V; I _{IK} = -18 mA | - | -0.85 | -1.2 | V |
| V _{IH} | HIGH-level input voltage | | 2.0 | - | - | V |
| V _{IL} | LOW-level input voltage | | - | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _{CC} = 3.0 V; I _O = -12 mA | 2.0 | 2.3 | - | V |
| V _{OL} | LOW-level output voltage | V _{CC} = 3.0 V; I _O = 12 mA | - | 0.5 | 0.8 | V |
| I _I | input leakage current | control pins | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} or GND | - | 0.1 | ±1 | μA |
| | | V _{CC} = 0 V or 3.6 V; V _I = 5.5 V | - | 0.1 | 10 | μA |
| | | data pins [2] | | | | |
| | | V _{CC} = 3.6 V; V _I = V _{CC} | - | 0.5 | 1 | μA |
| | | V _{CC} = 3.6 V; V _I = 0 V | - | 0.1 | -5 | μA |
| I _{OFF} | power-off leakage current | V _{CC} = 0 V; V _I or V _O = 0 V to 4.5 V | - | 0.1 | ±100 | μA |
| I _{BHL} | bus hold LOW current | data inputs; V _{CC} = 3 V; V _I = 0.8 V | 75 | 130 | - | μA |
| I _{BHH} | bus hold HIGH current | data inputs; V _{CC} = 3 V; V _I = 2.0 V | -75 | -140 | - | μA |
| I _{BHLO} | bus hold LOW overdrive current | data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [7] | 500 | - | - | μA |
| I _{BHHO} | bus hold HIGH overdrive current | data inputs; V _{CC} = 3.6 V; V _I = 0 V to 3.6 V [7] | -500 | - | - | μA |
| I _{EX} | external current | output in HIGH-state when V _O > V _{CC} ; V _O = 5.5 V; V _{CC} = 3.0 V | - | 10 | 125 | μA |
| I _{O(pu/pd)} | power-up/power-down output current | V _{CC} ≤ 1.2 V; V _O = 0.5 V to V _{CC} ; V _I = GND or V _{CC} ; n _{OEN} = don't care [8] | - | 1 | ±100 | μA |
| I _{OZ} | OFF-state output current | V _{CC} = 3.6 V; V _I = V _{IL} or V _{IH} | | | | |
| | | output HIGH; V _O = 3.0 V | - | 0.5 | 5 | μA |
| | | output LOW; V _O = 0.5 V | - | 0.5 | -5 | μA |
| I _{CC} | supply current | V _{CC} = 3.6 V; V _I = GND or V _{CC} ; I _O = 0 A | | | | |
| | | outputs HIGH | - | 0.07 | 0.1 | mA |
| | | outputs LOW | - | 3.9 | 5.5 | mA |
| | | outputs disabled [5] | - | 0.07 | 0.1 | mA |
| ΔI _{CC} | additional supply current | per input pin; V _{CC} = 3 V to 3.6 V; one input at V _{CC} - 0.6 V; other inputs at V _{CC} or GND [6] | - | 0.04 | 0.4 | mA |
| C _I | input capacitance | V _I = 0 V or V _{CC} | - | 3 | - | pF |
| C _O | output capacitance | V _O = 0 V or V _{CC} | - | 9 | - | pF |

- [1] All typical values for V_{CC} = 2.5 V ± 0.2 V are measured at V_{CC} = 2.5 V and T_{amb} = 25 °C.
All typical values for V_{CC} = 3.3 V ± 0.3 V are measured at V_{CC} = 3.3 V and T_{amb} = 25 °C.
- [2] Unused pins at V_{CC} or GND.
- [3] Not guaranteed.
- [4] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 2.5 V ± 0.2 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.
- [5] I_{CC} with outputs disabled is measured with outputs pulled to V_{CC} or GND.
- [6] This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND.
- [7] This is the bus hold overdrive current required to force the input to the opposite logic state.
- [8] This parameter is valid for any V_{CC} between 0 V and 1.2 V with a transition time of up to 10 ms.
From V_{CC} = 1.2 V to V_{CC} = 3.3 V ± 0.3 V a transition time of 100 μs is permitted. This parameter is valid for T_{amb} = 25 °C only.

10. Dynamic characteristics

Table 7. Dynamic characteristics

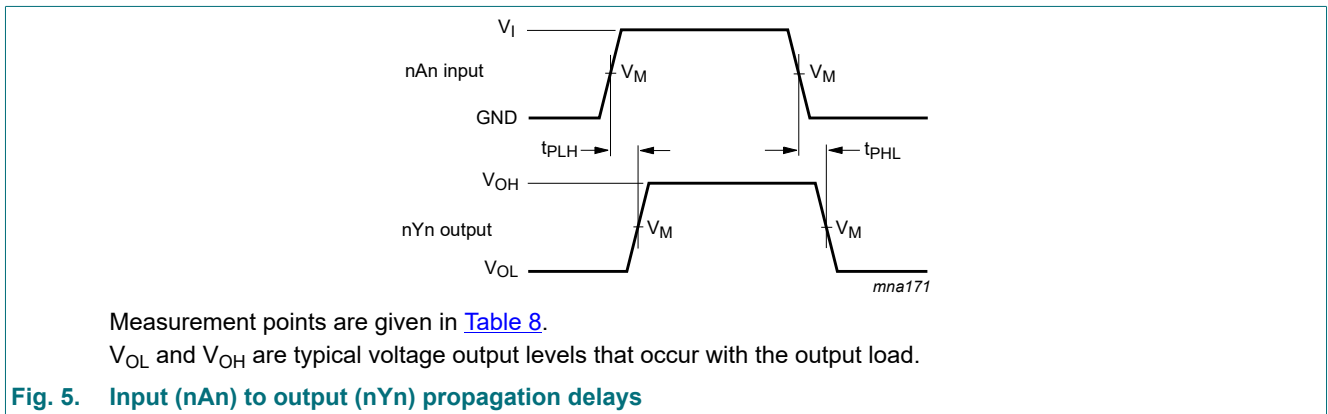
At recommended operating conditions; $T_{amb} = -40\text{ °C}$ to $+85\text{ °C}$;

Voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 7.

| Symbol | Parameter | Conditions | Min | Typ[1] | Max | Unit |
|--|-------------------------------------|--------------------------------------|-----|--------|-----|------|
| $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ | | | | | | |
| t_{PLH} | LOW to HIGH propagation delay | nAn to nYn; see Fig. 5 | 1.5 | 2.7 | 4.5 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nAn to nYn; see Fig. 5 | 1.5 | 2.3 | 3.5 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 2.5 | 4.7 | 7.5 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.5 | 2.9 | 4.7 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.5 | 3.2 | 5.2 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.0 | 2.4 | 4.0 | ns |
| $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | | | | | |
| t_{PLH} | LOW to HIGH propagation delay | nAn to nYn; see Fig. 5 | 1.0 | 2.2 | 3.3 | ns |
| t_{PHL} | HIGH to LOW propagation delay | nAn to nYn; see Fig. 5 | 1.0 | 2.0 | 3.0 | ns |
| t_{PZH} | OFF-state to HIGH propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.5 | 3.4 | 5.6 | ns |
| t_{PZL} | OFF-state to LOW propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.0 | 2.4 | 3.7 | ns |
| t_{PHZ} | HIGH to OFF-state propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.5 | 3.4 | 5.2 | ns |
| t_{PLZ} | LOW to OFF-state propagation delay | \overline{nOEn} to nYn; see Fig. 6 | 1.0 | 2.7 | 4.5 | ns |

- [1] All typical values for $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ are measured at $V_{CC} = 2.5\text{ V}$ and $T_{amb} = 25\text{ °C}$.
 All typical values for $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ are measured at $V_{CC} = 3.3\text{ V}$ and $T_{amb} = 25\text{ °C}$.

10.1. Waveforms and test circuit



20-bit buffer/line driver; non-inverting; with 30 Ω termination resistors; 3-state

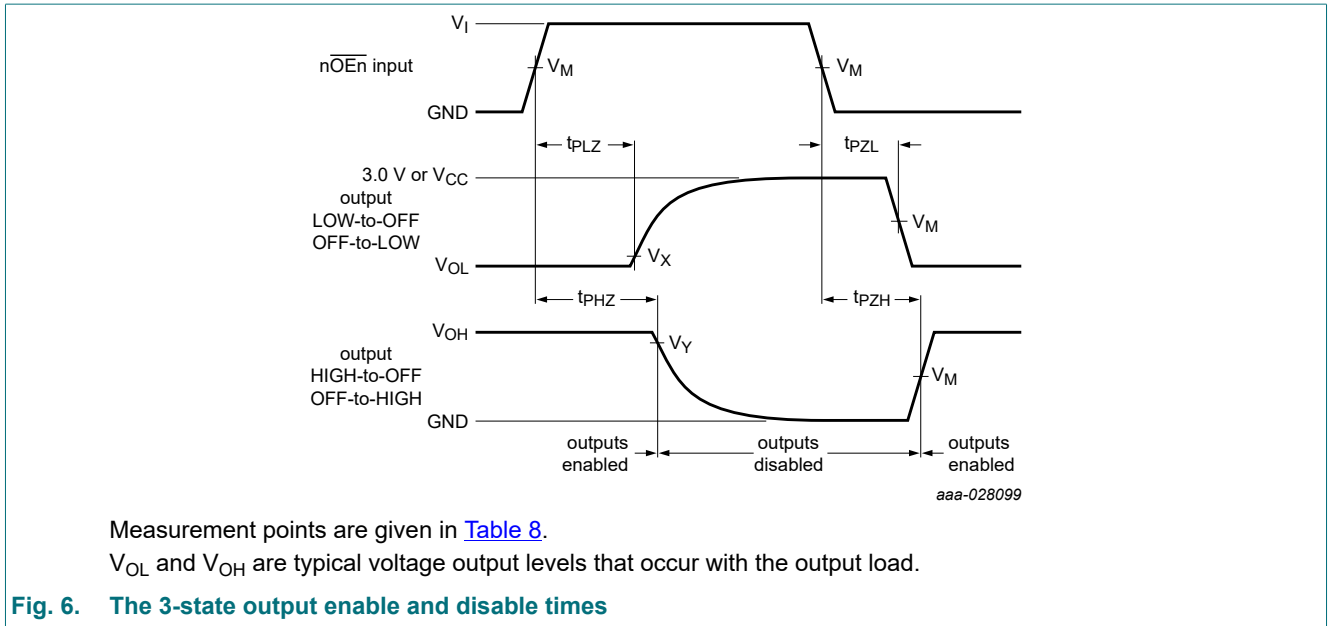


Table 8. Measurement points

| V_{CC} | Input | | Output | | |
|-----------------------------|----------|---------------------|---------------------|---------------------------|---------------------------|
| | V_I | V_M | V_M | V_X | V_Y |
| $V_{CC} \leq 2.7 \text{ V}$ | V_{CC} | $0.5 \times V_{CC}$ | $0.5 \times V_{CC}$ | $V_{OL} + 0.15 \text{ V}$ | $V_{OH} - 0.15 \text{ V}$ |
| $V_{CC} \geq 3.0 \text{ V}$ | 3.0 V | 1.5 V | 1.5 V | $V_{OL} + 0.3 \text{ V}$ | $V_{OH} - 0.3 \text{ V}$ |

20-bit buffer/line driver; non-inverting; with 30 Ω termination resistors; 3-state

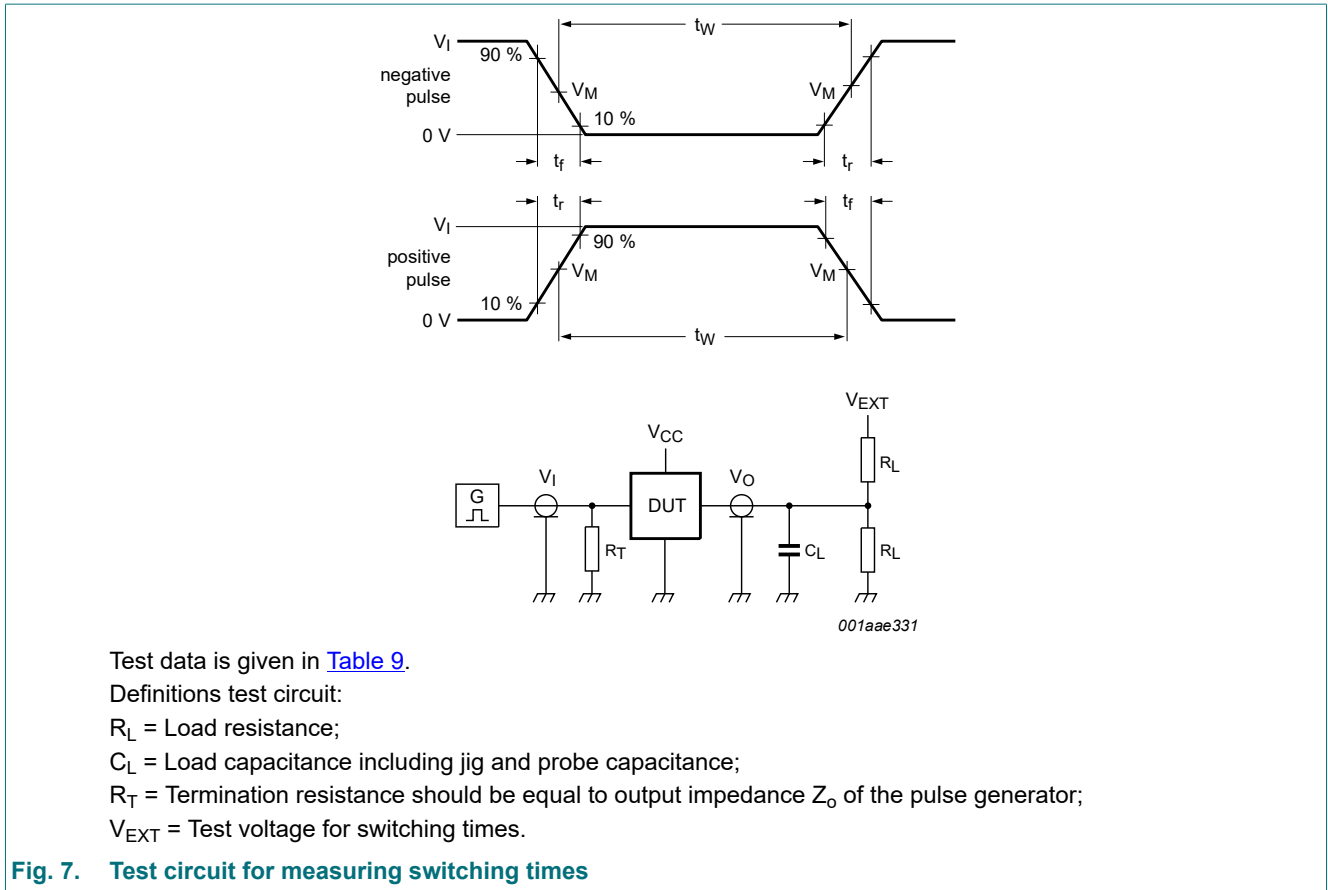


Fig. 7. Test circuit for measuring switching times

Table 9. Test data

| Input | | | | Load | | V_{EXT} | | |
|-------------------------------------|---------------|--------|---------------|-------|-------|--------------------|--------------------------|--------------------|
| V_I | f_i | t_w | t_r, t_f | C_L | R_L | t_{PHZ}, t_{PZH} | t_{PLZ}, t_{PZL} | t_{PLH}, t_{PHL} |
| 3.0 V or V_{CC} whichever is less | ≤ 10 MHz | 500 ns | ≤ 2.5 ns | 50 pF | 500 Ω | GND | 6 V or $V_{CC} \times 2$ | open |

11. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

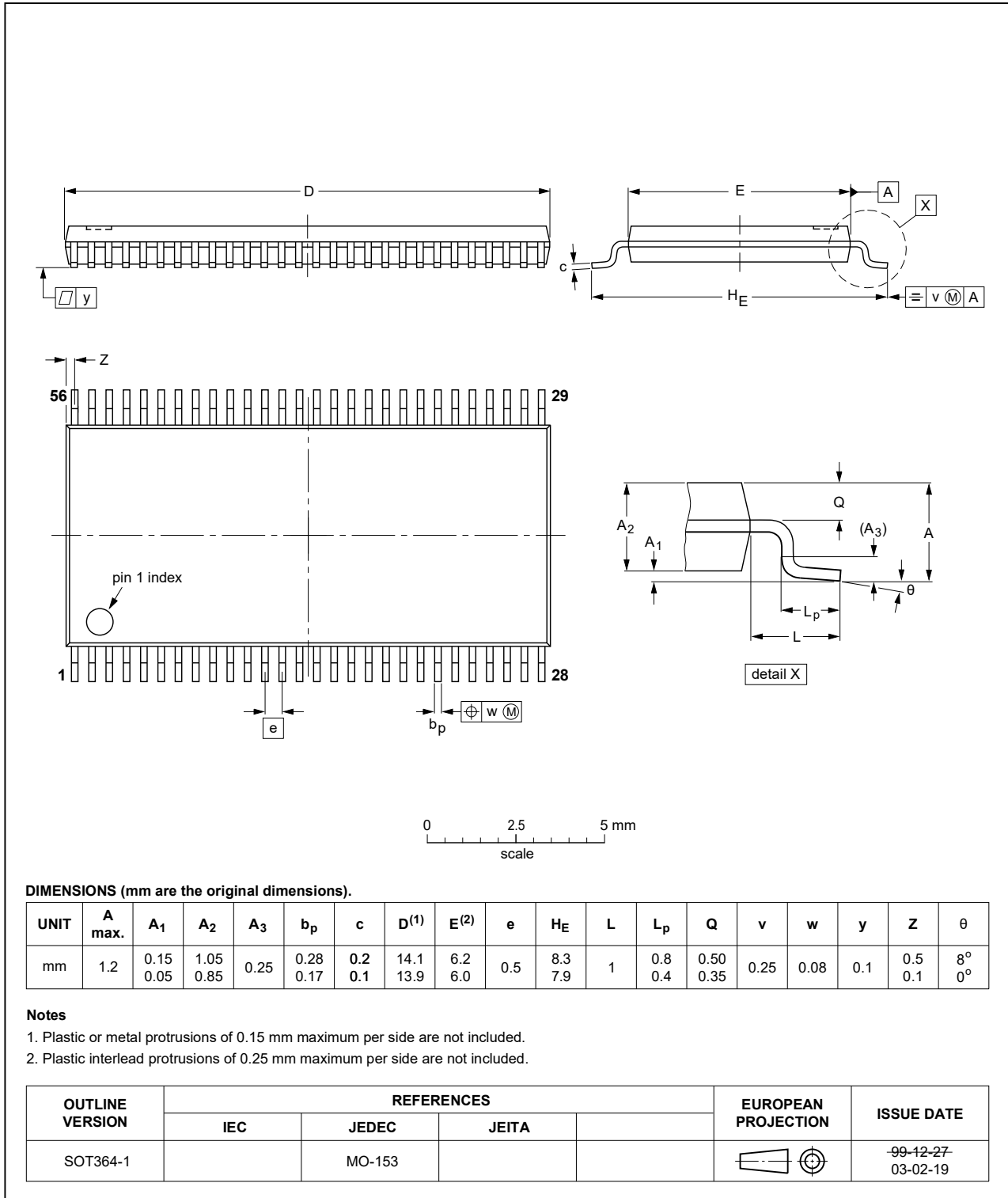


Fig. 8. Package outline SOT364-1 (TSSOP56)

12. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| ANSI | American National Standards Institute |
| BiCMOS | Bipolar Complementary Metal Oxide Semiconductor |
| CDM | Charged Device Model |
| DUT | Device Under Test |
| ESD | ElectroStatic Discharge |
| ESDA | ElectroStatic Discharge Association |
| HBM | Human Body Model |
| JEDEC | Joint Electron Device Engineering Council |
| TTL | Transistor-Transistor Logic |

13. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|------------------|--|-----------------------|---------------|------------------|
| 74ALVT162827 v.4 | 20240625 | Product data sheet | - | 74ALVT162827 v.3 |
| Modifications: | <ul style="list-style-type: none"> • Section 2: ESD specification updated according to the latest JEDEC standard. • Section 1 updated. | | | |
| 74ALVT162827 v.3 | 20180124 | Product data sheet | - | 74ALVT162827 v.2 |
| Modifications: | <ul style="list-style-type: none"> • The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate. • Type number 74ALVT162827DL (SOT371-1 / SSOP56) removed. | | | |
| 74ALVT162827 v.2 | 19980213 | Product specification | - | 74ALVT162827 v.1 |
| 74ALVT162827 v.1 | 19970501 | Product specification | - | - |

14. Legal information

Data sheet status

| Document status [1][2] | Product status [3] | Definition |
|--------------------------------|--------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
- [3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the internet at <https://www.nexperia.com>.

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