

# NP40N10YDF, NP40N10VDF, NP40N10PDF

100 V – 40 A – N-channel Power MOS FET

Application: Automotive

R07DS0361EJ0201

Rev.2.01

May 13, 2013

## Description

These products are N-channel MOS Field Effect Transistors designed for high current switching applications.

## Features

- Low on-state resistance
  - $R_{DS(on)} = 25 \text{ m}\Omega$  MAX. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ ) (NP40N10YDF)
  - $R_{DS(on)} = 26 \text{ m}\Omega$  MAX. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ ) (NP40N10VDF)
  - $R_{DS(on)} = 27 \text{ m}\Omega$  MAX. ( $V_{GS} = 10 \text{ V}$ ,  $I_D = 20 \text{ A}$ ) (NP40N10PDF)
- Low  $C_{iss}$ :  $C_{iss} = 2100 \text{ pF}$  TYP. ( $V_{DS} = 25 \text{ V}$ ,  $V_{GS} = 0 \text{ V}$ )
- Logic level drive type
- Designed for automotive application and AEC-Q101 qualified

## Outline

The diagram shows the internal structure of the MOSFET with labels for Drain, Gate, Source, and Body Diode. Below it are three physical package views: 8-pin HSON, TO-252, and TO-263. Each view includes pin numbering and a legend for pin functions.

**8-pin HSON**

1, 2, 3 : Source  
4 : Gate  
5, 6, 7, 8: Drain

**TO-252**

1. Gate  
2. Drain  
3. Source  
4. Fin (Drain)

**TO-263**

1. Gate  
2. Drain  
3. Source  
4. Fin (Drain)

Remark: Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

## Ordering Information

Part No.	Lead Plating	Packing		Package
NP40N10YDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP40N10YDF-E2-AY *1			Taping (E2 type)	
NP40N10VDF-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	TO-252 (MP-3ZP)
NP40N10VDF-E2-AY *1			Taping (E2 type)	
NP40N10PDF-E1-AY *1	Pure Sn (Tin)	Tape 800 p/reel	Taping (E1 type)	TO-263 (MP-25ZP)
NP40N10PDF-E2-AY *1			Taping (E2 type)	

Note: \*1. Pb-free (This product does not contain Pb in the external electrode)

**Absolute Maximum Ratings** ( $T_A = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to Source Voltage ( $V_{GS} = 0\text{ V}$ )	$V_{DSS}$	100	V
Gate to Source Voltage ( $V_{DS} = 0\text{ V}$ )	$V_{GSS}$	$\pm 20$	V
Drain Current (DC) ( $T_C = 25^\circ\text{C}$ )	$I_{D(DC)}$	$\pm 40$	A
Drain Current (pulse) <sup>*1</sup>	$I_{D(pulse)}$	$\pm 80$	A
Total Power Dissipation ( $T_C = 25^\circ\text{C}$ )	$P_{T1}$	120	W
<b>NP40N10YDF</b> Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>*2</sup>	$P_{T2}$	1.0	W
<b>NP40N10VDF</b> Total Power Dissipation ( $T_A = 25^\circ\text{C}$ ) <sup>*2</sup>		1.2	
<b>NP40N10PDF</b> Total Power Dissipation ( $T_A = 25^\circ\text{C}$ )		1.8	
Channel Temperature	$T_{ch}$	175	$^\circ\text{C}$
Storage Temperature	$T_{stg}$	-55 to +175	$^\circ\text{C}$
Single Avalanche Current <sup>*3</sup>	$I_{AS}$	25	A
Single Avalanche Energy <sup>*3</sup>	$E_{AS}$	61	mJ

**Thermal Resistance**

Channel to Case Thermal Resistance	$R_{th(ch-C)}$		1.25	$^\circ\text{C/W}$
Channel to Ambient Thermal Resistance <sup>*2</sup>	$R_{th(ch-A)}$	NP40N10YDF	150	$^\circ\text{C/W}$
		NP40N10VDF	125	$^\circ\text{C/W}$
		NP40N10PDF	83.3	$^\circ\text{C/W}$

Notes: <sup>\*1</sup>.  $T_C = 25^\circ\text{C}$ ,  $PW \leq 10\ \mu\text{s}$ , Duty Cycle  $\leq 1\%$

<sup>\*2</sup>. Mounted on glass epoxy substrate of 40 mm  $\times$  40 mm  $\times$  1.6 mm with 4% copper area (35  $\mu\text{m}$ )

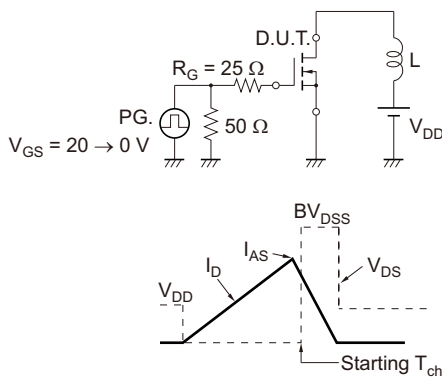
<sup>\*3</sup>.  $T_{ch(start)} = 25^\circ\text{C}$ ,  $V_{DD} = 50\text{ V}$ ,  $R_G = 25\ \Omega$ ,  $L = 100\ \mu\text{H}$ ,  $V_{GS} = 20\text{ V} \rightarrow 0\text{ V}$

Electrical Characteristics (T<sub>A</sub> = 25°C)

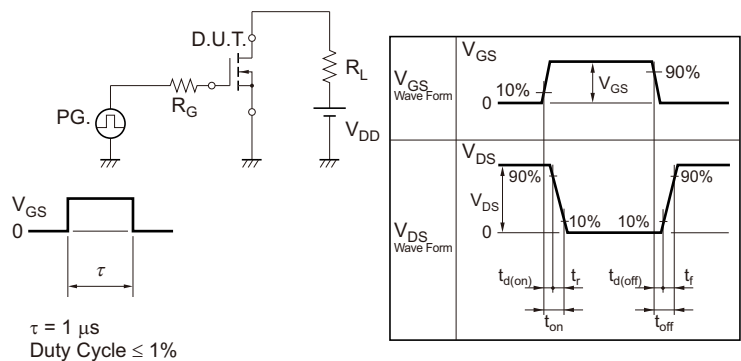
Item	Symbol	Min	Typ	Max	Unit	Test Conditions	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>			1	μA	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V	
Gate Leakage Current	I <sub>GSS</sub>			±100	nA	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	
Gate to Source Threshold Voltage	V <sub>GS(th)</sub>	1.5	2.0	2.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	
Forward Transfer Admittance *1	y <sub>fs</sub>	20	40		S	V <sub>DS</sub> = 5.0 V, I <sub>D</sub> = 20 A	
Drain to Source On-state Resistance *1	NP40N10YDF	R <sub>DS(on)1</sub>		21	25	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)2</sub>		23	30	mΩ	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)3</sub>		24	36	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A
	NP40N10VDF	R <sub>DS(on)1</sub>		21	26	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)2</sub>		23	31	mΩ	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)3</sub>		24	37	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A
	NP40N10PDF	R <sub>DS(on)1</sub>		21	27	mΩ	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)2</sub>		23	32	mΩ	V <sub>GS</sub> = 5.0 V, I <sub>D</sub> = 20 A
		R <sub>DS(on)3</sub>		24	38	mΩ	V <sub>GS</sub> = 4.5 V, I <sub>D</sub> = 20 A
Input Capacitance	C <sub>iss</sub>		2100	3150	pF	V <sub>DS</sub> = 25 V, V <sub>GS</sub> = 0 V,	
Output Capacitance	C <sub>oss</sub>		200	300	pF	f = 1 MHz	
Reverse Transfer Capacitance	C <sub>rss</sub>		80	144	pF		
Turn-on Delay Time	t <sub>d(on)</sub>		15	33	ns	V <sub>DD</sub> = 50 V, I <sub>D</sub> = 20 A,	
Rise Time	t <sub>r</sub>		16	40	ns	V <sub>GS</sub> = 10 V,	
Turn-off Delay Time	t <sub>d(off)</sub>		60	120	ns	R <sub>G</sub> = 0 Ω	
Fall Time	t <sub>f</sub>		5	13	ns		
Total Gate Charge	Q <sub>G</sub>		47	71	nC	V <sub>DD</sub> = 80 V,	
Gate to Source Charge	Q <sub>GS</sub>		8		nC	V <sub>GS</sub> = 10 V,	
Gate to Drain Charge	Q <sub>GD</sub>		12		nC	I <sub>D</sub> = 40 A	
Body Diode Forward Voltage *1	V <sub>F(S-D)</sub>		0.9	1.5	V	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V	
Reverse Recovery Time	t <sub>rr</sub>		67		ns	I <sub>F</sub> = 40 A, V <sub>GS</sub> = 0 V,	
Reverse Recovery Charge	Q <sub>rr</sub>		162		nC	di/dt = 100 A/μs	

Note: \*1. Pulsed test

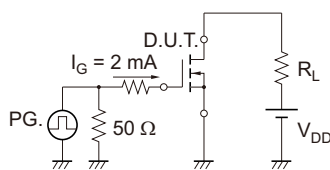
TEST CIRCUIT 1 AVALANCHE CAPABILITY



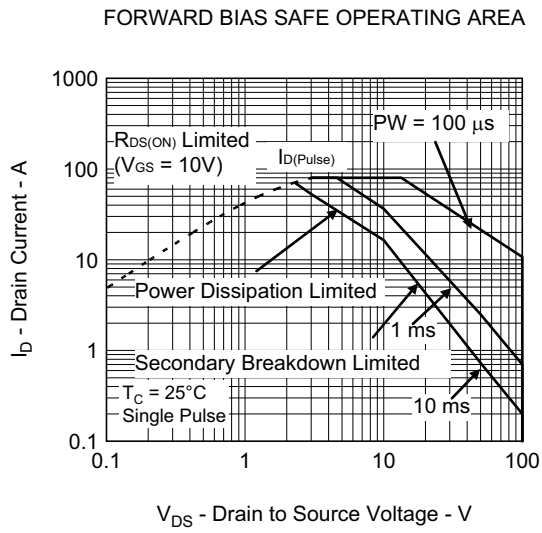
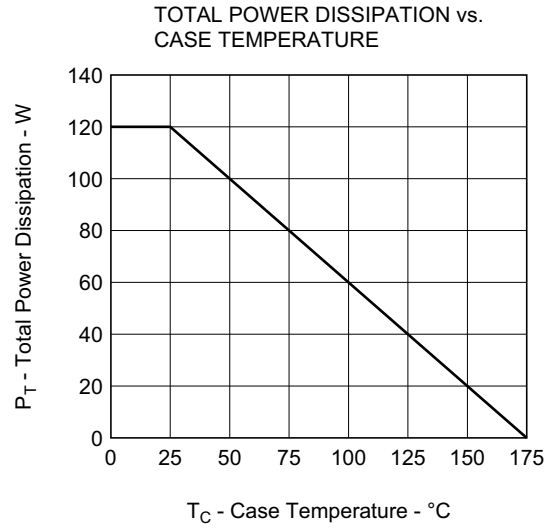
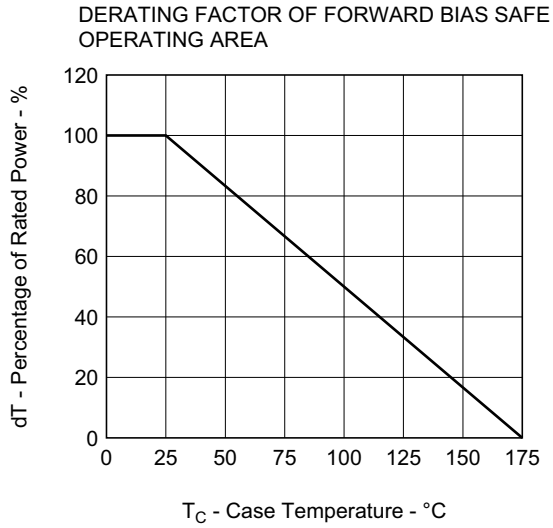
TEST CIRCUIT 2 SWITCHING TIME



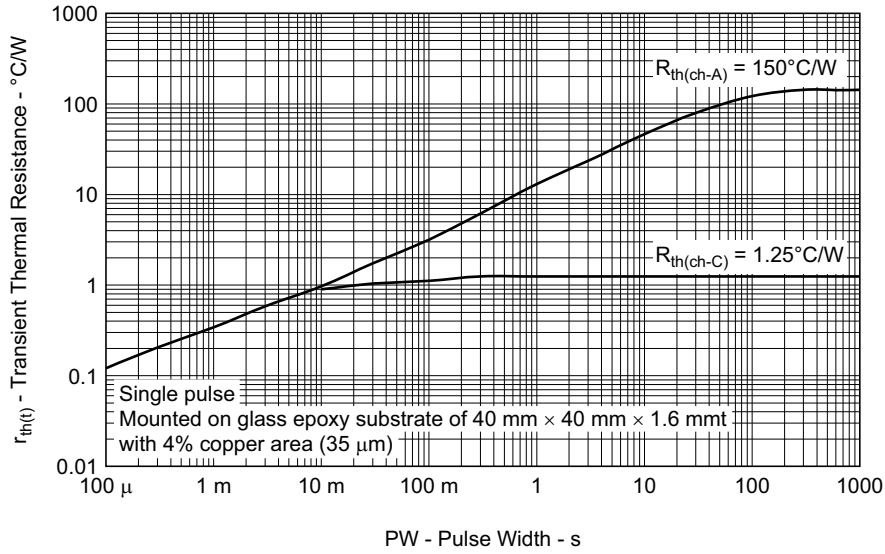
TEST CIRCUIT 3 GATE CHARGE



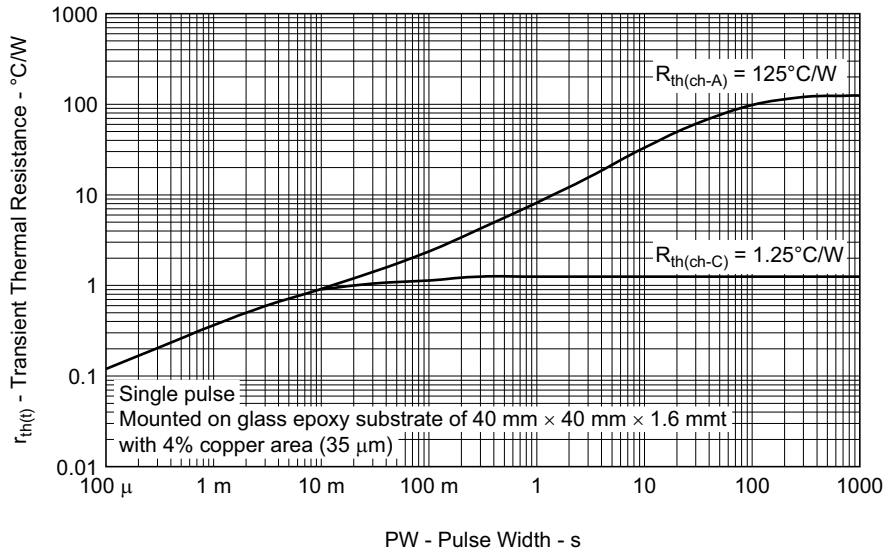
Typical Characteristics ( $T_A = 25^\circ\text{C}$ )



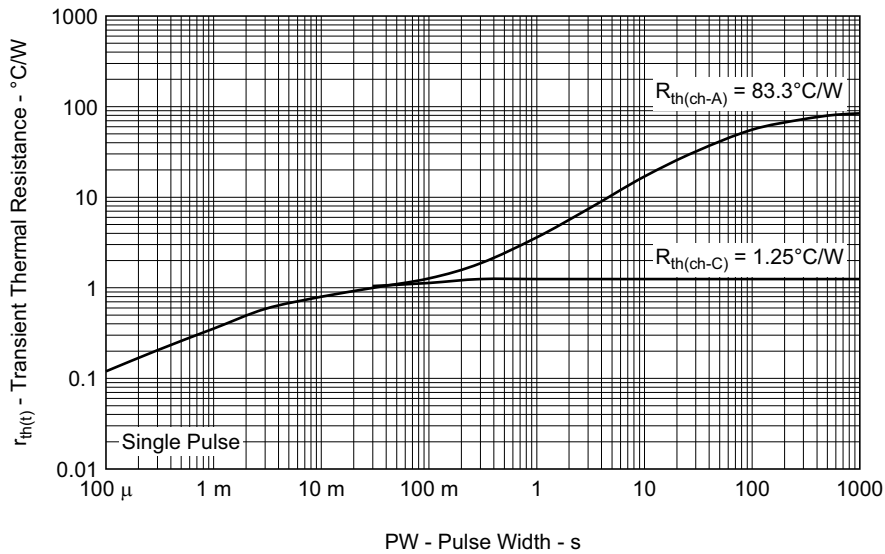
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10YDF)

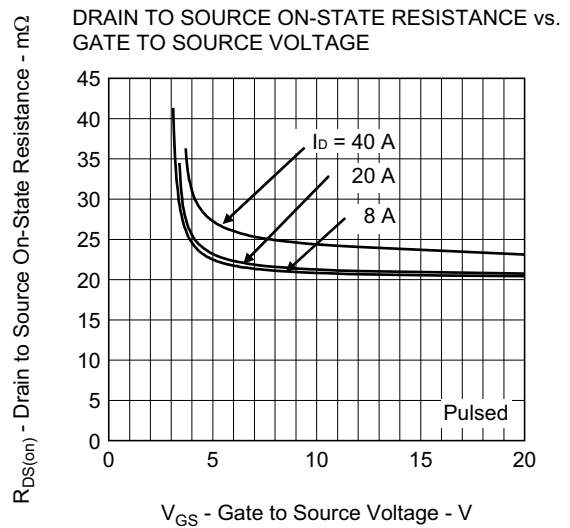
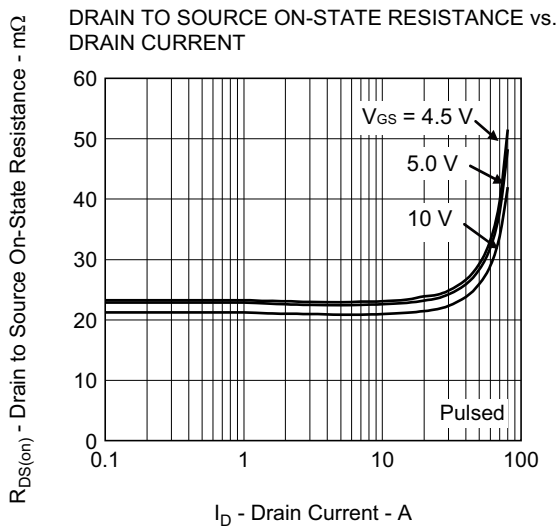
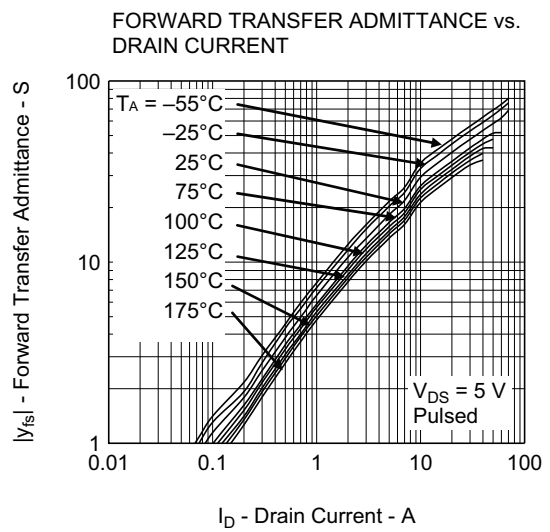
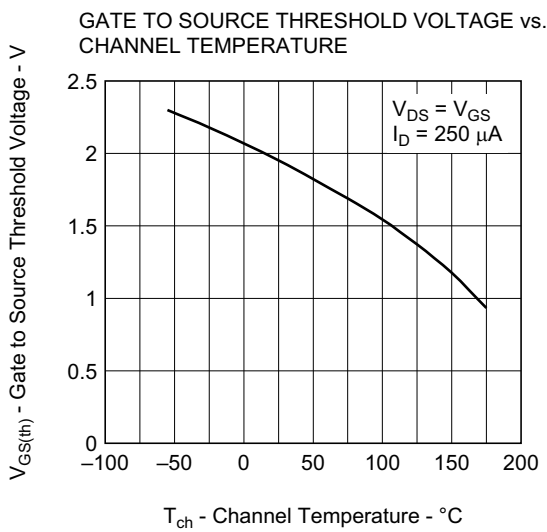
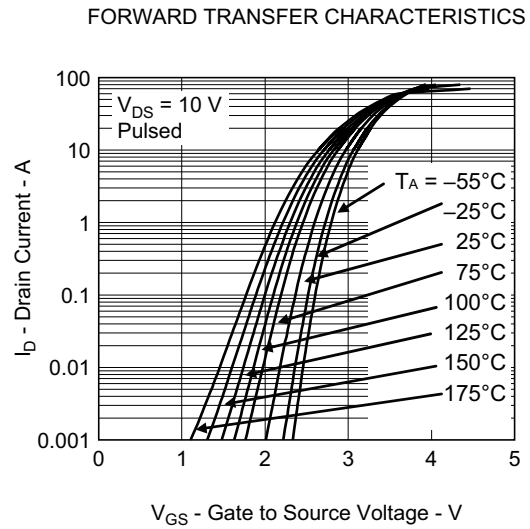
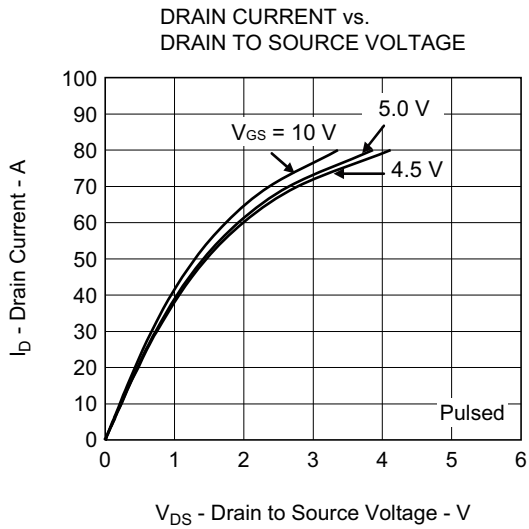


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10VDF)

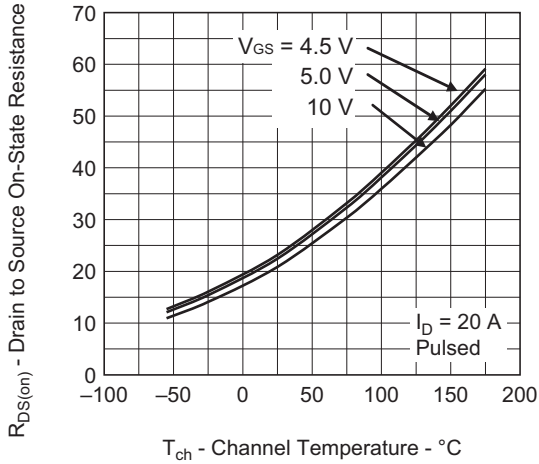


TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH (NP40N10PDF)

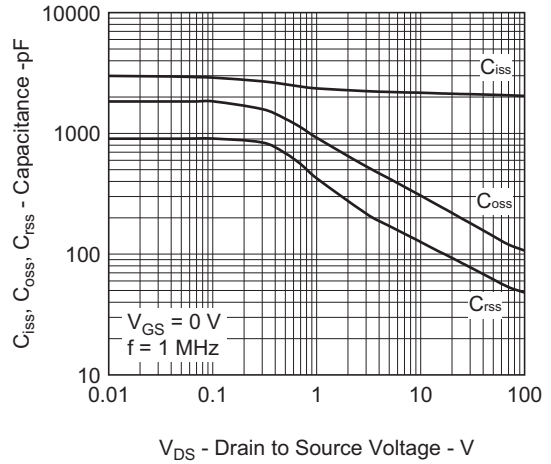




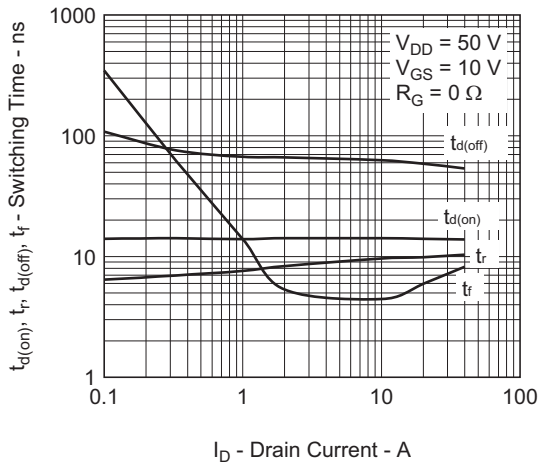
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



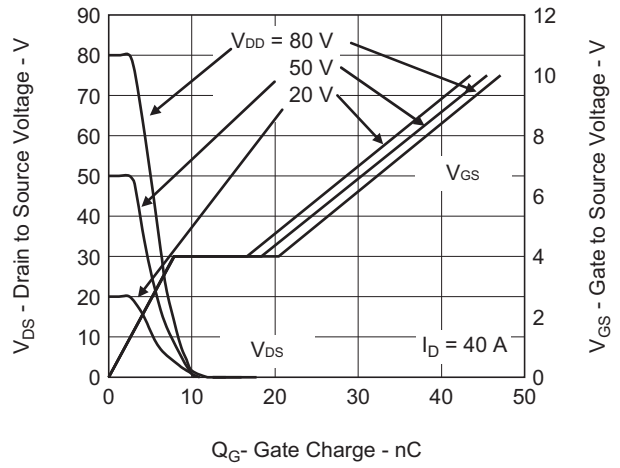
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



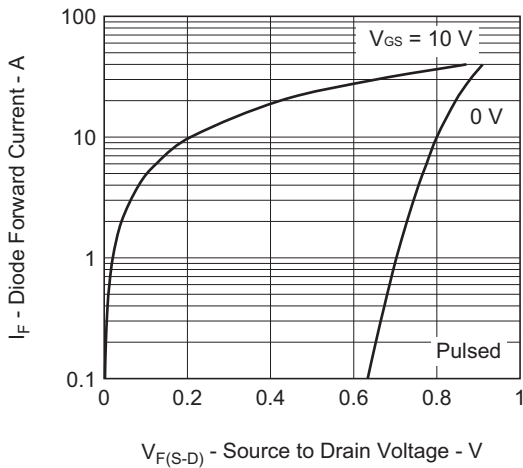
SWITCHING CHARACTERISTICS



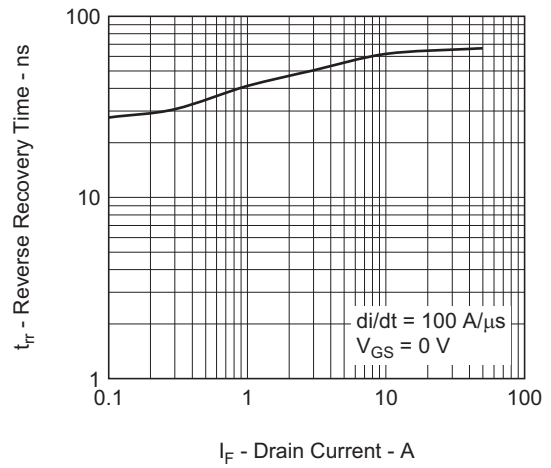
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



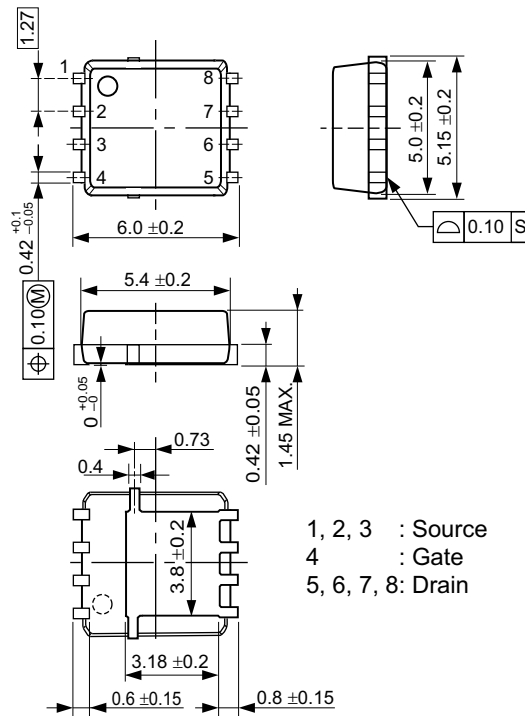
REVERSE RECOVERY TIME vs. DRAIN CURRENT



Package Drawings (Unit: mm)

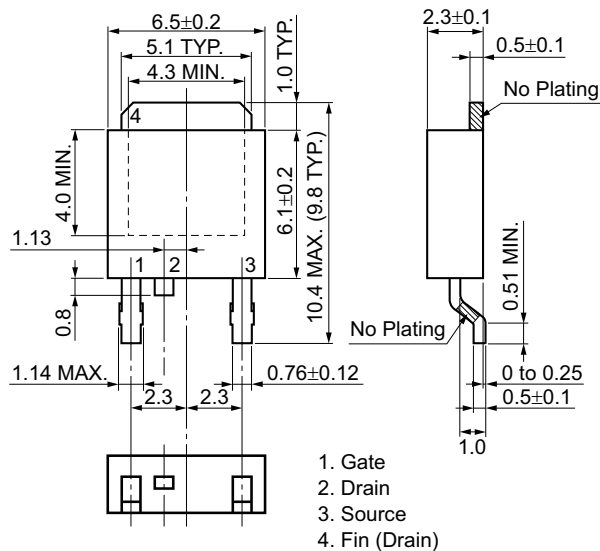
8-pin HSON (Mass: 0.13 g TYP.)

Renesas package code: PLSN0008KA-A



TO-252 (MP-3ZP) (Mass: 0.27 g TYP.)

Renesas package code: PRSS0004ZP-A





**Revision History****NP40N10YDF, NP40N10VDF, NP40N10PDF Data Sheet**

Rev.	Date	Description	
		Page	Summary
1.00	Feb 21, 2013	—	First Edition Issued
2.00	Mar 11, 2013	1	"Outline" added
		7	Modification of "CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE"
2.01	May 13, 2013	1	Modification of "Outline"
		8	Modification of "Package Drawings 8-pinHSON"

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**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

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Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-651-700, Fax: +44-1628-651-804

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670



**Renesas Electronics Singapore Pte. Ltd.**  
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Tel: +65-6213-0200, Fax: +65-6213-0300

**Renesas Electronics Malaysia Sdn.Bhd.**  
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