



# THE DATASHEET OF CDCM6208V1ERGZT

# CDCM6208 2:8 Clock Generator, Jitter Cleaner With Fractional Dividers

Check for Samples: [CDCM6208](#)

## 1 Features

- Superior Performance With Low Power:
  - Low Noise Synthesizer (265 fs-rms Typical Jitter) or Low Noise Jitter Cleaner (1.6 ps-rms Typical Jitter)
  - 0.5-W Typical Power Consumption
  - High Channel-to-Channel Isolation and Excellent PSRR
  - Device Performance Customizable Through Flexible 1.8-V, 2.5-V and 3.3-V Power Supplies, Allowing Mixed Output Voltages
- Flexible Frequency Planning:
  - 4x Integer Down-Divided Differential Clock Outputs Supporting LVPECL-Like, CML, or LVDS-Like Signaling
  - 4x Fractional or Integer Divided Differential Clock Outputs Supporting HCSL, LVDS-Like Signaling, or Eight CMOS Outputs
  - Fractional Output Divider Achieve 0 ppm to < 1 ppm Frequency Error and Eliminates Need for Crystal Oscillators and Other Clock Generators
  - Output Frequencies up to 800 MHz
- Two Differential Inputs, XTAL Support, Ability for Smart Switching
- SPI, I<sup>2</sup>C, and Pin Programmable
- Professional User GUI for Quick Design Turnaround
- 7 × 7 mm 48-VQFN package (RGZ)
- –40°C to 85°C Temperature Range

## 2 Applications

- Base Band Clocking (Wireless Infrastructure)
- Networking and Data Communications
- Micro and Pico Base Stations
- Keystone C66x Multicore DSP Clocking
- Storage Server, Portable Test Equipment
- Medical Imaging, High End A/V

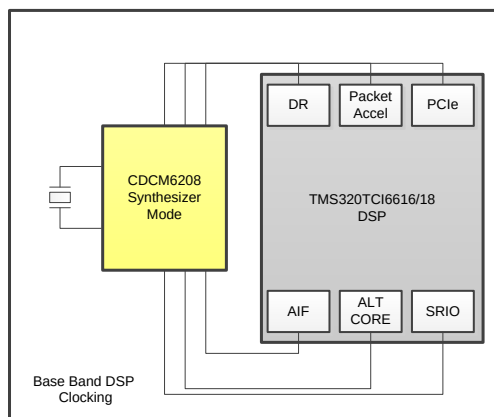
## 3 Description

The CDCM6208 is a highly versatile, low jitter low power frequency synthesizer which can generate eight low jitter clock outputs, selectable between LVPECL-like high-swing CML, normal-swing CML, LVDS-like low-power CML, HCSL, or LVCMOS, from one of two inputs that can feature a low frequency crystal or CML, LVPECL, LVDS, or LVCMOS signals for a variety of wireless infrastructure baseband, Small Cells, wireline data communication, computing, low power medical imaging and portable test and measurement applications. The CDCM6208 also features an innovative fractional divider architecture for four of its outputs that can generate any frequency with better than 1ppm frequency accuracy. The CDCM6208 can be easily configured through I<sup>2</sup>C or SPI programming interface and in the absence of serial interface, pin mode is also available that can set the device in 1 of 32 distinct pre-programmed configurations using control pins.

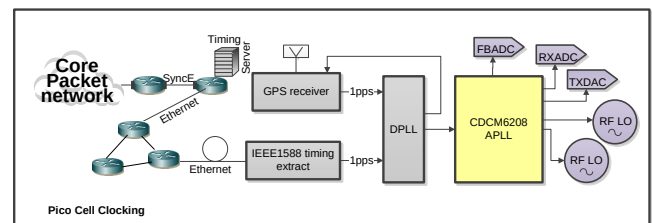
### Device Information

| DEVICE NAME | PACKAGE   | BODY SIZE         |
|-------------|-----------|-------------------|
| CDCM6208    | VQFN (48) | 7.00 mm × 7.00 mm |

### Simplified Schematic



### Simplified Schematic



## Table of Contents

|                                                                                                                                                            |          |                                                                               |           |
|------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|-------------------------------------------------------------------------------|-----------|
| <b>1 Features</b>                                                                                                                                          | <b>1</b> | 6.21 Worst Case Current Consumption                                           | 17        |
| <b>2 Applications</b>                                                                                                                                      | <b>1</b> | 6.22 Timing Requirements, I <sup>2</sup> C Timing                             | 17        |
| <b>3 Description</b>                                                                                                                                       | <b>1</b> | 6.23 Typical Characteristics                                                  | 19        |
| <b>4 Revision History</b>                                                                                                                                  | <b>2</b> | <b>7 Parameter Measurement Information</b>                                    | <b>21</b> |
| <b>5 Pin Configuration and Functions</b>                                                                                                                   | <b>4</b> | <b>8 Detailed Description</b>                                                 | <b>26</b> |
| <b>6 Specifications</b>                                                                                                                                    | <b>6</b> | 8.1 Overview                                                                  | 26        |
| 6.1 Absolute Maximum Ratings                                                                                                                               | 6        | 8.2 Functional Block Diagram                                                  | 26        |
| 6.2 ESD Ratings                                                                                                                                            | 6        | 8.3 Feature Description                                                       | 26        |
| 6.3 Recommended Operating Conditions                                                                                                                       | 7        | 8.4 Device Functional Modes                                                   | 35        |
| 6.4 Thermal Information, Airflow = 0 LFM                                                                                                                   | 7        | 8.5 Programming                                                               | 51        |
| 6.5 Thermal Information, Airflow = 150 LFM                                                                                                                 | 8        | 8.6 Register Maps                                                             | 52        |
| 6.6 Thermal Information, Airflow = 250 LFM                                                                                                                 | 8        | <b>9 Application and Implementation</b>                                       | <b>65</b> |
| 6.7 Thermal Information, Airflow = 500 LFM                                                                                                                 | 8        | 9.1 Application Information                                                   | 65        |
| 6.8 Single-Ended Input Characteristics (SI_MODE[1:0], SDI/SDA/PIN1, SCL/PIN4, SDO/ADD0/PIN2, SCS/ADD1/PIN3, STATUS1/PIN0, RESETN/PWR, PDN, SYNCN, REF_SEL) | 9        | 9.2 Typical Applications                                                      | 65        |
| 6.9 Single-Ended Input Characteristics (PRI_REF, SEC_REF)                                                                                                  | 9        | <b>10 Power Supply Recommendations</b>                                        | <b>74</b> |
| 6.10 Differential Input Characteristics (PRI_REF, SEC_REF)                                                                                                 | 10       | 10.1 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains | 74        |
| 6.11 Crystal Input Characteristics (SEC_REF)                                                                                                               | 10       | 10.2 Device Power-Up Timing                                                   | 75        |
| 6.12 Single-Ended Output Characteristics (STATUS1, STATUS0, SDO, SDA)                                                                                      | 11       | 10.3 Power Down                                                               | 78        |
| 6.13 PLL Characteristics                                                                                                                                   | 11       | 10.4 Power Supply Ripple Rejection (PSRR) versus Ripple Frequency             | 78        |
| 6.14 LVCMOS Output Characteristics                                                                                                                         | 12       | <b>11 Layout</b>                                                              | <b>79</b> |
| 6.15 LVPECL (High-Swing CML) Output Characteristics                                                                                                        | 13       | 11.1 Layout Guidelines                                                        | 79        |
| 6.16 CML Output Characteristics                                                                                                                            | 13       | 11.2 Reference Schematics                                                     | 81        |
| 6.17 LVDS (Low-Power CML) Output Characteristics                                                                                                           | 14       | <b>12 Device and Documentation Support</b>                                    | <b>85</b> |
| 6.18 HCSL Output Characteristics                                                                                                                           | 14       | 12.1 Documentation Support                                                    | 85        |
| 6.19 Output Skew and Sync to Output Propagation Delay Characteristics                                                                                      | 15       | 12.2 Receiving Notification of Documentation Updates                          | 85        |
| 6.20 Device Individual Block Current Consumption                                                                                                           | 16       | 12.3 Community Resources                                                      | 85        |
|                                                                                                                                                            |          | 12.4 Trademarks                                                               | 85        |
|                                                                                                                                                            |          | 12.5 Electrostatic Discharge Caution                                          | 85        |
|                                                                                                                                                            |          | 12.6 Glossary                                                                 | 85        |
|                                                                                                                                                            |          | <b>13 Mechanical, Packaging, and Orderable Information</b>                    | <b>85</b> |

## 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

| Changes from Revision F (April 2014) to Revision G            | Page |
|---------------------------------------------------------------|------|
| • Changed <i>Handling Ratings</i> table to <i>ESD Ratings</i> | 6    |
| • Added <a href="#">Table 7</a>                               | 38   |
| • Added <a href="#">Table 10</a>                              | 43   |

| Changes from Revision E (March 2013) to Revision F                                                                                                                                                                    | Page |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| • Changed layout of data sheet to conform to new TI standards. Added the following sections: Handling Ratings, Thermal Information, Typical Characteristics, Programming, Register Maps, Layout and Layout Guidelines | 1    |
| • Changed from zero to one                                                                                                                                                                                            | 53   |
| • Added text at the end of the first paragraph in <a href="#">Power Down</a> section                                                                                                                                  | 78   |
| • Changed $f_{OUT} = 122.88$ MHz, VDD Supply Noise = 100 mVpp                                                                                                                                                         | 78   |

## Changes from Revision D (March 2013) to Revision E Page

|                                                                                                                                                                      |    |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Changed the data sheet layout to the new TI standard .....                                                                                                         | 1  |
| • Added the Handling Ratings table .....                                                                                                                             | 6  |
| • Changed Pullup and Pulldown value From: MIN = 40 To: 35 kΩ and MAX = 60 To: 65 kΩ .....                                                                            | 9  |
| • Changed the from Random Jitter, Maximum in <a href="#">Table 2</a> From: 10k - 20MHZ To: 12k - 20MHZ and From: 0.5 ps-rms (int div) To: 0.3 ps-rms (int div) ..... | 27 |
| • Added new Note 1 to <a href="#">Table 2</a> .....                                                                                                                  | 27 |

## Changes from Revision C (September 2012) to Revision D Page

|                                                                                                                                                                          |    |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----|
| • Changed the Description of pin VDD_PRI_REF .....                                                                                                                       | 4  |
| • Changed the Description of pin VDD_SEC_REF .....                                                                                                                       | 4  |
| • Changed <a href="#">Figure 35</a> .....                                                                                                                                | 33 |
| • Changed <a href="#">Table 6</a> - Note 2 and row 10 - 0x1C, PinMode 29-V1, fout(Y7) From: 33.33 To: 44.44 .....                                                        | 36 |
| • Changed <a href="#">Table 8</a> - Note 2 and row 10 - 0x13, PinMode 20-V2, fout(Y7) From: 25 To: 12.5 .....                                                            | 40 |
| • Changed text in the PLL lock detect section From: "1/1000 <sup>th</sup> of the input reference frequency" To: "1/1000 <sup>th</sup> of the PFD update frequency" ..... | 45 |
| • Changed text in the PLL lock detect section From: "approximately 1000 input clock cycles" To: "approximately 1000 PFD update clock cycles" .....                       | 45 |
| • Changed <a href="#">Figure 60</a> , From: PDN held Low To: RESETN held low .....                                                                                       | 76 |
| • Changed <a href="#">Equation 4</a> .....                                                                                                                               | 78 |

## Changes from Revision B (August 2012) to Revision C Page

|                                                                         |    |
|-------------------------------------------------------------------------|----|
| • Changed <a href="#">Table 39</a> , 2:0 DIE_REVISION Description ..... | 63 |
| • Added text "Example: SERDES link with KeyStone™ I DSP" .....          | 66 |

## Changes from Revision A (June 2012) to Revision B Page

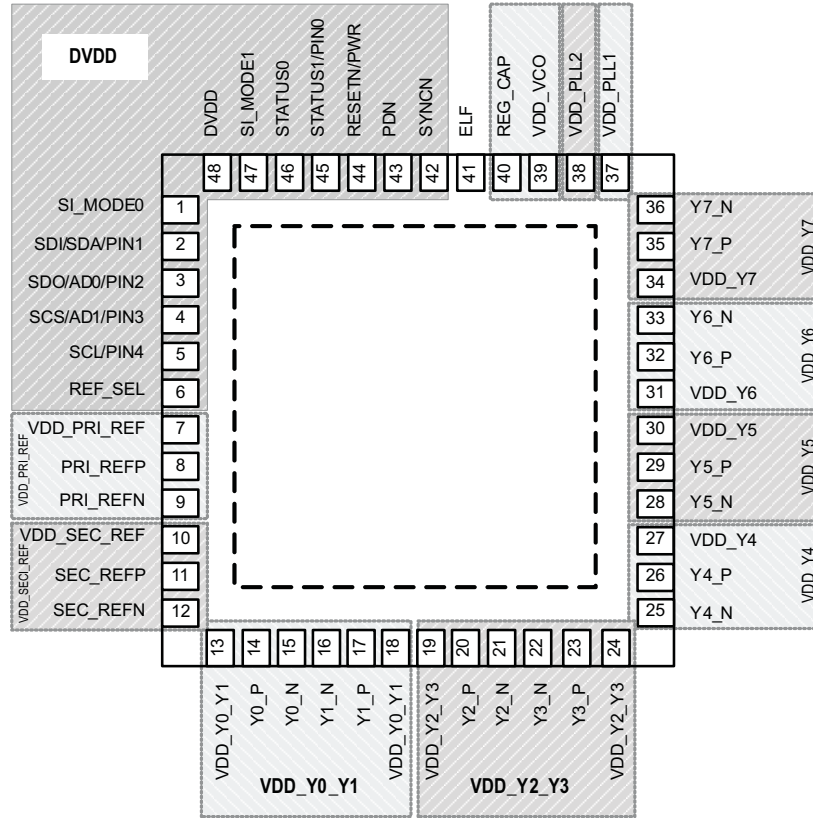
|                                                                                                                 |    |
|-----------------------------------------------------------------------------------------------------------------|----|
| • Editorial changes made throughout the data sheet .....                                                        | 1  |
| • Changed the Description of pin VDD_PRI_REF .....                                                              | 4  |
| • Changed the Description of pin VDD_SEC_REF .....                                                              | 4  |
| • Added Table Note 1 to the description of pin 44. ....                                                         | 6  |
| • Added Note to the Preventing false output frequencies in SPI/I2C mode at startup: section .....               | 34 |
| • Changed the NOTE following <a href="#">Table 12</a> .....                                                     | 45 |
| • Added Note to the I <sup>2</sup> C SERIAL INTERFACE section .....                                             | 49 |
| • Deleted text "All outputs PECL (Y4:0) and LVDS (Y7:4)." from the Conclusion statement .....                   | 69 |
| • Changed the text in the OUTPUT MUX on Y4 and Y5 section .....                                                 | 73 |
| • Changed the text in item 1 of the Staggered CLK output powerup for power sequencing of a DSP section .....    | 73 |
| • Changed the first paragraph in the Power Down section .....                                                   | 78 |
| • Changed the first paragraph in the Power Supply Ripple Rejection (PSRR) versus Ripple Frequency section ..... | 78 |

## Changes from Original (May 2012) to Revision A Page

|                                                                                                                                                 |   |
|-------------------------------------------------------------------------------------------------------------------------------------------------|---|
| • Changed the device From: Product Preview To: Production .....                                                                                 | 1 |
| • Section Header From: RESTN, PWR, SYNC To: RESETN, PWR, SYNCN, PDN, REF_SEL, SI_MODE[1:0] .....                                                | 9 |
| • Changed the R <sub>PULLUP</sub> parametres From: R <sub>PULLUP</sub> - Input Pullup Resistor To: R - Input Pullup and Pulldown Resistor ..... | 9 |

## 5 Pin Configuration and Functions

**RGZ Package  
48-Pin VQFN  
(Top View)**



**Pin Functions**

| PIN         |     | I/O    | TYPE                      | DESCRIPTION                                                                                                                                                                                                                                                                               |
|-------------|-----|--------|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME        | NO. |        |                           |                                                                                                                                                                                                                                                                                           |
| PRI_REFP    | 8   | Input  | Universal                 | Primary Reference Input +                                                                                                                                                                                                                                                                 |
| PRI_REFN    | 9   | Input  | Universal                 | Primary Reference Input –                                                                                                                                                                                                                                                                 |
| VDD_PRI_REF | 7   | PWR    | Analog                    | Supply pin for reference inputs to set between 1.8 V, 2.5 V, or 3.3 V, or connected to VDD_SEC_REF.                                                                                                                                                                                       |
| SEC_REFP    | 11  | Input  | Universal                 | Secondary Reference Input +                                                                                                                                                                                                                                                               |
| SEC_REFN    | 12  | Input  | Universal                 | Secondary Reference Input –                                                                                                                                                                                                                                                               |
| VDD_SEC_REF | 10  | PWR    | Analog                    | Supply pin for reference inputs to set between 1.8 V, 2.5 V, or 3.3 V, or connected to VDD_PRI_REF <sup>(1)</sup> .                                                                                                                                                                       |
| REF_SEL     | 6   | Input  | LVC MOS with 50-kΩ pullup | Manual Reference Selection MUX for PLL. In SPI or I <sup>2</sup> C mode the reference selection is also controlled through Register 4 bit 12. REF_SEL = 0 ( $\leq V_{IL}$ ): selects PRI_REF. REF_SEL = 1 ( $\geq V_{IH}$ ): selects SEC_REF (when Reg 4.12 = 1). See Table 5 for detail. |
| ELF         | 41  | Output | Analog                    | External loop filter pin for PLL                                                                                                                                                                                                                                                          |
| Y0_P        | 14  | Output | Universal                 | Output 0 Positive Pin                                                                                                                                                                                                                                                                     |
| Y0_N        | 15  | Output | Universal                 | Output 0 Negative Pin                                                                                                                                                                                                                                                                     |
| Y1_P        | 17  | Output | Universal                 | Output 1 Positive Pin                                                                                                                                                                                                                                                                     |
| Y1_N        | 16  | Output | Universal                 | Output 1 Negative Pin                                                                                                                                                                                                                                                                     |

(1) If Secondary input buffer is disabled (Register 4 Bit 5 = 0), it is possible to connect VDD\_SEC\_REF to GND.

### Pin Functions (continued)

| PIN                   |        | I/O              | TYPE                                                           | DESCRIPTION                                                                                                                                                                                      |
|-----------------------|--------|------------------|----------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME                  | NO.    |                  |                                                                |                                                                                                                                                                                                  |
| VDD_Y0_Y1<br>(2 pins) | 13, 18 | PWR              | Analog                                                         | Supply pin for outputs 0, 1 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                |
| Y2_P                  | 20     | Output           | Universal                                                      | Output 2 Positive Pin                                                                                                                                                                            |
| Y2_N                  | 21     | Output           | Universal                                                      | Output 2 Negative Pin                                                                                                                                                                            |
| Y3_P                  | 23     | Output           | Universal                                                      | Output 3 Positive Pin                                                                                                                                                                            |
| Y3_N                  | 22     | Output           | Universal                                                      | Output 3 Negative Pin                                                                                                                                                                            |
| VDD_Y2_Y3<br>(2 pins) | 19, 24 | PWR              | Analog                                                         | Supply pin for outputs 2, 3 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                |
| Y4_P                  | 26     | Output           | Universal                                                      | Output 4 Positive Pin                                                                                                                                                                            |
| Y4_N                  | 25     | Output           | Universal                                                      | Output 4 Negative Pin                                                                                                                                                                            |
| VDD_Y4                | 27     | PWR              | Analog                                                         | Supply pin for output 4 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                    |
| Y5_P                  | 29     | Output           | Universal                                                      | Output 5 Positive Pin                                                                                                                                                                            |
| Y5_N                  | 28     | Output           | Universal                                                      | Output 5 Negative Pin                                                                                                                                                                            |
| VDD_Y5                | 30     | PWR              | Analog                                                         | Supply pin for output 5 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                    |
| Y6_P                  | 32     | Output           | Universal                                                      | Output 6 Positive Pin                                                                                                                                                                            |
| Y6_N                  | 33     | Output           | Universal                                                      | Output 6 Negative Pin                                                                                                                                                                            |
| VDD_Y6                | 31     | PWR              | Analog                                                         | Supply pin for output 6 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                    |
| Y7_P                  | 35     | Output           | Universal                                                      | Output 7 Positive Pin                                                                                                                                                                            |
| Y7_N                  | 36     | Output           | Universal                                                      | Output 7 Negative Pin                                                                                                                                                                            |
| VDD_Y7                | 34     | PWR              | Analog                                                         | Supply pin for output 7 to set between 1.8 V, 2.5 V, or 3.3 V                                                                                                                                    |
| VDD_VCO               | 39     | PWR              | Analog                                                         | Analog power supply for PLL/VCO; This pin is sensitive to power supply noise; The supply of this pin and the VDD_PLL2 supply pin can be combined as they are both analog and sensitive supplies; |
| VDD_PLL1              | 37     | PWR              | Analog                                                         | Analog Power Supply Connections                                                                                                                                                                  |
| VDD_PLL2              | 38     | PWR              | Analog                                                         | Analog Power Supply Connections; This pin is sensitive to power supply noise; The supply of VDD_PLL2 and VDD_VCO can be combined as these pins are both power-sensitive, analog supply pins      |
| DVDD                  | 48     | PWR              | Analog                                                         | Digital Power Supply Connections; This is also the reference supply voltage for all control inputs and must match the expected input signal swing of control inputs.                             |
| GND                   | PAD    | PWR              | Analog                                                         | Power Supply Ground and Thermal Pad                                                                                                                                                              |
| STATUS0               | 46     | Output           | LVC MOS                                                        | Status pin 0 (see <a href="#">Table 12</a> for details)                                                                                                                                          |
| STATUS1/PIN0          | 45     | Output and Input | LVC MOS<br>no pull resistor                                    | STATUS1: Status pin in SPI/I <sup>2</sup> C modes. For details, see <a href="#">Table 10</a> for pin modes and <a href="#">Table 12</a> for status mode. PIN0: Control pin 0 in pin mode.        |
| SI_MODE1              | 47     | Input            | LVC MOS<br>with 50-k $\Omega$ pullup                           | Serial Interface Mode or Pin mode selection. SI_MODE[1:0]=00: SPI mode; SI_MODE[1:0]=01: I <sup>2</sup> C mode; SI_MODE[1:0]=10: Pin Mode (No serial programming); SI_MODE[1:0]=11: RESERVED     |
| SI_MODE0              | 1      |                  | LVC MOS<br>with 50-k $\Omega$ pulldown                         |                                                                                                                                                                                                  |
| SDI/SDA/PIN1          | 2      | I/O              | LVC MOS in<br>Open drain out<br>LVC MOS in<br>no pull resistor | SDI: SPI Serial Data Input SDA: I <sup>2</sup> C Serial Data (Read/Write bidirectional), open-drain output; requires a pullup resistor in I <sup>2</sup> C mode; PIN1: Control pin 1 in pin mode |
| SDO/AD0/PIN2          | 3      | Output/Input     | LVC MOS out<br>LVC MOS in<br>LVC MOS in<br>no pull resistor    | SDO: SPI Serial Data AD0: I <sup>2</sup> C Address Offset Bit 0 input; PIN2: Control pin 2 in pin mode                                                                                           |
| SCS/AD1/PIN 3         | 4      | Input            | LVC MOS no pull resistor                                       | SCS: SPI Latch Enable AD1: I <sup>2</sup> C Address Offset Bit 1 input; PIN3: Control pin 3 in pin mode                                                                                          |
| SCL/PIN4              | 5      | Input            | LVC MOS no pull resistor                                       | SCL: SPI/I <sup>2</sup> C Clock PIN4: Control pin 4 in pin mode                                                                                                                                  |

## Pin Functions (continued)

| PIN        |     | I/O    | TYPE                              | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|------------|-----|--------|-----------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| NAME       | NO. |        |                                   |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |
| RESETN/PWR | 44  | Input  | LVC MOS with 50-k $\Omega$ pullup | In SPI/I <sup>2</sup> C programming mode, external RESETN signal (active low). RESETN = V <sub>IL</sub> : device in reset (registers values are retained) RESETN = V <sub>IH</sub> : device active. The device can be programmed through SPI while RESETN is held low (this is useful to avoid any false output frequencies at power up). <sup>(2)</sup> In Pin mode this pin controls device core and I/O supply voltage setting. 0 = 1.8 V, 1 = 2.5/3.3 V for the device core and I/O power supply voltage. In pin mode, it is not possible to mix and match the supplies. All supplies should either be 1.8 V or 2.5/3.3 V. |
| REG_CAP    | 40  | Output | Analog                            | Regulator Capacitor; connect a 10- $\mu$ F cap with ESR below 1 $\Omega$ to GND at frequencies above 100 kHz                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |
| PDN        | 43  | Input  | LVC MOS with 50-k $\Omega$ pullup | Power Down Active low. When PDN = V <sub>IH</sub> is normal operation. When PDN = V <sub>IL</sub> , the device is disabled and current consumption minimized. Exiting power down resets the entire device and defaults all registers. It is recommended to connect a capacitor to GND to hold the device in power-down until the digital and PLL related power supplies are stable. See section on power down in the application section.                                                                                                                                                                                      |
| SYN CN     | 42  | Input  | LVC MOS with 50-k $\Omega$ pullup | Active low. Device outputs are synchronized on a low-to-high transition on the SYN CN pin. SYN CN held low disables all outputs.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               |

(2) Note: the device cannot be programmed in I<sup>2</sup>C while RESETN is held low.

## 6 Specifications

### 6.1 Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

|                                                 |                                       | MIN  | MAX                                         | UNIT |
|-------------------------------------------------|---------------------------------------|------|---------------------------------------------|------|
| VDD_PRI, VDD_SEC, VDD_Yx_Yy, VDD_PLL[2:1], DVDD | Supply voltage                        | –0.5 | 4.6                                         | V    |
| V <sub>IN</sub>                                 | Input voltage for CMOS control inputs | –0.5 | 4.6<br>AND<br>V <sub>DVDD</sub> + 0.5       | V    |
|                                                 | Input voltage for PRI/SEC inputs      |      | 4.6<br>AND<br>V <sub>VDDPRI,SEC</sub> + 0.5 | V    |
| V <sub>OUT</sub>                                | Output voltage                        | –0.5 | V <sub>YxYy</sub> + 0.5                     | V    |
| I <sub>IN</sub>                                 | Input current                         |      | 20                                          | mA   |
| I <sub>OUT</sub>                                | Output current                        |      | 50                                          | mA   |
| T <sub>J</sub>                                  | Junction temperature                  |      | 125                                         | °C   |
| T <sub>stg</sub>                                | Storage temperature                   | –65  | 150                                         | °C   |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

### 6.2 ESD Ratings

|                                 |                         | VALUE                                                        | UNIT  |
|---------------------------------|-------------------------|--------------------------------------------------------------|-------|
| V <sub>ESD</sub> <sup>(1)</sup> | Electrostatic discharge | Human Body Model (HBM) ESD Stress Voltage <sup>(2)</sup>     | ±2000 |
|                                 |                         | Charged Device Model (CDM) ESD Stress Voltage <sup>(3)</sup> | ±500  |

- (1) Electrostatic discharge (ESD) to measure device sensitivity and immunity to damage caused by assembly line electrostatic discharges in to the device.
- (2) Level listed above is the passing level per ANSI/ESDA/JEDEC JS-001. JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (3) Level listed above is the passing level per EIA-JEDEC JESD22-C101. JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

|                                                               |                                                                                                                  | MIN          | NOM         | MAX                   | UNIT |
|---------------------------------------------------------------|------------------------------------------------------------------------------------------------------------------|--------------|-------------|-----------------------|------|
| VDD_Yx_Yy                                                     | Output supply voltage                                                                                            | 1.71         | 1.8/2.5/3.3 | 3.465                 | V    |
| VDD_PLL1,<br>VDD_PLL2                                         | Core analog supply voltage                                                                                       | 1.71         | 1.8/2.5/3.3 | 3.465                 | V    |
| DVDD                                                          | Core digital supply voltage                                                                                      | 1.71         | 1.8/2.5/3.3 | 3.465                 | V    |
| VDD_PRI,<br>VDD_SEC                                           | Reference input supply voltage                                                                                   | 1.71         | 1.8/2.5/3.3 | 3.465                 | V    |
| $\Delta VDD/\Delta t$                                         | VDD power-up ramp time (0 to 3.3 V) PDN left open, all VDD tight together PDN low-high is delayed <sup>(1)</sup> |              |             | 50 < t <sub>PDN</sub> | ms   |
| T <sub>A</sub>                                                | Ambient Temperature                                                                                              | –40          |             | 85                    | °C   |
| <b>SDA and SCL in I<sup>2</sup>C Mode (SI_MODE[1:0] = 01)</b> |                                                                                                                  |              |             |                       |      |
| V <sub>I</sub>                                                | Input voltage                                                                                                    | DVDD = 1.8 V |             | 2.45                  | V    |
|                                                               |                                                                                                                  | DVDD = 3.3 V |             | 3.965                 | V    |
| d <sub>R</sub>                                                | Data rate                                                                                                        |              | 100<br>400  |                       | kbps |
| V <sub>IH</sub>                                               | High-level input voltage                                                                                         | 0.7 × DVDD   |             |                       | V    |
| V <sub>IL</sub>                                               | Low-level input voltage                                                                                          | 0.3 × DVDD   |             |                       | V    |
| C <sub>BUS_I2C</sub>                                          | Total capacitive load for each bus line                                                                          |              |             | 400                   | pF   |

- (1) For fast power up ramps under 50 ms and when all supply pins are driven from the same power supply source, PDN can be left floating. For slower power-up ramps or if supply pins are sequenced with uncertain time delays, PDN needs to be held low until DVDD, VDD\_PLLx, and VDD\_PRI/SEC reach at least 1.45-V supply voltage. See application section on mixing power supplies and particularly [Figure 59](#) for details.

### 6.4 Thermal Information, Airflow = 0 LFM<sup>(1)(2)(3)(4)</sup>

| THERMAL METRIC <sup>(1)</sup> |                                              | CDCM6208   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGZ (VQFN) |      |
|                               |                                              | 48 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 30.27      | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | 16.58      | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 6.83       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.23       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | 6.8        | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.06       | °C/W |

- (1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.  
(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).  
(3) Connected to GND with 36 thermal vias (0.3-mm diameter).  
(4) θ<sub>JB</sub> (junction to board) is used for the VQFN package, the main heat flow is from the junction to the GND pad of the VQFN.

## 6.5 Thermal Information, Airflow = 150 LFM<sup>(1)(2)(3)(4)</sup>

| THERMAL METRIC <sup>(1)</sup> |                                              | CDCM6208   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGZ (VQFN) |      |
|                               |                                              | 48 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 21.8       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | —          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 6.61       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.37       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | —          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.06       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

(3) Connected to GND with 36 thermal vias (0.3-mm diameter).

(4) θ<sub>JB</sub> (junction to board) is used for the VQFN package, the main heat flow is from the junction to the GND pad of the VQFN.

## 6.6 Thermal Information, Airflow = 250 LFM<sup>(1)(2)(3)(4)</sup>

| THERMAL METRIC <sup>(1)</sup> |                                              | CDCM6208   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGZ (VQFN) |      |
|                               |                                              | 48 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 19.5       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | —          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 6.6        | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.45       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | —          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.06       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

(3) Connected to GND with 36 thermal vias (0.3-mm diameter).

(4) θ<sub>JB</sub> (junction to board) is used for the VQFN package, the main heat flow is from the junction to the GND pad of the VQFN.

## 6.7 Thermal Information, Airflow = 500 LFM<sup>(1)(2)(3)(4)</sup>

| THERMAL METRIC <sup>(1)</sup> |                                              | CDCM6208   | UNIT |
|-------------------------------|----------------------------------------------|------------|------|
|                               |                                              | RGZ (VQFN) |      |
|                               |                                              | 48 PINS    |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance       | 17.7       | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance    | —          | °C/W |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance         | 6.58       | °C/W |
| ψ <sub>JT</sub>               | Junction-to-top characterization parameter   | 0.58       | °C/W |
| ψ <sub>JB</sub>               | Junction-to-board characterization parameter | —          | °C/W |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance | 1.05       | °C/W |

(1) For more information about traditional and new thermal metrics, see the [IC Package Thermal Metrics](#) application report.

(2) The package thermal resistance is calculated in accordance with JESD 51 and JEDEC2S2P (high-k board).

(3) Connected to GND with 36 thermal vias (0.3-mm diameter).

(4) θ<sub>JB</sub> (junction to board) is used for the VQFN package, the main heat flow is from the junction to the GND pad of the VQFN.

## 6.8 Single-Ended Input Characteristics (SI\_MODE[1:0], SDI/SDA/PIN1, SCL/PIN4, SDO/ADD0/PIN2, SCS/ADD1/PIN3, STATUS1/PIN0, RESETN/PWR, PDN, SYNCN, REF\_SEL)

DVDD = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                                              |                                                             | TEST CONDITIONS                                                     | MIN                    | TYP  | MAX        | UNIT |
|--------------------------------------------------------|-------------------------------------------------------------|---------------------------------------------------------------------|------------------------|------|------------|------|
| V <sub>IH</sub>                                        | Input high voltage                                          |                                                                     | 0.8 × DVDD             |      |            | V    |
| V <sub>IL</sub>                                        | Input low voltage                                           |                                                                     |                        |      | 0.2 × DVDD | V    |
| I <sub>IH</sub>                                        | Input high current                                          | DVDD = 3.465V, V <sub>IH</sub> = 3.465 V (pullup resistor excluded) |                        |      | 30         | μA   |
| I <sub>IL</sub>                                        | Input low current                                           | DVDD = 3.465V, V <sub>IL</sub> = 0 V                                |                        |      | −30        | μA   |
| ΔV/ΔT                                                  | PDN, RESETN, SYNCN, REF_SEL input edge rate                 | 20% – 80%                                                           | 0.75                   |      |            | V/ns |
| minPulse                                               | PDN, RESETN, SYNCN low pulse to trigger proper device reset |                                                                     | 10                     |      |            | ns   |
| C <sub>IN</sub>                                        | Input capacitance                                           |                                                                     |                        | 2.25 |            | pF   |
| RESETN, PWR, SYNCN, PDN, REF_SEL, SI_MODE[1:0]         |                                                             |                                                                     |                        |      |            |      |
| R                                                      | Input pullup and pulldown resistor                          |                                                                     | 35                     | 50   | 65         | kΩ   |
| SDA and SCL in I <sup>2</sup> C Mode (SI_MODE[1:0]=01) |                                                             |                                                                     |                        |      |            |      |
| V <sub>HYS_I2C</sub>                                   | Input hysteresis                                            | DVDD = 1.8 V                                                        | 0.1 V <sub>DVDD</sub>  |      |            | V    |
|                                                        |                                                             | DVDD = 2.5/3.3 V                                                    | 0.05 V <sub>DVDD</sub> |      |            | V    |
| I <sub>H</sub>                                         | High-level input current                                    | V <sub>I</sub> = DVDD                                               | −5                     |      | 5          | μA   |
| V <sub>OL</sub>                                        | Output low voltage                                          | I <sub>OL</sub> = 3 mA                                              |                        |      | 0.2 × DVDD | V    |
| C <sub>IN</sub>                                        | Input capacitance pin                                       |                                                                     |                        |      | 5          | pF   |

## 6.9 Single-Ended Input Characteristics (PRI\_REF, SEC\_REF)

VDD\_PRI, VDD\_SEC = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER         | TEST CONDITIONS                  | MIN                                                  | TYP  | MAX                   | UNIT |
|-------------------|----------------------------------|------------------------------------------------------|------|-----------------------|------|
| f <sub>IN</sub>   | VDD_PRI/SEC = 1.8 V              | 0.008                                                |      | 200                   | MHz  |
|                   | VDD_PRI/SEC = 3.3 V              | 0.008                                                |      | 250                   | MHz  |
| V <sub>IH</sub>   | Input high voltage               | 0.8 × VDD_PRI/VDD_SEC                                |      |                       | V    |
| V <sub>IL</sub>   | Input low voltage                |                                                      |      | 0.2 × VDD_PRI/VDD_SEC | V    |
| V <sub>HYST</sub> | Input hysteresis                 | 20                                                   | 65   | 150                   | mV   |
| I <sub>IH</sub>   | Input high current               | VDD_PRI/VDD_SEC = 3.465 V, V <sub>IH</sub> = 3.465 V |      | 30                    | μA   |
| I <sub>IL</sub>   | Input low current                | VDD_PRI/VDD_SEC = 3.465 V, V <sub>IL</sub> = 0 V     |      | –30                   | μA   |
| ΔV/ΔT             | Reference input edge rate        | 20% – 80%                                            | 0.75 |                       | V/ns |
| IDC <sub>SE</sub> | f <sub>PRI</sub> ≤ 200 MHz       | 40%                                                  |      | 60%                   |      |
|                   | 200 ≤ f <sub>PRI</sub> ≤ 250 MHz | 43%                                                  |      | 60%                   |      |
| C <sub>IN</sub>   | Input capacitance                |                                                      | 2.25 |                       | pF   |

## 6.10 Differential Input Characteristics (PRI\_REF, SEC\_REF)

VDD\_PRI, VDD\_SEC = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER           |                                                | TEST CONDITIONS                                                           | MIN                         | TYP | MAX                         | UNIT             |
|---------------------|------------------------------------------------|---------------------------------------------------------------------------|-----------------------------|-----|-----------------------------|------------------|
| f <sub>IN</sub>     | Reference and bypass input frequency           |                                                                           | 0.008                       |     | 250                         | MHz              |
| V <sub>I</sub>      | Differential input voltage swing, peak-to-peak | VDD_PRI/SEC = 2.5/3.3 V                                                   | 0.2                         |     | 1.6                         | V <sub>PP</sub>  |
|                     |                                                | VDD_PRI/SEC = 1.8 V                                                       | 0.2                         |     | 1                           | V <sub>PP</sub>  |
| V <sub>ICM</sub>    | Input common-mode voltage                      | CML input signaling, R4[7:6] = 00                                         | VDD_PRI/<br>VDD_SEC<br>-0.4 |     | VDD_PRI/<br>VDD_SEC<br>-0.1 | V                |
| V <sub>ICM</sub>    | Input common-mode voltage                      | LVDS, VDD_PRI/SEC = 1.8/2.5/3.3 V, R4[7:6] = 01, R4.1 = d.c., R4.0 = d.c. | 0.8                         | 1.2 | 1.5                         | V                |
| V <sub>HYST</sub>   | Input hysteresis                               | LVDS (Q4[7:6,4:3] = 01)                                                   | 15                          |     | 65                          | mV <sub>pp</sub> |
|                     |                                                | CML (Q4[7:6,4:3] = 00)                                                    | 20                          |     | 85                          | mV <sub>pp</sub> |
| I <sub>IH</sub>     | Input high current                             | VDD_PRI/SEC = 3.465 V, V <sub>IH</sub> = 3.465 V                          |                             |     | 30                          | μA               |
| I <sub>IL</sub>     | Input low current                              | VDD_PRI/SEC = 3.465V, V <sub>IL</sub> = 0 V                               |                             |     | −30                         | μA               |
| ΔV/ΔT               | Reference input edge rate                      | 20% – 80%                                                                 | 0.75                        |     |                             | V/ns             |
| IDC <sub>DIFF</sub> | Reference input duty cycle                     |                                                                           | 30%                         |     | 70%                         |                  |
| C <sub>IN</sub>     | Input capacitance                              |                                                                           |                             | 2.7 |                             | pF               |

## 6.11 Crystal Input Characteristics (SEC\_REF)

VDD\_SEC = 1.71 to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                          | TEST CONDITIONS         | MIN         | TYP  | MAX                | UNIT |
|------------------------------------|-------------------------|-------------|------|--------------------|------|
| Mode of oscillation                |                         | Fundamental |      |                    |      |
| Frequency                          | See note <sup>(1)</sup> | 10          |      | 30.72              | MHz  |
|                                    | See note <sup>(2)</sup> | 30.73       |      | 50                 | MHz  |
| Equivalent Series Resistance (ESR) | 10 MHz                  |             |      | 150 <sup>(3)</sup> | Ω    |
|                                    | 25 MHz                  |             |      | 70 <sup>(4)</sup>  |      |
|                                    | 50 MHz                  |             |      | 30 <sup>(5)</sup>  |      |
| On-chip load capacitance           | 1.8-V / 3.3-V SEC_REFP  | 3.5         | 4.5  | 5.5                | pF   |
|                                    | 1.8-V SEC_REFN          | 5.5         | 7.25 | 8.5                |      |
|                                    | 3.3-V SEC_REFN          | 6.5         | 7.34 | 8.5                |      |
| Drive level                        | See note <sup>(6)</sup> |             |      | 200                | μW   |

- (1) Verified with crystals specified for a load capacitance of C<sub>L</sub> = 8 pF, the PCB related capacitive load was estimated to be 2.3 pF, and completed with a load capacitors of 4 pF on each crystal pin connected to GND. XTALs tested: NX3225GA 10MHz EXS00A-CG02813 CRG, NX3225GA 19.44MHz EXS00A-CG02810 CRG, NX3225GA 25MHz EXS00A-CG02811 CRG, and NX3225GA 30.72MHz EXS00A-CG02812 CRG.
- (2) For 30.73 MHz to 50 MHz, TI recommends to verify sufficient negative resistance and initial frequency accuracy with the crystal vendor. The 50-MHz use case was verified with a NX3225GA 50MHz EXS00A-CG02814 CRG. To meet a minimum frequency error, the best choice of the XTAL was one with C<sub>L</sub> = 7 pF instead of C<sub>L</sub> = 8 pF.
- (3) With NX3225GA\_10M the measured remaining negative resistance on the EVM is 6430 Ω (43 x margin)
- (4) With NX3225GA\_25M the measured remaining negative resistance on the EVM is 1740 Ω (25 x margin)
- (5) With NX3225GA\_50M the measured remaining negative resistance on the EVM is 350 Ω (11 x margin)
- (6) Maximum drive level measured was 145 μW; XTAL should at least tolerate 200 μW

## 6.12 Single-Ended Output Characteristics (STATUS1, STATUS0, SDO, SDA)

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V; T<sub>A</sub> = –40°C to 85°C (Output load capacitance 10 pF unless otherwise noted)

| PARAMETER                                             | TEST CONDITIONS                                                                                                           | MIN        | TYP  | MAX        | UNIT               |
|-------------------------------------------------------|---------------------------------------------------------------------------------------------------------------------------|------------|------|------------|--------------------|
| V <sub>OH</sub> Output high voltage                   | Status 1, Status 0, and SDO only; SDA is open drain and relies on external pullup for high output; I <sub>OH</sub> = 1 mA | 0.8 × DVDD |      |            | V                  |
| V <sub>OL</sub> Output low voltage                    | I <sub>OL</sub> = 1 mA                                                                                                    |            |      | 0.2 × DVDD | V                  |
| V <sub>slew</sub> Output slew rate                    | 30% – 70%                                                                                                                 | 0.5        |      |            | V/ns               |
| I <sub>OZH</sub> 3-state output high current          | DVDD = 3.465 V, V <sub>IH</sub> = 3.465 V                                                                                 |            |      | 5          | μA                 |
| I <sub>OZL</sub> 3-state output low current           | DVDD = 3.465 V, V <sub>IL</sub> = 0 V                                                                                     |            |      | –5         | μA                 |
| t <sub>LOS</sub> Status loss of signal detection time | LOS_REFFvco                                                                                                               |            | 1    | 2          | 1/f <sub>PFD</sub> |
| t <sub>LOCK</sub> Status PLL lock detection time      | Detect lock                                                                                                               |            | 2304 |            | 1/f <sub>PFD</sub> |
|                                                       | Detect unlock                                                                                                             |            | 512  |            |                    |

## 6.13 PLL Characteristics

VDD\_PLLx, VDD\_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                                                           | TEST CONDITIONS                                                                                                                                                                | MIN   | TYP   | MAX  | UNIT   |
|---------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------|-------|------|--------|
| f <sub>VCO</sub> VCO frequency range                                | V1                                                                                                                                                                             | 2.39  |       | 2.55 | GHz    |
|                                                                     | V2                                                                                                                                                                             | 2.94  |       | 3.13 |        |
| K <sub>VCO</sub> VCO gain                                           | V1, 2.39 GHz                                                                                                                                                                   |       | 178   |      | MHz/V  |
|                                                                     | V1, 2.50 GHz                                                                                                                                                                   |       | 204   |      |        |
|                                                                     | V1, 2.55 GHz                                                                                                                                                                   |       | 213   |      |        |
|                                                                     | V2, 2.94 GHz                                                                                                                                                                   |       | 236   |      |        |
|                                                                     | V2, 3.00 GHz                                                                                                                                                                   |       | 250   |      |        |
|                                                                     | V2, 3.13 GHz                                                                                                                                                                   |       | 283   |      |        |
| f <sub>PFD</sub> PFD input frequency                                |                                                                                                                                                                                | 0.008 |       | 100  | MHz    |
| I <sub>CP-L</sub> High impedance mode charge pump leakage           |                                                                                                                                                                                |       | ±700  |      | nA     |
| f <sub>FOM</sub> Estimated PLL figure of merit (FOM)                | Measured in-band phase noise at the VCO output minus 20log(N-divider) at the flat region                                                                                       |       | –224  |      | dBc/Hz |
| t <sub>STARTUP</sub> Start-up time (see <a href="#">Figure 60</a> ) | Power supply ramp time of 1ms from 0 V to 1.7 V, final frequency accuracy of 10 ppm, f <sub>PFD</sub> = 25 MHz, CDCM6208 pin mode use case #2, C <sub>PDN_to_GND</sub> = 22 nF |       |       |      |        |
|                                                                     | with PRI input signal                                                                                                                                                          |       | 12.8  |      | ms     |
|                                                                     | with NDK 25 MHz crystal                                                                                                                                                        |       | 12.85 |      | ms     |

## 6.14 LVCMOS Output Characteristics

VDD\_Yx\_Yy = 1.71 V to 1.89V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                |                                          | TEST CONDITIONS                                          | MIN                    | TYP    | MAX                    | UNIT   |
|--------------------------|------------------------------------------|----------------------------------------------------------|------------------------|--------|------------------------|--------|
| f <sub>OUT-F</sub>       | Output frequency                         | Fract out divVDD_Yx_Yy = 2.5/3.3 V                       | 0.78                   |        | 250                    | MHz    |
|                          |                                          | Integer out divVDD_Yx_Yy = 2.5/3.3 V                     | 1.55                   |        | 250                    |        |
|                          |                                          | Int or frac out divVDD_Yx_Yy = 1.8 V                     | 0.78/1.5               |        | 200                    |        |
| f <sub>ACC-F</sub>       | Output frequency error <sup>(1)</sup>    | Fractional output divider                                | –1                     |        | 1                      | ppm    |
| V <sub>OH</sub>          | Output high voltage (normal mode)        | VDD_Yx = min to max,<br>I <sub>OH</sub> = –1 mA          | 0.8 ×<br>VDD_Y<br>x_Yy |        |                        | V      |
| V <sub>OL</sub>          | Output low voltage (normal mode)         | VDD_Yx = min to max,<br>I <sub>OL</sub> = 100 μA         |                        |        | 0.2 ×<br>VDD_Y<br>x_Yy | V      |
| V <sub>OH</sub>          | Output high voltage (slow mode)          | VDD_Yx = min to max,<br>I <sub>OH</sub> = –100 μA        | 0.7 ×<br>VDD_Y<br>x_Yy |        |                        | V      |
| V <sub>OL</sub>          | Output low voltage (slow mode)           | VDD_Yx = min to max,<br>I <sub>OL</sub> = 100 μA         |                        |        | 0.3 ×<br>VDD_Y<br>x_Yy | V      |
| I <sub>OH</sub>          | Output high current                      | V <sub>OUT</sub> = VDD_Yx_Yy/2                           |                        |        |                        |        |
|                          |                                          | Normal mode                                              | –50                    |        | –8                     | mA     |
|                          |                                          | Slow mode                                                | –45                    |        | –5                     | mA     |
| I <sub>OL</sub>          | Output low current                       | V <sub>OUT</sub> = VDD_Yx_Yy/2                           |                        |        |                        |        |
|                          |                                          | Normal mode                                              | 10                     |        | 55                     | mA     |
|                          |                                          | Slow mode                                                | 5                      |        | 40                     | mA     |
| t <sub>SLEW-RATE-N</sub> | Output rise/fall slew rate (normal mode) | 20% to 80%, VDD_Yx_Yy = 2.5/3.3 V, C <sub>L</sub> = 5 pF |                        | 5.37   |                        | V/ns   |
|                          | Output rise/fall slew rate (normal mode) | 20% to 80%, VDD_Yx_Yy = 1.8 V, C <sub>L</sub> = 5 pF     |                        | 2.62   |                        | V/ns   |
| t <sub>SLEW-RATE-S</sub> | Output rise/fall slew rate (slow mode)   | 20% to 80%, VDD_Yx_Yy = 2.5/3.3 V, C <sub>L</sub> = 5 pF |                        | 4.17   |                        | V/ns   |
|                          | Output rise/fall slew rate (slow mode)   | 20% to 80%, VDD_Yx_Yy = 1.8 V, C <sub>L</sub> = 5 pF     |                        | 1.46   |                        | V/ns   |
| PN-floor                 | Phase noise floor                        | f <sub>OUT</sub> = 122.88 MHz                            |                        | –159.5 | 154                    | dBc/Hz |
| ODC                      | Output duty cycle                        | Not in bypass mode                                       | 45%                    |        | 55%                    |        |
| R <sub>OUT</sub>         | Output impedance                         | V <sub>OUT</sub> = VDD_Yx/2                              |                        |        |                        |        |
|                          |                                          | Normal mode                                              | 30                     | 50     | 90                     | Ω      |
|                          |                                          | Slow mode                                                | 45                     | 74     | 130                    |        |

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of a multiple 1 over 2<sup>20</sup>, the actual output frequency error is 0.

Note: In LVCMOS Mode, positive and negative outputs are in phase.

## 6.15 LVPECL (High-Swing CML) Output Characteristics

VDD\_Yx\_Yy = 1.71 V to 3.465 V, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                      |                                          | TEST CONDITIONS                                                         |            | MIN             | TYP                  | MAX    | UNIT   |
|--------------------------------|------------------------------------------|-------------------------------------------------------------------------|------------|-----------------|----------------------|--------|--------|
| f <sub>OUT-I</sub>             | Output frequency                         | Integer Output Divider                                                  | CDCM6208V1 | 1.55            |                      | 800    | MHz    |
|                                |                                          |                                                                         | CDCM6208V2 | 1.91            |                      | 800    |        |
| V <sub>CM-DC</sub>             | Output DC-coupled common-mode voltage    | DC coupled with 50-Ω external termination to VDD_Yx_Yy                  |            | VDD_Yx_Yy – 0.4 |                      |        | V      |
| V <sub>OD</sub>                | Differential output voltage              | 100-Ω diff load AC coupling (see Figure 12), f <sub>OUT</sub> ≤ 250 MHz |            |                 |                      |        |        |
|                                |                                          | 1.71 V ≤ VDD_Yx_Yy ≤ 1.89 V                                             |            | 0.45            | 0.75                 | 1.12   | V      |
|                                |                                          | 2.375 V ≤ VDD_Yx_Yy ≤ 3.465 V                                           |            | 0.6             | 0.8                  | 1.12   | V      |
|                                |                                          | 100-Ω diff load AC coupling (see Figure 12), f <sub>OUT</sub> ≥ 250     |            |                 |                      |        |        |
|                                |                                          | 1.71 V ≤ VDD_Yx_Yy ≤ 1.89 V                                             |            |                 | 0.73                 |        | V      |
|                                |                                          | 2.375 V ≤ VDD_Yx_Yy ≤ 3.465 V                                           |            | 0.55            | 0.75                 | 1.12   | V      |
| V <sub>OUT</sub>               | Differential output peak-to-peak voltage |                                                                         |            |                 | 2 ×  V <sub>OD</sub> |        | V      |
| t <sub>R</sub> /t <sub>F</sub> | Output rise/fall time                    | ±200 mV around crossing point                                           |            | 109             |                      | 217    | ps     |
|                                |                                          | 20% to 80% V <sub>OD</sub>                                              |            |                 | 211                  |        | ps     |
| t <sub>slew</sub>              | Output rise/fall slew rate               |                                                                         |            | 3.7             | 5.1                  | 7.3    | V/ns   |
| PN-floor                       | Phase noise floor                        | VDD_Yx_Yy = 3.3 V (see Figure 54)                                       |            |                 | –161.4               | –155.8 | dBc/Hz |
| ODC                            | Output duty cycle                        | Not in bypass mode                                                      |            | 47.5%           |                      | 52.5%  |        |
| R <sub>OUT</sub>               | Output impedance                         | Measured from pin to VDD_Yx_Yy                                          |            |                 | 50                   |        | Ω      |

## 6.16 CML Output Characteristics

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.71 V to 1.89 V, 2.375V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                      |                                          | TEST CONDITIONS                                       |                     | MIN              | TYP                  | MAX    | UNIT   |
|--------------------------------|------------------------------------------|-------------------------------------------------------|---------------------|------------------|----------------------|--------|--------|
| f <sub>OUT-I</sub>             | Output frequency                         | Integer output divider                                | V1                  | 1.55             |                      | 800    | MHz    |
|                                |                                          |                                                       | V2                  | 1.91             |                      | 800    |        |
| V <sub>CM-AC</sub>             | Output AC-coupled common-mode voltage    | AC-coupled with 50-Ω receiver termination             |                     | VDD_Yx_Yy – 0.46 |                      |        | V      |
| V <sub>CM-DC</sub>             | Output DC-coupled common-mode voltage    | DC-coupled with 50-Ω on-chip termination to VDD_Yx_Yy |                     | VDD_Yx_Yy – 0.2  |                      |        | V      |
| V <sub>OD</sub>                | Differential output voltage              | 100-Ω diff load AC coupling (see Figure 12)           |                     | 0.3              | 0.45                 | 0.58   | V      |
| V <sub>OUT</sub>               | Differential output peak-to-peak voltage |                                                       |                     |                  | 2 ×  V <sub>OD</sub> |        | V      |
| t <sub>R</sub> /t <sub>F</sub> | Output rise/fall time                    | 20% to 80%                                            | VDDYx = 1.8 V       | 100              | 151                  | 300    | ps     |
|                                |                                          |                                                       | VDDYx = 2.5 V/3.3 V | 100              | 143                  | 200    | ps     |
| PN-floor                       | Phase noise floor at > 5-Hz offset       | f <sub>OUT</sub> = 122.88 MHz                         | VDD_Yx_Yy = 1.8 V   |                  | –161.2               | –155.8 | dBc/Hz |
|                                |                                          |                                                       | VDD_Yx_Yy = 3.3 V   |                  | 161.2                | –153.8 | dBc/Hz |
| ODC                            | Output duty cycle                        | Not in bypass mode                                    |                     | 47.5%            |                      | 52.5%  |        |
| R <sub>OUT</sub>               | Output impedance                         | Measured from pin to VDD_Yx_Yy                        |                     |                  | 50                   |        | Ω      |

## 6.17 LVDS (Low-Power CML) Output Characteristics

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.71 V to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                      |                                          | TEST CONDITIONS                                       |                    | MIN                  | TYP    | MAX    | UNIT   |
|--------------------------------|------------------------------------------|-------------------------------------------------------|--------------------|----------------------|--------|--------|--------|
| f <sub>OUT-I</sub>             | Output frequency                         | Integer output divider                                | CDCM6208V1         | 1.55                 |        | 400    | MHz    |
|                                |                                          |                                                       | CDCM6208V2         | 1.91                 |        | 400    |        |
| f <sub>OUT-F</sub>             | Output frequency                         | Fractional output divider                             |                    | 0.78                 |        | 400    | MHz    |
| f <sub>ACC-F</sub>             | Output frequency error <sup>(1)</sup>    | Fractional output divider                             |                    | –1                   |        | 1      | ppm    |
| V <sub>CM-AC</sub>             | Output AC-coupled common-mode voltage    | AC-coupled with 50-Ω receiver termination             |                    | VDD_Yx_Yy – 0.76     |        |        | V      |
| V <sub>CM-DC</sub>             | Output DC-coupled common-mode voltage    | DC-coupled with 50-Ω on-chip termination to VDD_Yx_Yy |                    | VDD_Yx_Yy – 0.13     |        |        | V      |
| V <sub>OD</sub>                | Differential output voltage              | 100-Ω diff load AC coupling (see Figure 12)           |                    | 0.247                | 0.34   | 0.454  | V      |
| V <sub>OUT</sub>               | Differential output peak-to-peak voltage |                                                       |                    | 2 ×  V <sub>OD</sub> |        |        | V      |
| t <sub>R</sub> /t <sub>F</sub> | Output rise/fall time                    | ±100 mV around crossing point                         |                    |                      |        | 300    | ps     |
| PN-floor                       | Phase noise floor                        | f <sub>OUT</sub> = 122.88 MHz                         | VDD_Yx = 1.8 V     |                      | –159.3 | –154.5 | dBc/Hz |
|                                |                                          |                                                       | VDD_Yx = 2.5/3.3 V |                      | –159.1 | –154.9 |        |
| ODC                            | Output duty cycle                        | Not in bypass mode                                    | Y[3:0]             | 47.5%                |        | 52.5%  |        |
|                                |                                          |                                                       | Y[7:4]             | 45%                  |        | 55%    |        |
| R <sub>OUT</sub>               | Output impedance                         | Measured from pin to VDD_Yx_Yy                        |                    |                      | 167    |        | Ω      |

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of a multiple of 1 over 2<sup>20</sup>, the actual output frequency error is 0.

## 6.18 HCSL Output Characteristics

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.71 to 1.89 V, 2.375 V to 2.625 V, 3.135 V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                      |                                          | TEST CONDITIONS                                                                                |                    | MIN                  | TYP    | MAX  | UNIT   |
|--------------------------------|------------------------------------------|------------------------------------------------------------------------------------------------|--------------------|----------------------|--------|------|--------|
| f <sub>OUT-I</sub>             | Output frequency                         | Integer output divider                                                                         | V1                 | 1.55                 |        | 400  | MHz    |
|                                |                                          |                                                                                                | V2                 | 1.91                 |        | 400  |        |
| f <sub>OUT-F</sub>             | Output frequency                         | Fractional output divider                                                                      |                    | 0.78                 |        | 400  | MHz    |
| f <sub>ACC-F</sub>             | Output frequency error <sup>(1)</sup>    | Fractional output divider                                                                      |                    | –1                   |        | 1    | ppm    |
| V <sub>CM</sub>                | Output common-mode voltage               | VDD_Yx_Yy = 2.5/3.3 V                                                                          |                    | 0.2                  | 0.34   | 0.55 | V      |
|                                |                                          | VDD_Yx_Yy = 1.8 V                                                                              |                    | 0.2                  | 0.33   | 0.55 |        |
| V <sub>OD</sub>                | Differential output voltage              | VDD_Yx_Yy = 2.5/3.3 V;                                                                         |                    | 0.4                  | 0.67   | 1    | V      |
| V <sub>OD</sub>                | Differential output voltage              | VDD_Yx_Yy = 1.8 V                                                                              |                    | 0.4                  | 0.65   | 1    | V      |
| V <sub>OUT</sub>               | Differential output peak-to-peak voltage | VDD_Yx_Yy = 2.5/3.3 V                                                                          |                    | 1                    |        | 2.1  | V      |
|                                | Differential output peak-to-peak voltage | VDD_Yx_Yy = 1.8 V                                                                              |                    | 2 ×  V <sub>OD</sub> |        |      |        |
| t <sub>R</sub> /t <sub>F</sub> | Output rise/fall time                    | Measured from V <sub>DIFF</sub> = –100 mV to V <sub>DIFF</sub> = +100mV, VDD_Yx_Yy = 2.5/3.3 V |                    | 100                  | 167    | 250  | ps     |
| t <sub>R</sub> /t <sub>F</sub> | Output rise/fall time                    | Measured from V <sub>DIFF</sub> = –100 mV to V <sub>DIFF</sub> = +100 mV, VDD_Yx_Yy = 1.8 V    |                    | 120                  | 192    | 295  | ps     |
| PN-floor                       | Phase noise floor                        | f <sub>OUT</sub> = 122.88 MHz                                                                  | VDD_Yx_Yy = 1.8 V  |                      | –158.8 | –153 | dBc/Hz |
|                                |                                          |                                                                                                | VDD_Yx = 2.5/3.3 V |                      | –157.6 | –153 |        |
| ODC                            | Output duty cycle                        | Not in bypass mode                                                                             |                    | 45%                  |        | 55%  |        |

(1) The User's GUI calculates exact frequency error. It is a fixed, static offset. If the desired output target frequency is with the exact reach of a ½ 2<sup>20</sup> multiple, the actual output frequency error is 0.

## 6.19 Output Skew and Sync to Output Propagation Delay Characteristics

VDD\_Yx\_Yy = 1.71 to 1.89 V, 2.375 V to 2.625 V, 3.135V to 3.465 V, T<sub>A</sub> = –40°C to 85°C

| PARAMETER                                                                                                    |                                                                                        | TEST CONDITIONS                                               |        | MIN | TYP  | MAX | UNIT                |
|--------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------|---------------------------------------------------------------|--------|-----|------|-----|---------------------|
| t <sub>PD-PS</sub>                                                                                           | Propagation delay SYNCN↑ to output toggling high                                       | V1: f <sub>VCO</sub> = 2.5 GHz                                | PS_A=4 | 9   | 10.5 | 11  | 1/f <sub>PS_A</sub> |
|                                                                                                              |                                                                                        |                                                               | PS_A=5 | 9   | 10.2 | 11  | 1/f <sub>PS_A</sub> |
|                                                                                                              |                                                                                        |                                                               | PS_A=6 | 9   | 10.0 | 11  | 1/f <sub>PS_A</sub> |
|                                                                                                              |                                                                                        | V2: f <sub>VCO</sub> = 3 GHz                                  | PS_A=4 | 10  | 10.9 | 12  | 1/f <sub>PS_A</sub> |
|                                                                                                              |                                                                                        |                                                               | PS_A=5 | 9   | 10.5 | 11  | 1/f <sub>PS_A</sub> |
|                                                                                                              |                                                                                        |                                                               | PS_A=6 | 9   | 10.2 | 11  | 1/f <sub>PS_A</sub> |
| Δt <sub>PD-PS</sub>                                                                                          | Part-to-part propagation delay variation SYNCN↑ to output toggling high <sup>(1)</sup> | Fixed supply voltage, temp, and device setting <sup>(1)</sup> |        | 0   |      | 1   | 1/f <sub>PS_A</sub> |
| OUTPUT SKEW – ALL OUTPUTS USE IDENTICAL OUTPUT SIGNALING, INTEGER DIVIDERS ONLY; PS_A = PS_B = 6, OUTDIV = 4 |                                                                                        |                                                               |        |     |      |     |                     |
| t <sub>SK,LVDS</sub>                                                                                         | Skew between Y[7:4] LVDS                                                               | Y[7:4] = LVDS                                                 |        |     |      | 40  | ps                  |
| t <sub>SK,LVDS</sub>                                                                                         | Skew between Y[3:0] LVDS                                                               | Y[3:0] = LVDS                                                 |        |     |      | 40  | ps                  |
| t <sub>SK,LVDS</sub>                                                                                         | Skew between Y[7:0] LVDS                                                               | Y[7:0] = LVDS                                                 |        |     |      | 80  | ps                  |
| t <sub>SK,CML</sub>                                                                                          | Skew between Y[3:0] CML                                                                | Y[3:0] = CML                                                  |        |     |      | 40  | ps                  |
| t <sub>SK,PECL</sub>                                                                                         | Skew between Y[3:0] PECL                                                               | Y[3:0] = LVPECL                                               |        |     |      | 40  | ps                  |
| t <sub>SK,HCSL</sub>                                                                                         | Skew between Y[7:4] HCSL                                                               | Y[7:4] = HCSL                                                 |        |     |      | 40  | ps                  |
| t <sub>SK,SE</sub>                                                                                           | Skew between Y[7:4] CMOS                                                               | Y[7:4] = CMOS                                                 |        |     |      | 50  | ps                  |
| OUTPUT SKEW - MIXED SIGNAL OUTPUT CONFIGURATION, INTEGER DIVIDERS ONLY; PS_A = PS_B = 6, OUTDIV = 4          |                                                                                        |                                                               |        |     |      |     |                     |
| t <sub>SK,CMOS-LVDS</sub>                                                                                    | Skew between Y[7:4] LVDS and CMOS mixed                                                | Y[4] = CMOS, Y[7:5] = LVDS                                    |        |     |      | 2.5 | ns                  |
| t <sub>SK,CMOS-PECL</sub>                                                                                    | Skew between Y[7:0] CMOS and LVPECL mixed                                              | Y[7:4] = CMOS, Y[3:0] = LVPECL                                |        |     |      | 2.5 | ns                  |
| t <sub>SK,PECL-LVDS</sub>                                                                                    | Skew between Y[3:0] LVPECL and LVDS mixed                                              | Y[0] = LVPECL, Y[3:1] = LVDS                                  |        |     |      | 120 | ps                  |
| t <sub>SK,PECL-CML</sub>                                                                                     | Skew between Y[3:0] LVPECL and CML mixed                                               | Y[0] = LVPECL, Y[3:1] = CML                                   |        |     |      | 40  | ps                  |
| t <sub>SK,LVDS-PECL</sub>                                                                                    | Skew between Y[7:0] LVDS and LVPECL mixed                                              | Y[7:4] = LVDS, Y[3:0] = LVPECL                                |        |     |      | 180 | ps                  |
| t <sub>SK,LVDS-HCSL</sub>                                                                                    | Skew between Y[7:4] LVDS and HCSL mixed                                                | Y[4] = LVDS, Y[7:5] = HCSL                                    |        |     |      | 250 | ps                  |
| OUTPUT SKEW - USING FRACTIONAL OUTPUT DIVISION; PS_A = PS_B = 6, OUTDIV = 3.125                              |                                                                                        |                                                               |        |     |      |     |                     |
| t <sub>SK,DIFF, frac</sub>                                                                                   | Skew between Y[7:4] LVDS using all fractional divider with the same divider setting    | Y[7:4] = LVDS                                                 |        |     |      | 200 | ps                  |

(1) SYNC is toggled 10,000 times for each device. Test is repeated over process voltage and temperature (PVT).

## CDCM6208

SCAS931G – MAY 2012 – REVISED JANUARY 2018

www.ti.com

### 6.20 Device Individual Block Current Consumption

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 1.8 V, 2.5 V, or 3.3 V, T<sub>A</sub> = –40°C to 85°C, Output Types = LVPECL/CML/LVDS/LVCMOS/HCSL

| BLOCK                   | CONDITION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   | TYPICAL CURRENT CONSUMPTION (mA)                                                                                                                                                                 |
|-------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Core                    | CDCM6208 Core, active mode, PS_A = PS_B = 4                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 75                                                                                                                                                                                               |
| Output Buffer           | CML output, AC-coupled with 100-Ω diff load                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 24.25                                                                                                                                                                                            |
|                         | LVPECL, AC-coupled with 100-Ω diff load                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     | 40                                                                                                                                                                                               |
|                         | LVCMOS output, transient, 'C <sub>L</sub> ' load, 'f' MHz output frequency, 'V' output swing                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | $1.8 + V \times f_{OUT} \times (C_L + 12 \times 10^{-12}) \times 10^3$                                                                                                                           |
|                         | LVDS output, AC-coupled with 100-Ω diff load                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                | 19.7                                                                                                                                                                                             |
|                         | HCSL output, 50-Ω load to GND on each output pin                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 31                                                                                                                                                                                               |
| Output Divide Circuitry | Integer Divider Bypass (Divide = 1)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 3                                                                                                                                                                                                |
|                         | Integer Divide Enabled, Divide > 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 8                                                                                                                                                                                                |
|                         | Fractional Divider Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 12                                                                                                                                                                                               |
|                         | additional current when PS_A differs from PS_B                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 15                                                                                                                                                                                               |
| Total Device, CDCM6208  | Device Settings (V2)<br>1. PRI input enabled, set to LVDS mode<br>2. SEC input XTAL<br>3. Input bypass off, PRI only sent to PLL<br>4. Reference clock 30.72 MHz<br>5. PRI input divider set to 1<br>6. Reference input divider set to 1<br>7. Charge Pump Current = 2.5 mA<br>8. VCO Frequency = 3.072 GHz<br>9. PS_A = PS_B divider ration = 4<br>10. Feedback divider ratio = 25<br>11. Output divider ratio = 5<br>12. Fractional divider pre-divider = 2<br>13. Fractional divider core input frequency = 384 MHz<br>14. Fractional divider value = 3.84, 5.76, 3.072, 7.68<br>15. CML outputs selected for CH0-3 (153.6 MHz)<br>LVDS outputs selected for CH4-7 (100 MHz, 66.66 MHz, 125 MHz, 50 MHz) | (excl. I <sub>termination_resistors</sub> )<br>1.8 V: 251 mA<br>2.5 V: 254 mA<br>3.3 V: 257 mA<br>(incl. I <sub>termination_resistors</sub> )<br>1.8 V: 310 mA<br>2.5 V: 313 mA<br>3.3 V: 316 mA |
| Total Device, CDCM6208  | Power Down (PDN = '0')                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | 0.35                                                                                                                                                                                             |

**Helpful Note:** The CDCM6208 User GUI does an excellent job estimating the total device current consumption based on the actual device configuration. Therefore, TI recommends using the GUI to estimate device power consumption.

The individual supply pin current consumption for Pin mode P23 was measured to come out the following:

**Table 1. Individual Supplies Measured**

|              |                                                                          | Y0-1  | Y2-3  | Y4    | Y5    | Y6    | Y7    | SEC<br>(V <sub>SEC</sub> = 1.8V) | SEC<br>(V <sub>SEC</sub> = 2.5V) | PRI | PLL1  | PLL2 | VCO | DVDD   | Total    |
|--------------|--------------------------------------------------------------------------|-------|-------|-------|-------|-------|-------|----------------------------------|----------------------------------|-----|-------|------|-----|--------|----------|
| Customer EVM | PWR PIN 39 = GND<br>V <sub>PRI</sub> = 1.8 V<br>V <sub>OUT</sub> = 1.8 V | 61 mA | 40 mA | 21 mA | 29 mA | 30 mA | 31 mA | 12 mA                            |                                  |     | 70 mA |      |     | 1.5 mA | 295.5 mA |

## 6.21 Worst Case Current Consumption

VDD\_Yx\_Yy, VDD\_PRI, VDD\_SEC, VDD\_PLLx, DVDD, VDD\_VCO = 3.45 V, T<sub>A</sub> = T-40 °C to 85 °C, Output Types = maximum swing, all blocks including duty cycle correction and fractional divider enabled and operating at maximum operation

| BLOCK                  | CONDITION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | CURRENT CONSUMPTION TYP / MAX                                                |
|------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| Total Device, CDCM6208 | <p>All conditions over PVT, AC-coupled outputs with all outputs terminated, device configuration:<br/>Device Settings (V2)</p> <ol style="list-style-type: none"> <li>PRI input enabled, set to LVDS mode</li> <li>SEC input XTAL</li> <li>Input bypass off, PRI only sent to PLL</li> <li>Reference clock 30.72 MHz</li> <li>PRI input divider set to 1</li> <li>Reference input divider set to 1</li> <li>Charge Pump Current = 2.5 mA</li> <li>VCO Frequency = 3.072 GHz</li> <li>PS_A = PS_B divider ration = 4</li> <li>Feedback divider ratio = 25</li> <li>Output divider ratio = 5</li> <li>Fractional divider pre-divider = 2</li> <li>Fractional divider core input frequency = 384 MHz</li> <li>Fractional divider value = 3.84, 5.76, 3.072, 7.68</li> <li>CML outputs selected for CH0-3 (153.6 MHz)</li> <li>LVDS outputs selected for CH4-7 (100MHz, 66.66 MHz, 125 MHz, 50 MHz)</li> </ol> | <p>1.8 V: 310 mA / +21% (excl term)<br/>3.3 V: 318 mA / +21% (excl term)</p> |

## 6.22 Timing Requirements, I<sup>2</sup>C Timing

| PARAMETER                  |                                                                                                                  | STANDARD MODE    |      | FAST MODE |     | UNIT |
|----------------------------|------------------------------------------------------------------------------------------------------------------|------------------|------|-----------|-----|------|
|                            |                                                                                                                  | MIN              | MAX  | MIN       | MAX |      |
| f <sub>SCL</sub>           | SCL clock frequency                                                                                              | 0                | 100  | 0         | 400 | kHz  |
| t <sub>SU(START)</sub>     | START setup time (SCL high before SDA low)                                                                       | 4.7              |      | 0.6       |     | μs   |
| t <sub>H(START)</sub>      | START hold time (SCL low after SDA low)                                                                          | 4                |      | 0.6       |     | μs   |
| t <sub>W(SCLL)</sub>       | SCL Low-pulse duration                                                                                           | 4.7              |      | 1.3       |     | μs   |
| t <sub>W(SCLH)</sub>       | SCL High-pulse duration                                                                                          | 4                |      | 0.6       |     | μs   |
| t <sub>H(SDA)</sub>        | SDA hold time (SDA valid after SCL low)                                                                          | 0 <sup>(1)</sup> | 3.45 | 0         | 0.9 | μs   |
| t <sub>SU(SDA)</sub>       | SDA setup time                                                                                                   | 250              |      | 100       |     | ns   |
| t <sub>r-in</sub>          | SCL / SDA input rise time                                                                                        |                  | 1000 |           | 300 | ns   |
| t <sub>f-in</sub>          | SCL / SDA input fall time                                                                                        |                  | 300  |           | 300 | ns   |
| t <sub>f-out</sub>         | SDA output fall time from V <sub>IH</sub> min to V <sub>IL</sub> max with a bus capacitance from 10 pF to 400 pF |                  | 250  |           | 250 | ns   |
| t <sub>SU(STOP)</sub>      | STOP setup time                                                                                                  | 4                |      | 0.6       |     | μs   |
| t <sub>BUS</sub>           | Bus free time between a STOP and START condition                                                                 | 4.7              |      | 1.3       |     | μs   |
| t <sub>glitch_filter</sub> | Pulse width of spikes suppressed by the input glitch filter                                                      | 75               | 300  | 75        | 300 | ns   |

(1) The I<sup>2</sup>C master must internally provide a hold time of at least 300 ns for the SDA signal to bridge the undefined region of the falling edge of SCL.

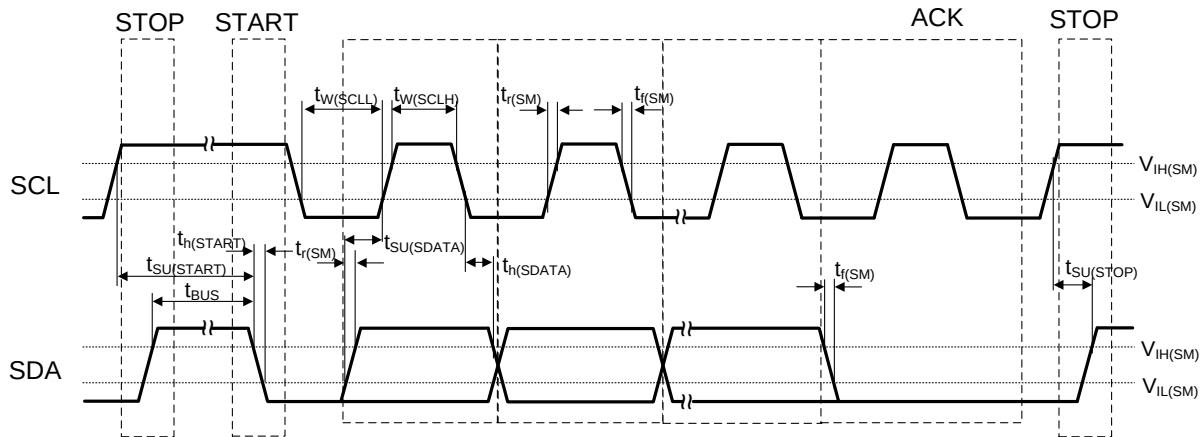


**Figure 1. I²C Timing Diagram**

For additional information, refer to the I²C-Bus specification, Version 2.1 (January 2000); the CDCM6208 meets the switching characteristics for standard mode and fast mode transfer.

## 6.23 Typical Characteristics

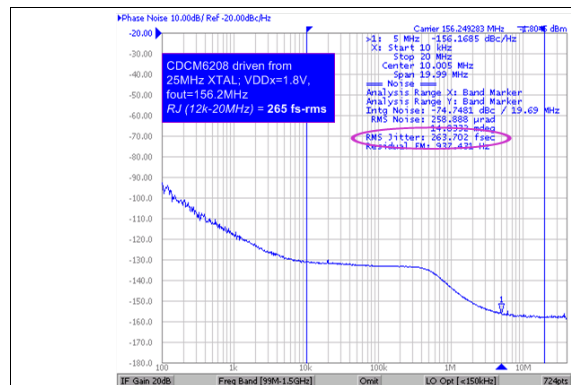


Figure 2. Typical Device Output Phase Noise and Jitter for 25 MHz

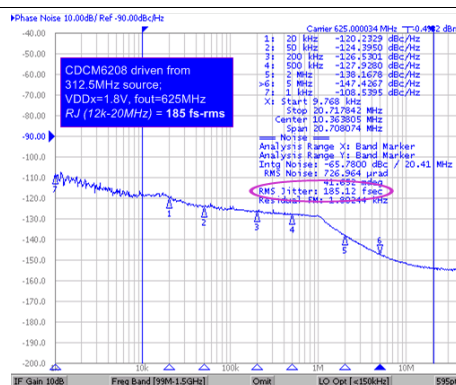


Figure 3. Typical Device Output Phase Noise and Jitter for 312.5 MHz

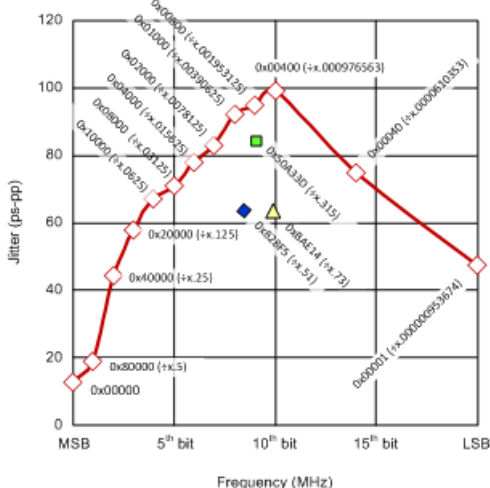


Figure 4. Fractional Divider Bit Selection Impact on Jitter ( $f_{FRAC} = 300$  MHz)

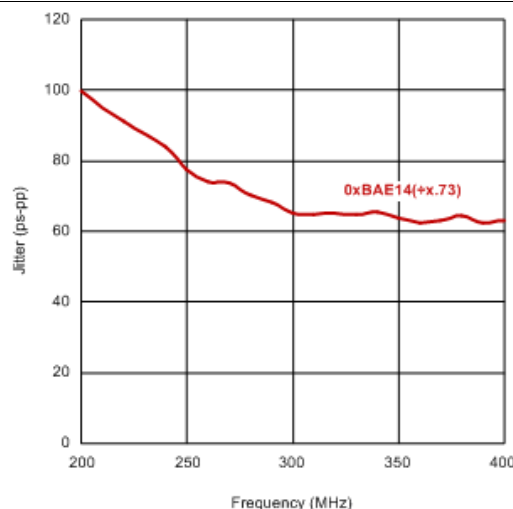


Figure 5. Fractional Divider Input Frequency Impact on Jitter (Using Divide by x.73 Example)

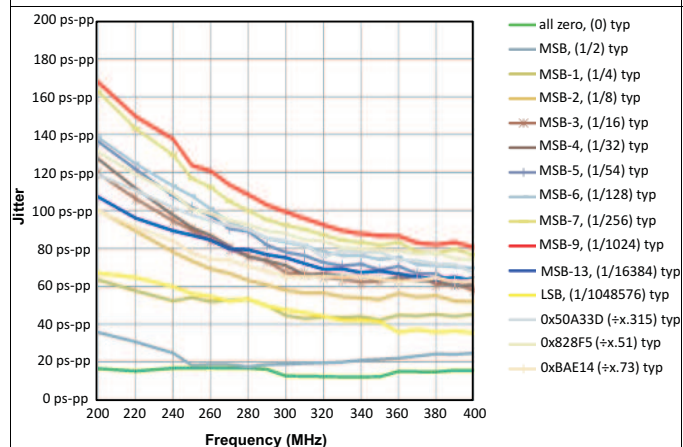


Figure 6. Fractional Divider Bit Selection Impact on  $T_J$  (Typical)

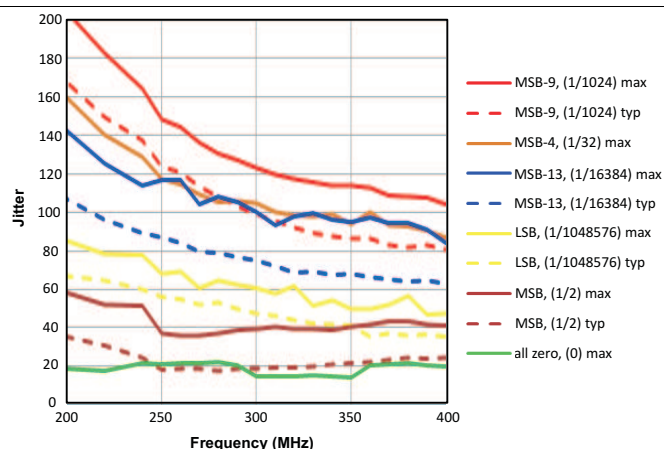


Figure 7. Fractional Divider Bit Selection Impact on  $T_J$  (Maximum Jitter Across Process, Voltage and Temperature)

## Typical Characteristics (continued)

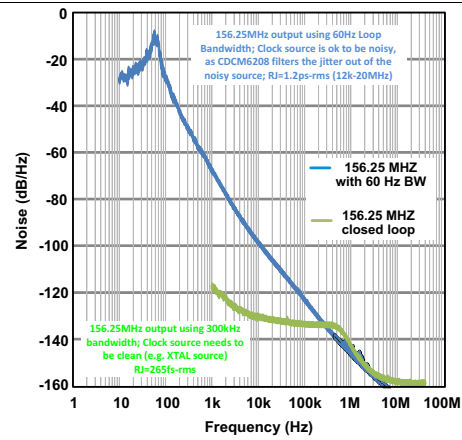


Figure 8. Phase Noise Plot for Jitter Cleaning Mode (Blue) and Synthesizer Mode (Green)

## 7 Parameter Measurement Information

This section describes the characterization test setup of each block in the CDCM6208.

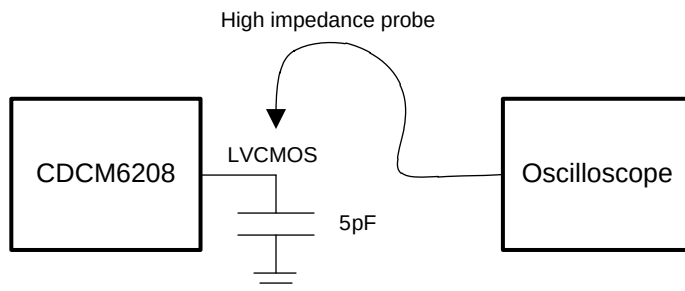


**Figure 9. LVC MOS Output AC Configuration During Device Test ( $V_{OH}$ ,  $V_{OL}$ ,  $t_{SLEW}$ )**

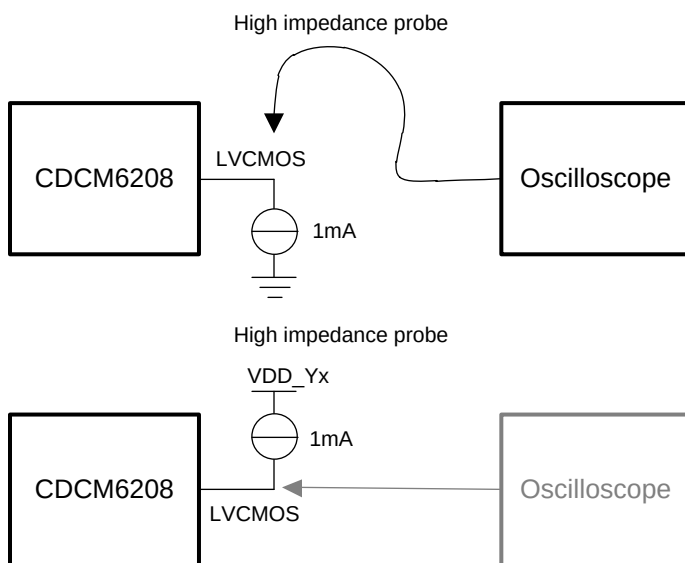


**Figure 10. LVC MOS Output DC Configuration During Device Test**

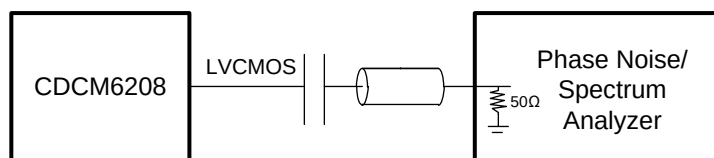


**Figure 11. LVC MOS Output AC Configuration During Device Phase Noise Test**

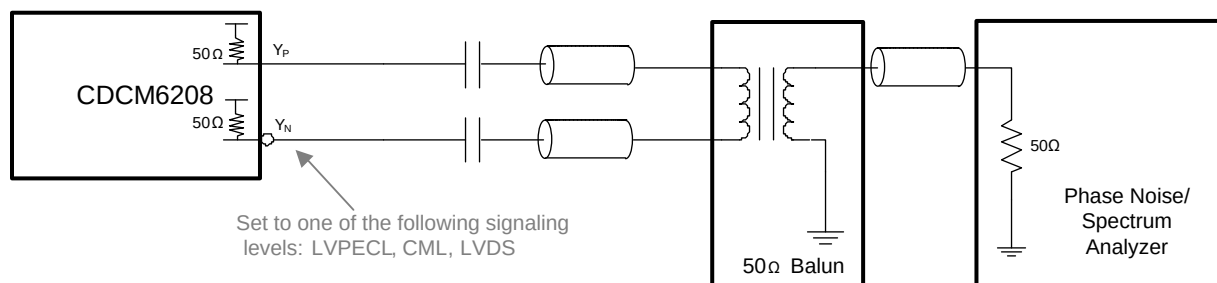


**Figure 12. LVDS, CML, and LVPECL Output AC Configuration During Device Test**

## Parameter Measurement Information (continued)

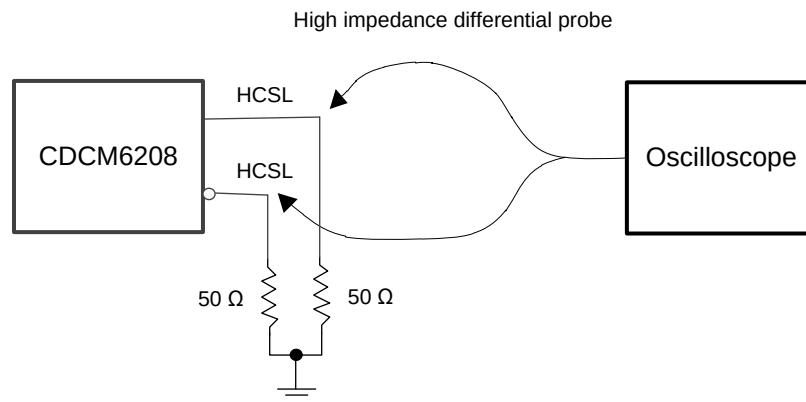


**Figure 13. HCSL Output DC Configuration During Device Test**

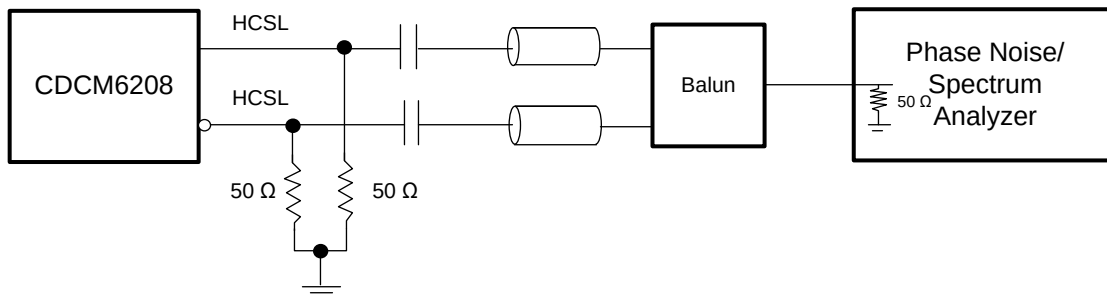


**Figure 14. HCSL Output AC Configuration During Device Test**

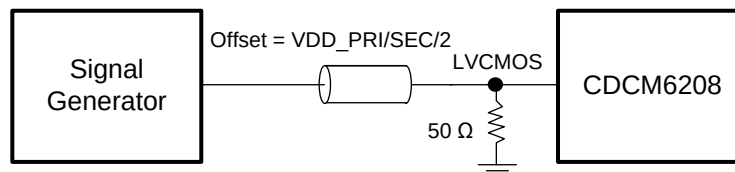


**Figure 15. LVCMOS Input DC Configuration During Device Test**

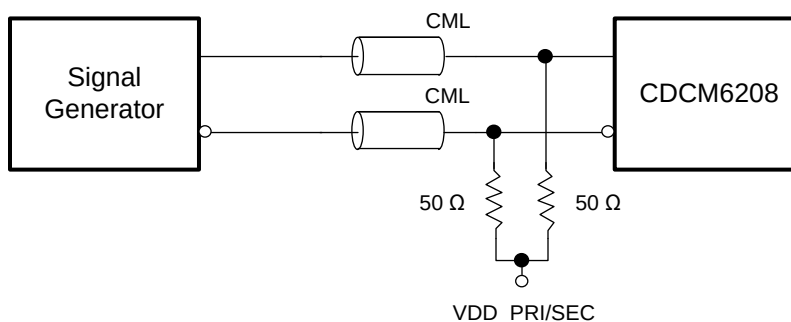


**Figure 16. CML Input DC Configuration During Device Test**

### Parameter Measurement Information (continued)

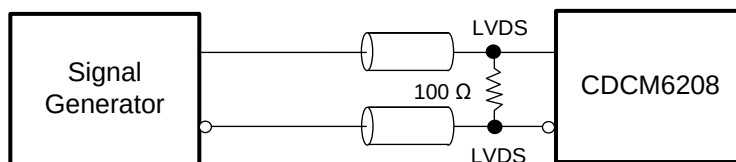


**Figure 17. LVDS Input DC Configuration During Device Test**

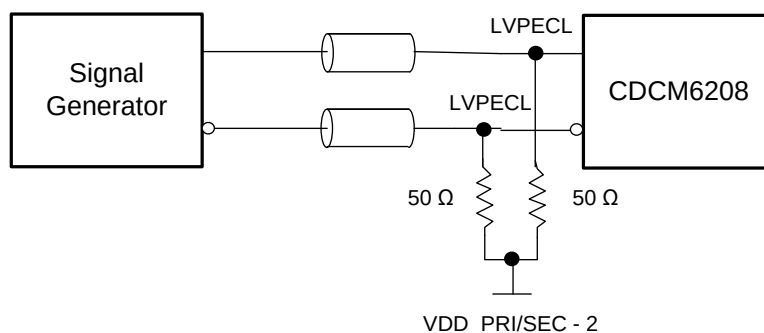


**Figure 18. LVPECL Input DC Configuration During Device Test**

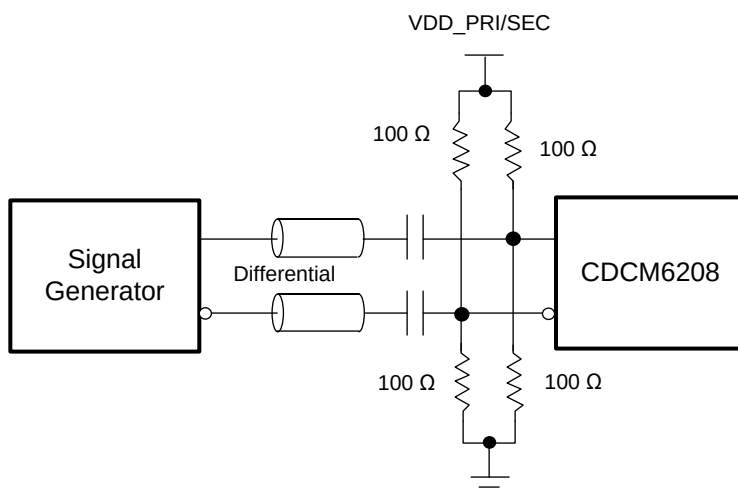


**Figure 19. Differential Input AC Configuration During Device Test**

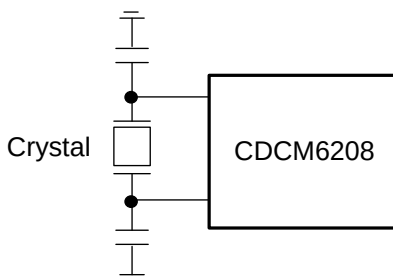


**Figure 20. Crystal Reference Input Configuration During Device Test**

### Parameter Measurement Information (continued)

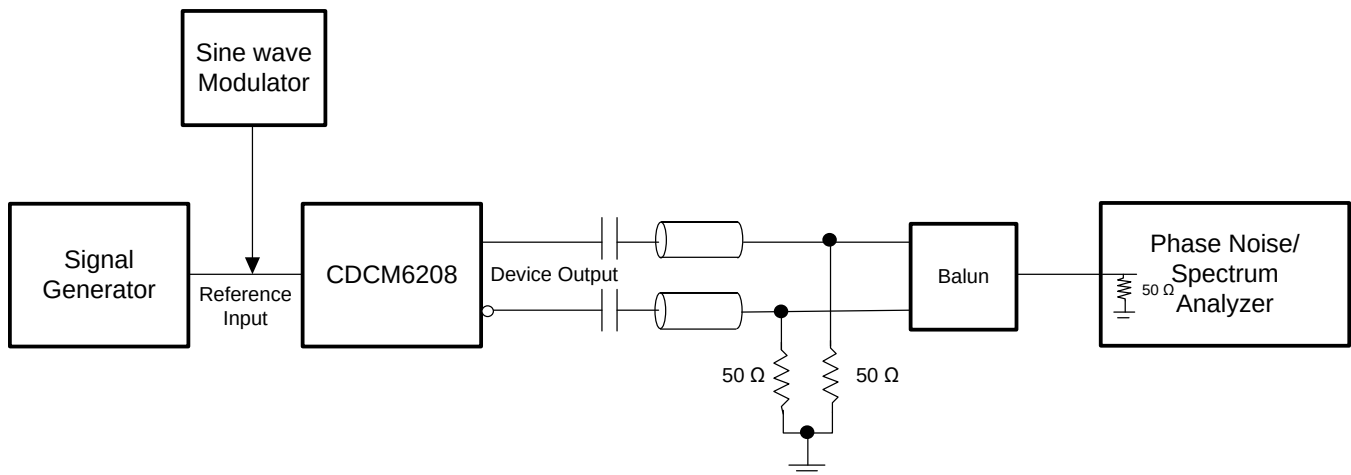


**Figure 21. Jitter Transfer Test Setup**

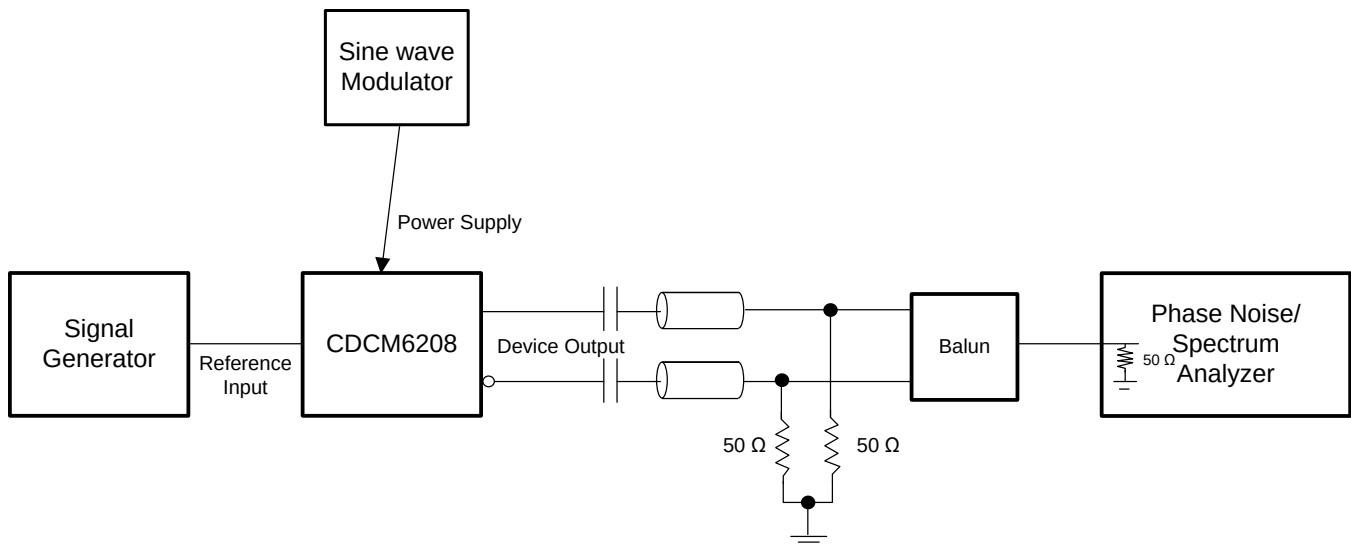


**Figure 22. PSNR Test Setup**

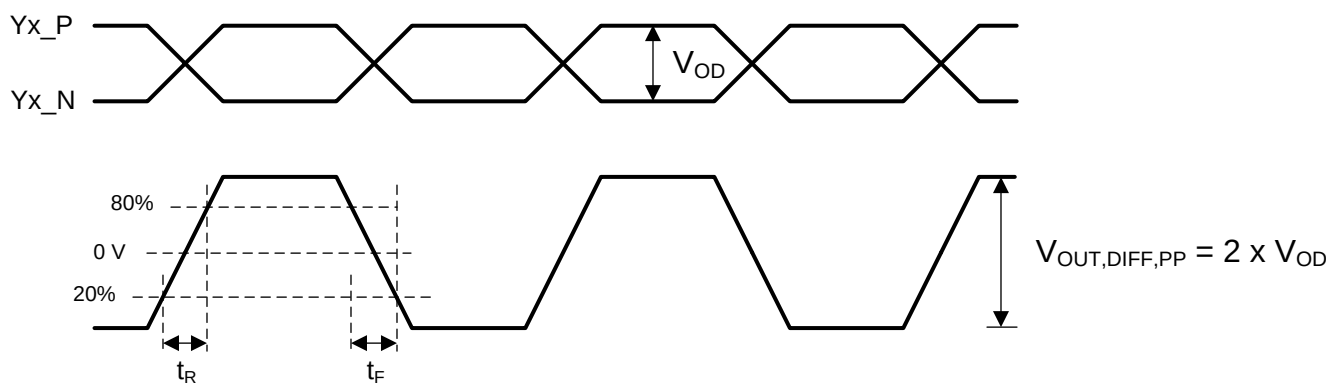


**Figure 23. Differential Output Voltage and Rise and Fall Time**

### Parameter Measurement Information (continued)

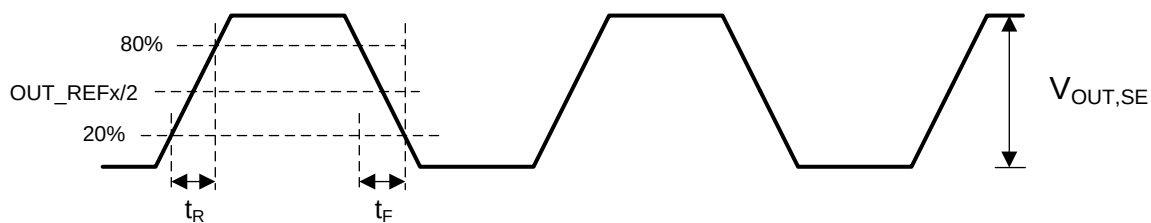


**Figure 24. Single-Ended Output Voltage and Rise and Fall Time**

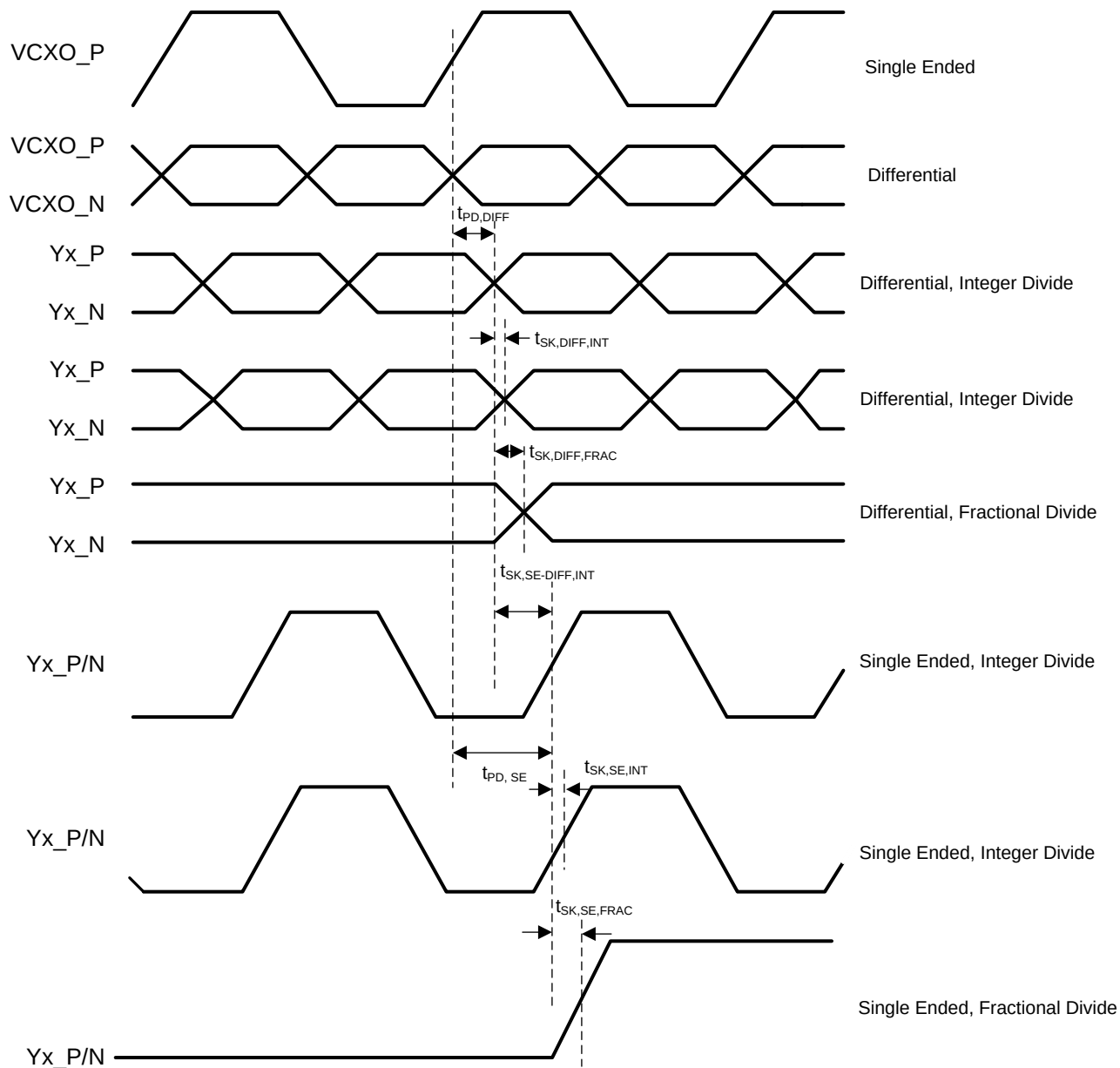


**Figure 25. Differential and Single-Ended Output Skew and Propagation Delay**

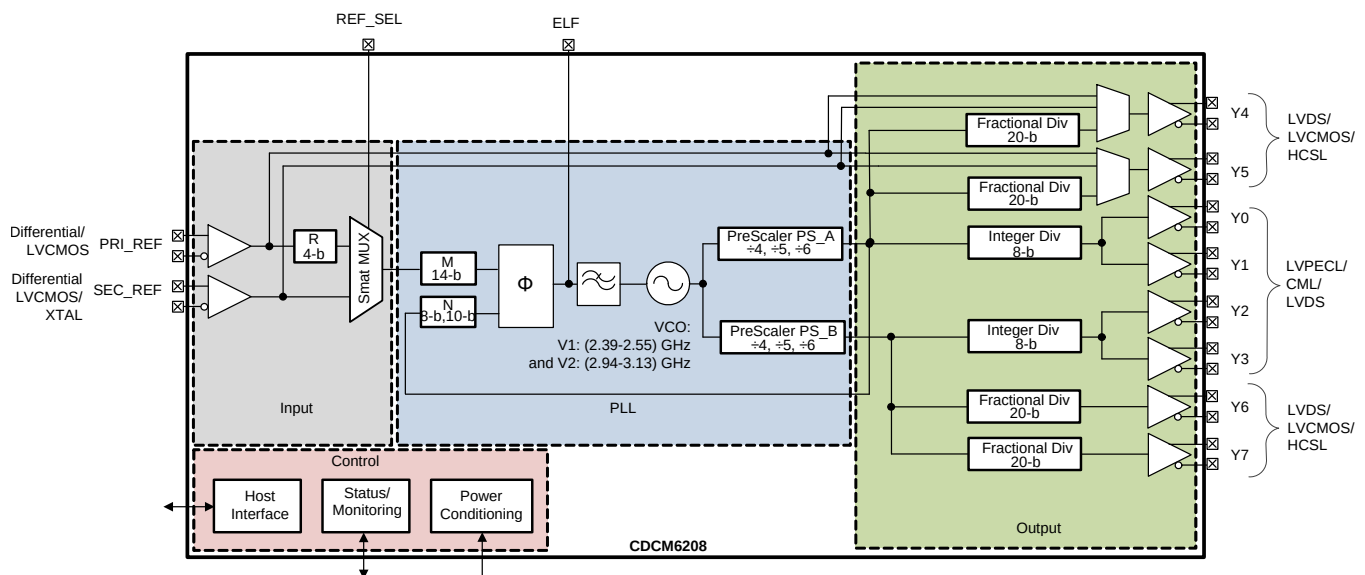
## 8 Detailed Description

### 8.1 Overview

In **synthesizer mode**, the overall output jitter performance is less than 0.5 ps-rms (10 k - 20 MHz) or 20 ps-pp on output using integer dividers and is between 50 to 220 ps-pp on outputs using fractional dividers depending on the prescaler output frequency.

In **jitter cleaner mode**, the overall output jitter is less than 2.1 ps-rms (10 k - 20 MHz) or 40 ps-pp on output using integer dividers and is less than 70 to 240 ps-pp on outputs using fractional dividers. The CDCM6208 is packaged in a small 48-pin, 7-mm × 7-mm VQFN package.

### 8.2 Functional Block Diagram



### 8.3 Feature Description

**Supply Voltage:** The CDCM6208 supply is internally regulated. Therefore, each core and I/O supply can be mixed and matched in any order according to the application needs. The device jitter performance is independent of supply voltage.

**Frequency Range:** The PLL includes dual reference inputs with input multiplexer, charge pump, loop filter, and VCO that operates from 2.39 GHz to 2.55 GHz (CDCM6208V1) and 2.94 GHz to 3.13 GHz (CDCM6208V2).

**Reference inputs:** The primary and secondary reference inputs support differential and single ended signals from 8 kHz to 250 MHz. The secondary reference input also supports crystals from 10 MHz to 50 MHz. There is a 4-bit reference divider available on the primary reference input. The input mux between the two references supports simply switching or can be configured as Smart MUX and supports glitchless input switching.

**Divider and Prescaler:** In addition to the 4-bit input divider of the primary reference a 14-b input divider at the output of input MUX and a cascaded 8-b and 10-b continuous feedback dividers are available. Two independent prescaler dividers offer divide by /4, /5 and /6 options of the VCO frequency of which any combination can then be chosen for a bank of 4 outputs (2 with fractional dividers and 2 that share an integer divider) through an output MUX. A total of 2 output MUXes are available.

**Phase Frequency Detector and Charge Pump:** The PFD input frequency can range from 8 kHz to 100 MHz. The charge pump gain is programmable and the loop filter consists of internal + partially external passive components and supports bandwidths from a few Hz up to 400 kHz.

## Feature Description (continued)

**Phase Noise:** The Phase Noise performance of the device can be summarized to:

**Table 2. Synthesizer Mode (Loop Filter BW >250 kHz)**

| RANDOM JITTER (ALL OUTPUTS)                                  |                                     |                        | TOTAL JITTER                                  |                                                    |
|--------------------------------------------------------------|-------------------------------------|------------------------|-----------------------------------------------|----------------------------------------------------|
| TYPICAL                                                      | MAXIMUM                             |                        | MAXIMUM                                       |                                                    |
| 10k-20MHz                                                    | 12k-20MHz                           | 10k-100MHz             | Integer divider<br>DJ-unbound<br>RJ 10k-20MHz | Fractional divider<br>DJ 10k-40MHz<br>RJ 10k-20MHz |
| 0.27 ps-rms (Integer division)<br>0.7ps-rms (fractional div) | 0.3 ps-rms (int div) <sup>(1)</sup> | 0.625 ps-rms (int div) | 20 ps-pp <sup>(2)</sup>                       | 50-220 ps-pp,<br>see <a href="#">Figure 30</a>     |

- (1) Integrated Phase Noise (12kHz - 20 MHz) for 156.25 MHz output clock measured at room temperature using a 25 MHz Low Noise reference source
- (2)  $T_J = 20$  ps<sub>pp</sub> applies for LVPECL, CML, and LVDS signaling.  $T_J$  lab characterization measured 8 ps<sub>pp</sub>, (typical) and 12 ps<sub>pp</sub> (max) over PVT.

**Table 3. Jitter Cleaner Mode (Loop Filter BW < 1 kHz)**

| RANDOM JITTER (ALL OUTPUTS)                                            |                      |                       | TOTAL JITTER                                  |                                                    |
|------------------------------------------------------------------------|----------------------|-----------------------|-----------------------------------------------|----------------------------------------------------|
| TYPICAL                                                                | MAXIMUM              |                       | MAXIMUM                                       |                                                    |
| 10k-20MHz                                                              | 10k-20MHz            | 10k-100MHz            | Integer divider<br>DJ unbound<br>RJ 10k-20MHz | Fractional divider<br>DJ 10k-40MHz<br>RJ 10k-20MHz |
| 1.6 ps-rms (Integer division)<br>2.3 ps-rms (fractional div) 10k-20MHz | 2.1 ps-rms (int div) | 2.14 ps-rms (int div) | 40 ps-pp                                      | 70-240 ps-pp,<br>see <a href="#">Figure 30</a>     |

**Spurious Performance:** The spurious performance is as follows:

- Less than -80 dBc spurious from PFD/reference clocks at 122.88 MHz output frequency in the Nyquist range.
- Less than -68 dBc spurious from output channel-to-channel coupling on the victim output at differential signaling level operated at 122.88 MHz output frequency in the Nyquist range.

### Device outputs:

The Device outputs offer multiple signaling formats: high-swing CML (LVPECL like), normal-swing CML (CML), low-swing CML (LVDS like), HCSL, and LVCMOS signaling.

**Table 4. Supported Output Formats and Frequency Ranges**

| Outputs | LVPECL | CML | LVDS | HCSL | LVCMOS | OUTPUT DIVIDER | FREQUENCY RANGE |
|---------|--------|-----|------|------|--------|----------------|-----------------|
| Y[3:0]  | X      | X   | X    |      |        | Integer only   | 1.55 - 800 MHz  |
| Y[7:4]  |        |     | X    | X    | X      | Integer        | 1.55 - 800 MHz  |
|         |        |     |      |      |        | Fractional     | 1.00 - 400 MHz  |

Outputs [Y0:Y3] are driven by 8-b continuous integer dividers per pair. Outputs [Y4:Y7] are each driven by 20-b fractional dividers that can achieve any frequency with better than 1ppm frequency accuracy. The output skew is typically less than 40 ps for differential outputs. The LVCMOS outputs support adjustable slew rate control to control EMI. Pairs of 2 outputs can be operated at 1.8 V, 2.5 V or 3.3 V power supply voltage.

**Device Configuration:** 32 distinct pin modes are available that cover many common use cases without the need for any serial programming of the device. For maximum flexibility the device also supports SPI and I<sup>2</sup>C programming. I<sup>2</sup>C offers 4 distinct addresses to support up to 4 devices on the same programming lines.

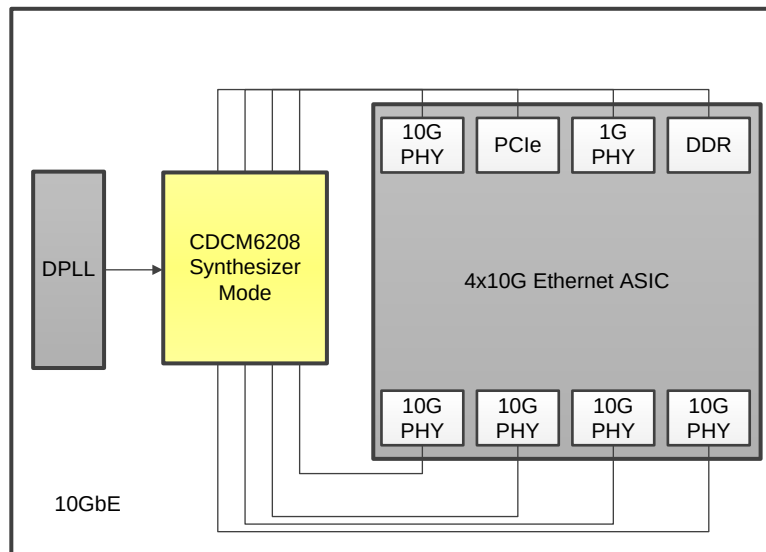


Figure 26. Typical Use Case: CDCM6208 Example in Wireless Infrastructure Baseband Application

### 8.3.1 Typical Device Jitter

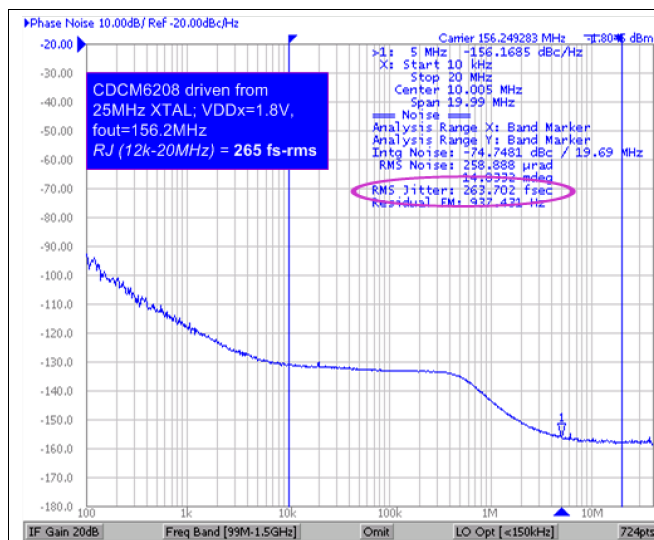


Figure 27. Typical Device Output Phase Noise and Jitter for 25 MHz

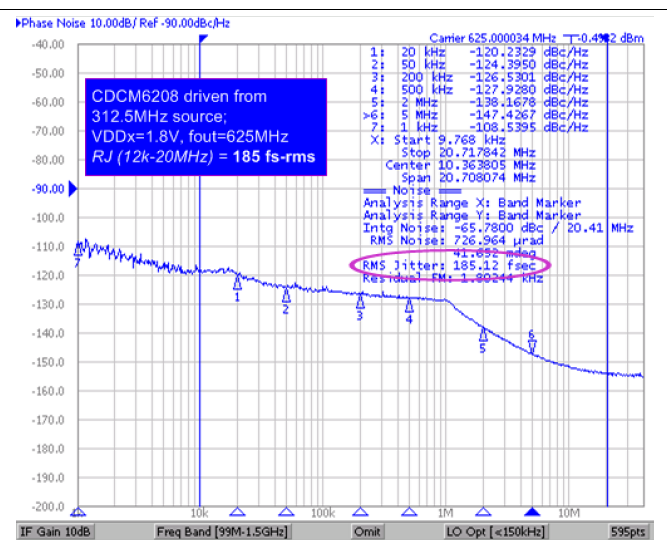


Figure 28. Typical Device Output Phase Noise and Jitter for 312.5 MHz

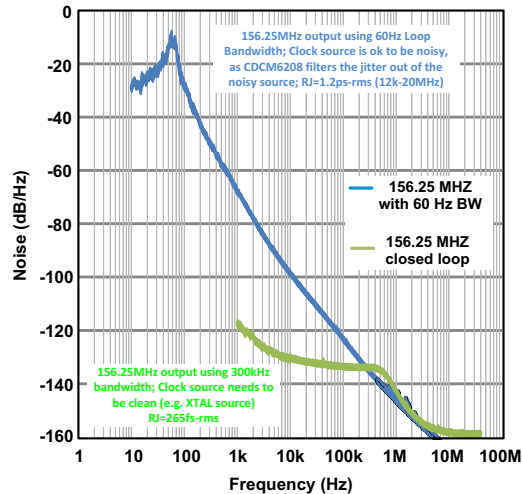


Figure 29. Phase Noise Plot for Jitter Cleaning Mode (Blue) and Synthesizer Mode (Green)

### 8.3.2 Universal Input Buffer (PRI\_REF, SEC\_REF)

The universal input buffers support multiple signaling formats (LVDS, CML or LVCMOS) and these require external termination schemes. The secondary input buffer also supports crystal inputs and [Crystal Input Characteristics \(SEC\\_REF\)](#) provides the characteristics of the crystal that can be used. Both inputs incorporate hysteresis.

### 8.3.3 VCO Calibration

The LC VCO is designed using high-Q monolithic inductors and has low phase noise characteristics. The VCO of the CDCM6208 must be calibrated to ensure that the clock outputs deliver optimal phase noise performance. Fundamentally, a VCO calibration establishes an optimal operating point within the tuning range of the VCO. While transparent to the user, the CDCM6208 and the host system perform the following steps comprising a VCO calibration sequence:

1. **Normal Operation** – When the CDCM6208 is in normal (operational) mode, the state of both the power down pin (PDN) and reset pin (RESETN) is high.
2. **Entering the reset state** – If the user wishes to restore all device defaults and initiate a VCO calibration sequence, then the host system must place the device in reset via the PDN pin, through the RESETN pin, or by removing and restoring device power. Pulling either of these pins low places the device in the reset state. Holding either pin low holds the device in reset.
3. **Exiting the reset state** – The device calibrates the VCO either by exiting the device reset state or through the device reset command initiated via the host interface. Exiting the reset state occurs automatically after power is applied and/or the system restores the state of the PDN or RESETN pins from the low to high state. Exiting the reset state using this method causes the device defaults to be loaded/reloaded into the device register bank. Invoking a device reset via the register bit does not restore device defaults; rather, the device retains settings related to the current clock frequency plan. Using this method allows for a VCO calibration for a frequency plan other than the default state (that is, the device calibrates the VCO based on the settings contained within the register bank at the time that the register bit is accessed). The nominal state of this bit is low. Writing this bit to a high state and then returning it to the low state invokes a device reset without restoring device defaults.
4. **Device stabilization** – After exiting the reset state as described in Step 3, the device monitors internal voltages and starts a reset timer. Only after internal voltages are at the correct level and the reset time has expired will the device initiate a VCO calibration. This ensures that the device power supplies and phase locked loops have stabilized prior to calibrating the VCO.
5. **VCO Calibration** – The CDCM6208 calibrates the VCO. During the calibration routine, the device holds all outputs in reset so that the CDCM6208 generates no spurious clock signals.

### 8.3.4 Reference Divider (R)

The reference (R) divider is a continuous 4-b counter (1 – 16) that is present on the primary input before the Smart Input MUX. It is operational in the frequency range of 8 kHz to 250 MHz. The output of the R divider sets the input frequency for the Smart MUX, and the auto switch capability of the Smart MUX can then be employed as long as the secondary input frequency is no more than  $\pm 20\%$  different from the output of the R divider.

### 8.3.5 Input Divider (M)

The input (M) divider is a continuous 14-b counter (1 – 16384) that is present after the Smart Input MUX. It is operational in the frequency range of 8 kHz to 250 MHz. The output of the M divider sets the PFD frequency to the PLL and should be in the range of 8 kHz to 100 MHz.

### 8.3.6 Feedback Divider (N)

The feedback (N) divider is made up of cascaded 8-b counter divider (1 – 256) followed by a 10-b counter divider (1 – 1024) that are present on the feedback path of the PLL. It is operational in the frequency range of 8 kHz to 800 MHz. The output of the N divider sets the PFD frequency to the PLL and should be in the range of 8 kHz to 100 MHz. The frequency out of the first divider is required to be less than or equal to 200 MHz to ensure proper operation.

### 8.3.7 Prescaler Dividers (PS\_A, PS\_B)

The prescaler (PS) dividers are fed by the output of the VCO and are distributed to the output dividers (PS\_A to the dividers for Outputs 0, 1, 4, and 5 and PS\_B to the dividers for Outputs 2, 3, 6, and 7. PS\_A also completes the PLL as it also drives the input of the Feedback Divider (N).

### 8.3.8 Phase Frequency Detector (PFD)

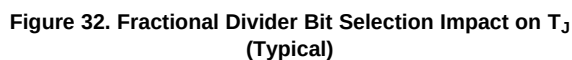
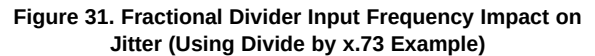
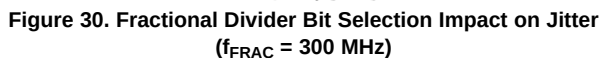
The PFD takes inputs from the Smart Input MUX output and the feedback divider output and produces an output that is dependent on the phase and frequency difference between the two inputs. The allowable range of frequencies at the inputs of the PFD is from 8 kHz to 100 MHz.

### 8.3.9 Charge Pump (CP)

The charge pump is controlled by the PFD which dictates either to pump up or down in order to charge or discharge the integrating section of the on-chip loop filter. The integrated and filtered charge pump current is then converted to a voltage that drives the control voltage node of the internal VCO through the loop filter. The range of the charge pump current is from 500  $\mu$ A to 4 mA.

### 8.3.10 Fractional Output Divider Jitter Performance

The fractional output divider jitter performance is a function of the fraction output divider input frequency as well as actual fractional divide setting itself. To minimize the fractional output jitter, TI recommends using the least number of fractional bits and the highest input frequency possible into the divider. As observable in [Figure 30](#), the largest jitter contribution occurs when only one fractional divider bit is selected, and especially when the bits in the middle range of the fractional divider are selected.



### 8.3.11 Device Block-Level Description

Copyright © 2012–2018, Texas Instruments Incorporated

### 8.3.12 Device Configuration Control

Figure 35 illustrates the relationships between device states, the control pins, device initialization and configuration, and device operational modes. In pin mode, the state of the control pins determines the configuration of the device for all device states. In programming mode, the device registers are initialized to their default state and the host can update the configuration by writing to the device registers.

A system may transition a device from pin mode to host connected mode by changing the state of the SI\_MODE pins and then triggering a device power cycle by toggling the PDN input pin (high-low-high); however, outputs will be disabled during the transition as the device registers are initialized to the host mode default state.

### 8.3.13 Configuring the RESETN Pin

Figure 34 shows two typical applications examples of the RESETN pin and usage of the PWR pin in Pin Mode.

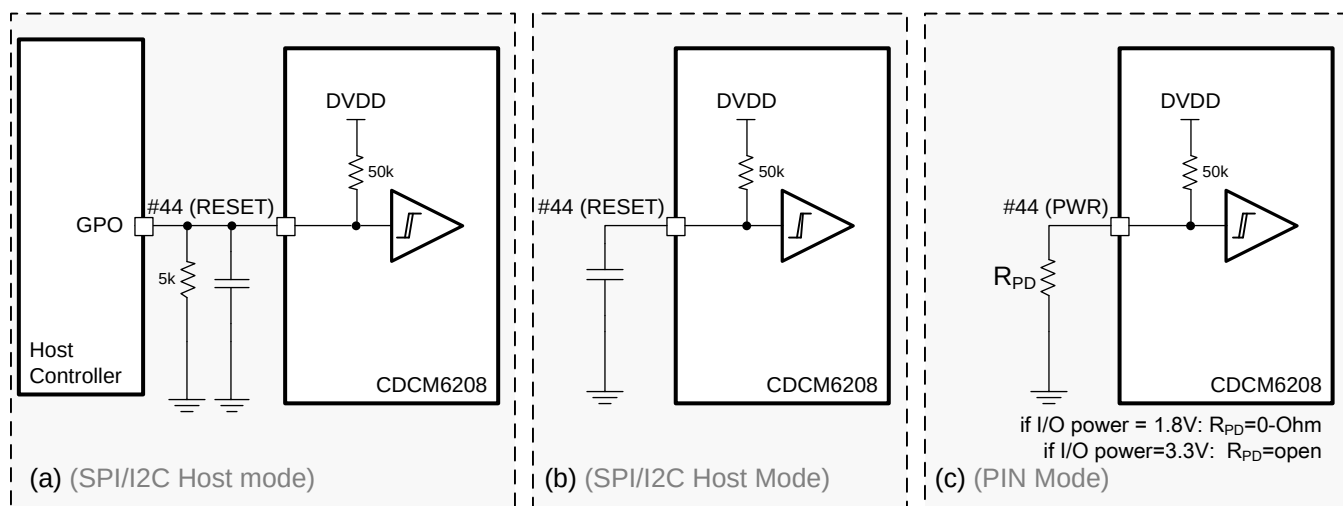


**Figure 34. RESETN/PWR Pin Configurations**

Figure 34 (a) SPI / I2C mode only: shows the RESETN pin connected to a digital device that controls device reset. The resistor and capacitor combination ensure reset is held low even if the CDCM6208 is powered up before the host controller output signal is valid.

Figure 34 (b) SPI / I2C mode only: shows a configuration in which the user wishes to introduce a delay between the time that the system applies power to the device and the device exiting reset. If the user does not use a capacitor, then the device effectively ignores the state of the RESETN pin.

Figure 34 (c) Pin mode only: shows a configuration useful if the device is used in Pin Mode. Here device pin number 44 becomes the PWR input. An external pull down resistor can be used to pull this pin down. If the resistor is not installed, the pin is internally pulled high.

Figure 35 shows how the different possible device configurations and when the VCO becomes calibrated and the outputs turn on and off.

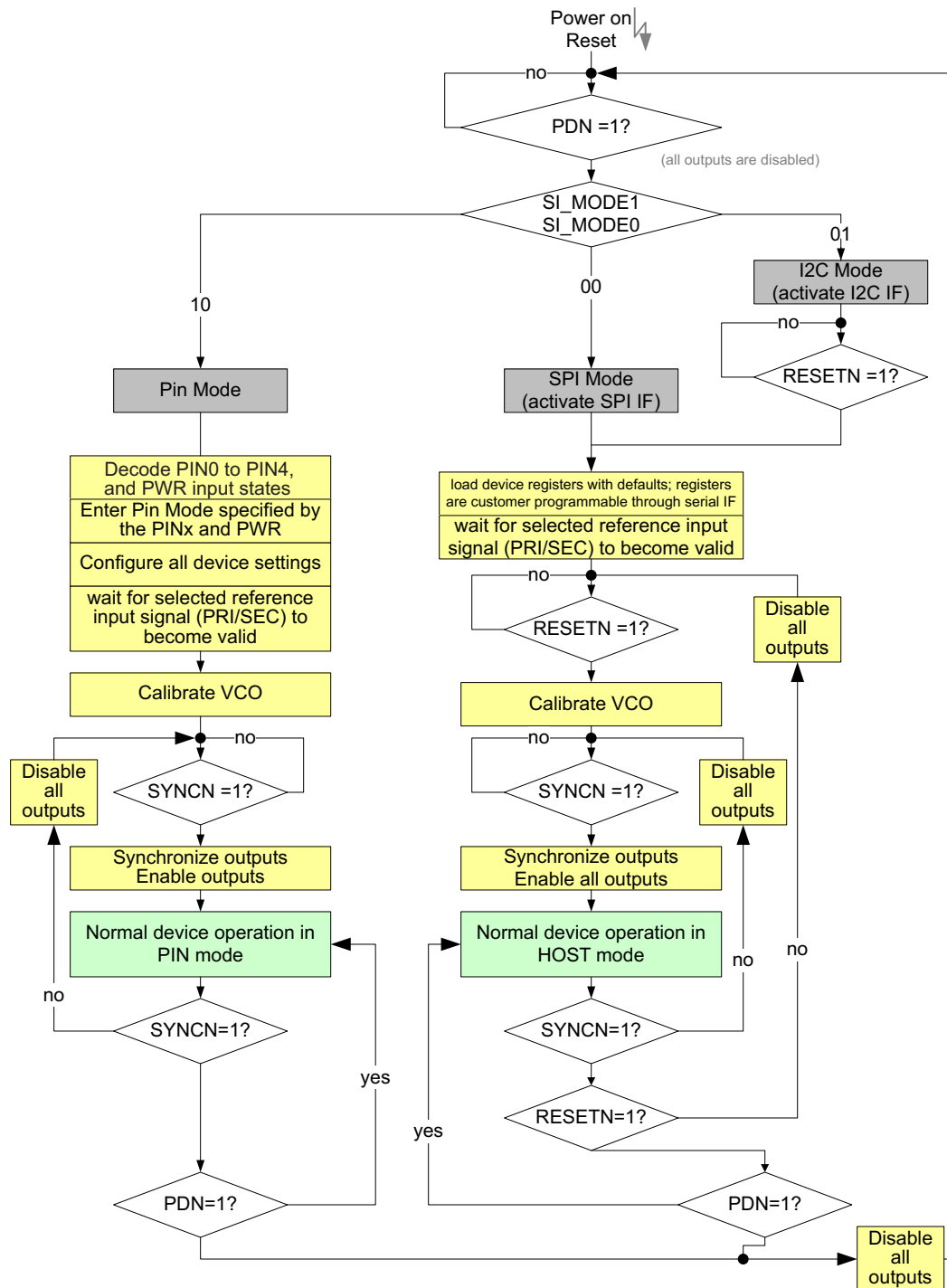


**Figure 35. Device Power Up and Configuration**

### 8.3.14 Preventing False Output Frequencies in SPI/I2C Mode at Start-Up

Some systems require a custom configuration and cannot tolerate any output to start up with a wrong frequency. Holding RESET low at power-up until the device is fully configured keeps all outputs disabled. The device calibrates automatically after RESET becomes released and starts out with the desired output frequency.

#### NOTE

The RESETN pin cannot be held low during I<sup>2</sup>C communication. Instead, use the SYNCN pin to disable the outputs during an I<sup>2</sup>C write operation, and toggle RESETN pin afterwards. Alternatively, other options exist such as using the RESETN bit in the register space to disable outputs until the write operation is complete.

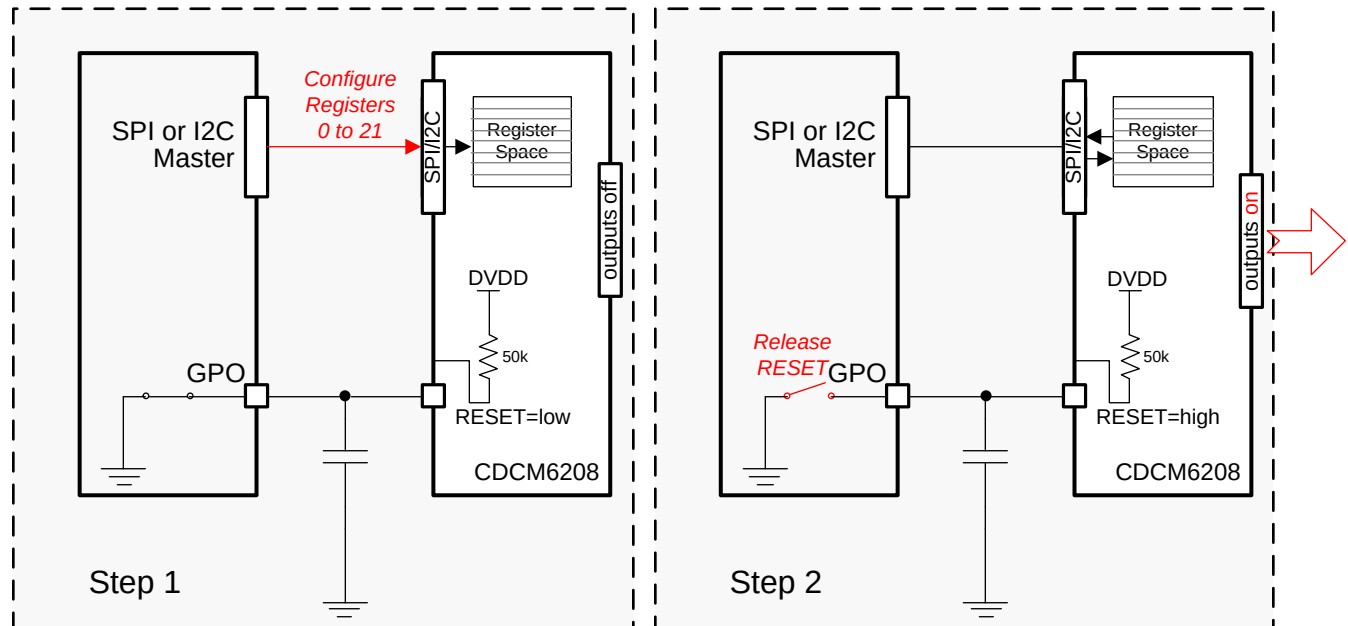


**Figure 36. Reset Pin Control During Register Loading**

### 8.3.15 Input MUX and Smart Input MUX

The Smart Input MUX supports auto-switching and manual-switching using control pin (and through register). The Smart Input MUX is designed such that glitches created during switching in both auto and manual modes are suppressed at the MUX output.

**Table 5. Input MUX Selection**

| SI_MODE1<br>PIN NO. 47 | REGISTER 4 BIT 13<br>SMUX_MODE_SEL | REGISTER 4 BIT 12<br>SMUX_REF_SEL | REF_SEL<br>PIN NO. 6 | SELECTED INPUT                                            |                                           |
|------------------------|------------------------------------|-----------------------------------|----------------------|-----------------------------------------------------------|-------------------------------------------|
| 0 (SPI/I2C mode)       | 0                                  | X                                 | X                    | Auto Select Priority is given to Primary Reference input. |                                           |
|                        | 1                                  | 0                                 | 1                    | Primary input                                             | input select through SPI/I <sup>2</sup> C |
|                        |                                    | 1                                 |                      | Secondary input                                           |                                           |
|                        |                                    | 1                                 | 0                    | Primary input                                             | input select through external pin         |
|                        |                                    |                                   | 1                    | Secondary input                                           |                                           |
| 1 (pin mode)           | not available                      |                                   | 0                    | Primary or Auto (see <a href="#">Table 6</a> )            |                                           |
|                        |                                    |                                   | 1                    | Secondary or Auto (see <a href="#">Table 6</a> )          |                                           |

**Example 1:** An application desired to auto-select the clock reference in SPI/I2C mode. During production testing however, the system needs to force the device to use the primary followed by the secondary input. The settings would be as follows:

1. Tie REF\_SEL pin always high
2. For primary clock input testing, use R4 [13:12] = 10
3. For secondary clock input testing, set R4 [13:12] = 11.
4. For the auto-mux setting in the final product shipment, set R3[13:12]=01 or 00

**Example 2:** The application wants to select the clock input manually without programming SPI/I2C. In this case, program R4[13:12] = 11, and select primary or secondary input by toggling REF\_SEL low or high.

**SmartMux input frequency limitation:** In the automatic mode, the frequencies of both inputs to the smart mux (PRI\_REF divided by R and SEC\_REF) need to be similar; however, they can vary by up to 20%.

**Switching behavior:** The input clocks can have any phase. When switching happens between one input clock to the other, the phase of the output clock slowly transitions to the phase of the newly selected input clock. There will be no-phase jump at the output. The phase transition time to the new reference clock signal depends on the PLL loop filter bandwidth. Auto-switch assigns higher priority to PRI\_REF and lower priority to SEC\_REF. The timing diagram of an auto-switch at the input MUX is shown in [Figure 37](#).

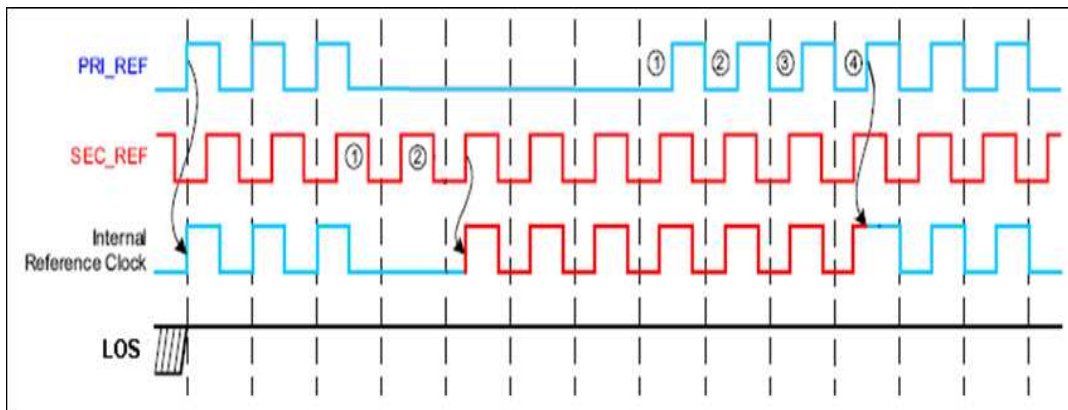


**Figure 37. Smart Input MUX Auto-Switch Mode Timing Diagram**

## 8.4 Device Functional Modes

### 8.4.1 Control Pins Definition

In the absence of a host interface, the CDCM6208 can be powered up in one of 32 pre-configured settings when the pins are SI\_MODE[1:0] = 10. The CDCM6208 has 5 control pins identified to achieve commonly used networking frequencies, and change output types. The Smart Input MUX for the PLL is set in most configurations to manual mode in pin mode. Based on the control pins settings for the on-chip PLL, the device generates the appropriate frequencies and appropriate output signaling types at start-up. In the case of the PLL loop filter, "JC" denotes PLL bandwidths of  $\leq 1$  kHz and "Synth" denotes PLL bandwidths of  $\geq 100$  kHz.

**CDCM6208**

SCAS931G – MAY 2012–REVISED JANUARY 2018

[www.ti.com](http://www.ti.com)
**Table 6. Pre-Configured Settings of CDCM6208V1 Accessible by PIN[4:0]<sup>(1)(2)</sup>**

| SL_MODE[1:0] | pin[4:0] | UseCase       | fin(PRI_REF) | Type | fin(SEC_REF) | Type    | REF_SEL (note 2) | f(PFD)  | f(VCO)  | fout(Y0) | Type | fout(Y1) | Type | fout(Y2) | Type | fout(Y3) | Type | fout(Y4) | Type | fout(Y5) | Type | fout(Y6) | Type | fout(Y7) | Type |
|--------------|----------|---------------|--------------|------|--------------|---------|------------------|---------|---------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| 00           | I/O      | SPI Default   | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | CML  | 156.25   | CML  | 125.00   | LVDS | 125.00   | LVDS | 66.66    | LVDS | 66.66    | LVDS | 100.00   | LVDS | 100.00   | LVDS |
| 01           | I/O      | I2C Default   | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | CML  | 156.25   | CML  | 125.00   | LVDS | 125.00   | LVDS | 66.66    | LVDS | 66.66    | LVDS | 100.00   | LVDS | 100.00   | LVDS |
| 11           | RESERVED |               |              |      |              |         |                  |         |         |          |      |          |      |          |      |          |      |          |      |          |      |          |      |          |      |
| 10           | 0x00     | PinMode 1-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2400    | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS |
| 10           | 0x01     | PinMode 2-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2400    | 100      | PECL | 100      | PECL | 100      | PECL | 100      | PECL | 100      | HCSL | 100      | HCSL | 100      | HCSL | 100      | HCSL |
| 10           | 0x02     | PinMode 3-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2400    | 100      | CML  | 100      | CML  | 100      | CML  | 100      | CML  | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS |
| 10           | 0x03     | PinMode 4-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS |
| 10           | 0x04     | PinMode 5-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | PECL | 156.25   | PECL | 156.25   | PECL | 156.25   | PECL | 156.25   | HCSL | 156.25   | HCSL | 156.25   | HCSL | 156.25   | HCSL |
| 10           | 0x05     | PinMode 6-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | CML  | 156.25   | CML  | 156.25   | CML  | 156.25   | CML  | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS |
| 10           | 0x06     | PinMode 7-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS |
| 10           | 0x07     | PinMode 8-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 125      | PECL | 125      | PECL | 125      | PECL | 125      | PECL | 125      | HCSL | 125      | HCSL | 125      | HCSL | 125      | HCSL |
| 10           | 0x08     | PinMode 9-V1  | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 125      | CML  | 125      | CML  | 125      | CML  | 125      | CML  | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS |
| 10           | 0x09     | PinMode 10-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 125      | LVDS | 125      | LVDS | 156.25   | LVDS | 156.25   | LVDS | 100      | LVDS | 100      | LVDS | 133.33   | LVDS | 25       | LVDS |
| 10           | 0x0A     | PinMode 11-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 312.5    | PECL | 312.5    | PECL | 312.5    | PECL | 312.5    | PECL | 312.5    | HCSL | 312.5    | HCSL | 312.5    | HCSL | 312.5    | HCSL |
| 10           | 0x0B     | PinMode 12-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | PECL | 156.25   | PECL | 100      | PECL | 100      | PECL | 156.25   | HCSL | 156.25   | HCSL | 100      | HCSL | 100      | HCSL |
| 10           | 0x0C     | PinMode 13-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | PECL | 156.25   | PECL | 156.25   | PECL | 156.25   | PECL | 125      | HCSL | 125      | HCSL | 125      | HCSL | 125      | HCSL |
| 10           | 0x0D     | PinMode 14-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2400    | 200      | PECL | 200      | PECL | 100      | PECL | 100      | PECL | 100      | HCSL | 100      | HCSL | 200      | HCSL | 200      | HCSL |
| 10           | 0x0E     | PinMode 15-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 500      | PECL | 500      | PECL | 250      | PECL | 250      | PECL | 125      | HCSL | 125      | HCSL | 100      | HCSL | 25       | CMOS |
| 10           | 0x0F     | PinMode 16-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 625      | PECL | 625      | PECL | 312.5    | PECL | 312.5    | PECL | 156.25   | HCSL | 156.25   | HCSL | 125      | HCSL | 25       | CMOS |
| 10           | 0x10     | PinMode 17-V1 | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72   | 2457.6  | 122.88   | PECL | 122.88   | PECL | 153.6    | PECL | 153.6    | PECL | 30.72    | CMOS | 153.6    | HCSL | 61.44    | HCSL | 122.88   | CMOS |
| 10           | 0x11     | PinMode 18-V1 | 24.8832      | LVDS | 24.8832      | Crystal | MANU             | 24.8832 | 2488.32 | 622.08   | CML  | 622.08   | CML  | 622.08   | CML  | 622.08   | CML  | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS |
| 10           | 0x12     | PinMode 19-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | LVDS | 156.25   | LVDS | 125      | LVDS | 125      | LVDS | 66.67    | LVDS | 25       | CMOS | 25       | LVDS | 100      | LVDS |
| 10           | 0x13     | PinMode 20-V1 | 0.008        | CMOS | 0.008        | CMOS    | MANU             | 0.008   | 2500    | 156.25   | LVDS | 156.25   | PECL | 125      | LVDS | 125      | LVDS | 125      | CMOS | 25       | LVDS | 100      | HCSL | 100      | HCSL |
| 10           | 0x14     | PinMode 21-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 100      | LVDS | 100      | LVDS | 156.25   | LVDS | 156.25   | LVDS | 122.88   | LVDS | 30.72    | LVDS | 66.67    | LVDS | 153.6    | LVDS |
| 10           | 0x15     | PinMode 22-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 100      | PECL | 100      | PECL | 156.25   | PECL | 156.25   | PECL | 100      | HCSL | 100      | HCSL | 100      | HCSL | 100      | HCSL |
| 10           | 0x16     | PinMode 23-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 100      | PECL | 100      | PECL | 156.25   | PECL | 156.25   | PECL | 100      | HCSL | 100      | HCSL | 156.25   | HCSL | 100      | HCSL |
| 10           | 0x17     | PinMode 24-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 125      | PECL | 125      | PECL | 100      | PECL | 100      | PECL | 100      | HCSL | 100      | HCSL | 100      | HCSL | 100      | HCSL |
| 10           | 0x18     | PinMode 25-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 100      | PECL | 100      | PECL | 156.25   | PECL | 156.25   | PECL | 100      | HCSL | 100      | HCSL | 155.52   | HCSL | 155.52   | HCSL |
| 10           | 0x19     | PinMode 26-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 156.25   | PECL | 156.25   | PECL | 100      | PECL | 100      | PECL | 125      | HCSL | 156.26   | HCSL | 212.5    | HCSL | 106.25   | HCSL |
| 10           | 0x1A     | PinMode 27-V1 | 25           | LVDS | 25           | Crystal | MANU             | 25      | 2500    | 100      | PECL | 100      | PECL | 250      | PECL | 250      | PECL | 100      | HCSL | 100      | HCSL | 100      | HCSL | 125      | HCSL |

(1) The functionality of the status 0 and status 1 pins in SPI and I<sup>2</sup>C mode is programmable.

(2) The REF\_SEL input pin selects the primary or secondary input in MANUAL mode. That is: If the system only uses a XTAL on the secondary input, REF\_SEL should be tied to VDD. The primary and secondary input stage power supply must be always connected.

For all pin modes, STATUS0 outputs the PLL\_LOCK signal and STATUS1 the LOSS OF REFERENCE.

General Note: in all pin mode, all voltage supplies must either be 1.8 V or 2.5/3.3 V and the PWR pin number 44 must be set to 0 or 1 accordingly. In SPI and I2C mode, the supply voltages can be "mixed and matched" as long as the corresponding register bits reflect the supply voltage setting for each desired 1.8 V or 2.5/3.3 V supply. Exception: inputs configured for LVDS signaling (Type = LVDS) are supply agnostic, and therefore can be powered from 2.5 V/3.3 V or 1.8 V regardless of the supply select setting of pin number 44.

**Table 6. Pre-Configured Settings of CDCM6208V1 Accessible by PIN[4:0]<sup>(1)(2)</sup> (continued)**

| SL_MODE[1:0]                                               | pin[4:0] | UseCase       | f <sub>in</sub> (PRL_REF) | Type | f <sub>in</sub> (SEC_REF) | Type    | REF_SEL (note 2) | f(PFD)  | f(VCO)  | f <sub>out</sub> (Y0) | Type | f <sub>out</sub> (Y1) | Type | f <sub>out</sub> (Y2) | Type | f <sub>out</sub> (Y3) | Type | f <sub>out</sub> (Y4) | Type | f <sub>out</sub> (Y5) | Type | f <sub>out</sub> (Y6) | Type | f <sub>out</sub> (Y7) | Type |
|------------------------------------------------------------|----------|---------------|---------------------------|------|---------------------------|---------|------------------|---------|---------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|
| 10                                                         | 0x1B     | PinMode 28-V1 | 25                        | LVDS | 25                        | Crystal | MANU             | 25      | 2500    | 100                   | PECL | 100                   | PECL | 250                   | PECL | 250                   | PECL | 100                   | HCSL | 100                   | HCSL | 125                   | HCSL | 66.67                 | HCSL |
| 10                                                         | 0x1C     | PinMode 29-V1 | 10                        | CMOS | 10                        | Crystal | AUTO             | 10      | 2400    | 25                    | LVDS | 25                    | LVDS | 80                    | LVDS | 80                    | LVDS | 100                   | LVDS | 50                    | LVDS | 66.67                 | LVDS | 44.44                 | CMOS |
| 10                                                         | 0x1D     | PinMode 30-V1 | 25                        | CMOS | 25                        | Crystal | MANU             | 25      | 2500    | 100                   | LVDS | 100                   | LVDS | 125                   | LVDS | 125                   | LVDS | 33.33                 | CMOS | 66.67                 | CMOS | 50                    | CMOS | 25                    | CMOS |
| 10                                                         | 0x1E     | PinMode 31-V1 | 30.72                     | LVDS | 30.72                     | LVDS    | MANU             | 30.72   | 2500    | 156.25                | PECL | 156.25                | PECL | 156.25                | PECL | 156.25                | PECL | 100                   | LVDS | 100                   | LVDS | 25                    | CMOS | 25                    | CMOS |
| 10                                                         | 0x1F     | PinMode 32-V1 | 25                        | LVDS | off                       | off     | MANU             | 25      | 2500    | 125                   | CML  | 125                   | CML  | 125                   | CML  | 125                   | CML  | 100                   | LVDS | 66.67                 | LVDS | 125                   | LVDS | 50                    | LVDS |
| Alternative pin mode usage by modifying input frequencies: |          |               |                           |      |                           |         |                  |         |         |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |
| 10                                                         | 0x01     | PinMode 2-V1  | 26.5625                   | LVDS | 26.5625                   | Crystal | MANU             | 26.5625 | 2550    | 106.25                | PECL | 106.25                | PECL | 106.25                | PECL | 106.25                | PECL | 106.25                | HCSL | 106.25                | HCSL | 106.25                | HCSL | 106.25                | HCSL |
| 10                                                         | 0x02     | PinMode 3-V1  | 26.5625                   | LVDS | 26.5625                   | Crystal | MANU             | 26.5625 | 2550    | 106.25                | CML  | 106.25                | CML  | 106.25                | CML  | 106.25                | CML  | 106.25                | LVDS | 106.25                | LVDS | 106.25                | LVDS | 106.25                | LVDS |
| 10                                                         | 0x03     | PinMode 4-V1  | 24                        | LVDS | 24                        | Crystal | MANU             | 24      | 2400    | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS |
| 10                                                         | 0x03     | PinMode 4-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                         | 0x03     | PinMode 4-V1  | 24.8832                   | LVDS | 24.8832                   | Crystal | MANU             | 24.8832 | 2488.32 | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS |
| 10                                                         | 0x04     | PinMode 5-V1  | 24                        | LVDS | 24                        | Crystal | MANU             | 24      | 2400    | 150                   | PECL | 150                   | PECL | 150                   | PECL | 150                   | PECL | 150                   | HCSL | 150                   | HCSL | 150                   | HCSL | 150                   | HCSL |
| 10                                                         | 0x04     | PinMode 5-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | HCSL | 153.6                 | HCSL | 153.6                 | HCSL | 153.6                 | HCSL |
| 10                                                         | 0x04     | PinMode 5-V1  | 24.8832                   | LVDS | 24.8832                   | Crystal | MANU             | 24.8832 | 2488.32 | 155.52                | PECL | 155.52                | PECL | 155.52                | PECL | 155.52                | PECL | 155.52                | HCSL | 155.52                | HCSL | 155.52                | HCSL | 155.52                | HCSL |
| 10                                                         | 0x05     | PinMode 6-V1  | 24                        | LVDS | 24                        | Crystal | MANU             | 24      | 2400    | 150                   | CML  | 150                   | CML  | 150                   | CML  | 150                   | CML  | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS | 150                   | LVDS |
| 10                                                         | 0x05     | PinMode 6-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 153.6                 | CML  | 153.6                 | CML  | 153.6                 | CML  | 153.6                 | CML  | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                         | 0x05     | PinMode 6-V1  | 24.8832                   | LVDS | 24.8832                   | Crystal | MANU             | 24.8832 | 2488.32 | 155.52                | CML  | 155.52                | CML  | 155.52                | CML  | 155.52                | CML  | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS | 155.52                | LVDS |
| 10                                                         | 0x06     | PinMode 7-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS |
| 10                                                         | 0x07     | PinMode 8-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 122.88                | PECL | 122.88                | PECL | 122.88                | PECL | 122.88                | PECL | 122.88                | HCSL | 122.88                | HCSL | 122.88                | HCSL | 122.88                | HCSL |
| 10                                                         | 0x08     | PinMode 9-V1  | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 122.88                | CML  | 122.88                | CML  | 122.88                | CML  | 122.88                | CML  | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS | 122.88                | LVDS |
| 10                                                         | 0x0A     | PinMode 11-V1 | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 307.2                 | PECL | 307.2                 | PECL | 307.2                 | PECL | 307.2                 | PECL | 307.2                 | HCSL | 307.2                 | HCSL | 307.2                 | HCSL | 307.2                 | HCSL |
| 10                                                         | 0x0C     | PinMode 13-V1 | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 122.88                | HCSL | 122.88                | HCSL | 122.88                | HCSL | 122.88                | HCSL |
| 10                                                         | 0x0D     | PinMode 14-V1 | 26.5625                   | LVDS | 26.5625                   | Crystal | MANU             | 26.5625 | 2550    | 212.5                 | PECL | 212.5                 | PECL | 106.25                | PECL | 106.25                | PECL | 106.25                | HCSL | 106.25                | HCSL | 212.5                 | HCSL | 212.5                 | HCSL |
| 10                                                         | 0x0E     | PinMode 15-V1 | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 491.52                | PECL | 491.52                | PECL | 245.76                | PECL | 245.76                | PECL | 122.88                | HCSL | 122.88                | HCSL | 98.304                | HCSL | 24.576                | CMOS |
| 10                                                         | 0x0F     | PinMode 16-V1 | 24.576                    | LVDS | 24.576                    | Crystal | MANU             | 24.576  | 2457.6  | 622.08                | PECL | 622.08                | PECL | 307.2                 | PECL | 307.2                 | PECL | 153.6                 | HCSL | 153.6                 | HCSL | 122.88                | HCSL | 24.576                | CMOS |
| 10                                                         | 0x11     | PinMode 18-V1 | 25                        | LVDS | 25                        | Crystal | MANU             | 25      | 2500    | 625                   | CML  | 625                   | CML  | 625                   | CML  | 625                   | CML  | 156.25                | LVDS | 156.25                | LVDS | 156.25                | LVDS | 156.25                | LVDS |

**Table 7. Pre-Configured Settings of CDCM6208V1H Accessible by PIN[4:0]<sup>(1)(2)</sup>**

| Pre-Configured Settings of CDCM6208 Accessible by PIN[4:0] |          |                  |              |         |              |         |                  |        |         |          |        |          |         |          |        |          |         |          |             |          |             |          |             |          |             |
|------------------------------------------------------------|----------|------------------|--------------|---------|--------------|---------|------------------|--------|---------|----------|--------|----------|---------|----------|--------|----------|---------|----------|-------------|----------|-------------|----------|-------------|----------|-------------|
| SL_MODE[1:0]                                               | pin[4:0] | UseCase          | fin(PRI_REF) | Type    | fin(SEC_REF) | Type    | REF_SEL (note 2) | f(PFD) | f(VCO)  | fout(Y0) | Type   | fout(Y1) | Type    | fout(Y2) | Type   | fout(Y3) | Type    | fout(Y4) | Type        | fout(Y5) | Type        | fout(Y6) | Type        | fout(Y7) | Type        |
| 00<br>01                                                   | out      | SPI/I2C Default  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2550    | 212.5    | LVPECL | Disable  | Disable | 106.25   | LVPECL | Disable  | Disable | 50       | LVC MOS N+P | Disable  | Disable     | 133.33   | HCSL        | Disable  | Disable     |
| 10                                                         | 0x00     | Pin Mode 1 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | LVPECL  | 25       | LVPECL | 25       | LVPECL  | 156.25   | HCSL        | 156.25   | HCSL        | 125      | LVC MOS N+P | 125      | LVC MOS N+P |
| 10                                                         | 0x01     | Pin Mode 2 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | LVPECL  | 156.25   | LVPECL | 156.25   | LVPECL  | 125      | LVC MOS N+P | 25       | LVC MOS P   | 125      | LVC MOS N+P | 125      | LVC MOS N+P |
| 10                                                         | 0x02     | Pin Mode 3 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 100      | LVPECL | 100      | LVPECL  | 100      | LVPECL | 100      | LVPECL  | 125      | LVC MOS N+P | 25       | LVC MOS N+P | 125      | LVC MOS N+P | 125      | LVC MOS N+P |
| 10                                                         | 0x03     | Pin Mode 4 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | LVPECL  | 25       | LVPECL | 25       | LVPECL  | 100      | HCSL        | 100      | HCSL        | 100      | HCSL        | 100      | HCSL        |
| 10                                                         | 0x04     | Pin Mode 5 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | CML     | 100      | LVPECL | 100      | CML     | 125      | LVC MOS P   | 50       | LVC MOS P   | 100      | HCSL        | 100      | LVC MOS P   |
| 10                                                         | 0x05     | Pin Mode 6 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | CML     | 100      | LVPECL | 100      | CML     | 125      | LVC MOS P   | 125      | HCSL        | 100      | HCSL        | 100      | LVC MOS N+P |
| 10                                                         | 0x06     | Pin Mode 7 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 100      | LVPECL | 100      | LVPECL  | 100      | CML    | 100      | CML     | 100      | LVC MOS P   | 125      | LVC MOS P   | 25       | LVC MOS N+P | 25       | LVC MOS N+P |
| 10                                                         | 0x07     | Pin Mode 8 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 100      | LVPECL | 100      | LVPECL  | 156.25   | LVPECL | 156.25   | LVPECL  | 100      | HCSL        | 100      | HCSL        | 25       | LVC MOS P   | 66.667   | LVC MOS P   |
| 10                                                         | 0x08     | Pin Mode 9 - V1  | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 125      | LVPECL | 125      | LVPECL  | 125      | CML    | 125      | CML     | 125      | LVDS        | 100      | LVDS        | 100      | LVC MOS P   | 24       | LVC MOS P   |
| 10                                                         | 0x09     | Pin Mode 10 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | Disable  | Disable | 100      | CML    | 100      | CML     | 125      | LVDS        | 100      | HCSL        | 100      | LVC MOS P   | 24       | LVC MOS P   |
| 10                                                         | 0x0A     | Pin Mode 11 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 125      | LVPECL | 125      | LVPECL  | 25       | LVPECL | 25       | LVPECL  | 156.25   | LVDS        | 156.25   | HCSL        | 100      | HCSL        | 100      | LVC MOS P   |
| 10                                                         | 0x0B     | Pin Mode 12 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | CML    | 156.25   | LVDS    | 125      | CML    | 125      | LVDS    | Disable  | Disable     | 25       | LVC MOS P   | 100      | HCSL        | 66.67    | LVC MOS P   |
| 10                                                         | 0x0C     | Pin Mode 13 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | LVPECL  | 100      | LVPECL | 100      | CML     | 25       | HCSL        | 25       | LVC MOS P   | 100      | LVC MOS P   | 66.667   | LVC MOS P   |
| 10                                                         | 0x0D     | Pin Mode 14 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 125      | LVPECL | 125      | LVPECL  | 25       | LVPECL | 25       | LVPECL  | 100      | HCSL        | 100      | LVC MOS P   | 25       | LVC MOS P   | 66.667   | LVC MOS P   |
| 10                                                         | 0x0E     | Pin Mode 15 - V1 | 25           | LVC MOS | 25           | XTAL    | MANU             | 25     | 2500    | 156.25   | LVPECL | 156.25   | CML     | 125      | CML    | 125      | CML     | 12       | LVC MOS P   | 25       | LVC MOS P   | 50       | LVC MOS P   | 100      | HCSL        |
| 10                                                         | 0x0F     | Pin Mode 16 - V1 | 38.88        | LVC MOS | 38.88        | LVC MOS | MANU             | 38.88  | 2488.32 | 622.08   | LVPECL | Disable  | Disable | 155.52   | LVPECL | 155.52   | LVPECL  | 155.52   | LVDS        | 155.52   | LVDS        | 77.76    | LVDS        | 77.76    | LVDS        |

- (1) The functionality of the status 0 and status 1 pins in SPI and I<sup>2</sup>C mode is programmable.
- (2) The REF\_SEL input pin selects the primary or secondary input in MANUAL mode. That is: If the system only uses a XTAL on the secondary input, REF\_SEL should be tied to VDD. The primary and secondary input stage power supply must be always connected.  
For all pin modes, STATUS0 outputs the PLL\_LOCK signal.  
General Note: in all pin mode, all voltage supplies must either be 1.8 V or 2.5/3.3 V and the PWR pin number 44 must be set to 0 or 1 accordingly. In SPI and I2C mode, the supply voltages can be *mixed and matched* as long as the corresponding register bits reflect the supply voltage setting for each desired 1.8 V or 2.5/3.3 V supply. Exception: inputs configured for LVDS signaling (Type = LVDS) are supply agnostic, and therefore can be powered from 2.5 V/3.3 V or 1.8 V regardless of the supply select setting of pin number 44.

Table 7. Pre-Configured Settings of CDCM6208V1H Accessible by PIN[4:0]<sup>(1)(2)</sup> (continued)

Pre-Configured Settings of CDCM6208 Accessible by PIN[4:0]

| SI_MODE[1:0] | pin[4:0] | Use Case         | f <sub>in</sub> (PRL_REF) | Type    | f <sub>in</sub> (SEC_REF) | Type    | REF_SEL<br>(note 2) | f(PFD) | f(VCO)  | f <sub>out</sub> (Y0) | Type   | f <sub>out</sub> (Y1) | Type    | f <sub>out</sub> (Y2) | Type   | f <sub>out</sub> (Y3) | Type    | f <sub>out</sub> (Y4) | Type        | f <sub>out</sub> (Y5) | Type        | f <sub>out</sub> (Y6) | Type        | f <sub>out</sub> (Y7) | Type        |
|--------------|----------|------------------|---------------------------|---------|---------------------------|---------|---------------------|--------|---------|-----------------------|--------|-----------------------|---------|-----------------------|--------|-----------------------|---------|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|-----------------------|-------------|
| 10           | 0x10     | Pin Mode 17 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 100                   | CML    | 100                   | CML     | 125                   | CML    | 125                   | CML     | 83.33                 | LVC MOS P   | 25                    | LVC MOS N+P | 100                   | LVC MOS N+P | 125                   | LVC MOS N+P |
| 10           | 0x11     | Pin Mode 18 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2400    | 100                   | LVPECL | 100                   | LVPECL  | 100                   | LVPECL | 100                   | LVPECL  | 25                    | LVC MOS P   | Disable               | Disable     | 40                    | LVC MOS P   | 66.667                | LVC MOS P   |
| 10           | 0x12     | Pin Mode 19 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 156.25                | CML    | 156.25                | LVDS    | 100                   | CML    | 100                   | LVDS    | Disable               | Disable     | 25                    | LVC MOS N+P | 66.67                 | LVC MOS P   | 100                   | HCSL        |
| 10           | 0x13     | Pin Mode 20 - V1 | 38.88                     | LVC MOS | 38.88                     | LVC MOS | MANU                | 38.88  | 2488.32 | 155.52                | LVPECL | 155.52                | LVPECL  | 155.52                | LVPECL | 155.52                | LVPECL  | 77.76                 | LVDS        | Disable               | Disable     | Disable               | Disable     | 25                    | LVC MOS N+P |
| 10           | 0x14     | Pin Mode 21 - V1 | 38.88                     | LVC MOS | 38.88                     | LVC MOS | MANU                | 38.88  | 2488.32 | 77.76                 | LVPECL | Disable               | Disable | 77.76                 | LVDS   | Disable               | Disable | 77.76                 | LVC MOS N+P | 77.76                 | LVC MOS N+P | 38.88                 | LVC MOS N+P | 25                    | LVC MOS N+P |
| 10           | 0x15     | Pin Mode 22 - V1 | 19.2                      | LVC MOS | 19.2                      | LVC MOS | MANU                | 0.8    | 2500    | 100                   | LVPECL | Disable               | Disable | 125                   | LVPECL | Disable               | Disable | 125                   | LVC MOS N+P | 25                    | LVC MOS N+P | 66.67                 | LVC MOS P   | 2.048                 | LVC MOS P   |
| 10           | 0x16     | Pin Mode 23 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 100                   | LVPECL | 100                   | LVPECL  | 125                   | LVPECL | 125                   | LVPECL  | Disable               | Disable     | 25                    | LVC MOS P   | 66.667                | LVC MOS P   | 2.048                 | LVC MOS P   |
| 10           | 0x17     | Pin Mode 24 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 125                   | LVDS   | 125                   | LVDS    | 100                   | LVDS   | 100                   | LVDS    | 100                   | LVDS        | 100                   | LVC MOS N+P | 25                    | LVDS        | 25                    | LVC MOS N+P |
| 10           | 0x18     | Pin Mode 25 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2400    | 100                   | LVDS   | 100                   | LVDS    | 100                   | LVDS   | 100                   | LVDS    | 25                    | LVDS        | 25                    | LVC MOS P   | 133.33                | LVDS        | 66.67                 | LVC MOS P   |
| 10           | 0x19     | Pin Mode 26 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 156.25                | LVPECL | 156.25                | CML     | 125                   | LVPECL | 125                   | CML     | Disable               | Disable     | 25                    | LVC MOS N+P | 66.67                 | LVC MOS P   | 2.048                 | LVC MOS P   |
| 10           | 0x1A     | Pin Mode 27 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 156.25                | LVPECL | 156.25                | LVPECL  | 125                   | LVPECL | 125                   | LVPECL  | 133.33                | LVDS        | 25                    | LVC MOS P   | 100                   | HCSL        | 100                   | HCSL        |
| 10           | 0x1B     | Pin Mode 28 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2400    | 100                   | LVPECL | 100                   | LVPECL  | 96                    | LVPECL | Disable               | Disable | 133.33                | HCSL        | 33.33                 | LVC MOS P   | 14.31818              | LVC MOS P   | 48                    | LVC MOS P   |
| 10           | 0x1C     | Pin Mode 29 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 156.25                | LVPECL | 156.25                | CML     | 100                   | LVPECL | 100                   | CML     | 25                    | HCSL        | 25                    | LVDS        | 100                   | HCSL        | 100                   | HCSL        |
| 10           | 0x1D     | Pin Mode 30 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 156.25                | LVPECL | 156.25                | CML     | 125                   | LVPECL | 125                   | CML     | 25                    | LVDS        | 33.33                 | LVC MOS P   | 100                   | HCSL        | 50                    | LVC MOS P   |
| 10           | 0x1E     | Pin Mode 31 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 125                   | LVPECL | 125                   | LVPECL  | 25                    | LVPECL | 25                    | LVPECL  | 156.25                | LVDS        | Disable               | Disable     | 100                   | LVDS        | 12                    | LVC MOS P   |
| 10           | 0x1F     | Pin Mode 32 - V1 | 25                        | LVC MOS | 25                        | XTAL    | MANU                | 25     | 2500    | 125                   | LVPECL | 125                   | LVPECL  | 100                   | LVPECL | 100                   | LVPECL  | 156.25                | LVDS        | Disable               | Disable     | 25                    | LVC MOS N+P | 25                    | LVC MOS N+P |

# CDCM6208

SCAS931G – MAY 2012–REVISED JANUARY 2018

www.ti.com

**Table 8. Pre-Configured Settings of CDCM6208V2 Accessible by PIN[4:0]<sup>(1)(2)</sup>**

| SL_MODE[1:0] | pin[4:0] | UseCase       | fin(PRI_REF) | Type | fin(SEC_REF) | Type    | REF_SEL (note 2) | f(PFD) | f(VCO)  | fout(Y0) | Type | fout(Y1) | Type | fout(Y2) | Type | fout(Y3) | Type | fout(Y4) | Type | fout(Y5) | Type | fout(Y6) | Type | fout(Y7) | Type |
|--------------|----------|---------------|--------------|------|--------------|---------|------------------|--------|---------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|----------|------|
| 00           | I/O      | SPI Default   | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72  | 3072    | 153.60   | LVDS | 153.60   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 61.44    | LVDS | 61.44    | LVDS | 30.72    | LVDS | 30.72    | LVDS |
| 01           | I/O      | I2C Default   | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72  | 3072    | 153.60   | LVDS | 153.60   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 61.44    | LVDS | 61.44    | LVDS | 30.72    | LVDS | 30.72    | LVDS |
| 11           | RESERVED |               |              |      |              |         |                  |        |         |          |      |          |      |          |      |          |      |          |      |          |      |          |      |          |      |
| 10           | 0x00     | PinMode 1-V2  | 19.44        | LVDS | 19.44        | Crystal | MANU             | 19.44  | 3110.4  | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS |
| 10           | 0x01     | PinMode 2-V2  | 19.44        | LVDS | 19.44        | Crystal | MANU             | 19.44  | 3110.4  | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS |
| 10           | 0x02     | PinMode 3-V2  | 19.44        | LVDS | 19.44        | Crystal | MANU             | 19.44  | 3110.4  | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | PECL | 155.52   | HCSL | 155.52   | HCSL | 155.52   | HCSL | 155.52   | HCSL |
| 10           | 0x03     | PinMode 4-V2  | 19.44        | LVDS | 19.44        | Crystal | MANU             | 19.44  | 3110.4  | 622.08   | PECL | 622.08   | PECL | 622.08   | PECL | 622.08   | PECL | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS |
| 10           | 0x04     | PinMode 5-V2  | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 125      | PECL | 125      | PECL | 125      | PECL | 125      | PECL | 100      | HCSL | 100      | HCSL | 100      | HCSL | 100      | HCSL |
| 10           | 0x05     | PinMode 6-V2  | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS | 100      | LVDS |
| 10           | 0x06     | PinMode 7-V2  | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 250      | LVDS | 250      | LVDS | 250      | LVDS | 250      | LVDS | 250      | LVDS | 250      | LVDS | 250      | LVDS | 250      | LVDS |
| 10           | 0x07     | PinMode 8-V2  | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 200      | PECL | 200      | PECL | 200      | PECL | 200      | PECL | 200      | HCSL | 200      | HCSL | 200      | HCSL | 200      | HCSL |
| 10           | 0x08     | PinMode 9-V2  | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 187.5    | PECL | 187.5    | PECL | 187.5    | PECL | 187.5    | PECL | 187.5    | HCSL | 187.5    | HCSL | 187.5    | HCSL | 187.5    | HCSL |
| 10           | 0x09     | PinMode 10-V2 | 38.4         | LVDS | 38.4         | Crystal | MANU             | 38.4   | 3072    | 153.6    | LVDS | 153.6    | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 153.6    | LVDS | 153.6    | LVDS |
| 10           | 0x0A     | PinMode 11-V2 | 38.4         | LVDS | 38.4         | Crystal | MANU             | 9.6    | 3072    | 153.6    | LVDS | 153.6    | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 153.6    | LVDS | 153.6    | LVDS |
| 10           | 0x0B     | PinMode 12-V2 | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 100      | LVDS | x        | x    | x        | x    | x        | x    | 100      | HCSL | 25       | CMOS | 24       | CMOS | 27       | CMOS |
| 10           | 0x0C     | PinMode 13-V2 | 122.88       | LVDS | 122.88       | LVDS    | MANU             | 3.072  | 3072    | 153.6    | LVDS | 153.6    | LVDS | 122.88   | LVDS | 122.88   | LVDS | 30.72    | LVDS | 30.72    | LVDS | 61.44    | LVDS | 61.44    | LVDS |
| 10           | 0x0D     | PinMode 14-V2 | 153.6        | LVDS | 153.6        | LVDS    | MANU             | 0.384  | 3072    | 153.6    | LVDS | 153.6    | LVDS | 122.88   | LVDS | 122.88   | LVDS | 30.72    | LVDS | 30.72    | LVDS | 61.44    | LVDS | 61.44    | LVDS |
| 10           | 0x0E     | PinMode 15-V2 | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72  | 2949.12 | 491.52   | PECL | 491.52   | PECL | 245.76   | PECL | 245.76   | PECL | 122.88   | LVDS | 122.88   | LVDS | 61.44    | LVDS | 30.72    | LVDS |
| 10           | 0x0F     | PinMode 16-V2 | 19.44        | LVDS | 19.44        | Crystal | MANU             | 19.44  | 3110.4  | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 155.52   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS |
| 10           | 0x10     | PinMode 17-V2 | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72  | 2949.12 | 245.76   | LVDS | 245.76   | LVDS | 245.76   | LVDS | 245.76   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS | 122.88   | LVDS |
| 10           | 0x11     | PinMode 18-V2 | 25           | LVDS | 25           | Crystal | MANU             | 6.25   | 3125    | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 156.25   | LVDS | 106.25   | LVDS | 106.25   | LVDS | 106.25   | LVDS | 106.25   | LVDS |
| 10           | 0x12     | PinMode 19-V2 | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 106.25   | LVDS | 106.25   | LVDS | 106.25   | LVDS | 106.25   | LVDS |
| 10           | 0x13     | PinMode 20-V2 | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3125    | 156.25   | PECL | 156.25   | PECL | 125      | PECL | 125      | PECL | 66.67    | CMOS | 33.33    | CMOS | 50       | CMOS | 12.5     | CMOS |
| 10           | 0x14     | PinMode 21-V2 | 25           | CMOS | 25           | Crystal | MANU             | 25     | 3125    | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 66.67    | LVDS | 156.25   | LVDS | 125      | LVDS | 100      | LVDS |
| 10           | 0x15     | PinMode 22-V2 | 25           | LVDS | 25           | Crystal | MANU             | 1      | 3072    | 153.6    | LVDS | 153.6    | LVDS | 122.88   | LVDS | 122.88   | LVDS | 66.67    | LVDS | 156.25   | LVDS | 30.72    | LVDS | 100      | LVDS |
| 10           | 0x16     | PinMode 23-V2 | 19.2         | LVDS | 19.2         | Crystal | MANU             | 3.84   | 2949.12 | 122.88   | LVDS | 122.88   | PECL | 122.88   | LVDS | 122.88   | LVDS | 30.72    | LVDS | 66.67    | LVDS | 153.6    | LVDS | 250      | LVDS |
| 10           | 0x17     | PinMode 24-V2 | 30.72        | LVDS | 30.72        | Crystal | MANU             | 30.72  | 2949.12 | 122.88   | LVDS | 122.88   | LVDS | 30.72    | LVDS | 30.72    | LVDS | 66.67    | LVDS | 100      | LVDS | 156.25   | LVDS | 156.25   | LVDS |
| 10           | 0x18     | PinMode 25-V2 | 25           | LVDS | 25           | Crystal | MANU             | 25     | 3000    | 125      | LVDS | 125      | LVDS | 125      | LVDS | 125      | LVDS | 68.75    | LVDS | 68.75    | LVDS | 68.75    | LVDS | 68.75    | LVDS |
| 10           | 0x19     | PinMode 26-V2 | 10           | LVDS | 10           | Crystal | MANU             | 0.08   | 2949.12 | 245.76   | PECL | 245.76   | PECL | 122.88   | PECL | 122.88   | PECL | 125      | LVDS | 100      | LVDS | 307.2    | LVDS | 307.2    | LVDS |
| 10           | 0x1A     | PinMode 27-V2 | 30.72        | LVDS | 30.72        | LVDS    | MANU             | 30.72  | 2949.12 | 122.88   | LVDS | x        | x    | 30.72    | LVDS | 30.72    | LVDS | 156.25   | LVDS | 156.25   | LVDS | 100      | LVDS | 66.67    | LVDS |
| 10           | 0x1B     | PinMode 28-V2 | 10           | CMOS | 10           | LVDS    | MANU             | 0.08   | 2949.12 | 245.76   | CML  | 245.76   | CML  | 122.88   | CML  | 122.88   | CML  | 30.72    | LVDS | 66.67    | LVDS | 156.25   | LVDS | 307.2    | LVDS |

- (1) The functionality of the status 0 and status 1 pins in SPI and I<sup>2</sup>C mode is programmable.
- (2) The REF\_SEL input pin selects the primary or secondary input in MANUAL mode. That is: If the system only uses a XTAL on the secondary input, REF\_SEL should be tied to VDD. The primary and secondary input stage power supply must be always connected.
- For all pin modes, STATUS0 outputs the PLL\_LOCK signal and STATUS1 the LOSS OF REFERENCE.
- General Note: in all pin mode, all voltage supplies must either be 1.8 V or 2.5/3.3 V and the PWR pin number 44 must be set to 0 or 1 accordingly. In SPI and I<sup>2</sup>C mode, the supply voltages can be *mixed and matched* as long as the corresponding register bits reflect the supply voltage setting for each desired 1.8-V or 2.5/3.3-V supply.

**Table 8. Pre-Configured Settings of CDCM6208V2 Accessible by PIN[4:0]<sup>00</sup> (continued)**

| SL_MODE[1:0]                                              | pin[4:0] | UseCase       | f <sub>in</sub> (PRI_REF) | Type | f <sub>in</sub> (SEC_REF) | Type    | REF_SEL (note 2) | f(PFD) | f(VCO)  | f <sub>out</sub> (Y0) | Type | f <sub>out</sub> (Y1) | Type | f <sub>out</sub> (Y2) | Type | f <sub>out</sub> (Y3) | Type | f <sub>out</sub> (Y4) | Type | f <sub>out</sub> (Y5) | Type | f <sub>out</sub> (Y6) | Type | f <sub>out</sub> (Y7) | Type |
|-----------------------------------------------------------|----------|---------------|---------------------------|------|---------------------------|---------|------------------|--------|---------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|-----------------------|------|
| 10                                                        | 0x1C     | PinMode 29-V2 | 19.44                     | LVDS | 19.44                     | Crystal | MANU             | 0.01   | 3125    | 156.25                | LVDS | 156.25                | LVDS | 125                   | LVDS | 125                   | LVDS | 66.67                 | LVDS | 100                   | LVDS | 25                    | LVDS | 25                    | LVDS |
| 10                                                        | 0x1D     | PinMode 30-V2 | 30.72                     | LVDS | 30.72                     | Crystal | MANU             | 30.72  | 2949.12 | 737.28                | PECL | 737.28                | PECL | 491.52                | PECL | 491.52                | PECL | 122.88                | HCSL | 122.88                | HCSL | 122.88                | LVDS | 122.88                | LVDS |
| 10                                                        | 0x1E     | PinMode 31-V2 | 30.72                     | LVDS | 30.72                     | Crystal | MANU             | 30.72  | 3072    | 614.4                 | PECL | 614.4                 | PECL | 307.2                 | PECL | 307.2                 | PECL | 153.6                 | HCSL | 153.6                 | HCSL | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                        | 0x1F     | PinMode 32-V2 | 30.72                     | LVDS | 30.72                     | Crystal | MANU             | 30.72  | 3072    | 153.6                 | CML  | 153.6                 | CML  | 153.6                 | CML  | 153.6                 | CML  | 100                   | LVDS | 66.67                 | LVDS | 125                   | LVDS | 50                    | LVDS |
| Alternative PinMode usage by modifying input frequencies: |          |               |                           |      |                           |         |                  |        |         |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |                       |      |
| 10                                                        | 0x00     | PinMode 1-V2  | 19.2                      | LVDS | 19.2                      | Crystal | MANU             | 19.2   | 3072    | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                        | 0x01     | PinMode 2-V2  | 19.2                      | LVDS | 19.2                      | Crystal | MANU             | 19.2   | 3072    | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | PECL | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                        | 0x03     | PinMode 4-V2  | 19.2                      | LVDS | 19.2                      | Crystal | MANU             | 19.2   | 3072    | 614.4                 | PECL | 614.4                 | PECL | 614.4                 | PECL | 614.4                 | PECL | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS | 153.6                 | LVDS |
| 10                                                        | 0x11     | PinMode 18-V1 | 25                        | LVDS | 25                        | Crystal | MANU             | 25     | 2500    | 625                   | CML  | 625                   | CML  | 625                   | CML  | 625                   | CML  | 156.25                | LVDS | 156.25                | LVDS | 156.25                | LVDS | 156.25                | LVDS |

**CDCM6208**

SCAS931G – MAY 2012–REVISED JANUARY 2018

[www.ti.com](http://www.ti.com)

## 8.4.2 Loop Filter Recommendations for Pin Modes

The following two tables provide the internal charge pump and R3/C3 settings for pin modes. The designer can either design their own optimized loop filter, or use the suggested loop filter in the [Table 10](#).

**Table 9. CDCM6208V1 Loop Filter Recommendation for Pin Mode**

| SI_MODE [1:0] | PIN[4:0] | USECASE          | f(PFD)<br>[MHz] | ICP<br>[mA] | SUGGESTED LOOP FILTER<br>C1/R2/C2 | INTERNAL LPF COMPONENTS |          |
|---------------|----------|------------------|-----------------|-------------|-----------------------------------|-------------------------|----------|
|               |          |                  |                 |             |                                   | R3                      | C3       |
| 00            | out      | SPI Default      | 25              | 2.5         | 100pF/500R/22nF                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x00     | Pin Mode 1 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x01     | Pin Mode 2 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x02     | Pin Mode 3 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x03     | Pin Mode 4 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x04     | Pin Mode 5 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x05     | Pin Mode 6 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x06     | Pin Mode 7 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x07     | Pin Mode 8 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x08     | Pin Mode 9 - V1  | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x09     | Pin Mode 10 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0A     | Pin Mode 11 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0B     | Pin Mode 12 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0C     | Pin Mode 13 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0D     | Pin Mode 14 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0E     | Pin Mode 15 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x0F     | Pin Mode 16 - V1 | 25              | 2.5         | 220pF/400/22nF                    | 100 $\Omega$            | 242.5 pF |
| 10            | 0x10     | Pin Mode 17 - V1 | 30.72           | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x11     | Pin Mode 18 - V1 | 24.8832         | 2.5         | 100pF/500R/22nF                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x12     | Pin Mode 19 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x13     | Pin Mode 20 - V1 | 0.008           | 0.5         | 1uF/1.3k/22uF                     | 4010 $\Omega$           | 562.5 pF |
| 10            | 0x14     | Pin Mode 21 - V1 | 25              | 2.5         | 100pF/500R/22nF                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x15     | Pin Mode 22 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x16     | Pin Mode 23 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x17     | Pin Mode 24 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x18     | Pin Mode 25 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x19     | Pin Mode 26 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x1A     | Pin Mode 27 - V1 | 25              | 2.5         |                                   | 10 $\Omega$             | 30.0 pF  |
| 10            | 0x1B     | Pin Mode 28 - V1 | 25              | 2.5         |                                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x1C     | Pin Mode 29 - V1 | 10              | 2.5         | 20pF/1210/68nF                    | 100 $\Omega$            | 242.5 pF |
| 10            | 0x1D     | Pin Mode 30 - V1 | 25              | 2.5         | 100pF/500R/22nF                   | 100 $\Omega$            | 242.5 pF |
| 10            | 0x1E     | Pin Mode 31 - V1 | 0.04            | 0.5         | 4.7uF/250/47uF                    | 4010 $\Omega$           | 562.5 pF |
| 10            | 0x1F     | Pin Mode 32 - V1 | 25              | 2.5         | 100pF/500R/22nF                   | 100 $\Omega$            | 242.5 pF |

**Table 10. CDCM6208V1H Loop Filter Recommendation for Pin Mode**

| SI_MODE<br>[1:0] | pin[4:0] | UseCase          | f(PFD) | ICP  | suggested loop Filter | Internal LPF<br>components |       |
|------------------|----------|------------------|--------|------|-----------------------|----------------------------|-------|
|                  |          |                  | [MHz]  | [mA] | C1/R2/C2              | R3                         | C3    |
| 00<br>01         | out      | SPI/I2C Default  | 25     | 2.5  | 100pF/500/22nF        | 10 Ohm                     | 35 pF |
| 10               | 0x00     | Pin Mode 1 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x01     | Pin Mode 2 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x02     | Pin Mode 3 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x03     | Pin Mode 4 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x04     | Pin Mode 5 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x05     | Pin Mode 6 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x06     | Pin Mode 7 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x07     | Pin Mode 8 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x08     | Pin Mode 9 - V1  | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x09     | Pin Mode 10 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0A     | Pin Mode 11 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0B     | Pin Mode 12 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0C     | Pin Mode 13 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0D     | Pin Mode 14 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0E     | Pin Mode 15 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x0F     | Pin Mode 16 - V1 | 38.88  | 2.0  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x10     | Pin Mode 17 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x11     | Pin Mode 18 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x12     | Pin Mode 19 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x13     | Pin Mode 20 - V1 | 38.88  | 2.0  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x14     | Pin Mode 21 - V1 | 38.88  | 2.0  | 10pF/2.8k/4.7nF       | 10 Ohm                     | 35 pF |
| 10               | 0x15     | Pin Mode 22 - V1 | 0.8    | 3.0  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x16     | Pin Mode 23 - V1 | 25     | 2.5  | 100pF/500/22nF        | 10 Ohm                     | 35 pF |
| 10               | 0x17     | Pin Mode 24 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x18     | Pin Mode 25 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x19     | Pin Mode 26 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1A     | Pin Mode 27 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1B     | Pin Mode 28 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1C     | Pin Mode 29 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1D     | Pin Mode 30 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1E     | Pin Mode 31 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |
| 10               | 0x1F     | Pin Mode 32 - V1 | 25     | 2.5  |                       | 10 Ohm                     | 35 pF |

**CDCM6208**

SCAS931G – MAY 2012–REVISED JANUARY 2018

[www.ti.com](http://www.ti.com)
**Table 11. CDCM6208V2 Loop Filter Recommendation for Pin Mode**

| SI_MODE [1:0] | PIN[4:0] | USECASE          | f(PFD)<br>[MHz] | ICP<br>[mA] | SUGGESTED LOOP FILTER<br>C1/R2/C2 | INTERNAL LPF COMPONENTS |          |
|---------------|----------|------------------|-----------------|-------------|-----------------------------------|-------------------------|----------|
|               |          |                  |                 |             |                                   | R3                      | C3       |
| 00            | out      | SPI Default      | 30.72           | 2.5         | 470pF/560R/100nF                  | 100 Ω                   | 242.5 pF |
| 10            | 0x00     | Pin Mode 1 - V1  | 19.44           | 2.5         | 330pF/530R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x01     | Pin Mode 2 - V1  | 19.44           | 0.5         | 4.7uF/10R/100uF                   | 4010 Ω                  | 562.5 pF |
| 10            | 0x02     | Pin Mode 3 - V1  | 19.44           | 2.5         | 330pF/530R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x03     | Pin Mode 4 - V1  | 19.44           | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x04     | Pin Mode 5 - V1  | 25              | 2.5         | 200pF/400R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x05     | Pin Mode 6 - V1  | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x06     | Pin Mode 7 - V1  | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x07     | Pin Mode 8 - V1  | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x08     | Pin Mode 9 - V1  | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x09     | Pin Mode 10 - V1 | 38.4            | 2.5         | 220p/280R/22n                     | 100 Ω                   | 242.5 pF |
| 10            | 0x0A     | Pin Mode 11 - V1 | 9.6             | 0.5         | 4.7uF/10R/100uF                   | 4010 Ω                  | 562.5 pF |
| 10            | 0x0B     | Pin Mode 12 - V1 | 25              | 2.5         | 200pF/400R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x0C     | Pin Mode 13 - V1 | 3.072           | 0.5         | 10uF/15R/100uF                    | 4010 Ω                  | 562.5 pF |
| 10            | 0x0D     | Pin Mode 14 - V1 | 0.384           | 0.5         | 10uF/42R/100uF                    | 4010 Ω                  | 562.5 pF |
| 10            | 0x0E     | Pin Mode 15 - V1 | 30.72           | 2.5         | 470pF/560R/100nF                  | 100 Ω                   | 242.5 pF |
| 10            | 0x0F     | Pin Mode 16 - V1 | 19.44           | 2.5         | 330pF/530R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x10     | Pin Mode 17 - V1 | 30.72           | 2.5         | 470pF/560R/100nF                  | 100 Ω                   | 242.5 pF |
| 10            | 0x11     | Pin Mode 18 - V1 | 6.25            | 2.5         | 100p/1.1k/10n                     | 530 Ω                   | 310.0 pF |
| 10            | 0x12     | Pin Mode 19 - V1 | 25              | 2.5         | 200pF/400R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x13     | Pin Mode 20 - V1 | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x14     | Pin Mode 21 - V1 | 25              | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x15     | Pin Mode 22 - V1 | 1               | 2.5         | 100p/1.5k/100n                    | 4010 Ω                  | 562.5 pF |
| 10            | 0x16     | Pin Mode 23 - V1 | 3.84            | 1.5         | 22nF/220R/1uF                     | 1050 Ω                  | 562.5 pF |
| 10            | 0x17     | Pin Mode 24 - V1 | 30.72           | 2.5         | 470pF/560R/100nF                  | 100 Ω                   | 242.5 pF |
| 10            | 0x18     | Pin Mode 25 - V1 | 25              | 2.5         | 200pF/400R/22nF                   | 100 Ω                   | 242.5 pF |
| 10            | 0x19     | Pin Mode 26 - V1 | 0.08            | 1           | 5uF/100/100uF                     | 4010 Ω                  | 562.5 pF |
| 10            | 0x1A     | Pin Mode 27 - V1 | 30.72           | 2.5         | 470pF/560R/100nF                  | 10 Ω                    | 242.5 pF |
| 10            | 0x1B     | Pin Mode 28 - V1 | 0.08            | 1           | 5uF/100/100uF                     | 4010 Ω                  | 562.5 pF |
| 10            | 0x1C     | Pin Mode 29 - V1 | 0.01            | 1.5         | 5uF/200/100uF                     | 4010 Ω                  | 562.5 pF |
| 10            | 0x1D     | Pin Mode 30 - V1 | 30.72           | 2.5         | 470pF/560R/100nF                  | 100 Ω                   | 242.5 pF |
| 10            | 0x1E     | Pin Mode 31 - V1 | 30.72           | 2.5         |                                   | 100 Ω                   | 242.5 pF |
| 10            | 0x1F     | Pin Mode 32 - V1 | 30.72           | 2.5         |                                   | 100 Ω                   | 242.5 pF |

### 8.4.3 Status Pins Definition

The device vitals such as input signal quality, smart mux input selection, and PLL lock can be monitored by reading device registers or at the status pins STATUS1, and STATUS0. Register 3[12:7] allows for customization of which vitals are mapped to these two pins. Table 12 lists the three events that can be mapped to each status pin and which can also be read in the register space.

**Table 12. CDCM6208 Status Pin Definition List**

| STATUS<br>SIGNAL NAME | SIGNAL TYPE | SIGNAL NAME | REGISTER BIT<br>NO. | DESCRIPTION                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |
|-----------------------|-------------|-------------|---------------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| SEL_REF               | LVC MOS     | STATUS0, 1  | Reg 3.12<br>Reg 3.9 | Indicates Reference Selected for PLL:<br>0 → Primary input selected to drive PLL<br>1 → Secondary input selected to drive PLL                                                                                                                                                                                                                                                                                                                                                                                                                                  |
| LOS_REF               | LVC MOS     | STATUS0, 1  | Reg 3.11<br>Reg 3.8 | Loss of selected reference input observed at active input:<br>0 → Reference input present<br>1 → Loss of reference input<br>Important Note 1: For LOS_REF to operate properly, the secondary input SEC_IN must be enabled. Set register Q4.5=1. If register Q4.5 is set to zero, LOS_REF will output a static high signal regardless of the actual input signal status on PRI_IN.                                                                                                                                                                              |
| PLL_UNLOCK            | LVC MOS     | STATUS0, 1  | Reg 3.10<br>Reg 3.7 | Indicates unlock status for PLL (digital):<br>PLL locked → Q21.02 = 0 and $V_{STATUS0/1} = V_{IH}$<br>PLL unlocked → Q21.2 = 1 and $V_{STATUS0/1} = V_{IL}$ See note <sup>(1)</sup><br>Note 2: If the smartmux is enabled and both reference clocks stall, the STATUSx output signal will 98% of the time indicate the LOS condition with a static high signal. However, in 2% of the cases, the LOS detection engine erroneously stalls at a state where the STATUSx output PLL lock indicator will signalize high for 511 out of every 512 PFD clock cycles. |

(1) The reverse logic between the register Q21.2 and the external output signal on STATUS0 or STATUS1.

#### NOTE

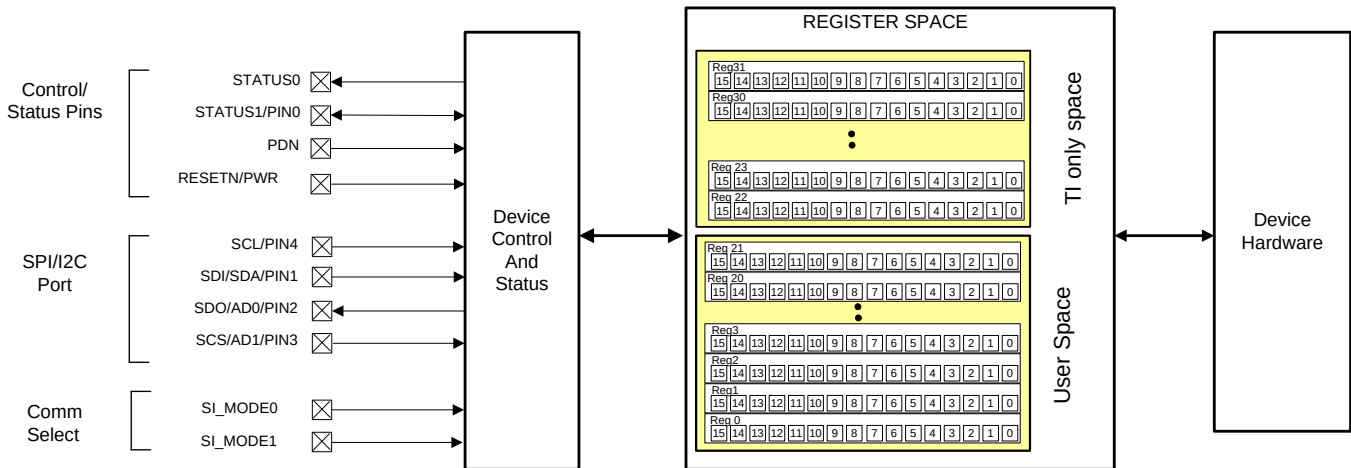
It is recommended to assert only one out of the three register bits for each of the status pins. For example, to monitor the PLL lock status on STATUS0 and the selected reference clock sources on STATUS1 output, the device register settings would be Q3.12 = Q3.7 = 1 and Q3.11 = Q3.10 = Q3.9 = Q3.8 = 0. If a status pin is unused, it is recommended to set the according 3 register bits to zero (for example, Q3[12:9] = 0 for STATUS0 = 0). If more than one bit is enabled for each STATUS signal, the function becomes OR'ed. For example, if Q3.11 = Q3.10 = 1 and Q3.12 = 0, the STATUS0 output would be high either if the device goes out of lock or the selected reference clock signal is lost.

### 8.4.4 PLL Lock Detect

The PLL lock detection circuit is a digital detection circuit which detects any frequency error, even a single cycle slip. The PLL unlock is signalized when a certain number of cycle slips have been exceeded, at which point the counter is reset. A frequency error of 2% will cause PLL unlock to stay low. A 0.5% frequency error shows up as toggling the PLL lock output with roughly 50% duty cycle at roughly 1/1000<sup>th</sup> of the PFD update frequency to the device. A frequency error of 1ppm would show up as rare toggling low for a duration of approximately 1000 PFD update clock cycles. If the system plans using PLL lock to toggle a system reset, then consider adding an RC filter on the PLL LOCK output (Status 1 or Status 0) to avoid rare cycle slips from triggering an entire system reset.

### 8.4.5 Interface and Control

The host (DSP, Microcontroller, FPGA, etc) configures and monitors the CDCM6208 through the SPI or I<sup>2</sup>C port. The host reads and writes to a collection of control/status bits called the register file. Typically, a hardware block is controlled and monitored via a specific grouping of bits located within the register file. The host controls and monitors certain device-wide critical parameters directly, through control/status pins. In the absence of a host, the CDCM6208 can be configured to operate in pin mode where the control pins [PIN0-PIN4] can be set appropriately to generate the necessary clock outputs out of the device.



SPI: SI\_MODE[1:0]=00; I2C: SI\_MODE[1:0]=01; Pin Mode: SI\_MODE[1:0]=10

**Figure 38. CDCM6208 Interface and Control Block**

Within this register space, there are certain bits that have read/write access. Other bits are read-only (an attempt to write to a read only bit will not change the state of the bit).

#### 8.4.5.1 Register File Reference Convention

Figure 39 shows the method this document employs to refer to an individual register bit or a grouping of register bits. If a drawing or text references an individual bit, the format is to specify the register number first and the bit number second. The CDCM6208 contains 21 registers that are 16 bits wide. The register addresses and the bit positions both begin with the number zero (0). A period separates the register address and bit address. The first bit in the register file is address 'R0.0' meaning that it is located in Register 0 and is bit position 0. The last bit in the register file is address R31.15 referring to the 16<sup>th</sup> bit of register address 31 (the 32<sup>nd</sup> register in the device

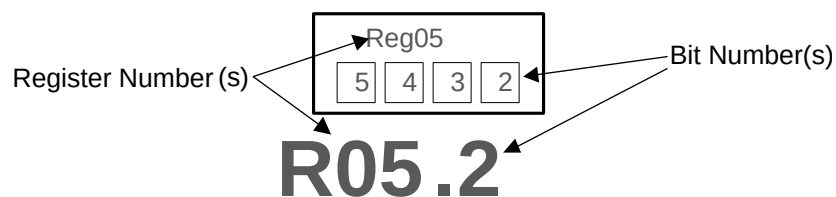


**Figure 39. CDCM6208 Register Reference Format**

### 8.4.5.2 SPI - Serial Peripheral Interface

To enable the SPI port, tie the communication select pins SI\_MODE[1:0] to ground. SPI is a master/slave protocol in which the host system is always the master; therefore, the host always initiates communication to/from the device. The SPI interface consists of four signal pins. The device SPI address is 0000.

Table 13. Serial Port Signals in SPI Mode

| PIN          |        | I/O    | DESCRIPTION                     |
|--------------|--------|--------|---------------------------------|
| NAME         | NUMBER |        |                                 |
| SDI/SDA/PIN1 | 2      | Input  | SDI: SPI Serial Data Input      |
| SDO/AD0/PIN2 | 3      | Output | SDO: SPI Serial Data            |
| SCS/AD1/PIN3 | 4      | Input  | SCS: SPI Latch Enable           |
| SCL/PIN4     | 5      | Input  | SCL: SPI/I <sup>2</sup> C Clock |

The host must present data to the device MSB first. A message includes a transfer direction bit, an address field, and a data field as depicted in Figure 40

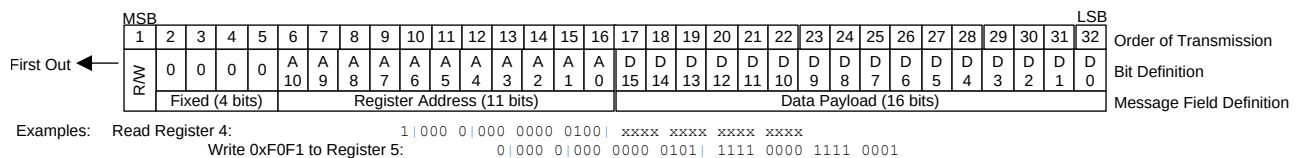


Figure 40. CDCM6208 SPI Message Format

#### 8.4.5.2.1 Writing to the CDCM6208

To initiate a SPI data transfer, the host asserts the SCS (serial chip select) pin low. The first rising edge of the clock signal (SCL) transfers the bit presented on the SDI pin of the CDCM6208. This bit signals if a read (first bit high) or a write (first bit low) will transpire. The SPI port shifts data to the CDCM6208 with each rising edge of SCL. Following the W/R bit are 4 fixed bits followed by 11 bits that specify the address of the target register in the register file. The 16 bits that follow are the data payload. If the host sends an incomplete message, (i.e. the host de-asserts the SCS pin high prior to a complete message transmission), then the CDCM6208 aborts the transfer, and device makes no changes to the register file or the hardware. Figure 42 shows the format of a write transaction on the CDCM6208 SPI port. The host signals the CDCM6208 of the completed transfer and disables the SPI port by de-asserting the SCS pin high.

#### 8.4.5.2.2 Reading From the CDCM6208

As with the write operation, the host first initiates a SPI transfer by asserting the SCS pin low. The host signals a read operation by shifting a logical high in the first bit position, signaling the CDCM6208 that the host is imitating a read data transfer from the device. During the portion of the message in which the host specifies the CDCM6208 register address, the host presents this information on the SDI pin of the device (for the first 15 clock cycles after the W/R bit). During the 16 clock cycles that follow, the CDCM6208 presents the data from the register specified in the first half of the message on the SDO pin. The SDO output is 3-stated anytime SCS is high, so that multiple SPI slave devices can be connected to the same serial bus. The host signals the CDCM6208 that the transfer is complete by de-asserting the SCS pin high.

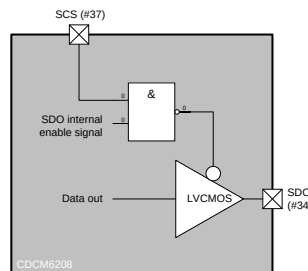


Figure 41. Reading From the CDCM6208

### 8.4.5.2.3 Block Write/Read Operation

The device supports a block write and block read operation. The host need only specify the lowest address of the sequence of addresses that the host needs to access. The CDCM6208 will automatically increment the internal register address pointer if the SCS pin remains low after the SPI port finishes the initial 32-bit transmission sequence. Each transmission of 16 bits (a data payload width) results in the device automatically incrementing the address pointer (provided the SCS pin remains active low for all sequences).

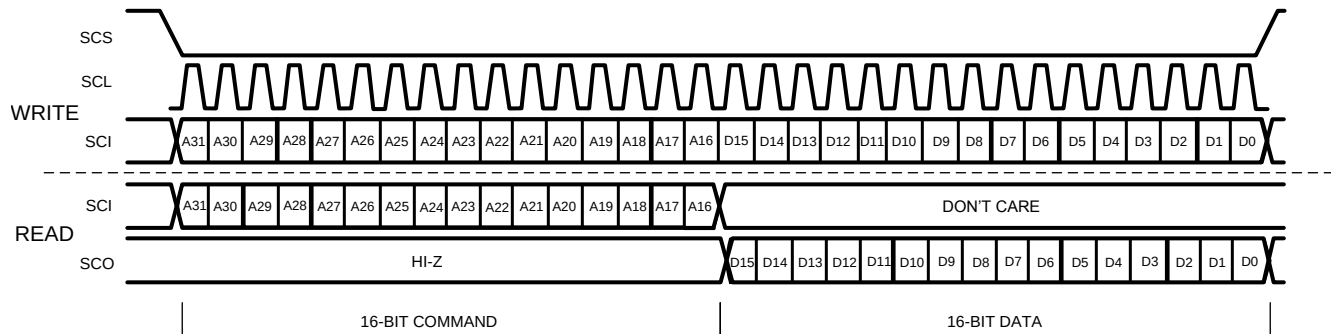


**Figure 42. CDCM6208 SPI Port Message Sequencing**

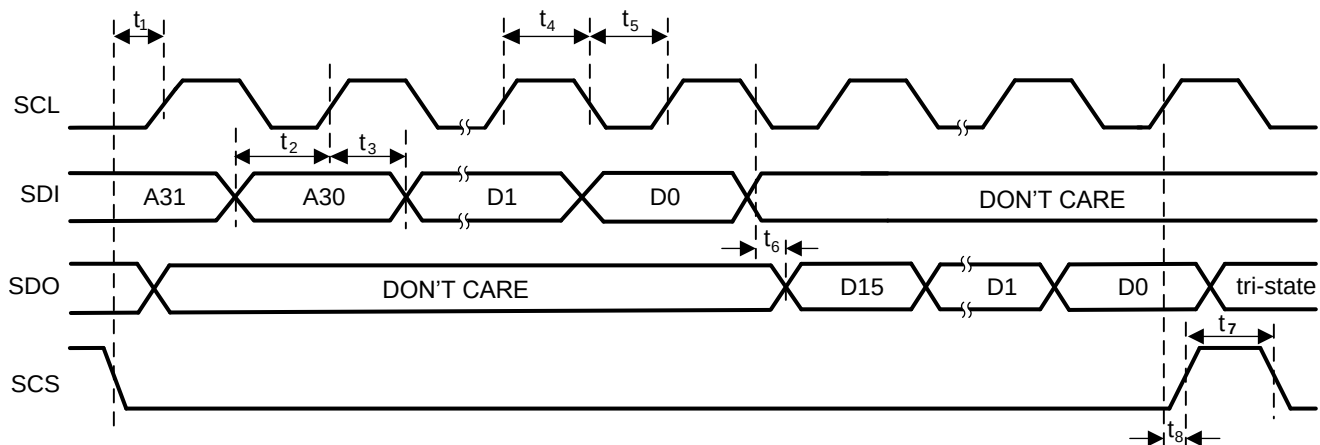


**Figure 43. CDCM6208 SPI Port Timing**

**Table 14. SPI Timing**

| PARAMETER                                               | MIN | TYP | MAX | UNIT |
|---------------------------------------------------------|-----|-----|-----|------|
| $f_{\text{Clock}}$ Clock Frequency for the SCL          |     |     | 20  | MHz  |
| $t_1$ SPI_LE to SCL setup time                          | 10  |     |     | ns   |
| $t_2$ SDI to SCL setup time                             | 10  |     |     | ns   |
| $t_3$ SDO to SCL hold time                              | 10  |     |     | ns   |
| $t_4$ SCL high duration                                 | 25  |     |     | ns   |
| $t_5$ SCL low duration                                  | 25  |     |     | ns   |
| $t_6$ SCL to SCS Setup time                             | 10  |     |     | ns   |
| $t_7$ SCS Pulse Width                                   | 20  |     |     | ns   |
| $t_8$ SDI to SCL Data Valid (First Valid Bit after SCS) | 10  |     |     | ns   |

#### 8.4.5.2.4 I<sup>2</sup>C Serial Interface

With SI\_MODE1=0 and SI\_MODE0=1 the CDCM6208 enters I<sup>2</sup>C mode. The I<sup>2</sup>C port on the CDCM6208 works as a slave device and supports both the 100 kHz standard mode and 400 kHz fast mode operations. Fast mode imposes a glitch tolerance requirement on the control signals. Therefore, the input receivers ignore pulses of less than 50 ns duration. The inputs of the device also incorporates a Schmitt trigger at the SDA and SCL inputs to provide receiver input hysteresis for increased noise robustness.

#### NOTE

Communication through I<sup>2</sup>C is not possible while RESETN is held low.

In an I<sup>2</sup>C bus system, the CDCM6208 acts as a slave device and is connected to the serial bus (data bus SDA and clock bus SCL). The SDA port is bidirectional and uses an open drain driver to permit multiple devices to be connected to the same serial bus. The CDCM6208 allows up to four unique CDCM6208 slave devices to occupy the I<sup>2</sup>C bus in addition to any other I<sup>2</sup>C slave device with a different I<sup>2</sup>C address. These slave devices are accessed via a 7-bit slave address transmitted as part of an I<sup>2</sup>C packet. Only the device with a matching slave address responds to subsequent I<sup>2</sup>C commands. The device slave address is 10101xx (the two LSBs are determined by the AD1 and AD0 pins). The five MSBs are hard-wired, while the two LSBs are set through pins on device power up.

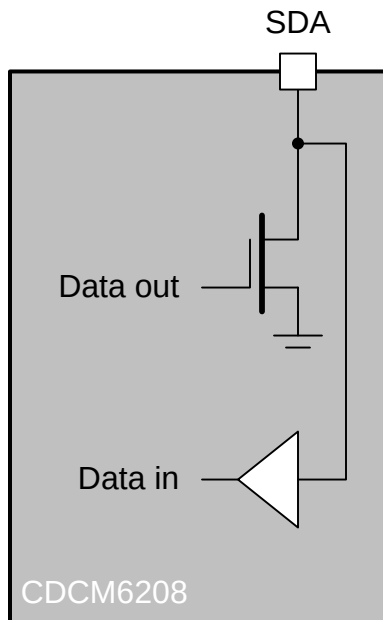


**Figure 44. I<sup>2</sup>C Serial Interface**

During the data transfer through the I<sup>2</sup>C port interface, one clock pulse is generated for each data bit transferred. The data on the SDA line must be stable during the high period of the clock. The high or low state of the data line can change only when the clock signal on the SCL line is low. The start data transfer condition is characterized by a high-to-low transition on the SDA line while SCL is high. The stop data transfer condition is characterized by a low-to-high transition on the SDA line while SCL is high. The start and stop conditions are always initiated by the master. Every byte on the SDA line must be eight bits long. Each byte must be followed by an acknowledge bit and bytes are sent MSB first.

The acknowledge bit (A) or non-acknowledge bit (A) is the 9<sup>th</sup> bit attached to any 8-bit data byte and is always generated by the receiver to inform the transmitter that the byte has been received (when A = 0) or not (when A = 1). A = 0 is done by pulling the SDA line low during the 9<sup>th</sup> clock pulse and A = 1 is done by leaving the SDA line high during the 9<sup>th</sup> clock pulse.

The I<sup>2</sup>C master initiates the data transfer by asserting a start condition which initiates a response from all slave devices connected to the serial bus. Based on the 8-bit address byte sent by the master over the SDA line (consisting of the 7-bit slave address (MSB first) and an R/W bit), the device whose address corresponds to the transmitted address responds by sending an acknowledge bit. All other devices on the bus remain idle while the selected device waits for data transfer with the master. The CDCM6208 slave address bytes are given in below table.

After the data transfer has occurred, stop conditions are established. In write mode, the master asserts a stop condition to end data transfer during the 10<sup>th</sup> clock pulse following the acknowledge bit for the last data byte from the slave. In read mode, the master receives the last data byte from the slave but does not pull SDA low during the 9<sup>th</sup> clock pulse. This is known as a non-acknowledge bit. By receiving the non-acknowledge bit, the slave knows the data transfer is finished and enters the idle mode. The master then takes the data line low during the low period before the 10<sup>th</sup> clock pulse, and high during the 10<sup>th</sup> clock pulse to assert a stop condition.

For "Register Write/Read" operations, the I<sup>2</sup>C master can individually access addressed registers, that are made of two 8-bit data bytes.

**Table 15. I<sup>2</sup>C Slave Address Byte**

| A6 | A5 | A4 | A3 | A2 | AD1 | AD0 | R/W |
|----|----|----|----|----|-----|-----|-----|
| 1  | 0  | 1  | 0  | 1  | 0   | 0   | 1/0 |
| 1  | 0  | 1  | 0  | 1  | 0   | 1   | 1/0 |
| 1  | 0  | 1  | 0  | 1  | 1   | 0   | 1/0 |
| 1  | 0  | 1  | 0  | 1  | 1   | 1   | 1/0 |

## 8.5 Programming

**Table 16. Generic Programming Sequence**

|     |                                                   |
|-----|---------------------------------------------------|
| S   | Start Condition                                   |
| Sr  | Repeated Condition                                |
| R/W | 1 = Read (Rd) from slave; 0 = Write (Wr) to slave |
| A   | Acknowledge (ACK = 0 and NACK = 1)                |
| P   | Stop Condition                                    |
|     | Master to Slave Transmission                      |
|     | Slave to Master Transmission                      |

**Figure 45. Register Write Programming Sequence**

|   |               |    |   |                  |   |                  |   |           |   |           |   |   |
|---|---------------|----|---|------------------|---|------------------|---|-----------|---|-----------|---|---|
| 1 | 7             | 1  | 1 | 8                | 1 | 8                | 1 | 8         | 1 | 8         | 1 | 1 |
| S | SLAVE Address | Wr | A | Register Address | A | Register Address | A | Data Byte | A | Data Byte | A | P |

**Figure 46. Register Read Programming Sequence**

|   |               |    |   |                  |   |                  |   |   |               |    |   |           |   |           |   |   |
|---|---------------|----|---|------------------|---|------------------|---|---|---------------|----|---|-----------|---|-----------|---|---|
| 1 | 7             | 1  | 1 | 8                | 1 | 8                | 1 | 1 | 1             | 1  | 1 | 8         | 1 | 8         | 1 | 1 |
| S | SLAVE Address | Wr | A | Register Address | A | Register Address | A | S | Slave Address | Rd | A | Data Byte | A | Data Byte | A | P |

## 8.6 Register Maps

In SPI/I<sup>2</sup>C mode the device can be configured through twenty registers. Register 4 configures the input, Reg 0-3 the PLL and dividers, and Register 5 - 20 configures the 8 different outputs.

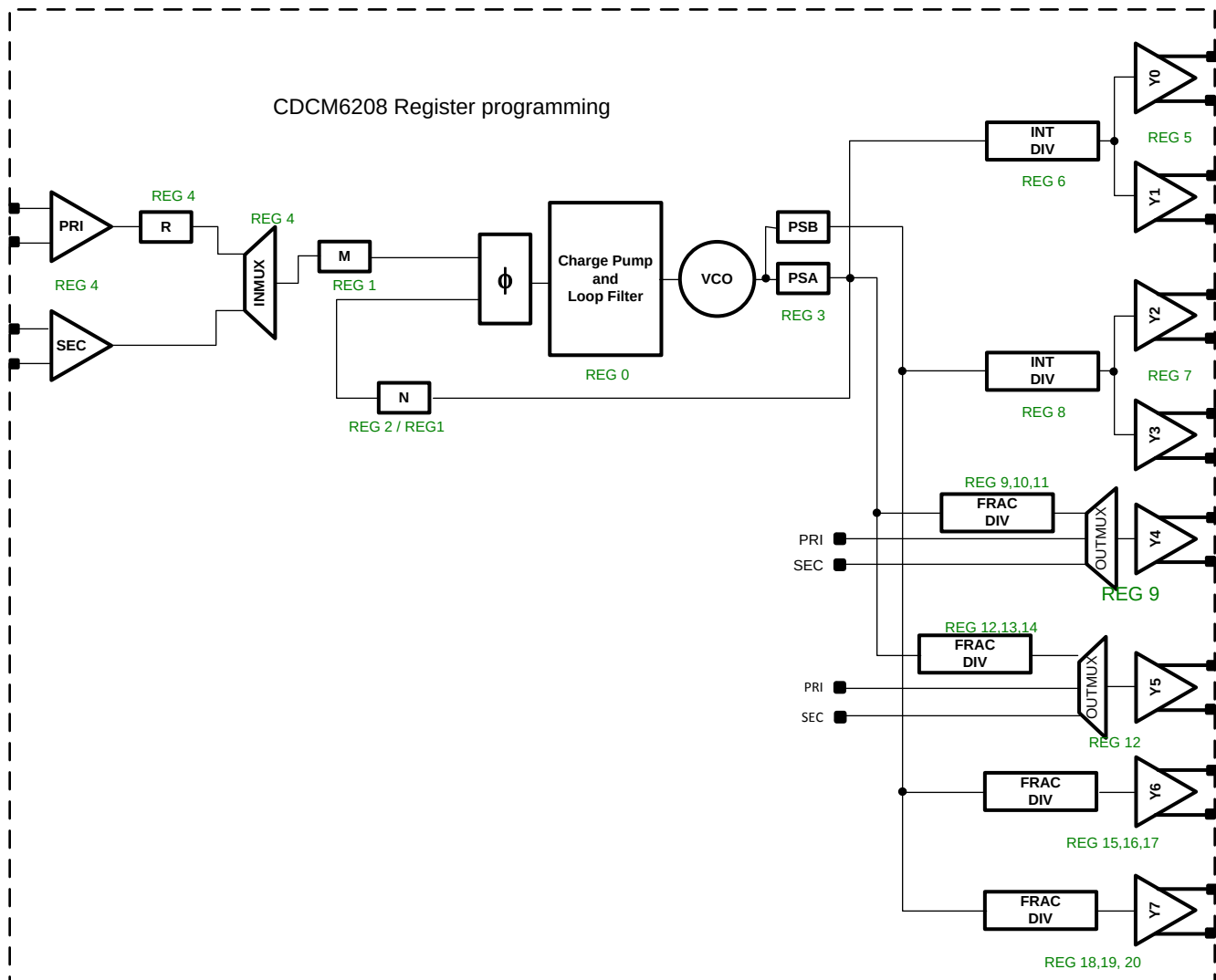


**Figure 47. Device Register Map**

## Register Maps (continued)

**Table 17. Register 0**

| BIT   | BIT NAME     | RELATED BLOCK                 | DESCRIPTION/FUNCTION                                                                                                                                                                       |
|-------|--------------|-------------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:10 | RESERVED     |                               | These bits must be set to 0                                                                                                                                                                |
| 9:7   | LF_C3[2:0]   | PLL Internal Loop Filter (C3) | PLL Internal Loop Filter Capacitor (C3) Selection<br>000 → 35 pF<br>001 → 112.5 pF<br>010 → 177.5 pF<br>011 → 242.5 pF<br>100 → 310 pF<br>101 → 377.5 pF<br>110 → 445 pF<br>111 → 562.5 pF |
| 6:4   | LF_R3[2:0]   | PLL Internal Loop Filter (R3) | PLL Internal Loop Filter Resistor (R3) Selection<br>000 → 10 Ω<br>001 → 30 Ω<br>010 → 60 Ω<br>011 → 100 Ω<br>100 → 530 Ω<br>101 → 1050 Ω<br>110 → 2080 Ω<br>111 → 4010 Ω                   |
| 3:1   | PLL_ICP[2:0] | PLL Charge Pump               | PLL Charge Pump Current Setting<br>000 → 500 μA<br>001 → 1.0 mA<br>010 → 1.5 mA<br>011 → 2.0 mA<br>100 → 2.5 mA<br>101 → 3.0 mA<br>110 → 3.5 mA<br>111 → 4.0 mA                            |
| 0     | RESERVED     |                               | This bit is tied to one statically, and it is recommended to set to 1 when writing to register.                                                                                            |

**Table 18. Register 1**

| BIT  | BIT NAME         | RELATED BLOCK          | DESCRIPTION/FUNCTION                                                         |
|------|------------------|------------------------|------------------------------------------------------------------------------|
| 15:2 | PLL_REFDIV[13:0] | PLL Reference Divider  | PLL Reference 14-b Divider Selection<br>(Divider value is register value +1) |
| 1:0  | PLL_FBDIV1[9:8]  | PLL Feedback Divider 1 | PLL Feedback 10-b Divider Selection, Bits 9:8                                |

**Table 19. Register 2**

| BIT  | BIT NAME        | RELATED BLOCK          | DESCRIPTION/FUNCTION                                                                  |
|------|-----------------|------------------------|---------------------------------------------------------------------------------------|
| 15:8 | PLL_FBDIV1[7:0] | PLL Feedback Divider 1 | PLL Feedback 10-b Divider Selection, Bits 7:0<br>(Divider value is register value +1) |
| 7:0  | PLL_FBDIV0[7:0] | PLL Feedback Divider 0 | PLL Feedback 8-b Divider Selection<br>(Divider value is register value +1)            |

**Table 20. Register 3**

| BIT   | BIT NAME       | RELATED BLOCK           | DESCRIPTION/FUNCTION                                                                                                                                                |
|-------|----------------|-------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:13 | RESERVED       |                         | These bits must be set to 0                                                                                                                                         |
| 12    | ST1_SEL_REFCLK | Device Status           | Reference clock status enable on Status 1 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                     |
| 11    | ST1_LOR_EN     |                         | Loss-of-reference Enable on Status 1 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                          |
| 10    | ST1_PLLLOCK_EN |                         | PLL Lock Indication Enable on Status 1 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                        |
| 9     | ST0_SEL_REFCLK |                         | Reference clock status enable on Status 0 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                     |
| 8     | ST0_LOR_EN     |                         | Loss-of-reference Enable on Status 0 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                          |
| 7     | ST0_PLLLOCK_EN |                         | PLL Lock Indication Enable on Status 0 pin:<br>0 → Disable<br>1 → Enable (See <a href="#">Table 12</a> for full description)                                        |
| 6     | RSTN           | Device Reset            | Device Reset Selection:<br>0 → Device In Reset (retains register values)<br>1 → Normal Operation                                                                    |
| 5     | SYNCN          | Output Divider          | Output Channel Dividers Synchronization Enable:<br>0 → Forces synchronization<br>1 → Exits synchronization                                                          |
| 4     | ENCAL          | PLL/VCO                 | PLL/VCO Calibration Enable:<br>0 → Disable<br>1 → Enable                                                                                                            |
| 3:2   | PS_B[1:0]      | PLL Prescaler Divider B | PLL Prescaler 1 Integer Divider Selection:<br>00 → Divide-by-4<br>01 → Divide-by-5<br>10 → Divide-by-6<br>11 → RESERVED<br>used for Y2, Y3, Y6, and Y7              |
| 1:0   | PS_A[1:0]      | PLL Prescaler Divider A | PLL Prescaler 0 Integer Divider Selection:<br>00 → Divide-by-4<br>01 → Divide-by-5<br>10 → Divide-by-6<br>11 → RESERVED<br>used in PLL feedback, Y0, Y1, Y4, and Y5 |

**Table 21. Register 4**

| BIT   | BIT NAME                  | RELATED BLOCK             | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                                                                                      |
|-------|---------------------------|---------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15:14 | SMUX_PW[1:0]              | Reference Input Smart MUX | Smart MUX Pulse Width Selection. This bit controls the Smart MUX delay and waveform reshaping.<br>00 → PLL Smart MUX Clock Delay and Reshape Disabled (default in all pin modes)<br>01 → PLL Smart MUX Clock Delay Enable<br>10 → PLL Smart MUX Clock Reshape Enable<br>11 → PLL Smart MUX Clock Delay and Reshape Enable |
| 13    | SMUX_MODE_SEL             |                           | Smart MUX Mode Selection:<br>0 → Auto select<br>1 → Manual select<br>Note: in Auto select mode, both input buffers must be enabled. Set R4.5 = 1 and R4.2 = 1                                                                                                                                                             |
| 12    | SMUX_REF_SEL              |                           | Smart MUX Selection for PLL Reference:<br>0 → Primary<br>1 → Secondary (only if REF_SEL pin is high)<br>This bit is ignored when smartmux is set to auto select (for example, R4.13 = 0). See Table 12 for details.                                                                                                       |
| 11:8  | CLK_PRI_DIV[3:0]          | Primary Input Divider     | Primary Input (R) Divider Selection:<br>0000 → Divide by 1<br>1111 → Divide by 16                                                                                                                                                                                                                                         |
| 7:6   | SEC_SELBUF[1:0]           | Secondary Input           | Secondary Input Buffer Type Selection:<br>00 → CML<br>01 → LVDS<br>10 → LVCMOS<br>11 → Crystal                                                                                                                                                                                                                            |
| 5     | EN_SEC_CLK                |                           | Secondary input enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                                                                                                      |
| 4:3   | PRI_SELBUF[1:0]           | Primary Input             | Primary Input Buffer Type Selection:<br>00 → CML<br>01 → LVDS<br>10 → LVCMOS<br>11 → LVCMOS                                                                                                                                                                                                                               |
| 2     | EN_PRI_CLK                |                           | Primary input enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                                                                                                        |
| 1     | SEC_SUPPLY <sup>(1)</sup> | Secondary Input           | Supply voltage for secondary input:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                                                                                                                                                                                                                                                         |
| 0     | PRI_SUPPLY <sup>(2)</sup> | Primary Input             | Supply voltage for primary input:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                                                                                                                                                                                                                                                           |

- (1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0. To ensure best device performance this registers should be updated after power-up to reflect the true VDD\_SEC supply voltage used.
- (2) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0. To ensure best device performance this registers should be updated after power-up to reflect the true VDD\_PRI supply voltage used.

**Table 22. Register 5**

| BIT | BIT NAME                    | RELATED BLOCK           | DESCRIPTION/FUNCTION                                                                                  |
|-----|-----------------------------|-------------------------|-------------------------------------------------------------------------------------------------------|
| 15  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 14  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 13  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 12  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 11  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 10  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 9   | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 8:7 | SEL_DRV_R_CH1[1:0]          | Output Channel 1        | Output Channel 1 Type Selection:<br>00, 01 → LVDS<br>10 → CML<br>11 → PECL                            |
| 6:5 | EN_CH1[1:0]                 |                         | Output channel 1 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1 |
| 4:3 | SEL_DRV_R_CH0[1:0]          | Output Channel 0        | Output Channel 0 Type Selection:<br>00, 01 → LVDS<br>10 → CML<br>11 → PECL                            |
| 2:1 | EN_CH0[1:0]                 |                         | Output channel 0 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1 |
| 0   | SUPPLY_CH0_1 <sup>(1)</sup> | Output Channels 0 and 1 | Output Channels 0 and 1 Supply Voltage Selection:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                       |

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 23. Register 6**

| BIT | BIT NAME       | RELATED BLOCK           | DESCRIPTION/FUNCTION                                                                            |
|-----|----------------|-------------------------|-------------------------------------------------------------------------------------------------|
| 15  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 14  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 13  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 12  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 11  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 10  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 9   | RESERVED       |                         | This bit must be set to 0                                                                       |
| 8   | RESERVED       |                         | This bit must be set to 0                                                                       |
| 7:0 | OUTDIV0_1[7:0] | Output Channels 0 and 1 | Output channels 0 and 1 8-b output integer divider setting (Divider value is register value +1) |

**Table 24. Register 7**

| BIT | BIT NAME                    | RELATED BLOCK           | DESCRIPTION/FUNCTION                                                                                  |
|-----|-----------------------------|-------------------------|-------------------------------------------------------------------------------------------------------|
| 15  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 14  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 13  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 12  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 11  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 10  | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 9   | RESERVED                    |                         | This bit must be set to 0                                                                             |
| 8:7 | SEL_DRV_R_CH3[1:0]          | Output Channel 3        | Output Channel 3 Type Selection:<br>00, 01 → LVDS<br>10 → CML<br>11 → PECL                            |
| 6:5 | EN_CH3[1:0]                 |                         | Output channel 3 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1 |
| 4:3 | SEL_DRV_R_CH2[1:0]          | Output Channel 2        | Output Channel 2 Type Selection:<br>00, 01 → LVDS<br>10 → CML<br>11 → PECL                            |
| 2:1 | EN_CH2[1:0]                 |                         | Output channel 2 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1 |
| 0   | SUPPLY_CH2_3 <sup>(1)</sup> | Output Channels 2 and 3 | Output Channels 2 and 3 Supply Voltage Selection:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                       |

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 25. Register 8**

| BIT | BIT NAME       | RELATED BLOCK           | DESCRIPTION/FUNCTION                                                                            |
|-----|----------------|-------------------------|-------------------------------------------------------------------------------------------------|
| 15  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 14  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 13  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 12  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 11  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 10  | RESERVED       |                         | This bit must be set to 0                                                                       |
| 9   | RESERVED       |                         | This bit must be set to 0                                                                       |
| 8   | RESERVED       |                         | This bit must be set to 0                                                                       |
| 7:0 | OUTDIV2_3[7:0] | Output Channels 2 and 3 | Output channels 2 and 3 8-b output integer divider setting (Divider value is register value +1) |

**Table 26. Register 9**

| BIT   | BIT NAME                  | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                       |
|-------|---------------------------|------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                  |
| 14:13 | OUTMUX_CH4[1:0]           | Output Channel 4 | Output MUX setting for output channel 4:<br>00 and 11 → PLL<br>01 → Primary input<br>10 → Secondary input                                                                                                                                                  |
| 12:10 | PRE_DIV_CH4[2:0]          |                  | Output channel 4 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q9.9 = 0)<br>000 → Divide by 2<br>001 → Divide by 3<br>111 → Divide by 1 (only for CDCM6208 with $f_{VCO} \leq 2.4$ GHz)<br>All other combinations reserved |
| 9     | EN_FRACDIV_CH4            |                  | Output channel 4 fractional divider enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                   |
| 8     | LVC MOS_SLEW_CH4          |                  | Output channel 4 LVCMOS output slew:<br>0 → Normal<br>1 → Slow                                                                                                                                                                                             |
| 7     | EN_LVCMOS_N_CH4           |                  | Output channel 4 negative-side LVCMOS enable:<br>0 → Disable<br>1 → Enable (Negative side can only be enabled if positive side is enabled)                                                                                                                 |
| 6     | EN_LVCMOS_P_CH4           |                  | Output channel 4 positive-side LVCMOS enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                 |
| 5     | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                  |
| 4:3   | SEL_DRV R_CH4[2:0]        |                  | Output channel 4 type selection:<br>00 or 01 → LVDS<br>10 → LVCMOS<br>11 → HCSL                                                                                                                                                                            |
| 2:1   | EN_CH4[1:0]               |                  | Output channel 4 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1                                                                                                                                                      |
| 0     | SUPPLY_CH4 <sup>(1)</sup> |                  | Output channel 4 Supply Voltage Selection:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                                                                                                                                                                                   |

(1) It is ok to power up the device with a 2.5 V / 3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 27. Register 10**

| BIT  | BIT NAME        | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                              |
|------|-----------------|------------------|-----------------------------------------------------------------------------------|
| 15   | RESERVED        |                  | This bit must be set to 0                                                         |
| 14   | RESERVED        |                  | This bit must be set to 0                                                         |
| 13   | RESERVED        |                  | This bit must be set to 0                                                         |
| 12   | RESERVED        |                  | This bit must be set to 0                                                         |
| 11:4 | OUTDIV4[7:0]    | Output Channel 4 | Output channel 4 8-b integer divider setting (Divider value is register value +1) |
| 3:0  | FRACDIV4[19:16] |                  | Output channel 4 20-b fractional divider setting, bits 19 - 16                    |

**Table 28. Register 11**

| BIT  | BIT NAME       | RELATED BLOCK    | DESCRIPTION/FUNCTION                                          |
|------|----------------|------------------|---------------------------------------------------------------|
| 15:0 | FRACDIV4[15:0] | Output Channel 4 | Output channel 4 20-b fractional divider setting, bits 15 - 0 |

**Table 29. Register 12**

| BIT   | BIT NAME                  | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                                |
|-------|---------------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                           |
| 14:13 | OUTMUX_CH5[1:0]           | Output Channel 5 | Output MUX setting for output channel 5:<br>00 and 11 → PLL<br>01 → Primary input<br>10 → Secondary input                                                                                                                                                           |
| 12:10 | PRE_DIV_CH5[2:0]          |                  | Output channel 5 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q12.9 = 0)<br>000 → Divide by 2<br>001 → Divide by 3<br>111 → Divide by 1; (only for CDCM6208 with $f_{VCO} \leq 2.4\text{GHz}$ )<br>All other combinations reserved |
| 9     | EN_FRACDIV_CH5            |                  | Output channel 5 fractional divider enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                            |
| 8     | LVC MOS_SLEW_CH5          |                  | Output channel 5 LVC MOS output slew:<br>0 → Normal<br>1 → Slow                                                                                                                                                                                                     |
| 7     | EN_LVC MOS_N_CH5          |                  | Output channel 5 negative-side LVC MOS enable:<br>0 → Disable<br>1 → Enable (Negative side can only be enabled if positive side is enabled)                                                                                                                         |
| 6     | EN_LVC MOS_P_CH5          |                  | Output channel 5 positive-side LVC MOS enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                         |
| 5     | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                           |
| 4:3   | SEL_DRVR_CH5[2:0]         |                  | Output channel 5 type selection:<br>00 or 01 → LVDS<br>10 → LVC MOS<br>11 → HCSL                                                                                                                                                                                    |
| 2:1   | EN_CH5[1:0]               |                  | Output channel 5 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1                                                                                                                                                               |
| 0     | SUPPLY_CH5 <sup>(1)</sup> |                  | Output channel 5 Supply Voltage Selection:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                                                                                                                                                                                            |

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 30. Register 13**

| BIT  | BIT NAME        | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                              |
|------|-----------------|------------------|-----------------------------------------------------------------------------------|
| 15   | RESERVED        |                  | This bit must be set to 0                                                         |
| 14   | RESERVED        |                  | This bit must be set to 0                                                         |
| 13   | RESERVED        |                  | This bit must be set to 0                                                         |
| 12   | RESERVED        |                  | This bit must be set to 0                                                         |
| 11:4 | OUTDIV5[7:0]    | Output Channel 5 | Output channel 5 8-b integer divider setting (Divider value is register value +1) |
| 3:0  | FRACDIV5[19:16] |                  | Output channel 5 20-b fractional divider setting, bits 19-16                      |

**Table 31. Register 14**

| BIT  | BIT NAME       | RELATED BLOCK    | DESCRIPTION/FUNCTION                                        |
|------|----------------|------------------|-------------------------------------------------------------|
| 15:0 | FRACDIV5[15:0] | Output Channel 5 | Output channel 5 20-b fractional divider setting, bits 15-0 |

**Table 32. Register 15**

| BIT   | BIT NAME                  | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                                  |
|-------|---------------------------|------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                             |
| 14    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                             |
| 13    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                             |
| 12:10 | PRE_DIV_CH6[2:0]          | Output Channel 6 | Output channel 6 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q15.9 = 0)<br>000 → Divide by 2<br>001 → Divide by 3<br>111 → Divide by 1; (only for CDCM6208V1 with $f_{VCO} \leq 2.4\text{GHz}$ )<br>All other combinations reserved |
| 9     | EN_FRACDIV_CH6            |                  | Output channel 6 fractional divider enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                              |
| 8     | LVC MOS_SLEW_CH6          |                  | Output channel 6 LVCMOS output slew:<br>0 → Normal<br>1 → Slow                                                                                                                                                                                                        |
| 7     | EN_LVCMOS_N_CH6           |                  | Output channel 6 negative-side LVCMOS enable:<br>0 → Disable<br>1 → Enable (Negative side can only be enabled if positive side is enabled)                                                                                                                            |
| 6     | EN_LVCMOS_P_CH6           |                  | Output channel 6 positive-side LVCMOS enable:<br>0 → Disable<br>1 → Enable                                                                                                                                                                                            |
| 5     | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                             |
| 4:3   | SEL_DRVR_CH6[1:0]         |                  | Output channel 6 type selection:<br>00 or 01 → LVDS<br>10 → LVCMOS<br>11 → HCSL                                                                                                                                                                                       |
| 2:1   | EN_CH6[1:0]               |                  | Output channel 6 enable:<br>00 → Disable<br>01 → Enable<br>10 → Drive static 0<br>11 → Drive static 1                                                                                                                                                                 |
| 0     | SUPPLY_CH6 <sup>(1)</sup> |                  | Output channel 6 Supply Voltage Selection:<br>0 → 1.8 V<br>1 → 2.5/3.3 V                                                                                                                                                                                              |

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 33. Register 16**

| BIT  | BIT NAME        | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                              |
|------|-----------------|------------------|-----------------------------------------------------------------------------------|
| 15   | RESERVED        |                  | This bit must be set to 0                                                         |
| 14   | RESERVED        |                  | This bit must be set to 0                                                         |
| 13   | RESERVED        |                  | This bit must be set to 0                                                         |
| 12   | RESERVED        |                  | This bit must be set to 0                                                         |
| 11:4 | OUTDIV6[7:0]    | Output Channel 6 | Output channel 6 8-b integer divider setting (Divider value is register value +1) |
| 3:0  | FRACDIV6[19:16] |                  | Output channel 6 20-b fractional divider setting, bits 19-16                      |

**Table 34. Register 17**

| BIT  | BIT NAME       | RELATED BLOCK    | DESCRIPTION/FUNCTION                                        |
|------|----------------|------------------|-------------------------------------------------------------|
| 15:0 | FRACDIV6[15:0] | Output Channel 6 | Output channel 6 20-b fractional divider setting, bits 15-0 |

**Table 35. Register 18**

| BIT   | BIT NAME                  | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                         |
|-------|---------------------------|------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                    |
| 14    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                    |
| 13    | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                    |
| 12:10 | PRE_DIV_CH7[2:0]          | Output Channel 7 | Output channel 7 fractional divider's 3-b pre-divider setting (this pre-divider is bypassed if Q18.9 = 0)<br>000 → Divide by 2<br>001 → Divide by 3<br>111 → Divide by 1; (only for CDCM6208 with $f_{VCO} \leq 2.4$ GHz)<br>All other combinations reserved |
| 9     | EN_FRACDIV_CH7            |                  | Output channel 7 fractional divider enable: 0 → Disable, 1 → Enable                                                                                                                                                                                          |
| 8     | LVC MOS_SLEW_CH7          |                  | Output channel 7 LVC MOS output slew: 0 → Normal, 1 → Slow                                                                                                                                                                                                   |
| 7     | EN_LVC MOS_N_CH7          |                  | Output channel 7 negative-side LVC MOS enable: 0 → Disable, 1 → Enable (Negative side can only be enabled if positive side is enabled)                                                                                                                       |
| 6     | EN_LVC MOS_P_CH7          |                  | Output channel 7 positive-side LVC MOS enable: 0 → Disable, 1 → Enable                                                                                                                                                                                       |
| 5     | RESERVED                  |                  | This bit must be set to 0                                                                                                                                                                                                                                    |
| 4:3   | SEL_DRVR_CH7[2:0]         |                  | Output channel 7 type selection: 00 or 01 → LVDS, 10 → LVC MOS, 11 → HC SL                                                                                                                                                                                   |
| 2:1   | EN_CH7[1:0]               |                  | Output channel 7 enable: 00 → Disable, 01 → Enable, 10 → Drive static low, 11 → Drive static high                                                                                                                                                            |
| 0     | SUPPLY_CH7 <sup>(1)</sup> |                  | Output channel 7 Supply Voltage Selection: 0 → 1.8 V, 1 → 2.5/3.3 V                                                                                                                                                                                          |

(1) It is ok to power up the device with a 2.5 V/3.3 V supply while this bit is set to 0 and to update this bit thereafter.

**Table 36. Register 19**

| BIT  | BIT NAME        | RELATED BLOCK    | DESCRIPTION/FUNCTION                                                              |
|------|-----------------|------------------|-----------------------------------------------------------------------------------|
| 15   | RESERVED        |                  | This bit must be set to 0                                                         |
| 14   | RESERVED        |                  | This bit must be set to 0                                                         |
| 13   | RESERVED        |                  | This bit must be set to 0                                                         |
| 12   | RESERVED        |                  | This bit must be set to 0                                                         |
| 11:4 | OUTDIV7[7:0]    | Output Channel 7 | Output channel 7 8-b integer divider setting (Divider value is register value +1) |
| 3:0  | FRACDIV7[19:16] |                  | Output channel 7 20-b fractional divider setting, bits 19-16                      |

**Table 37. Register 20**

| BIT  | BIT NAME       | RELATED BLOCK    | DESCRIPTION/FUNCTION                                        |
|------|----------------|------------------|-------------------------------------------------------------|
| 15:0 | FRACDIV7[15:0] | Output Channel 7 | Output channel 7 20-b fractional divider setting, bits 15-0 |

**Table 38. Register 21 (Read Only)**

| BIT | BIT NAME   | RELATED BLOCK            | DESCRIPTION/FUNCTION                                                                                                                                                                                                                                                      |
|-----|------------|--------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 14  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 13  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 12  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 11  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 10  | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 9   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 8   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 7   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 6   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 5   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 4   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 3   | RESERVED   |                          | This bit will read a 0                                                                                                                                                                                                                                                    |
| 2   | PLL_UNLOCK | Device Status Monitoring | Indicates unlock status for PLL (digital):<br>0 → PLL locked<br>1 → PLL unlocked<br>Note: the external output signal on Status 0 or Status 1 uses a reversed logic, and indicates "lock" with a V <sub>OH</sub> signal and unlock with a V <sub>OL</sub> signaling level. |
| 1   | LOS_REF    |                          | Loss of reference input observed at input Smart MUX output in observation window for PLL:<br>0 → Reference input present<br>1 → Loss of reference input                                                                                                                   |
| 0   | SEL_REF    |                          | Indicates Reference Selected for PLL:<br>0 → Primary<br>1 → Secondary                                                                                                                                                                                                     |

**Table 39. Register 40 (Read Only)**

| BIT | BIT NAME     | RELATED BLOCK      | DESCRIPTION/FUNCTION                                                                                             |
|-----|--------------|--------------------|------------------------------------------------------------------------------------------------------------------|
| 15  | RESERVED     |                    | Ignore                                                                                                           |
| 14  | RESERVED     |                    | Ignore                                                                                                           |
| 13  | RESERVED     |                    | Ignore                                                                                                           |
| 12  | RESERVED     |                    | Ignore                                                                                                           |
| 11  | RESERVED     |                    | Ignore                                                                                                           |
| 10  | RESERVED     |                    | Ignore                                                                                                           |
| 9   | RESERVED     |                    | Ignore                                                                                                           |
| 8   | RESERVED     |                    | Ignore                                                                                                           |
| 7   | RESERVED     |                    | Ignore                                                                                                           |
| 6   | RESERVED     |                    | Ignore                                                                                                           |
| 5:3 | VCO_VERSION  | Device Information | Indicates the device version (Read only):<br>000 → CDCM6208V1<br>001 → CDCM6208V2                                |
| 2:0 | DIE_REVISION |                    | Indicates the silicon die revision (Read only):<br>00X --> Engineering Prototypes<br>010 --> Production Material |

**Table 40. Default Register Setting for SPI/I2C Modes**

| Register | CDCM6208V1 | CDCM6208V2 |
|----------|------------|------------|
| 0        | 0x01B9     | 0x01B9     |
| 1        | 0x0000     | 0x0000     |
| 2        | 0x0018     | 0x0013     |
| 3        | 0x08F4     | 0x08F5     |
| 4        | 0x30EC     | 0x30EC     |
| 5        | 0x0132     | 0x0022     |
| 6        | 0x0003     | 0x0003     |
| 7        | 0x0022     | 0x0022     |
| 8        | 0x0003     | 0x0004     |
| 9        | 0x0202     | 0x0002     |
| 10       | 0x003B     | 0x0090     |
| 11       | 0x01EC     | 0x0000     |
| 12       | 0x0202     | 0x0002     |
| 13       | 0x003B     | 0x0090     |
| 14       | 0x01EC     | 0x0000     |
| 15       | 0x0002     | 0x0002     |
| 16       | 0x0040     | 0x0090     |
| 17       | 0x0000     | 0x0000     |
| 18       | 0x0002     | 0x0002     |
| 19       | 0x0040     | 0x0130     |
| 20       | 0x0000     | 0x0000     |
| :        | :          | :          |
| 40       | 0XXX01     | 0XXX09     |

## 9 Application and Implementation

### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 9.1 Application Information

The CDCM6208 is a highly integrated clock generator and jitter cleaner. The CDCM6208 derives its output clocks from an on-chip oscillator which can be buffered through integer or fractional output dividers.

### 9.2 Typical Applications

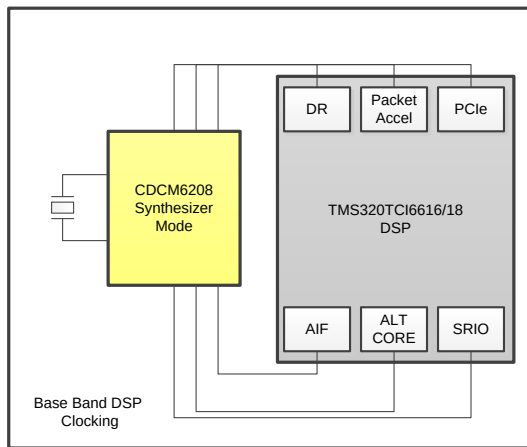


**Figure 48. Typical Application Circuit**

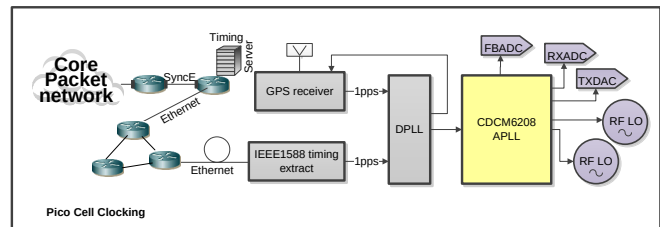


**Figure 49. Typical Application Circuit**

#### 9.2.1 Design Requirements

The most jitter sensitive application besides driving A-to-D converters are systems deploying a serial link using Serializer and De-serializer implementation (for example, a 10 GigEthernet). Fully estimating the clock jitter impact on the link budget requires an understanding of the transmit PLL bandwidth and the receiver CDR bandwidth.

#### 9.2.2 Detailed Design Procedures

##### 9.2.2.1 Jitter Considerations in SERDES Systems

As shown in [Figure 50](#), the bandwidth of TX and RX is the frequency range in which clock jitter adds without any attenuation to the jitter budget of the link. Outside of these frequencies, the SERDES link will attenuate clock jitter with a 20 dB/dec or even steeper roll-off.

## Typical Applications (continued)

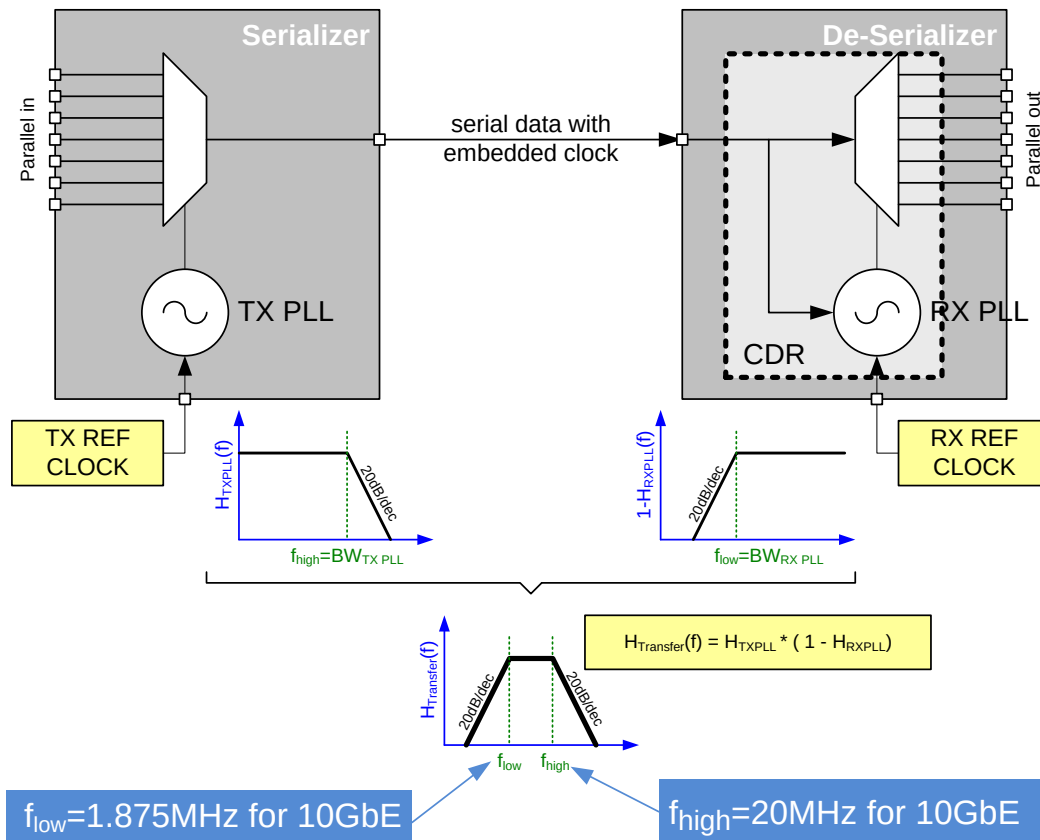


**Figure 50. Serial Link Jitter Budget Explanation**

Example: SERDES link with KeyStone™ I DSP

The SERDES TX PLL of the TI KeyStone™ I DSP family (see [Hardware Design Guide for KeyStone Devices \(SPRAB12\)](#)) for the SRIO interface has a 13-MHz PLL bandwidth (Low Pass Characteristic, see [Figure 50](#)). The CDCM6208V2, pin-mode 27, was characterized in this example over Process, Voltage and Temperature (PVT) with a low-pass filter of 13 MHz to simulate the TX PLL. The attenuation is higher or equal to 20 dB/dec; therefore, the characterization used 20 dB/dec as worst case.

## Typical Applications (continued)

Table 41 shows the maximum total jitter over PVT with and without a low-pass filter.

**Table 41. Maximum Total Jitter<sup>(1)</sup> Over PVT With and Without Low-Pass Filter**

| OUTPUT | FREQUENCY [MHz]             | MAX T <sub>J</sub> [ps]<br>DSP SPEC | MAX T <sub>J</sub> [ps]<br>WITHOUT LOW-PASS FILTER | MAX T <sub>J</sub> [ps]<br>WITH 13-MHz LOW-PASS<br>FILTER |
|--------|-----------------------------|-------------------------------------|----------------------------------------------------|-----------------------------------------------------------|
| Y0     | 122.88                      | 56                                  | 9.43                                               | 8.19                                                      |
| Y2     | 30.72                       | 56                                  | 9.60                                               | 7.36                                                      |
| Y3     | 30.72                       | 56                                  | 9.47                                               | 7.42                                                      |
| Y4     | 156.25<br>(6 bit fraction)  | 56                                  | 57.66                                              | 17.48                                                     |
| Y5     | 156.25<br>(20 bit fraction) | 56                                  | 76.87                                              | 32.32                                                     |
| Y6     | 100.00                      | 56                                  | 86.30                                              | 33.86                                                     |
| Y7     | 66.667                      | 300                                 | 81.71                                              | 35.77                                                     |

(1) Input signal: 250-fs RMS (Integration Range 12 kHz to 5 MHz)

Figure 51 shows the maximum Total Jitter with and without low-pass filter characteristic and the maximum TI KeyStone™ I specification.

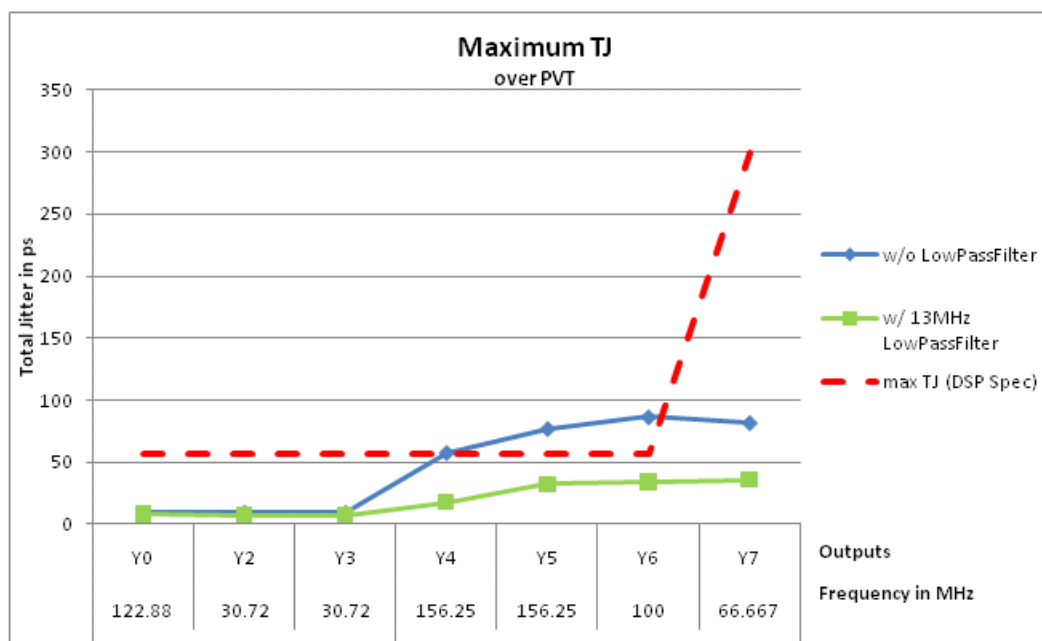


**Figure 51. Maximum Jitter Over PVT**

### NOTE

Due to the damping characteristic of the DSP SERDES PLLs, the actual T<sub>J</sub> data can be worse.

### 9.2.2.2 Jitter Considerations in ADC and DAC Systems

A/D and D/A converters are sensitive to clock jitter in two ways: They are sensitive to phase noise in a particular frequency band, and also have maximum spur level requirements to achieve maximum noise floor sensitivity. The following test results were achieved connecting the CDCM6208 to ADC and DACs:

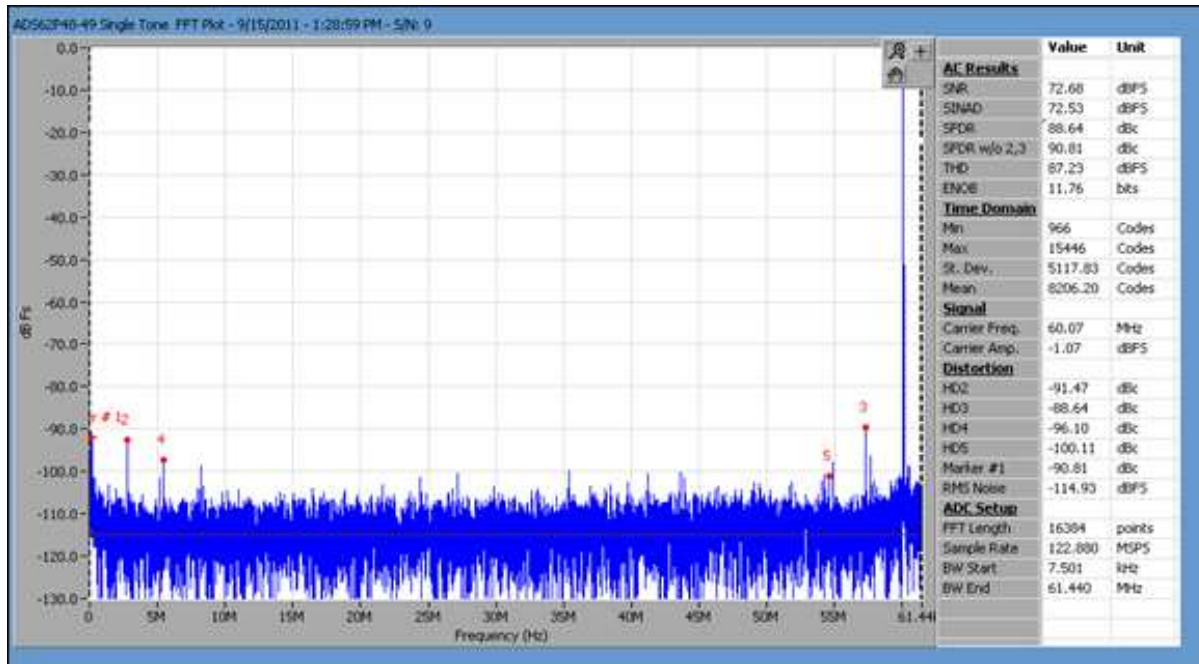


Figure 52. IF = 60 MHz Fclk = 122.88 MHz Baseline (Lab Clk Generator) ADC: ADS62P48-49

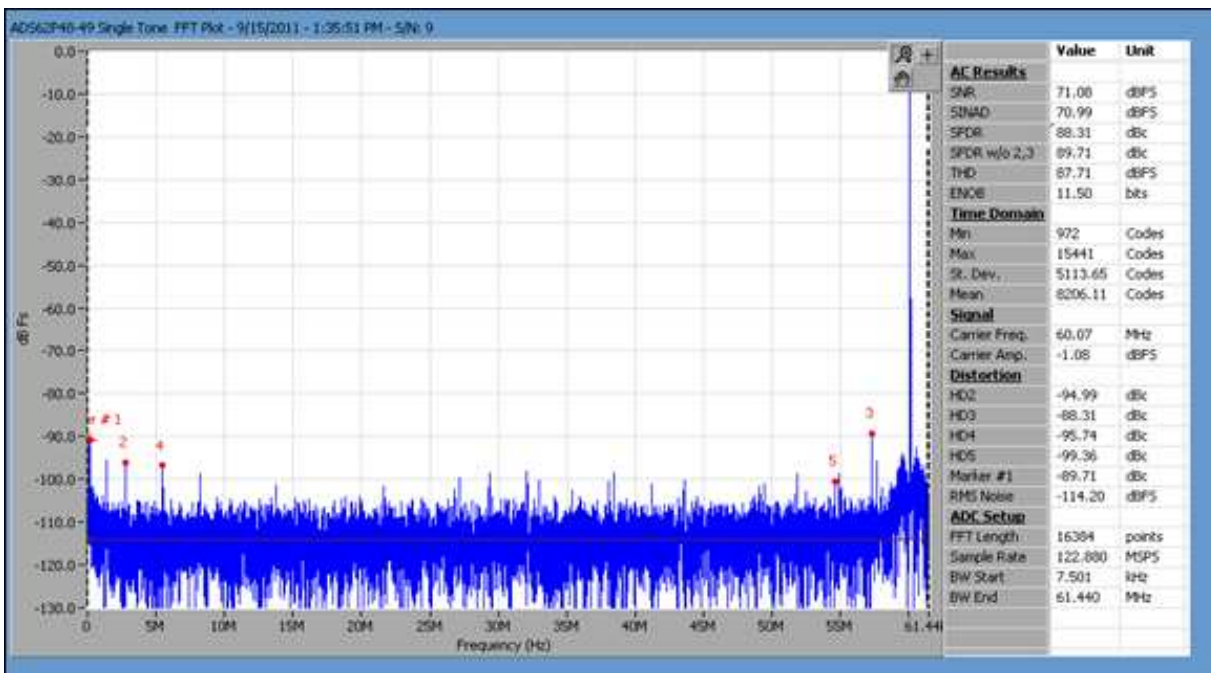


Figure 53. IF = 60 MHz Fclk = 122.88 MHz CDCM6208 Driving ADC

**Observation:** Up to an IF = 100 MHz, the ADC performance when driven by the CDCM6208 (Figure 53) is similar to when the ADC is driven by an expensive lab signal generator with additional passive source filtering (Figure 52).

**Conclusion:** Therefore, the CDCM6208 is usable for applications up to 100 MHz IF. For IF above 100 MHz, the SNR starts degrading in our experiments. Measurements were conducted with ADC connected to Y0 and other outputs running at different integer frequencies.

#### NOTE

For crosstalk, TI highly recommends configuring both pre-dividers identically, otherwise the SFDR and SNR suffer due to crosstalk between the two pre-divider frequencies.

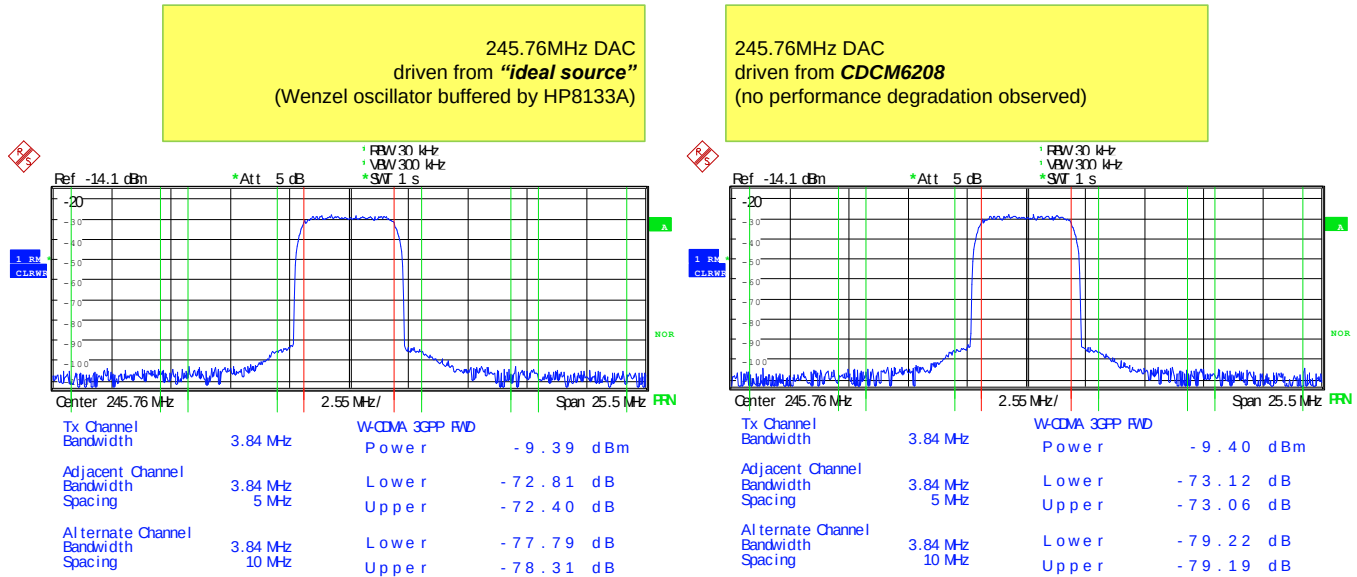


**Figure 54. DAC Driven by Lab Source and CDCM6208 in Comparison (Performance Identical)**

**Observation/Conclusion:** The DAC performance was not degraded at all by the CDCM6208 compared to driving the DAC with a perfect lab source. Therefore, the CDCM6208 provides sufficient low noise to drive a 245.76 MHz DAC.

#### 9.2.2.3 Configuring the PLL

The CDCM6208 allows configuring the PLL to accommodate various input and output frequencies either through an I<sup>2</sup>C or SPI programming interface or in the absence of programming, the PLL can be configured through control pins. The PLL can be configured by setting the Smart Input MUX, Reference Divider, PLL Loop Filter, Feedback Divider, Prescaler Divider, and Output Dividers.

For the PLL to operate in closed-loop mode, the following condition in Equation 1 has to be met when using primary input for the reference clock, and the condition in Equation 2 has to be met when using secondary input for the reference clock.

$$\frac{f_{\text{PRI\_REF}}}{(M \times R)} = \frac{f_{\text{VCO}}}{(N \times \text{PS\_A})} \quad (1)$$

$$\frac{f_{\text{SEC\_REF}}}{M} = \frac{f_{\text{VCO}}}{(N \times \text{PS\_A})} \quad (2)$$

In Equation 1 and Equation 2,  $f_{\text{PRI\_REF}}$  is the reference input frequency on the primary input and  $f_{\text{SEC\_REF}}$  is the reference input frequency on the secondary input,  $R$  is the reference divider,  $M$  is the input divider,  $N$  is the feedback divider, and  $\text{PS\_A}$  the prescaler divider A.

The output frequency,  $f_{OUT}$ , is a function of  $f_{VCO}$ , the prescaler A, and the output divider (O), and is given by Equation 3. (Use PS\_B in for outputs 2, 3, 6, and 7).

$$f_{OUT} = \frac{f_{OSC}}{(O \times PS\_A)} \quad (3)$$

When the output frequency plan calls for the use of some output dividers as fractional values, the following steps are needed to calculate the closest achievable frequencies for those using fractional output dividers and the frequency errors (difference between the desired frequency and the closest achievable frequency).

- Based on system needs, decide the frequencies that need to have best possible jitter performance.
- Once decided, these frequencies need to be placed on integer output dividers.
- Then a frequency plan for these frequencies with strict jitter requirements can be worked out using the common divisor algorithm.
- Once the integer divider plans are worked out, the PLL settings (including VCO frequency, feedback divider, input divider and prescaler divider) can be worked out to map the input frequency to the frequency out of the prescaler divider.
- Then calculate the fractional divider values (whose values must be greater than 2) that are needed to support the output frequencies that are not part of the common frequency plan from the common divisor algorithm already worked out.
- For each fractional divider value, try to represent the fractional portion in a 20-bit binary scheme, where the first fractional bit is represented as 0.5, the second fractional bit is represented as 0.25, third fractional bit is represented as 0.125 and so on. Continue this process until the entire 20-bit fractional binary word is exhausted.
- Once exhausted, the fraction can be calculated as a cumulative sum of the fractional bit x fractional value of the fractional bit. Once this is done, the closest achievable output frequency can be calculated with the mathematical function of the frequency out of the prescaler divider divided by the achievable fractional divider.
- The frequency error can then be calculated as the difference between the desired frequency and the closest achievable frequency.

#### 9.2.2.4 Programmable Loop Filter

The on-chip PLL supports a partially internal and partially external loop filter configuration for all PLL loop bandwidths where the passive external components C1, C2, and R2 are connected to the ELF pin as shown in Figure 55 to achieve PLL loop bandwidths from 400 kHz down to 10 Hz.

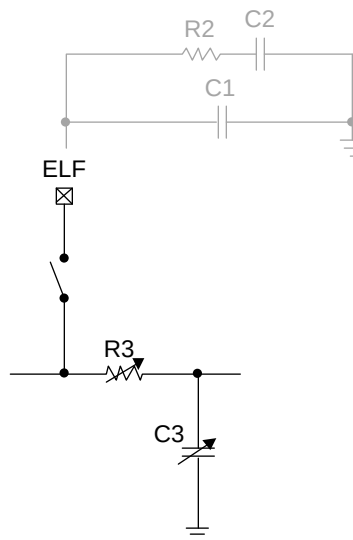


**Figure 55. CDCM6208 PLL Loop Filter Topology**

### 9.2.2.5 Loop filter Component Selection

The loop filter setting and external resistor selection is important to set the PLL to best possible bandwidth and to minimize jitter. A high bandwidth ( $\geq 100$  kHz) provides best input signal tracking and is therefore desired with a clean input reference (synthesizer mode). A low bandwidth ( $\leq 1$  kHz) is desired if the input signal quality is unknown (jitter cleaner mode). TI provides a software tool that makes it easy to select the right loop filter components. C1, R2, and C2 are external loop filter components, connected to the ELF pin. The 3<sup>rd</sup> pole of the loop filter is device internal with R3 and C3 register selectable.

### 9.2.2.6 Device Output Signaling

**LVDS-like:** All outputs Y[7:0] support LVDS-like signaling. The actual output stage uses a CML structure and drives a signal swing identical to LVDS (approximately 350 mV). The output slew rate is faster than standard LVDS for best jitter performance. The LVDS-like outputs should be AC-coupled when interfacing to a LVDS receiver. See reference schematic [Figure 69](#) for an example. The supply voltage for outputs configured LVDS can be selected freely between 1.8 V and 3.3 V.

**LVPECL-like:** Outputs Y[3:0] support LVPECL-like signaling. The actual output stage uses a CML structure but drives the same signal amplitude and rise time as true emitter coupled logic output stages. The LVPECL-like outputs should be AC-coupled, and contrary to standard PECL designs, no external termination resistor to VCC-2V is used (fewer components for lowest BOM cost). See reference schematic [Figure 69](#) for an example. The supply voltage for outputs configured LVPECL-like is recommended to be 3.3 V, though even 1.8 V provides nearly the same output swing and performance at much lower power consumption.

**CML:** Outputs Y[3:0] support standard CML signaling. The supply voltage for outputs configured CML can be selected freely between 1.8 V and 3.3 V. A true CML receiver can be driven DC coupled. All other differential receiver should connected using AC coupling. See reference schematic [Figure 69](#) for a circuit example.

**HCSL:** Outputs Y[7:4] support HCSL signaling. The supply voltage for outputs configured HCSL can be selected freely between 1.8 V and 3.3 V. HCSL is referenced to GND, and requires external 50- $\Omega$  termination to GND. See the reference schematic for an example.

**CMOS:** Outputs Y[7:4] support 1.8-V, 2.5-V, and 3.3-V CMOS signaling. A fast or reduced slew rate can be selected through register programming. Each differential output port can drive one or two CMOS output signals. Both signals are *in-phase*, meaning their phase offset is zero degrees, and not 180°. The output swing is set by providing the according supply voltage (for example, if VDD\_Y4=2.5 V, the output swing on Y4 will be 2.5-V CMOS). Outputs configured for CMOS should only be terminated with a series-resistor near the device output to preserve the full signal swing. Terminating CMOS signals with a 50- $\Omega$  resistor to GND would reduce the output signal swing significantly.

### 9.2.2.7 Integer Output Divider (IO)

Each integer output divider is made up of a continuous 10-b counter. The output buffer itself contributes only little to the total device output jitter due to a low output buffer phase noise floor. The typical output phase noise floor at an output frequency of 122.88 MHz, 20-MHz offset from the carrier measures as follows: LVCMOS: –157.8 dBc/Hz, LVDS: –158 dBc/Hz, LVPECL: –158.25 dBc/Hz, HCSL: –160 dBc/Hz. Therefore, the overall contribution of the output buffer to the total jitter is approximately 50 fs-rms (12 k – 20 MHz). An actual measurement of phase noise floor with different output frequencies for one nominal yielded the results in [Table 42](#):

**Table 42. Output Noise Floor**

| f <sub>OUT</sub> | LVDS (Y0)     | PECL (Y0)     | CML (Y0)      | HCSL (Y4)     | CMOS 3p3V (Y7) |
|------------------|---------------|---------------|---------------|---------------|----------------|
| 737.28 MHz       | –154.0 dBc/Hz | –154.8 dBc/Hz | –154.4 dBc/Hz | –153.1 dBc/Hz | –150.9 dBc/Hz  |
| 368.64 MHz       | –157.0 dBc/Hz | –155.8 dBc/Hz | –156.4 dBc/Hz | –153.9 dBc/Hz | –153.1 dBc/Hz  |
| 184.32 MHz       | –157.3 dBc/Hz | –158.6 dBc/Hz | 158.1 dBc/Hz  | –154.7 dBc/Hz | –156.2 dBc/Hz  |
| 92.16 MHz        | –161.2 dBc/Hz | –161.6 dBc/Hz | –161.4 dBc/Hz | –155.2 dBc/Hz | –159.4 dBc/Hz  |
| 46.08 MHz        | –162.2 dBc/Hz | –165.0 dBc/Hz | –163.0 dBc/Hz | –154.0 dBc/Hz | –162.8 dBc/Hz  |

### 9.2.2.8 Fractional Output Divider (FOD)

The CDCM6208 incorporates a fractional output divider on Y[7:4], allowing these outputs to run at non-integer output divide ratios of the PLL frequencies. This feature is useful when systems require different, unrelated frequencies. The fractional output divider architecture is shown in Figure 56.

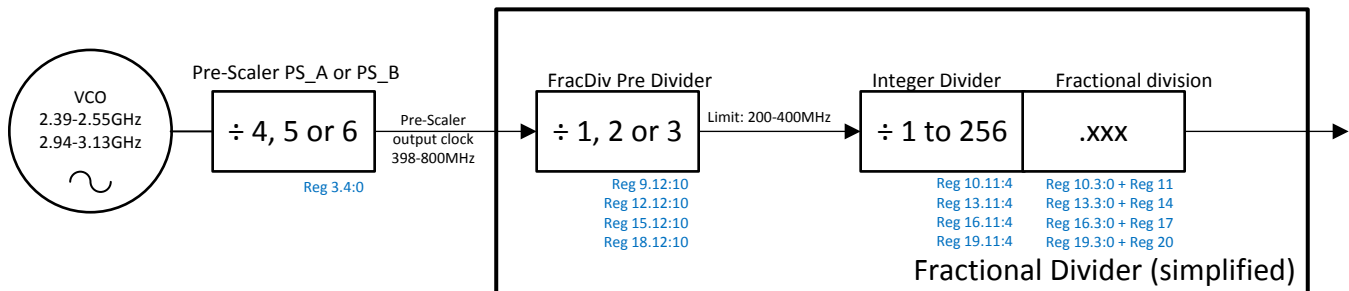


**Figure 56. Fractional Output Divider Principle Architecture (Simplified Graphic, not Showing Output Divider Bypass Options)**

The fractional output divider requires an input frequency between 400 MHz and 800 MHz, and outputs any frequency equal or less than 400 MHz (the minimum fractional output divider setting is 2). The fractional divider block has a first stage integer pre-divider followed by a fractional sigma-delta output divider block that is deep enough such as to generate any output frequency in the range of 0.78 MHz to 400 MHz from any input frequency in the range of 400 MHz to 800 MHz with a worst case frequency accuracy of no more than  $\pm 1$ ppm. The fractional values available are all possible 20-b representations of fractions within the following range:

- $1.0 \leq \text{frac}_{\text{DIV}} \leq 1.9375$
- $2.0 \leq \text{frac}_{\text{DIV}} \leq 3.875$
- $4.0 \leq \text{frac}_{\text{DIV}} \leq 5.875$
- $x.0 \leq \text{frac}_{\text{DIV}} \leq (x + 1) + 0.875$  with x being all even numbers from x = 2, 4, 6, 8, 10, ..., 254
- $254.0 \leq \text{frac}_{\text{DIV}} \leq 255.875$
- $256.0 \leq \text{frac}_{\text{DIV}} \leq 256.99999$

The CDCM6208 user GUI comprehends the fractional divider limitations; therefore, using the GUI to comprehend frequency planning is recommended.

The fractional divider output jitter is a function of fractional divider input frequency and furthermore depends on which bits are exercised within the fractional divider. Exercising only MSB or LSB bits provides better jitter than exercising bits near the center of the fractional divider. Jitter data are provided in this document, and vary from 50 ps-pp to 200 ps-pp, when the device is operated as a frequency synthesizer with high PLL bandwidths (approximately 100 kHz to 400 kHz). When the device is operated as a jitter cleaner with low PLL bandwidths (< 1 kHz), its additive total jitter increases by as much as 30 ps-pp. The fractional divider can be used in integer mode. However, if only an integer divide ratio is needed, it is important to disable the corresponding fractional divider enable bit, which engages the higher performing integer divider.

### 9.2.2.9 Output Synchronization

Both types of output dividers can be synchronized using the SYNCN signal. For the CDCM6208, this signal comes from the SYNCN pin or the soft SYNCN register bit R3.5. The most common way to execute the output synchronization is to toggle the SYNCN pin. When SYNC is asserted ( $V_{\text{SYNCN}} \leq V_{\text{IL}}$ ), all outputs are disabled (high-impedance) and the output dividers are reset. When SYNC is de-asserted ( $V_{\text{SYNCN}} \geq V_{\text{IH}}$ ), the device first internally latches the signal, then retimes the signal with the pre-scaler, and finally turns all outputs on simultaneously. The first rising edge of the outputs is therefore approximately 15 ns to 20 ns delayed from the SYNC pin assertion. For one particular device configuration, the uncertainty of the delay is  $\pm 1$  PS\_A clock cycles. For one particular device and one particular configuration, the delay uncertainty is one PS\_A clock cycle.

The SYNC feature is particularly helpful in systems with multiple CDCM6208. If SYNC is released simultaneously for all devices, the total remaining output skew uncertainty is  $\pm 1$  clock cycles for all devices configured to identical pre-scaler settings. For devices with varying pre-scaler settings, the total part-to-part skew uncertainty due to sync remains  $\pm 2$  clock cycles.

Outputs Y0, Y1, Y4, and Y5 are aligned with the PS\_A output while outputs Y2, Y3, Y6, and Y7 are aligned with the PS\_B output). All outputs Y[7:0] turn on simultaneously, if PS\_B and PS\_A are set to identical divide values (PS\_A=PS\_B).

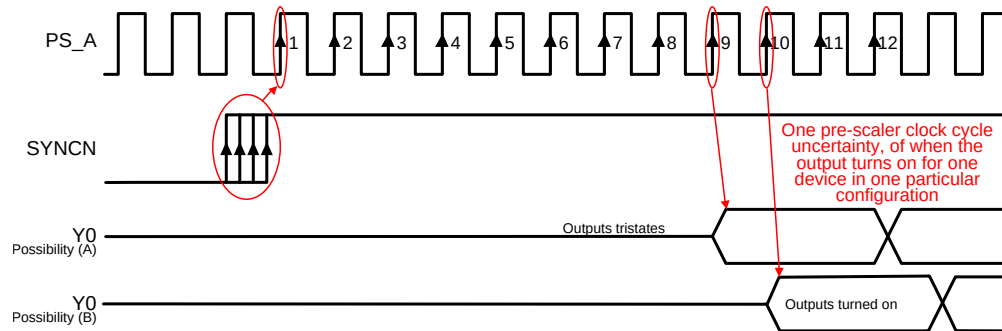


Figure 57. SYNCN to Output Delay Uncertainty

#### 9.2.2.10 Output Mux on Y4 and Y5

The CDCM6208 device outputs Y4 and Y5 can either be used as independent fractional outputs or allow bypassing of the PLL in order to output the primary or secondary input signal directly.

#### 9.2.2.11 Staggered CLK Output Power Up for Power Sequencing of a DSP

DSPs are sensitive to any kind of voltage swing on unpowered input rails. To protect the DSP from long-term reliability problems, TI recommends avoiding any clock signal to the DSP until the DSP power rail is also powered up. This can be achieved in two ways using the CDCM6208:

1. **Digital control:** Initiating a configuration of all registers so that all outputs are disabled, and then turning on outputs one by one through serial interface after each DSP rail becomes powered up accordingly.
2. **Output Power supply domain control:** An even easier scheme might be to connect the clock output power supply VDD\_Yx to the corresponding DSP input clock supply domain. In this case, the CDCM6208 output will remain disabled until the DSP rails ramps up as well. Figure 58 shows the turnon behavior.

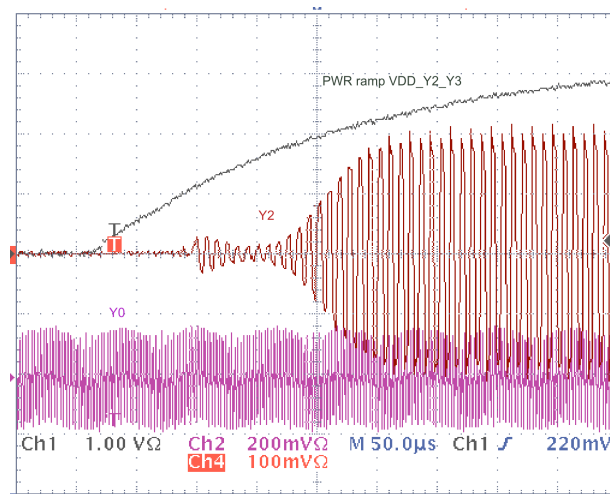


Figure 58. Sequencing the Output Turnon Through Sequencing the Output Supplies  
Output Y2 Powers Up While Output Y0 is Already Running

## 10 Power Supply Recommendations

### 10.1 Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains

#### 10.1.1 Mixing Supplies

The CDCM6208 incorporates a very flexible power supply architecture. Each building block has its own power supply domain, and can be driven independently with 1.8 V, 2.5 V, or 3.3 V. This is especially of advantage to minimize total system cost by deploying multiple low-cost LDOs instead of one, more-expensive LDO. This also allows mixed IO supply voltages (for example, one CMOS output with 1.8 V, another with 3.3 V) or interfacing to a SPI/I2C controller with 3.3-V supply while other blocks are driven from a lower supply voltage to minimize power consumption. The CDCM6208 current consumption is practically independent of the supply voltage, and therefore a lower supply voltage consumes lower device power. Also note that outputs Y3:0 if used for PECL swing will provide higher output swing if the according output domains are connected to 2.5 V or 3.3 V.

#### 10.1.2 Power-On Reset

The CDCM6208 integrates a built-in POR circuit, that holds the device in power down until all input, digital, and PLL supplies have reached at least 1.06 V (minimum) to 1.24 V (maximum). After this power-on release, device internal counters start (see [Device Power-Up Timing](#)) followed by device calibration. While the device digital circuit resets properly at this supply voltage level, the device is not ready to calibrate at such a low voltage. Therefore, for slow power-up ramps, the counters expire before the supply voltage reaches the minimum voltage of 1.71 V. Hence for slow power-supply ramp rates, it is necessary to delay calibration further using the PDN input.

#### 10.1.3 Slow Power-Up Supply Ramp

No particular power supply sequence is required for the CDCM6208. However, it is necessary to ensure that device calibration occurs AFTER the DVDD supply as well as the VDD\_PLL1, VDD\_PLL2, VDD\_PRI, and VDD\_SEC supply are all operational, and the voltage on each supply is higher than 1.45. This is best realized by delaying the PDN low-to-high transition. The PDN input incorporates a 50-k $\Omega$  resistor to DVDD. Assuming the DVDD supply ramp has a fixed time relationship to the slowest of all PLL and input power supplies, a capacitor from PDN to GND can delay the PDN input signal sufficiently to toggle PDN low-to-high AFTER all other supplies are stable. However, if the DVDD supply ramps much sooner than the PLL or input supplies, additional means are necessary to prevent PDN from toggling too early. A premature toggling of PDN would possibly result in failed PLL calibration, which can only be corrected by re-calibrating the PLL by either toggling PDN or RESET high-low-high.

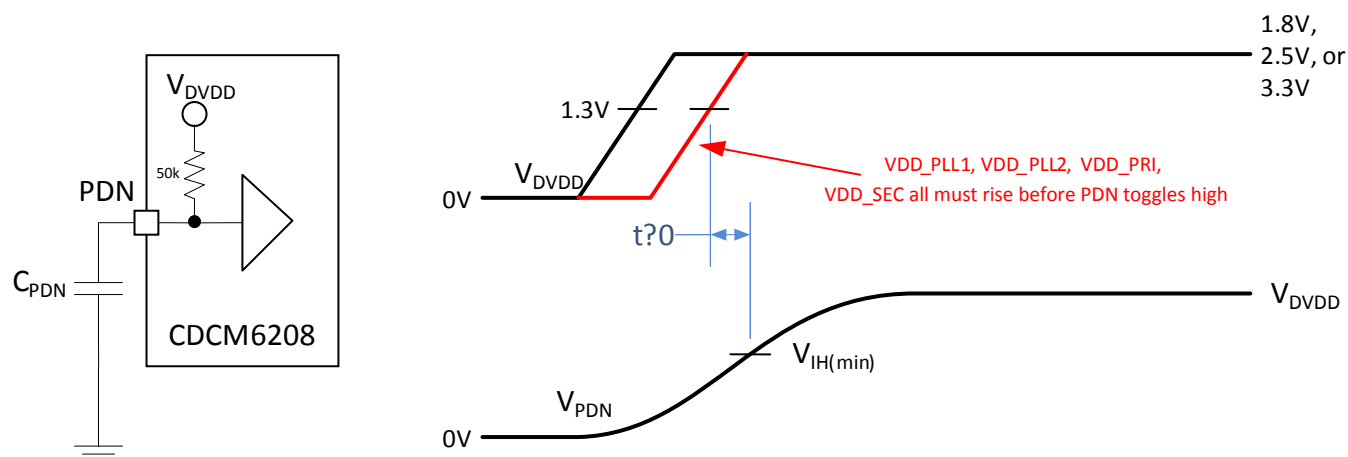


**Figure 59. PDN Delay When Using Slow Ramping Power Supplies (Supply Ramp > 50 ms)**

## Power Rail Sequencing, Power Supply Ramp Rate, and Mixing Supply Domains (continued)

### 10.1.4 Fast Power-Up Supply Ramp

If the supply ramp time for DVDD, VDD\_PLL1, VDD\_PLL2, VDD\_PRI, and VDD\_SEC are faster than 50 ms from 0 V to 1.8 V, no special provisions are necessary on PDN; the PDN pin can be left floating. Even an external capacitor to GND can be omitted in this circumstance, as the device delays calibration sufficiently by internal means.

### 10.1.5 Delaying VDD\_Yx\_Yy to Protect DSP IOs

DSPs and other highly integrated processors sometimes do not permit any clock signal to be present until the DSP power supply for the corresponding IO is also present. The CDCM6208 allows to either sequence output clock signals by writing to the corresponding output enable bit through SPI/I2C, or alternatively it is possible to connect the DSP IO supply and the CDCM6208 output supply together, in which case the CDCM6208 output will not turn on until the DSP supply is also valid. This second implementation avoids SPI/I2C programming.

## 10.2 Device Power-Up Timing

Before the device outputs turn on after power up, the device goes through the following initialization routine:

**Table 43. Power-Up Timing Procedure**

| STEP                                    | DURATION                                                                                                                                                                                             | COMMENTS                                                                                                                                                                                                                                                                                                          |
|-----------------------------------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Step 1: Power up ramp                   | Depends on customer supply ramp time                                                                                                                                                                 | The POR monitor holds the device in power-down or reset until the VDD supply voltage reaches 1.06 V (min) to 1.26 V (max)                                                                                                                                                                                         |
| Step 2: XO startup (if crystal is used) | Depends on XTAL. Could be several ms;<br>For NX3225GA 25 MHz typical XTAL startup time measures 200 $\mu$ s.                                                                                         | This step assumes RESETN = 1 and PDN = 1. The XTAL startup time is the time it takes for the XTAL to oscillate with sufficient amplitude. The CDCM6208 has a built-in amplitude detection circuit, and holds the device in reset until the XTAL stage has sufficient swing.                                       |
| Step 3: Ref Clock Counter               | 64k Reference clock cycles at PFD input                                                                                                                                                              | This counter of 64 k clock cycles needs to expire before any further power-up step is done inside the device. This counter ensures that the input to the PFD from PRI or SEC input has stabilized in frequency. The duration of this step can range from 640 $\mu$ s ( $f_{PFD}$ = 100 MHz) to 8 sec (8 kHz PFD). |
| Step 4: FBCLK counter                   | 64k FBCLK cycles with CW=32;<br>The duration is similar to Step 3, or can be more accurately estimated as:<br>V1: approximately 64k x PS_A x N/2.48 GHz<br>V2: approximately 64k x PS_A x N/3.05 GHz | The Feedback counter delays the startup by another 64k PFD clock cycles. This is so that all counters are well initialized and also ensure additional timing margin for the reference clock to settle. This step can range from 640 $\mu$ s ( $f_{PFD}$ = 100 MHz) to 8 sec ( $f_{PFD}$ = 8 kHz).                 |
| Step 5: VCO calibration                 | 128k PFD reference clock cycles                                                                                                                                                                      | This step calibrates the VCO to the exact frequency range, and takes exactly 128k PFD clock cycles. The duration can therefore range from 1280 $\mu$ s ( $f_{PFD}$ = 100 MHz) to 16 sec ( $f_{PFD}$ = 8 KHz).                                                                                                     |
| Step 6: PLL lock time                   | approximately 3 x LBW                                                                                                                                                                                | The Outputs turn on immediately after calibration. A small frequency error remains for the duration of approximately 3 x LBW (so in synthesizer mode typically 10 $\mu$ s). The initial output frequency will be lower than the target output frequency, as the loop filter starts out initially discharged.      |
| Step 7: PLL Lock indicator high         | approximately 2305 PFD clock cycles                                                                                                                                                                  | The PLL lock indicator if selected on output STATUS0 or STATUS1 will go high after approximately 2048 to 2560 PFD clock cycles to indicate PLL is now locked.                                                                                                                                                     |

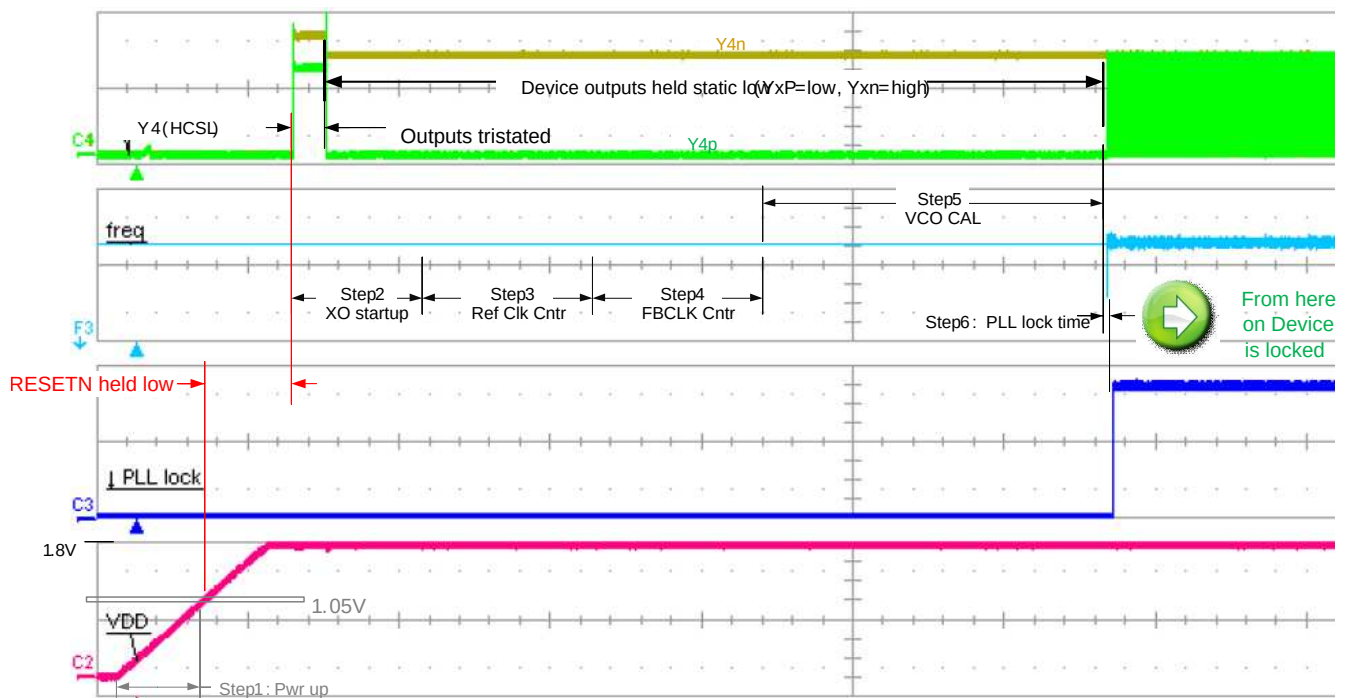


**Figure 60. Power-Up Time**

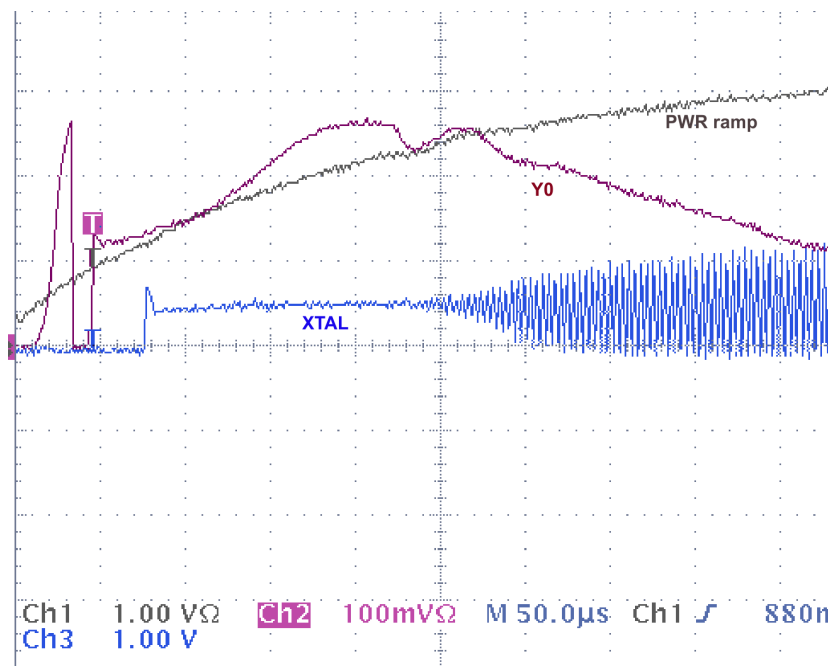


**Figure 61. XTAL Start-Up Using NX3225GA 25 MHz (Step 2)**

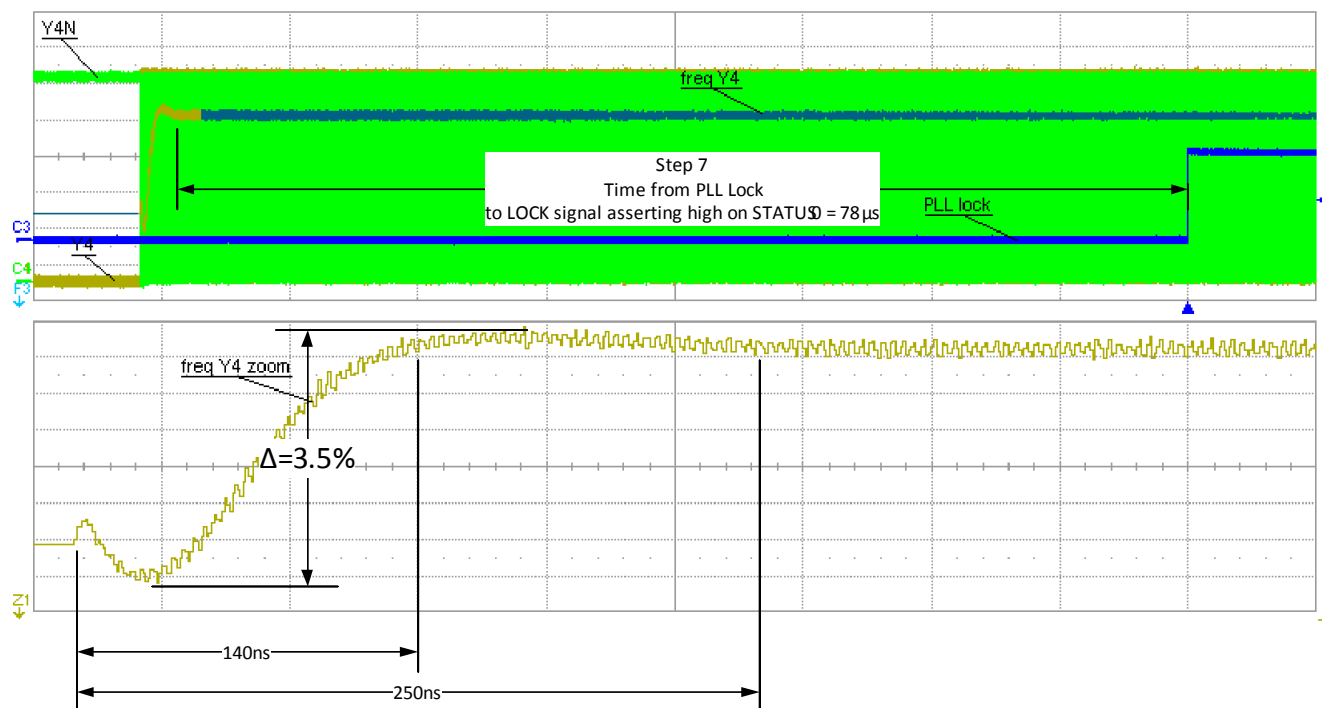


Figure 62. PLL Lock Behavior (Step 6)

### 10.3 Power Down

When the PDN pin = 0, the device enters a complete power down mode with a current consumption of no more than 1 mA from the entire device. Exiting power down resets the entire device and defaults all registers. It is recommended to connect a capacitor between the PDN pin and GND to implement a RC time delay and ensure the digital and PLL related power supplies are stable before the device calibration sequences is initiated. Refer to [Power Rail Sequencing](#), [Power Supply Ramp Rate](#), and [Mixing Supply Domains](#) for more details.

### 10.4 Power Supply Ripple Rejection (PSRR) versus Ripple Frequency

Many system designs become increasingly more sensitive to power supply noise rejection. To simplify design and cost, the CDCM6208 has built-in internal voltage regulation, which improves the power supply noise rejection over designs with no regulators. As a result, the following output rejection is achieved:

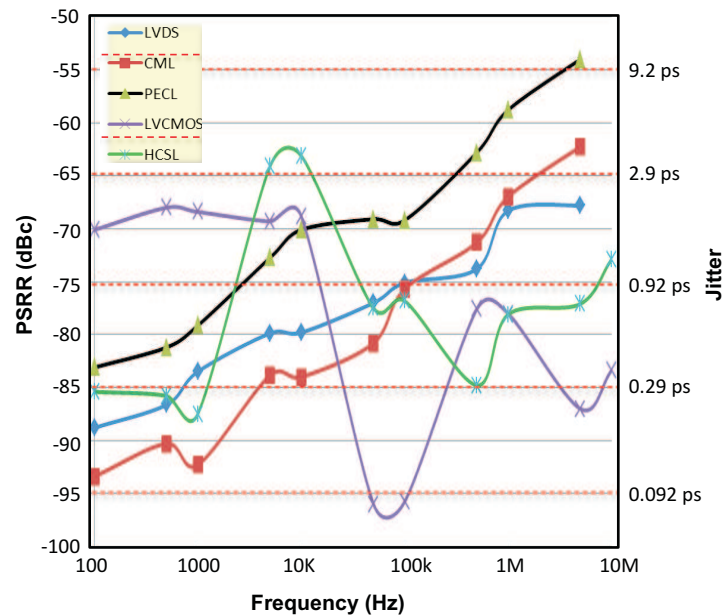


**Figure 63. PSRR (in dBc and DJ [ps]) Over Frequency [Hz] and Output Signal Format**  
 $f_{OUT} = 122.88 \text{ MHz}$   
 $VDD \text{ Supply Noise} = 100 \text{ mVpp}$

The DJ due to PSRR can be estimated using [Equation 4](#):

$$\text{Deterministic Jitter (ps}_{p-p}\text{)} = \frac{2 \times 10^{(\text{spur}/20)}}{\pi \times f_{CLK}} \times 10^{12} \quad (4)$$

**Example:** Therefore, if 100 mV noise with a frequency of 10 kHz were observed at the output supply, the according output jitter for a 122.88-MHz output signal with LVDS signaling could be estimated with DJ = 0.7 ps.

## 11 Layout

### 11.1 Layout Guidelines

Employing the thermally enhanced printed-circuit board layout shown in [Figure 64](#) insures good thermal performance of the solution. Observing good thermal layout practices enables the thermal pad on the backside of the VQFN-48 package to provide a good thermal path between the die contained within the package and the ambient air. This thermal pad also serves as the ground connection the device; therefore, a low inductance connection to the ground plane is essential.

[Figure 64](#) shows a layout optimized for good thermal performance and a good power supply connection as well. The 7×7 filled via pattern facilitates both considerations.

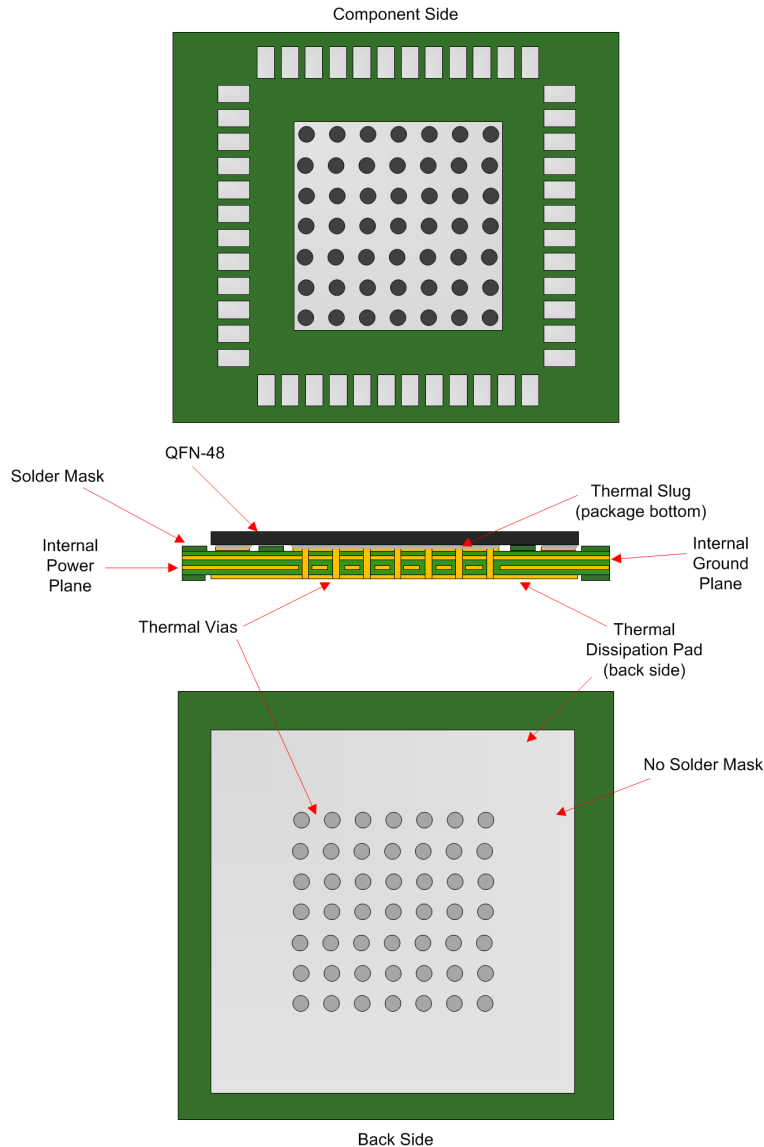


**Figure 64. Recommended PCB Layout of CDCM6208**

## Layout Guidelines (continued)

Figure 65 shows the conceptual layout detailing the recommended placement of power supply bypass capacitors. If the capacitors are mounted on the back side, 0402 components can be employed; however, soldering to the Thermal Dissipation Pad can be difficult. For component side mounting, use 0201 body size capacitors to facilitate signal routing. Keep the connections between the bypass capacitors and the power supply on the device as short as possible. Ground the other side of the capacitor using a low impedance connection to the ground plane.

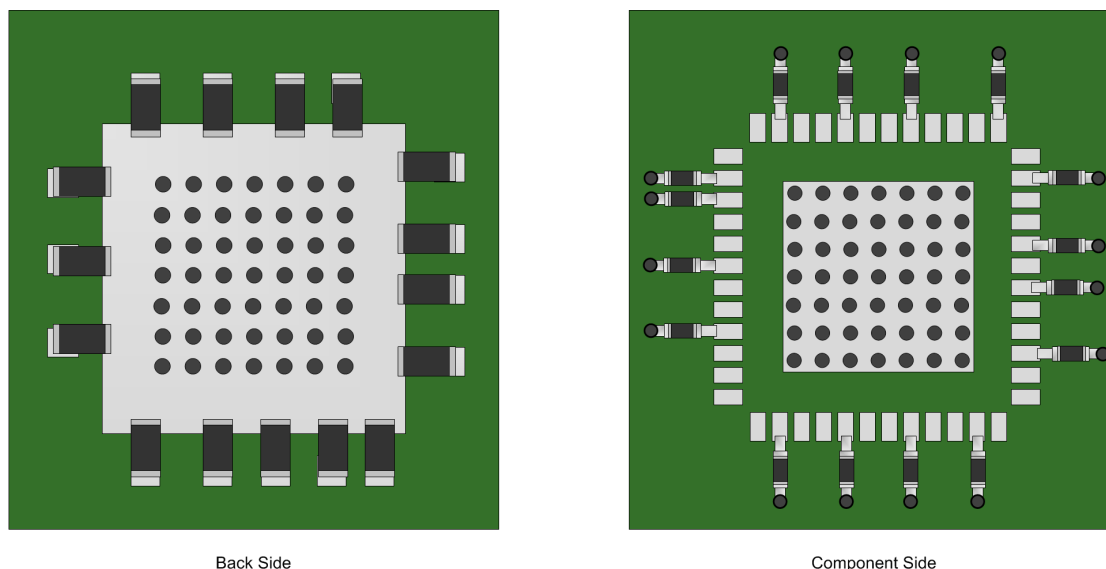


**Figure 65. PCB Conceptual Layouts**

## 11.2 Reference Schematics

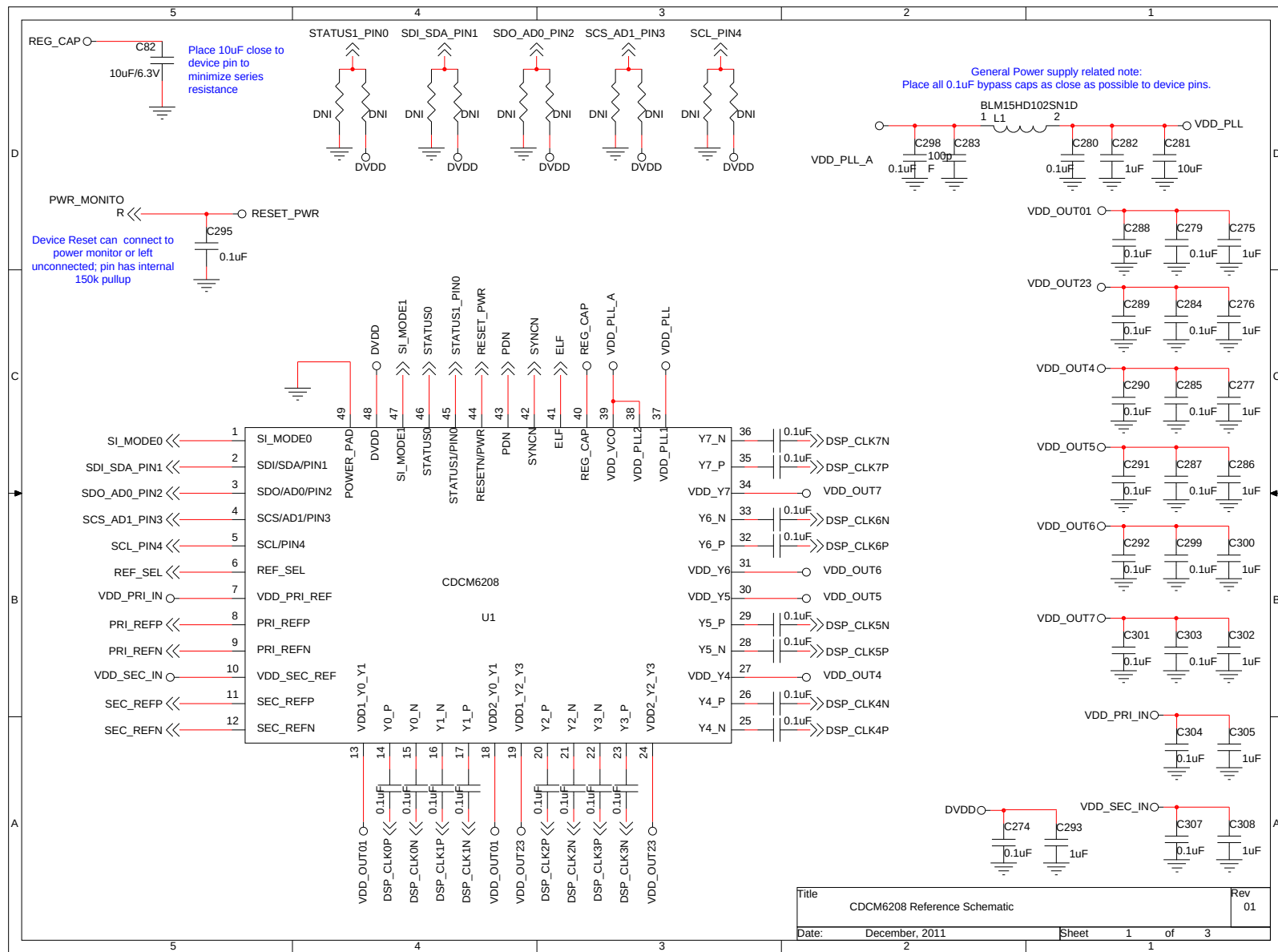


Figure 66. Schematic Page 1

## Reference Schematics (continued)

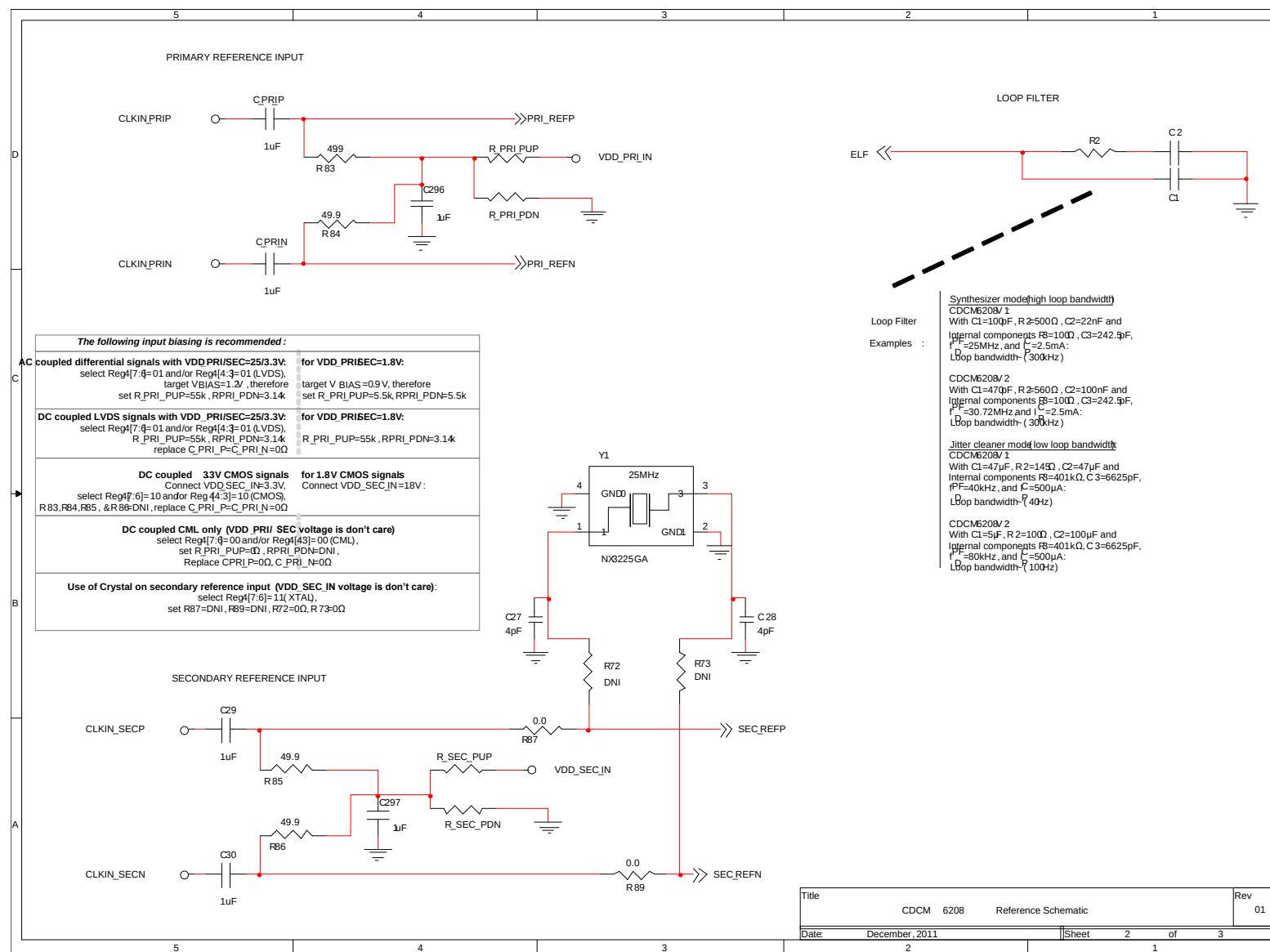


Figure 67. Schematic Page 2

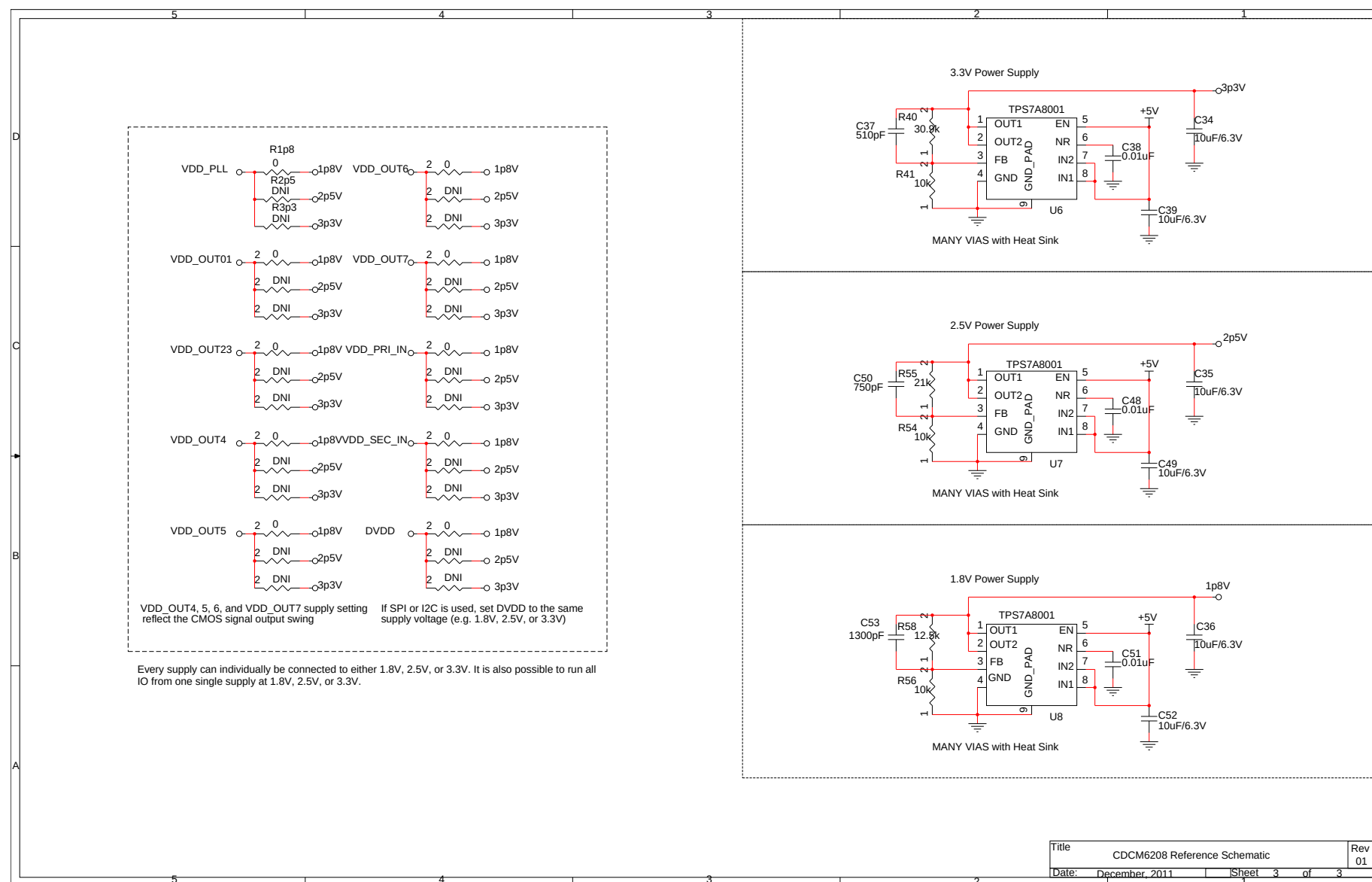


Figure 68. Schematic Page 3

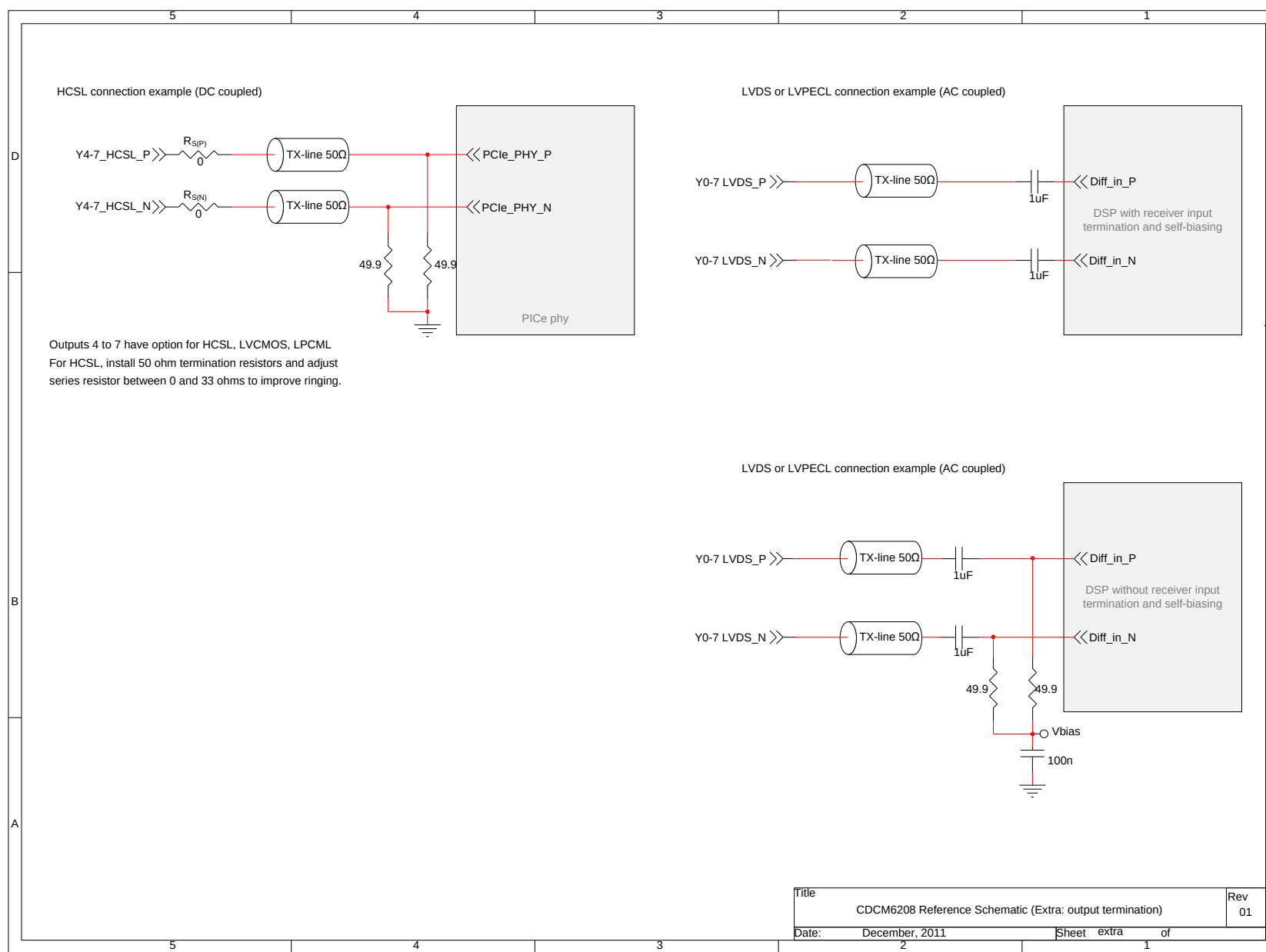


Figure 69. Schematic Page 4

## 12 Device and Documentation Support

### 12.1 Documentation Support

#### 12.1.1 Related Documentation

For related documentation, see the following:

[Hardware Design Guide for KeyStone Devices](#) (SPRABI2)

### 12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 12.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 12.4 Trademarks

KeyStone, E2E are trademarks of Texas Instruments.  
All other trademarks are the property of their respective owners.

### 12.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

### 12.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| CDCM6208V1HRGZR  | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | CM6208V1H               | <a href="#">Samples</a> |
| CDCM6208V1RGZR   | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | CDCM6208V1              | <a href="#">Samples</a> |
| CDCM6208V1RGZT   | ACTIVE        | VQFN         | RGZ                | 48   | 250            | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | CDCM6208V1              | <a href="#">Samples</a> |
| CDCM6208V2RGZR   | ACTIVE        | VQFN         | RGZ                | 48   | 2500           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | CDCM6208V2              | <a href="#">Samples</a> |
| CDCM6208V2RGZT   | ACTIVE        | VQFN         | RGZ                | 48   | 250            | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 85    | CDCM6208V2              | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

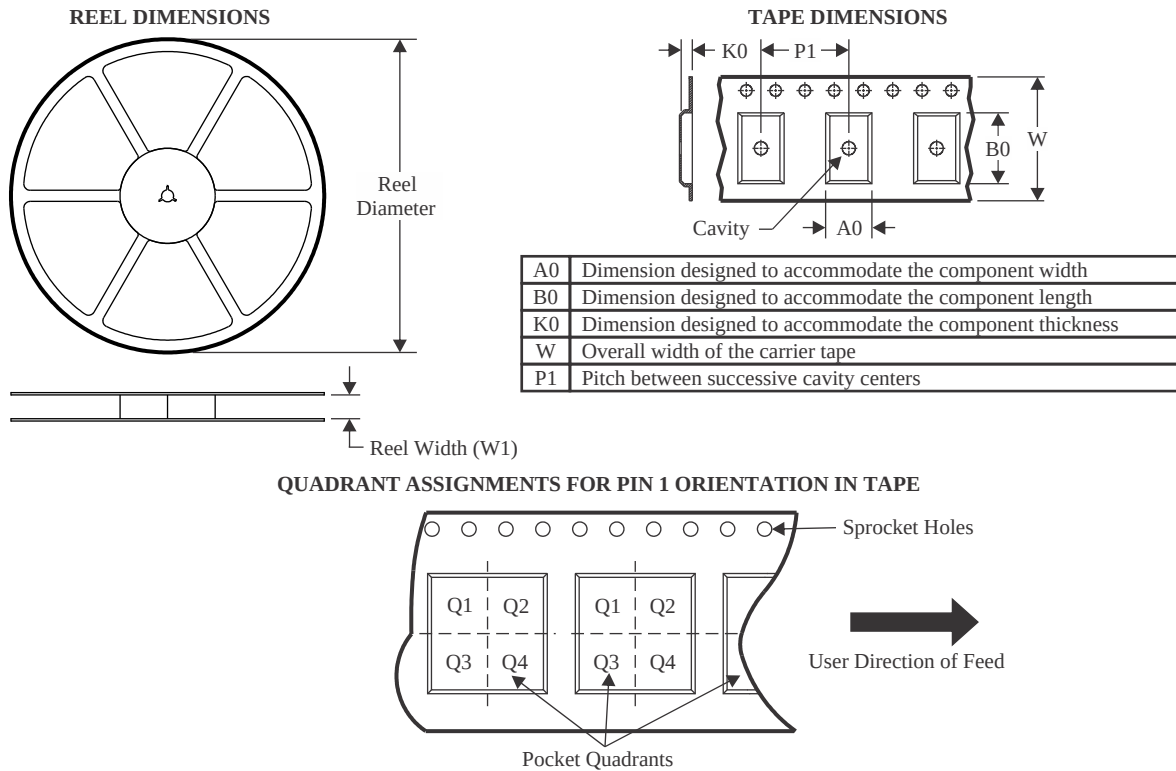
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

---

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

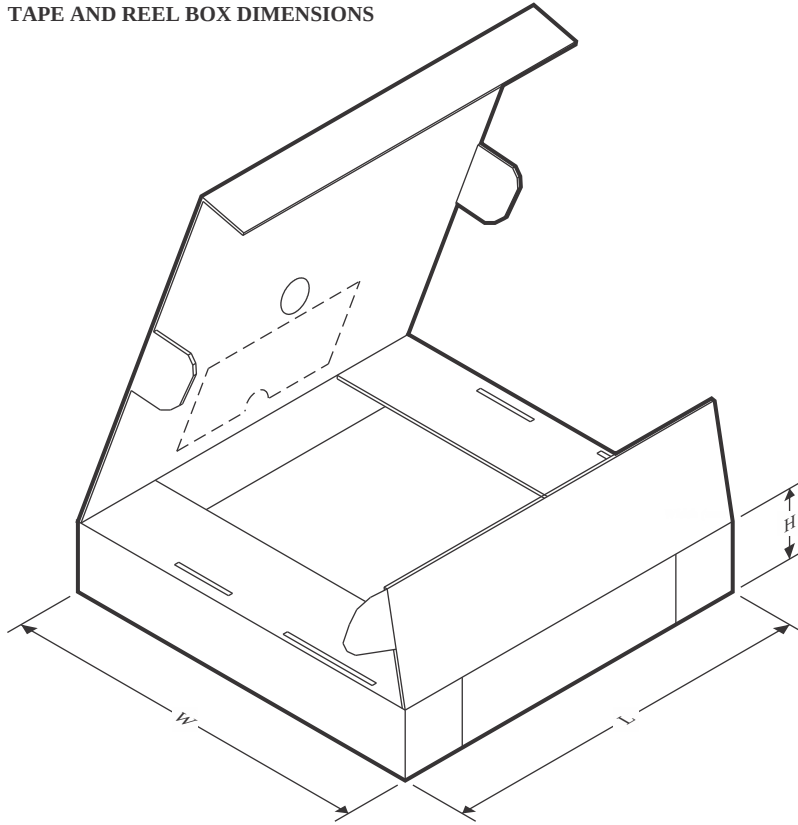
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**TAPE AND REEL INFORMATION**


\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|-----------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| CDCM6208V1HRGZR | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.3     | 12.0    | 16.0   | Q2            |
| CDCM6208V1RGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CDCM6208V1RGZT  | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CDCM6208V2RGZR  | VQFN         | RGZ             | 48   | 2500 | 330.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |
| CDCM6208V2RGZT  | VQFN         | RGZ             | 48   | 250  | 180.0              | 16.4               | 7.3     | 7.3     | 1.1     | 12.0    | 16.0   | Q2            |

## TAPE AND REEL BOX DIMENSIONS



\*All dimensions are nominal

| Device          | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|-----------------|--------------|-----------------|------|------|-------------|------------|-------------|
| CDCM6208V1HRGZR | VQFN         | RGZ             | 48   | 2500 | 356.0       | 356.0      | 36.0        |
| CDCM6208V1RGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| CDCM6208V1RGZT  | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |
| CDCM6208V2RGZR  | VQFN         | RGZ             | 48   | 2500 | 367.0       | 367.0      | 38.0        |
| CDCM6208V2RGZT  | VQFN         | RGZ             | 48   | 250  | 210.0       | 185.0      | 35.0        |

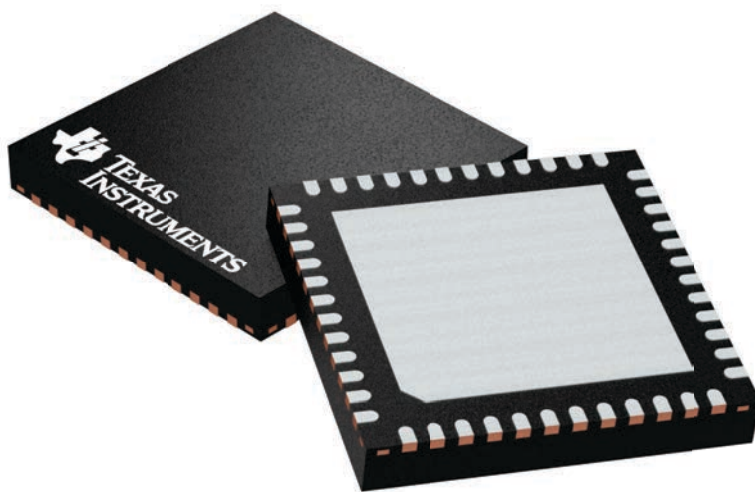
## GENERIC PACKAGE VIEW

**RGZ 48**

**VQFN - 1 mm max height**

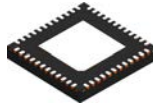
7 x 7, 0.5 mm pitch

PLASTIC QUADFLAT PACK- NO LEAD

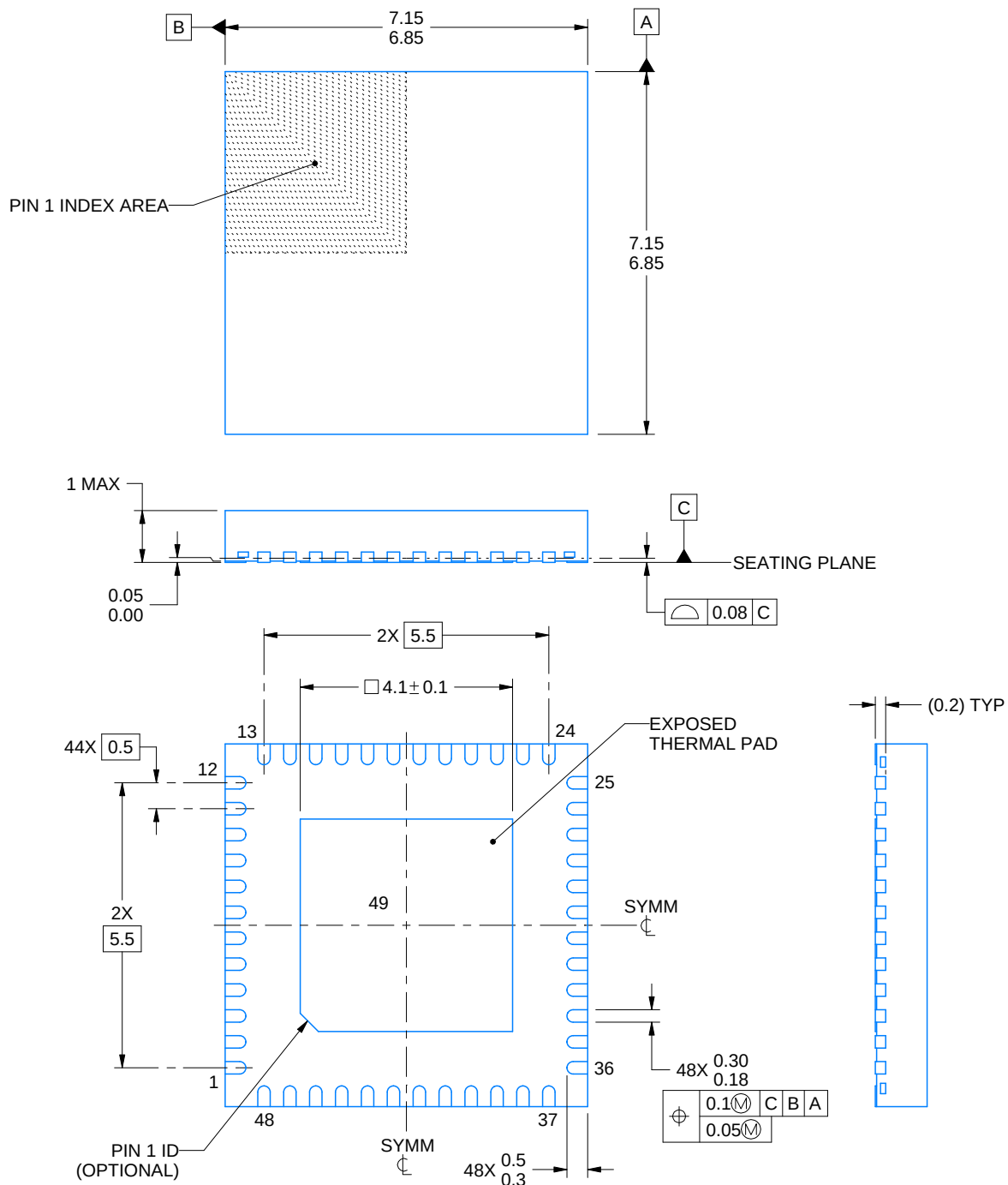


Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224671/A

**RGZ0048B****PACKAGE OUTLINE****VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



4218795/B 02/2017

**NOTES:**

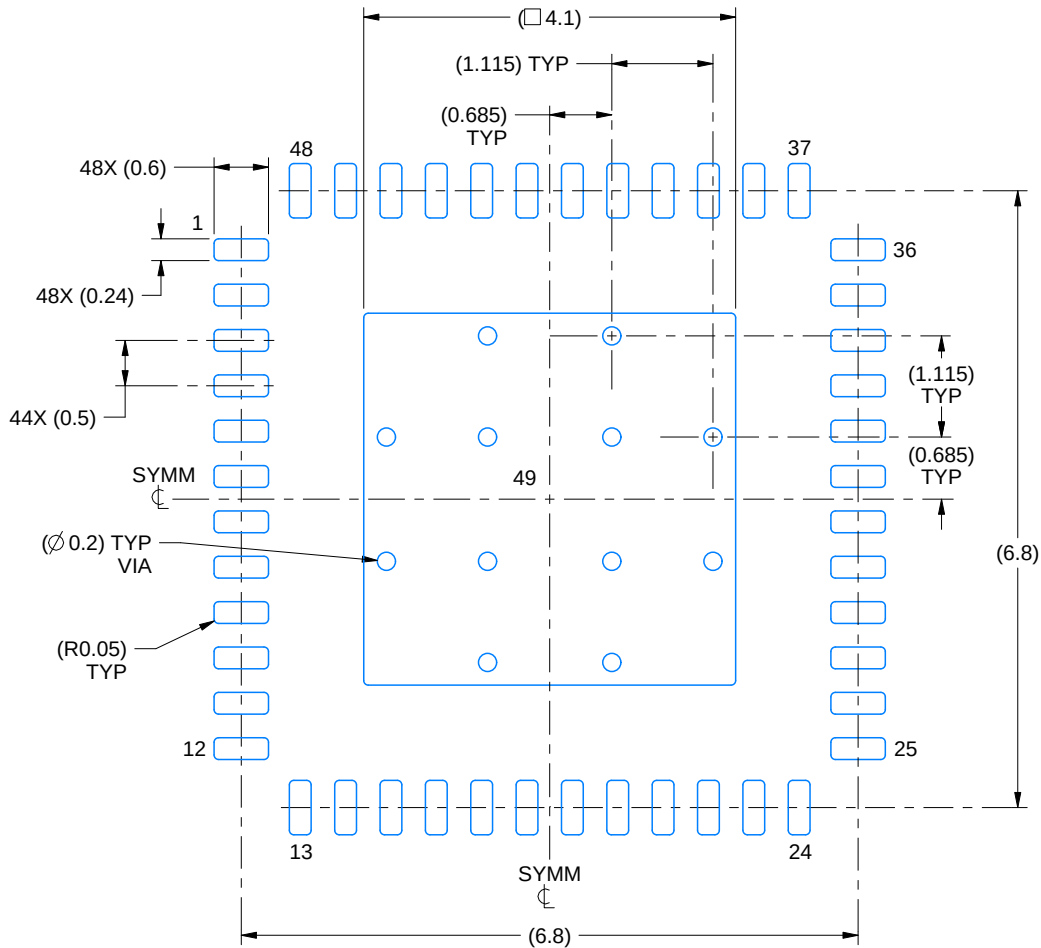
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

# EXAMPLE BOARD LAYOUT

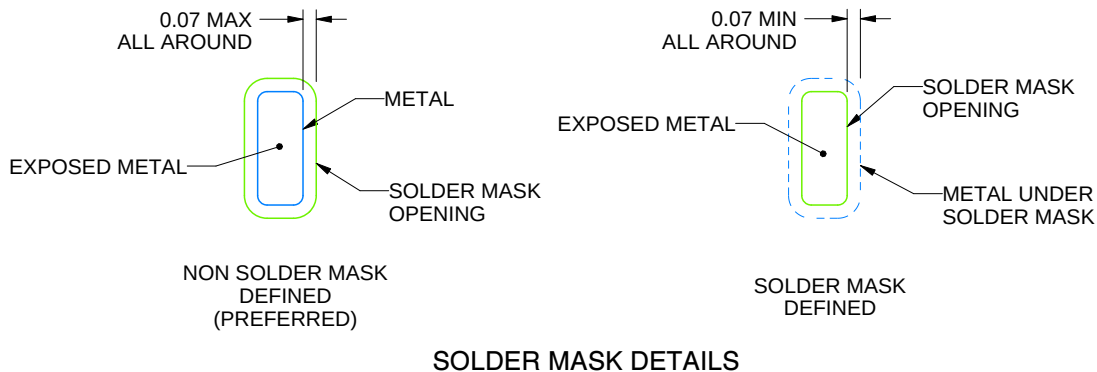
RGZ0048B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**LAND PATTERN EXAMPLE**  
EXPOSED METAL SHOWN  
SCALE:12X



**SOLDER MASK DETAILS**

4218795/B 02/2017

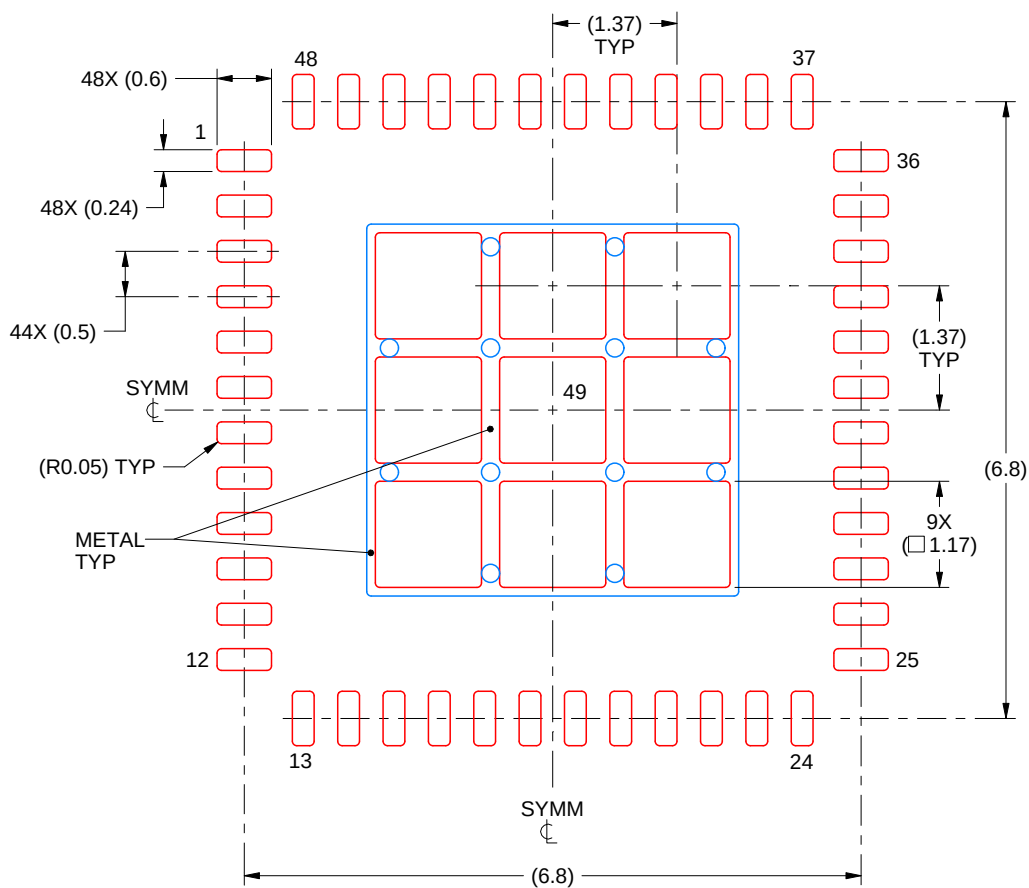
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sluea271](http://www.ti.com/lit/sluea271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

**RGZ0048B**

## VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



## SOLDER PASTE EXAMPLE

BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 49  
73% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:12X

4218795/B 02/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2024, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

⊖ View [CDCM6208V1ERGZT](#) on WIN SOURCE

⊖ [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management