



THE DATASHEET OF INA129SHKJ



INA12x-HT Precision, Low-Power Instrumentation Amplifiers

1 Features

- Low Offset Voltage: 25 μ V Typical
- Low Input Bias Current: 50 nA Typical ⁽¹⁾
- High CMR: 95 dB Typical⁽¹⁾
- Inputs Protected to ± 40 V
- Wide Supply Range: ± 2.25 V to ± 18 V
- Low Quiescent Current: 2 mA Typical⁽¹⁾

2 Applications

- Bridge Amplifiers
- Thermocouple Amplifiers
- RTD Sensor Amplifiers
- Medical Instrumentation
- Data Acquisition
- Supports Extreme Temperature Applications:
 - Controlled Baseline
 - One Assembly/Test Site
 - One Fabrication Site
 - Available in Extreme Temperature Ranges (-55°C to 210°C) ⁽²⁾
 - Extended Product Life Cycle
 - Extended Product-Change Notification
 - Product Traceability

3 Description

The INA128-HT and INA129-HT are low-power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make them ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth even at high gain. A single external resistor sets any gain from 1 to 10000. The INA128-HT provides an industry-standard gain equation; the INA129-HT gain equation is compatible with the AD620.

The INA128-HT and INA129-HT are laser trimmed for very low offset voltage (25 μ V Typ) and high common-mode rejection (93 dB at $G \geq 100$). These devices operate with power supplies as low as ± 2.25 V, and quiescent current of 2 mA, typically. Internal input protection can withstand up to ± 40 V without damage.

Texas Instruments' high-temperature products use highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.

The INA129-HT is available in 8-pin ceramic DIP and 8-pin ceramic surface-mount packages, specified for the -55°C to 210°C temperature range. The INA128-HT is available in an 8-pin SOIC-8 surface-mount package, specified for the -55°C to 175°C temperature range.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE (NOM) |
|-------------|-------------|--------------------|
| INA128-HT | SOIC (8) | 4.90 mm x 3.91 mm |
| INA129-HT | CFP (8) | 6.90 mm x 5.65 mm |
| | CDIP SB (8) | 11.81 mm x 7.49 mm |

- (1) Typical values for 210°C application.
 (2) Custom temperature ranges available.

- (1) For all available packages, see the orderable addendum at the end of the data sheet.

4 Simplified Schematic

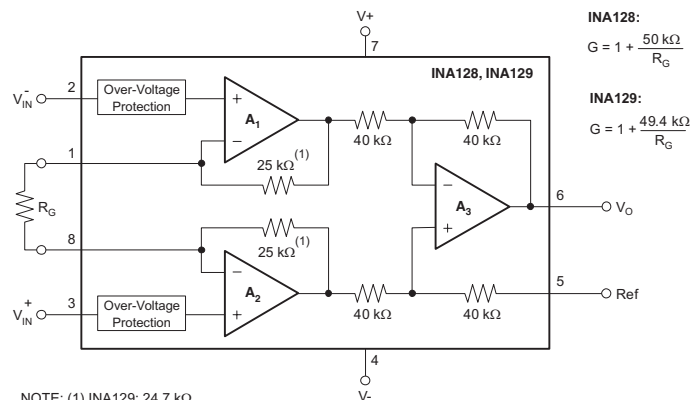


Table of Contents

| | | | |
|--|-----------|--|-----------|
| 1 Features | 1 | 8.3 Feature Description..... | 14 |
| 2 Applications | 1 | 8.4 Device Functional Modes..... | 15 |
| 3 Description | 1 | 9 Application and Implementation | 16 |
| 4 Simplified Schematic | 1 | 9.1 Application Information..... | 16 |
| 5 Revision History | 2 | 9.2 Typical Application | 16 |
| 6 Pin Configuration and Functions | 3 | 10 Power Supply Recommendations | 20 |
| 7 Specifications | 5 | 10.1 Low Voltage Operation | 20 |
| 7.1 Absolute Maximum Ratings | 5 | 11 Layout | 22 |
| 7.2 ESD Ratings | 5 | 11.1 Layout Guidelines | 22 |
| 7.3 Recommended Operating Conditions..... | 5 | 11.2 Layout Example | 22 |
| 7.4 Thermal Information: INA128-HT..... | 5 | 12 Device and Documentation Support | 23 |
| 7.5 Electrical Characteristics: INA128-HT..... | 6 | 12.1 Device Support..... | 23 |
| 7.6 Electrical Characteristics: INA129-HT..... | 8 | 12.2 Related Links | 23 |
| 7.7 Typical Characteristics | 11 | 12.3 Trademarks | 23 |
| 8 Detailed Description | 14 | 12.4 Electrostatic Discharge Caution..... | 23 |
| 8.1 Overview | 14 | 12.5 Glossary | 23 |
| 8.2 Functional Block Diagram | 14 | 13 Mechanical, Packaging, and Orderable Information | 23 |

5 Revision History

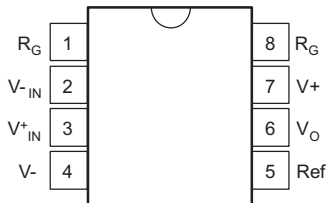
Changes from Revision E (July 2013) to Revision F

Page

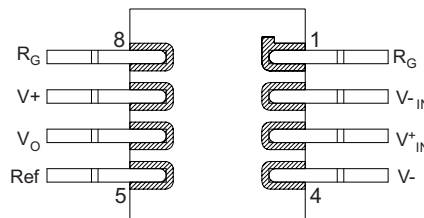
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section
- 1**
- Deleted *Ordering Information* table; for all available packages, see the package option addendum
- 3**

6 Pin Configuration and Functions

**D, HKJ, or JDJ Package
8-Pin SOIC, CFP, or CDIP SB
Top View**



**HKQ Package
8-Pin CFP
Top View**



HKQ as formed or HKJ mounted dead bug

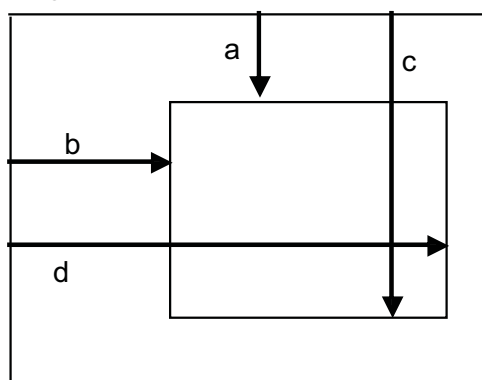
Pin Functions

| PIN | | I/O | DESCRIPTION |
|------|------|-------|---|
| NAME | NO. | | |
| Ref | 5 | I | Output voltage reference |
| RG | 1, 8 | O | Gain resistor connection |
| V+ | 7 | Power | Positive power supply voltage from 2.25 V to 18 V |
| V- | 4 | Power | Negative power supply voltage from -2.25 V to -18 V |
| V+IN | 3 | I | Non-inverting input voltage |
| V-IN | 2 | I | Inverting input voltage |
| VO | 6 | O | Output voltage |

Bare Die Information

| DIE THICKNESS | BACKSIDE FINISH | BACKSIDE POTENTIAL | BOND PAD METALLIZATION COMPOSITION |
|---------------|------------------------|--------------------|------------------------------------|
| 15 mils | Silicon with backgrind | GND | Al-Si-Cu (0.5%) |

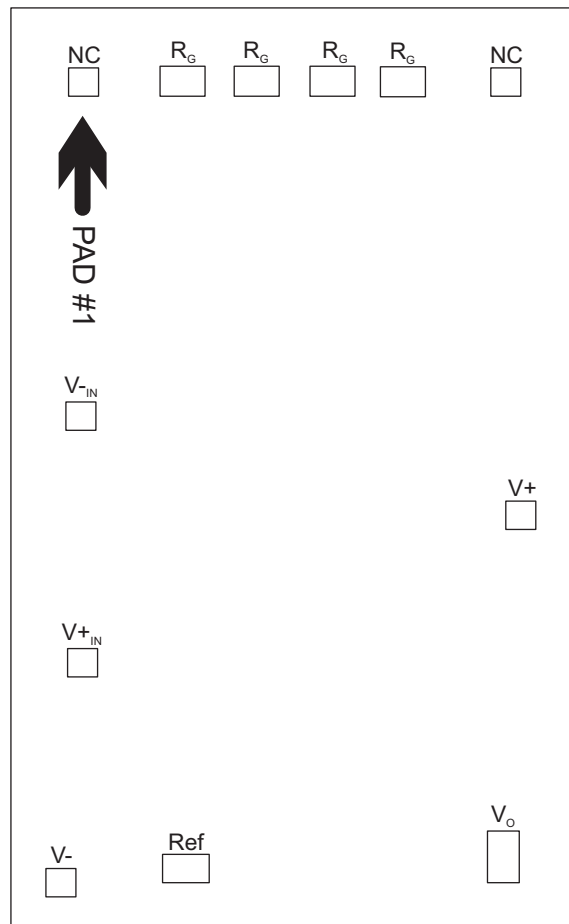
Origin



Bond Pad Coordinates in Mils

| DESCRIPTION | PAD NUMBER | a | b | c | d |
|-------------------------------|------------|-------|-------|-------|-------|
| NC | 1 | -57.4 | -31.1 | -53.3 | -27 |
| V _{-IN} | 2 | -9.85 | -31.4 | -5.75 | -27.3 |
| V _{+IN} | 3 | 25.05 | -31.4 | 29.15 | -27.3 |
| V- | 4 | 56.2 | -34.3 | 60.3 | -30.2 |
| Ref | 5 | 53.75 | -17.6 | 57.85 | -11 |
| V _O | 6 | 50.35 | 27.8 | 56.95 | 31.9 |
| V+ | 7 | 7.75 | 30.2 | 11.85 | 34.3 |
| NC | 8 | -57.4 | 28.4 | -53.3 | 32.5 |
| R _G ⁽¹⁾ | 9 | -57.4 | 13.4 | -53.3 | 20 |
| R _G ⁽¹⁾ | 10 | -57.5 | 2.7 | -53.4 | 9.3 |
| R _G ⁽¹⁾ | 11 | -57.5 | -7.9 | -53.4 | -1.3 |
| R _G ⁽¹⁾ | 12 | -57.4 | -18.6 | -53.3 | -12 |

- (1) Pads 9 and 10 must both be bonded to a common point and correspond to package pin 8. Pads 11 and 12 must both be bonded to a common point and correspond to package pin 1.



7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | MIN | MAX | UNIT |
|---------------------------------------|----------------------------------|------------|-----|------|
| Voltage | Supply | | ±18 | V |
| | Analog input | | ±40 | |
| Current | Output short-circuit (to ground) | Continuous | | |
| Operating temperature | HKJ, HKQ, KGD and JD packages | –55 | 210 | °C |
| | D package | –55 | 175 | |
| Storage temperature, T _{stg} | HKJ, HKQ, KGD and JD packages | –55 | 210 | °C |
| | D package | –55 | 175 | |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

| | | VALUE | UNIT |
|--|--|-------|------|
| A. INA218-HT (D, HKJ, or JDJ Package) | | | |
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±2000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±50 | |
| B. INA129-HT (HKQ Package) | | | |
| V _(ESD) Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾ | ±4000 | V |
| | Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾ | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|--|---------|-----|----------|------|
| V power supply | ±2.25 | ±15 | ±18 | V |
| Input common-mode voltage range for V _O = 0 | V – 2 V | | V + –2 V | |
| T _A operating temperature INA128-HT | –55 | | 175 | °C |
| T _A operating temperature INA129-HT | –55 | | 210 | °C |

7.4 Thermal Information: INA128-HT

| THERMAL METRIC ⁽¹⁾ | | INA128-HT | UNIT |
|-------------------------------|--|-----------|------|
| | | D [SOIC] | |
| | | 8 PINS | |
| R _{θJA} | Junction-to-ambient thermal resistance | 110 | °C/W |
| R _{θJC(top)} | Junction-to-case (top) thermal resistance | 57 | |
| R _{θJB} | Junction-to-board thermal resistance | 54 | |
| ψ _{JT} | Junction-to-top characterization parameter | 11 | |
| ψ _{JB} | Junction-to-board characterization parameter | 53 | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

7.5 Electrical Characteristics: INA128-HT

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | | | $T_A = 175^\circ\text{C}^{(1)}$ | | | UNIT |
|--|---|--|--------------------------------|----------------------------------|---------------------------------|------------------------|--------------------------------|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| INPUT | | | | | | | | |
| OFFSET VOLTAGE, RTI | | | | | | | | |
| Initial | $T_A = 25^\circ\text{C}$ | | ± 25 $\pm 100/\text{G}$ | ± 125 $\pm 1000/\text{G}$ | | | | μV |
| vs temperature | $T_A = T_{\text{MIN}} \text{ to } T_{\text{MAX}}$ | | ± 0.2 $\pm 5/\text{G}$ | ± 1 $\pm 20/\text{G}$ | | | ± 3.5 $\pm 80/\text{G}$ | $\mu\text{V}/^\circ\text{C}$ |
| vs power supply | $V_S = \pm 2.25 \text{ V to } \pm 18 \text{ V}$ | | | ± 2 $\pm 200/\text{G}$ | | | ± 5 $\pm 500/\text{G}$ | $\mu\text{V}/\text{V}$ |
| Long-term stability | | | $\pm 1 \pm 3/\text{G}$ | | | $\pm 1 \pm 3/\text{G}$ | | $\mu\text{V}/\text{mo}$ |
| Impedance, differential | | | $10^{10} \parallel 2$ | | | $10^{10} \parallel 2$ | | $\Omega \parallel \text{pF}$ |
| Common mode | | | $10^{11} \parallel 9$ | | | $10^{11} \parallel 9$ | | $\Omega \parallel \text{pF}$ |
| Common mode voltage range ⁽²⁾ | $V_O = 0 \text{ V}$ | $(V+) - 2$ | $(V+) - 1.4$ | | $(V+) - 2$ | $(V+) - 1.4$ | | V |
| | | $(V-) + 2$ | $(V-) + 1.7$ | | $(V-) + 2$ | $(V-) + 1.7$ | | V |
| Safe input voltage | | | | ± 40 | | | ± 40 | V |
| Common-mode rejection | $V_{\text{CM}} = \pm 13 \text{ V},$ $\Delta R_S = 1 \text{ k}\Omega$ | | | | | | | dB |
| | G = 1 | 58 | 86 | | 58 | 75 | | |
| | G = 10 | 78 | 106 | | 78 | 85 | | |
| | G = 100 | 99 | 125 | | 99 | 110 | | |
| | G = 1000 | 113 | 130 | | 113 | 120 | | |
| CURRENT | | | | | | | | |
| Bias current | | | ± 2 | ± 10 | | | ± 45 | nA |
| vs temperature | | | ± 30 | | | ± 550 | | $\text{pA}/^\circ\text{C}$ |
| Offset Current | | | ± 1 | ± 10 | | | ± 45 | nA |
| vs temperature | | | ± 30 | | | ± 550 | | $\text{pA}/^\circ\text{C}$ |
| NOISE | | | | | | | | |
| Noise voltage, RTI | G = 1000, $R_S = 0 \Omega$ | | | | | | | |
| f = 10 Hz | | | 10 | | | 10 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| f = 100 Hz | | | 8 | | | 8 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| f = 1 kHz | | | 8 | | | 8 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_B = 0.1 \text{ Hz to } 10 \text{ Hz}$ | | | 0.2 | | | 0.8 | | μV_{PP} |
| Noise current | | | | | | | | |
| f = 10 Hz | | | 0.9 | | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| f = 1 kHz | | | 0.3 | | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_B = 0.1 \text{ Hz to } 10 \text{ Hz}$ | | | 30 | | | | | pA_{PP} |

- (1) Minimum and maximum parameters are characterized for operation at $T_A = 175^\circ\text{C}$, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
- (2) Input common-mode range varies with output voltage — see typical curves.

Electrical Characteristics: INA128-HT (continued)

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = -55°C to +125°C | | | T _A = 175°C ⁽¹⁾ | | | UNIT | | |
|------------------------------------|------------------------------------|----------------------------------|------------|--------------------|---------------------------------------|------------|--------------------|----------|-----|----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | | | |
| GAIN | | | | | | | | | | |
| Gain equation | | 1 + (50 kΩ/R _G) | | | 1 + (50 kΩ/R _G) | | | V/V | | |
| Range of gain | | 1 | | 10000 | 1 | | 10000 | V/V | | |
| Gain error | G = 1 | | ±0.01 | ±0.1 | | ±0.1% | ±0.5% | | | |
| | G = 10 | | ±0.02 | ±0.5 | | ±0.5% | ±1% | | | |
| | G = 100 | | ±0.05 | ±0.7 | | ±0.7% | ±1.5% | | | |
| | G = 1000 | | ±0.5 | ±2.5 | | ±2% | ±4% | | | |
| Gain vs temperature ⁽³⁾ | G = 1 | | ±1 | ±10 | | ±75 | | ppm/°C | | |
| 50-kΩ resistance ⁽³⁾⁽⁴⁾ | | | ±25 | ±100 | | ±75 | | ppm/°C | | |
| Nonlinearity | V _O = ±13.6 V, G = 1 | | ±0.0001 | ±0.001 | | | ±0.008 | % of FSR | | |
| | G = 10 | | ±0.0003 | ±0.002 | | | ±0.01 | | | |
| | G = 100 | | ±0.0005 | ±0.002 | | | ±0.01 | | | |
| | G = 1000 | | ±0.001 | See ⁽⁵⁾ | | ±0.6 | See ⁽⁵⁾ | | | |
| OUTPUT | | | | | | | | | | |
| Voltage | Positive | R _L = 10 kΩ | (V+) - 1.4 | (V+) - 0.9 | (V+) - 1.4 | (V+) - 0.9 | | V | | |
| | Negative | R _L = 10 kΩ | (V-) + 1.4 | (V-) + 0.8 | (V-) + 1.4 | (V-) + 0.8 | | | | |
| Load capacitance stability | | | | 1000 | | 1000 | | pF | | |
| Short-circuit current | | | | +6/-15 | | +6/-15 | | mA | | |
| FREQUENCY RESPONSE | | | | | | | | | | |
| Bandwidth, -3 dB | G = 1 | | | 1300 | | | 1100 | kHz | | |
| | G = 10 | | | 700 | | | 700 | | | |
| | G = 100 | | | 200 | | | 190 | | | |
| | G = 1000 | | | 20 | | | 17.5 | | | |
| Slew rate | V _O = ±10 V, G = 10 | | | 4 | | | 4 | V/μs | | |
| Settling time, 0.01% | G = 1 | | | 7 | | | 7 | μs | | |
| | G = 10 | | | 7 | | | 7 | | | |
| | G = 100 | | | 9 | | | 9 | | | |
| | G = 1000 | | | 80 | | | 80 | | | |
| Overload recovery | 50% overdrive | | | 4 | | | 4 | μs | | |
| POWER SUPPLY | | | | | | | | | | |
| Voltage range | | | ±2.25 | ±15 | ±18 | ±2.25 | ±15 | ±18 | V | |
| Current, total | V _{IN} = 0 V | | | ±0.7 | ±1 | | | ±1 | mA | |
| TEMPERATURE RANGE | | | | | | | | | | |
| Specification | | | | -55 | | | | +125 | 175 | °C |
| Operating | | | | -55 | | | | +125 | 175 | °C |

(3) Specified by wafer test.

(4) Temperature coefficient of the 50-kΩ term in the gain equation.

(5) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.

7.6 Electrical Characteristics: INA129-HT

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $T_A = -55^\circ\text{C to } +125^\circ\text{C}$ | | | $T_A = 210^\circ\text{C}^{(1)}$ | | | UNIT |
|--|---|--|--------------------------------|----------------------------------|---------------------------------|---------------------------------|-----|------------------------------|
| | | MIN | TYP | MAX | MIN | TYP | MAX | |
| INPUT | | | | | | | | |
| OFFSET VOLTAGE, RTI | | | | | | | | |
| Initial | $T_A = 25^\circ\text{C}$ | | ± 25 $\pm 100/\text{G}$ | ± 125 $\pm 1000/\text{G}$ | | | | μV |
| vs temperature | $T_A = T_{\text{MIN}}$ to T_{MAX} | | ± 0.2 $\pm 5/\text{G}$ | ± 1 $\pm 20/\text{G}$ | | ± 1 $\pm 850/\text{G}$ | | $\mu\text{V}/^\circ\text{C}$ |
| vs power supply | $V_S = \pm 2.25\text{ V to } \pm 18\text{ V}$ | | ± 0.2 $\pm 20/\text{G}$ | ± 2 $\pm 200/\text{G}$ | | ± 20 $\pm 1000/\text{G}$ | | $\mu\text{V}/\text{V}$ |
| Long-term stability | | | ± 1 $\pm 3/\text{G}$ | | | ± 1 $\pm 3/\text{G}$ | | $\mu\text{V}/\text{mo}$ |
| Impedance, differential | | | $10^{10} \parallel 2$ | | | $10^{10} \parallel 2$ | | $\Omega \parallel \text{pF}$ |
| Common mode | | | $10^{11} \parallel 9$ | | | $10^{11} \parallel 9$ | | $\Omega \parallel \text{pF}$ |
| Common mode voltage range ⁽²⁾ | $V_O = 0\text{ V}$ | $(V+) - 2$ | $(V+) - 1.4$ | | $(V+) - 2$ | $(V+) - 1.4$ | | V |
| | | $(V-) + 2$ | $(V-) + 1.7$ | | $(V-) + 2$ | $(V-) + 1.7$ | | V |
| Safe input voltage | | | | ± 40 | | ± 40 | | V |
| Common-mode rejection | $V_{\text{CM}} = \pm 13\text{ V},$ $\Delta R_S = 1\text{ k}\Omega$ | | | | | | | dB |
| | G = 1 | 58 | 86 | | 53 | | | |
| | G = 10 | 78 | 106 | | 69 | | | |
| | G = 100 | 99 | 125 | | 89 | | | |
| | G = 1000 | 113 | 130 | | 95 | | | |
| CURRENT | | | | | | | | |
| Bias current | | | ± 2 | ± 10 | | ± 50 | | nA |
| vs temperature | | | ± 30 | | | ± 600 | | $\text{pA}/^\circ\text{C}$ |
| Offset Current | | | ± 1 | ± 10 | | ± 50 | | nA |
| vs temperature | | | ± 30 | | | ± 600 | | $\text{pA}/^\circ\text{C}$ |
| NOISE | | | | | | | | |
| Noise voltage, RTI | G = 1000, $R_S = 0\ \Omega$ | | | | | | | |
| f = 10 Hz | | | 10 | | | 25 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| f = 100 Hz | | | 8 | | | 20 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| f = 1 kHz | | | 8 | | | 20 | | $\text{nV}/\sqrt{\text{Hz}}$ |
| $f_B = 0.1\text{ Hz to } 10\text{ Hz}$ | | | 0.2 | | | 2 | | μV_{PP} |
| Noise current | | | | | | | | |
| f = 10 Hz | | | 0.9 | | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| f = 1 kHz | | | 0.3 | | | | | $\text{pA}/\sqrt{\text{Hz}}$ |
| $f_B = 0.1\text{ Hz to } 10\text{ Hz}$ | | | 30 | | | | | pA_{PP} |

- (1) Minimum and maximum parameters are characterized for operation at $T_A = 210^\circ\text{C}$, but may not be production tested at that temperature. Production test limits with statistical guardbands are used to ensure high temperature performance.
- (2) Input common-mode range varies with output voltage — see typical curves.

Electrical Characteristics: INA129-HT (continued)

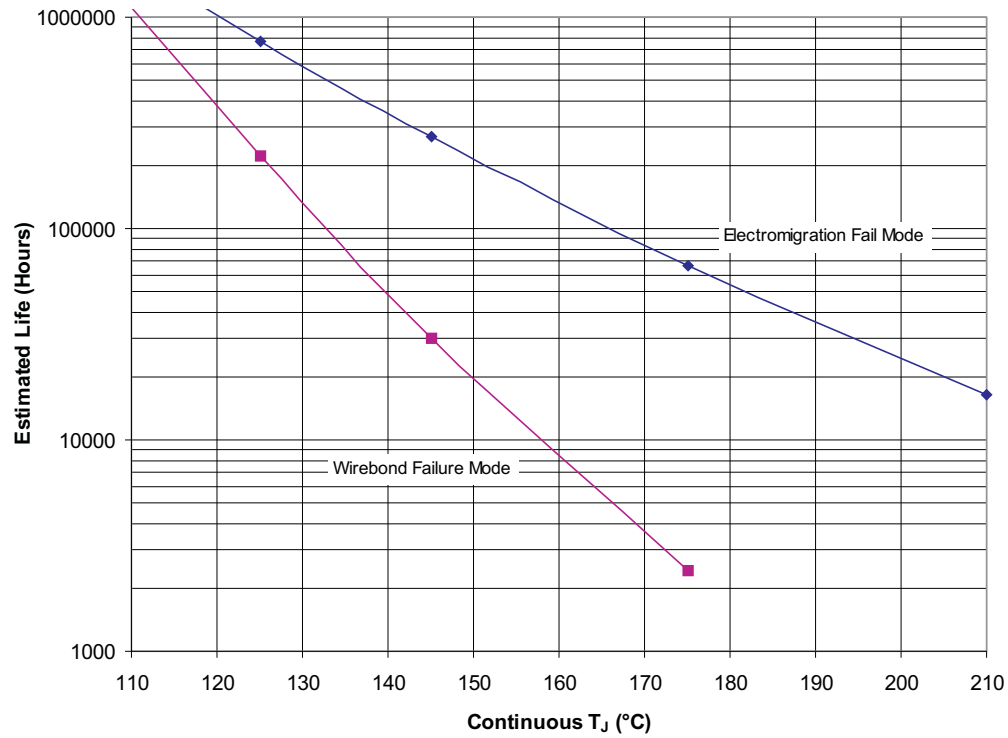
over operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | T _A = -55°C to +125°C | | | T _A = 210°C ⁽¹⁾ | | | UNIT | |
|--------------------------------------|------------------------------------|----------------------------------|------------|--------------------|---------------------------------------|------------|--------------------|----------|----|
| | | MIN | TYP | MAX | MIN | TYP | MAX | | |
| GAIN | | | | | | | | | |
| Gain equation | | $1 + (49.4 \text{ k}\Omega/R_G)$ | | | $1 + (49.4 \text{ k}\Omega/R_G)$ | | | V/V | |
| Range of gain | | 1 | | 10000 | 1 | | 10000 | V/V | |
| Gain error | G = 1 | | ±0.01% | ±0.1% | | ±1.1% | | | |
| | G = 10 | | ±0.02% | ±0.5% | | ±2.6% | | | |
| | G = 100 | | ±0.05% | ±0.7% | | ±13.5% | | | |
| | G = 1000 | | ±0.5% | ±2.5% | | ±65.5% | | | |
| Gain vs temperature ⁽³⁾ | G = 1 | | ±1 | ±10 | | ±100 | | ppm/°C | |
| 49.4-kΩ resistance ⁽³⁾⁽⁴⁾ | | | ±25 | ±100 | | ±100 | | ppm/°C | |
| Nonlinearity | V _O = ±13.6 V, G = 1 | | ±0.0001 | ±0.001 | | ±0.1 | | % of FSR | |
| | G = 10 | | ±0.0003 | ±0.002 | | ±0.2 | | | |
| | G = 100 | | ±0.0005 | ±0.002 | | ±0.7 | | | |
| | G = 1000 | | ±0.001 | See ⁽⁵⁾ | | ±2.4 | See ⁽⁵⁾ | | |
| OUTPUT | | | | | | | | | |
| Voltage | Positive | R _L = 10kΩ | (V+) - 1.4 | (V+) - 0.9 | (V+) - 1.4 | (V+) - 0.9 | | V | |
| | Negative | R _L = 10kΩ | (V-) + 1.4 | (V-) + 0.8 | (V-) + 1.4 | (V-) + 0.8 | | | |
| Load capacitance stability | | | | 1000 | | 1000 | | pF | |
| Short-circuit current | | | | +6/-15 | | +12/-5 | | mA | |
| FREQUENCY RESPONSE | | | | | | | | | |
| Bandwidth, -3 dB | G = 1 | | | 1300 | | 850 | | kHz | |
| | G = 10 | | | 700 | | 400 | | | |
| | G = 100 | | | 200 | | 50 | | | |
| | G = 1000 | | | 20 | | 7.5 | | | |
| Slew rate | V _O = ±10 V, G = 10 | | | 4 | | 4 | | V/μs | |
| Settling time, 0.01% | G = 1 | | | 7 | | 10 | | μs | |
| | G = 10 | | | 7 | | 10 | | | |
| | G = 100 | | | 9 | | 30 | | | |
| | G = 1000 | | | 80 | | 150 | | | |
| Overload recovery | 50% overdrive | | | 4 | | 4 | | μs | |
| POWER SUPPLY | | | | | | | | | |
| Voltage range | | | ±2.25 | ±15 | ±18 | ±2.25 | ±15 | ±18 | V |
| Current, total | V _{IN} = 0 V | | | ±0.7 | ±1 | | ±2 | | mA |
| TEMPERATURE RANGE | | | | | | | | | |
| Specification | | | -55 | | +125 | | | 210 | °C |
| Operating | | | -55 | | +125 | | | 210 | °C |

(3) Specified by wafer test.

(4) Temperature coefficient of the 49.4-kΩ term in the gain equation.

(5) Nonlinearity measurements in G = 1000 are dominated by noise. Typical nonlinearity is ±0.001%.



- (1) See the data sheet for absolute maximum and minimum recommended operating conditions.
- (2) The predicted operating lifetime vs. junction temperature is based on reliability modeling using electromigration as the dominant failure mechanism affecting device wearout for the specific device process and design characteristics.
- (3) Wirebond lifetime is only applicable for D package.

Figure 1. INA128HD, INA129SKGD1, and INA129SKGD2 Operating Life Derating Chart

7.7 Typical Characteristics

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

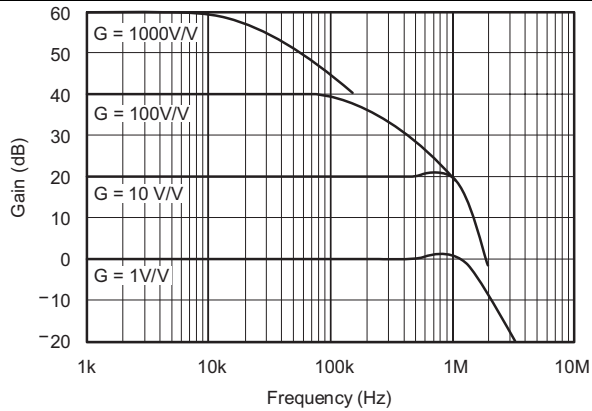


Figure 2. Gain vs Frequency

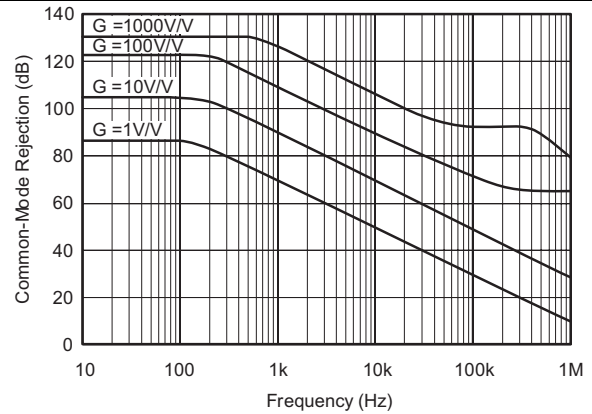


Figure 3. Common-Mode Rejection vs Frequency

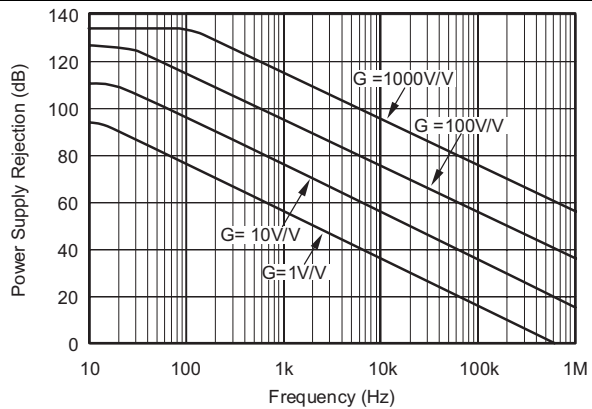


Figure 4. Positive Power-Supply Rejection vs Frequency

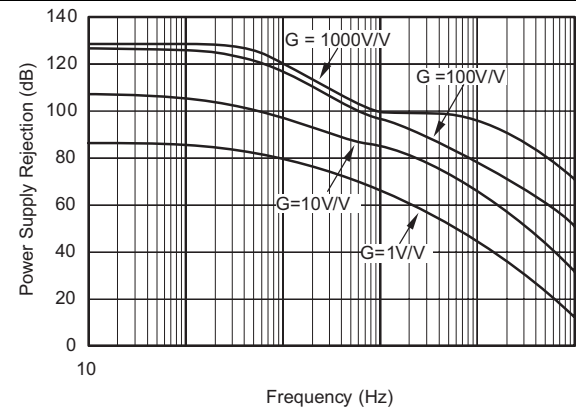


Figure 5. Negative Power-Supply Rejection vs Frequency

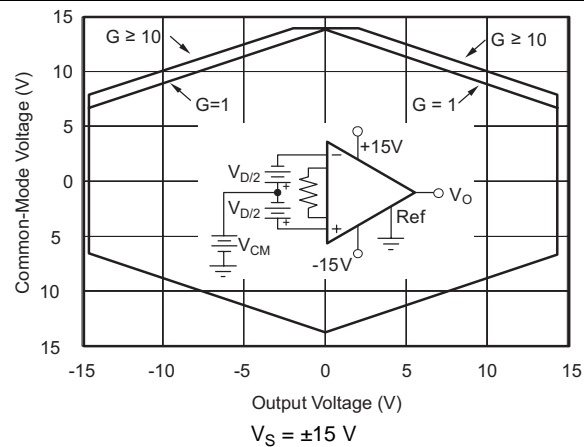


Figure 6. Input Common-Mode Range vs Output Voltage

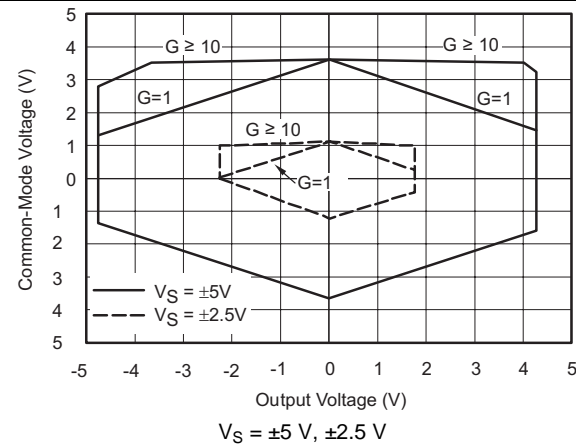


Figure 7. Input Common-Mode Range vs Output Voltage

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

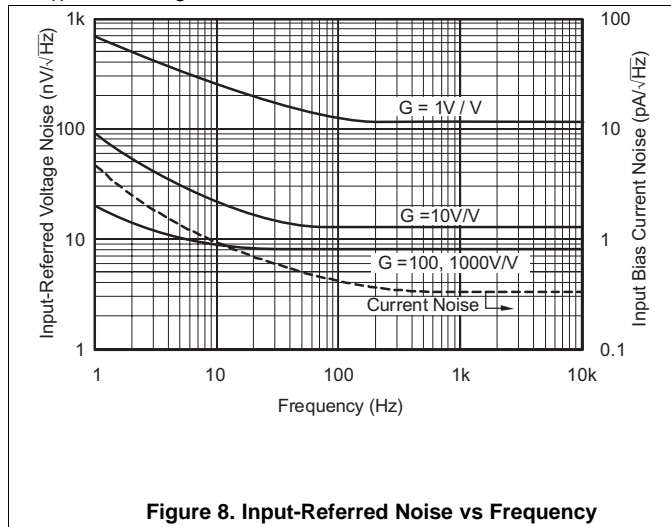


Figure 8. Input-Referred Noise vs Frequency

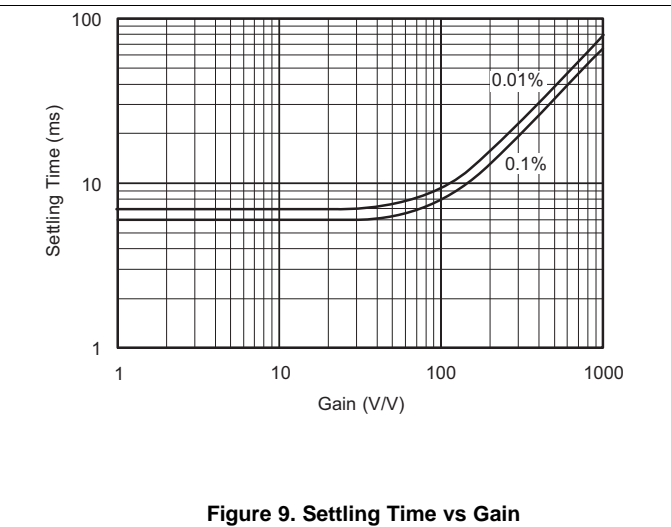


Figure 9. Settling Time vs Gain

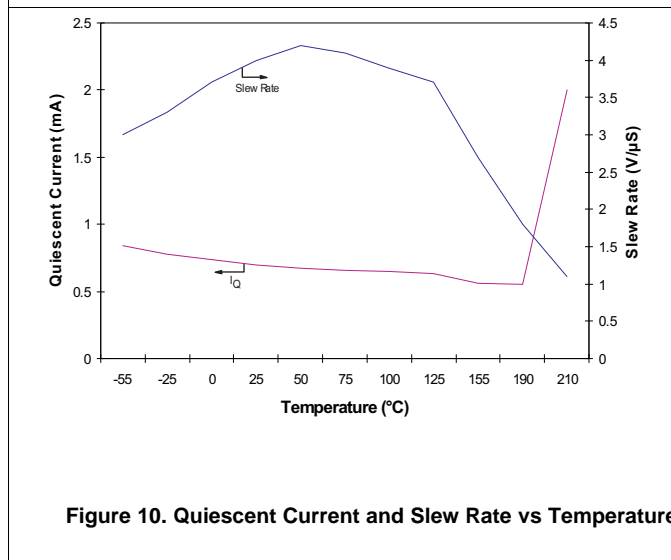


Figure 10. Quiescent Current and Slew Rate vs Temperature

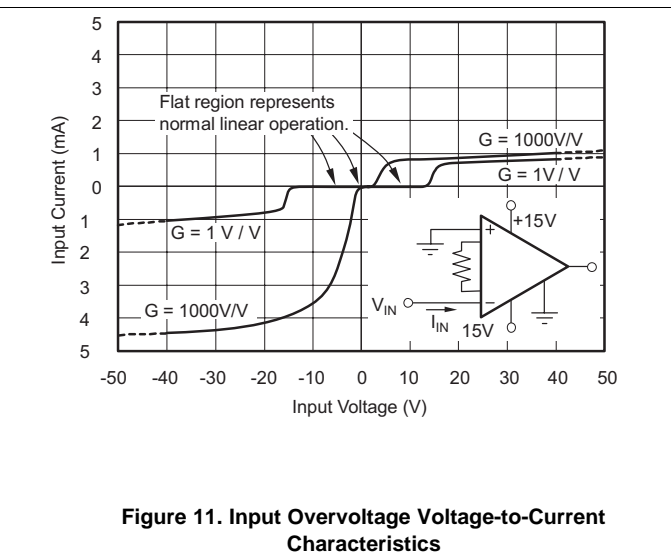


Figure 11. Input Overvoltage Voltage-to-Current Characteristics

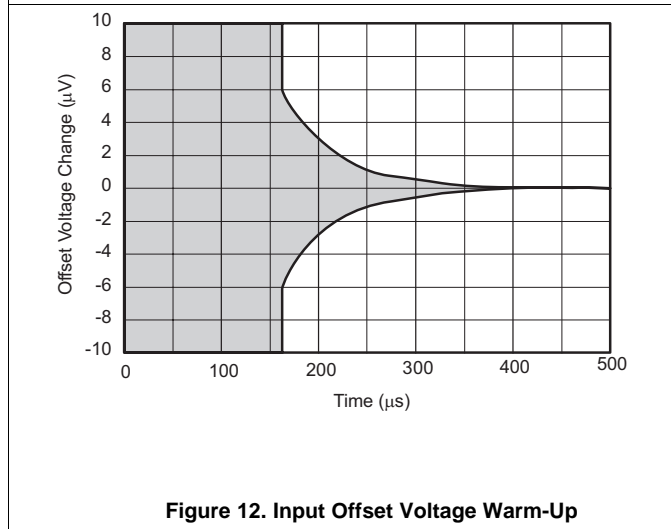


Figure 12. Input Offset Voltage Warm-Up

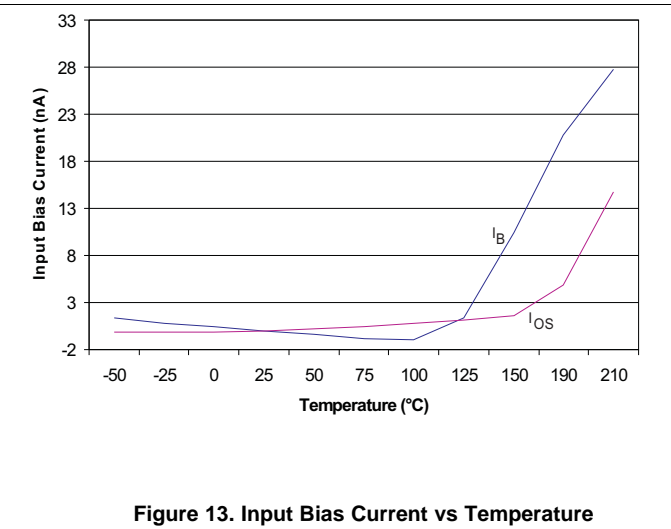


Figure 13. Input Bias Current vs Temperature

Typical Characteristics (continued)

At $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{ V}$, unless otherwise noted.

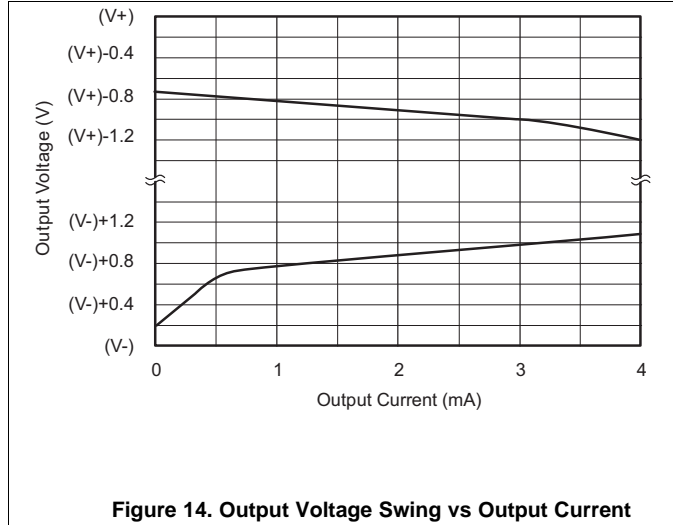


Figure 14. Output Voltage Swing vs Output Current

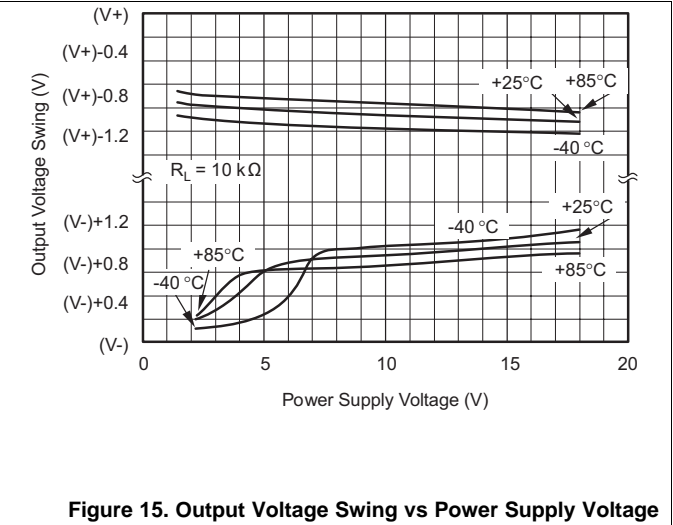


Figure 15. Output Voltage Swing vs Power Supply Voltage

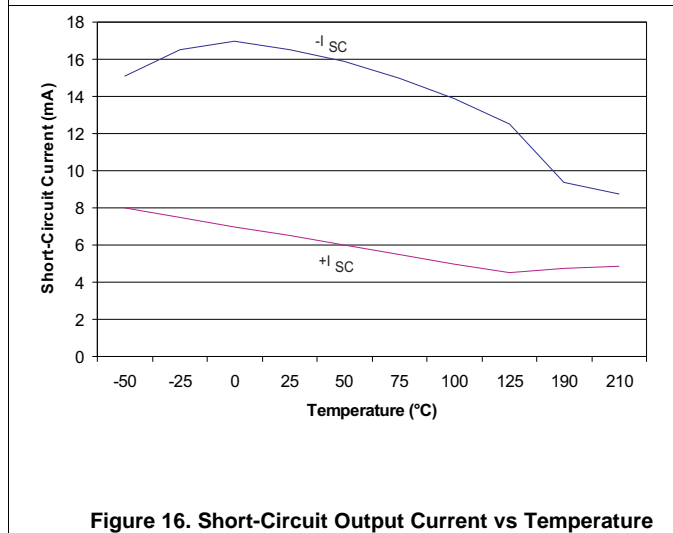


Figure 16. Short-Circuit Output Current vs Temperature

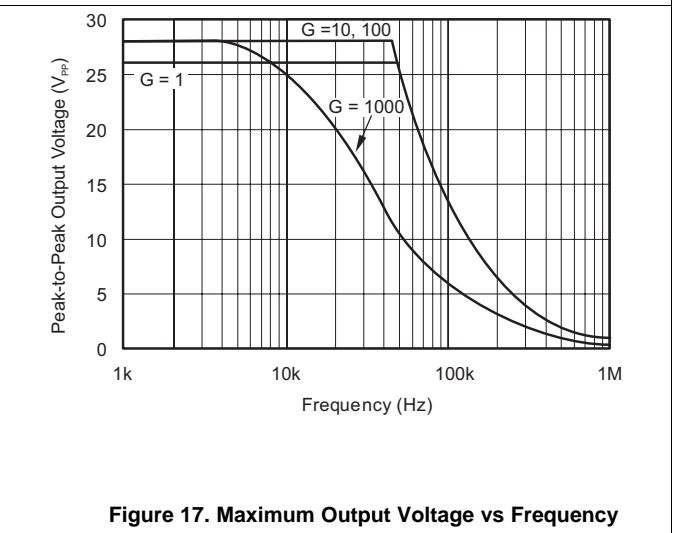


Figure 17. Maximum Output Voltage vs Frequency

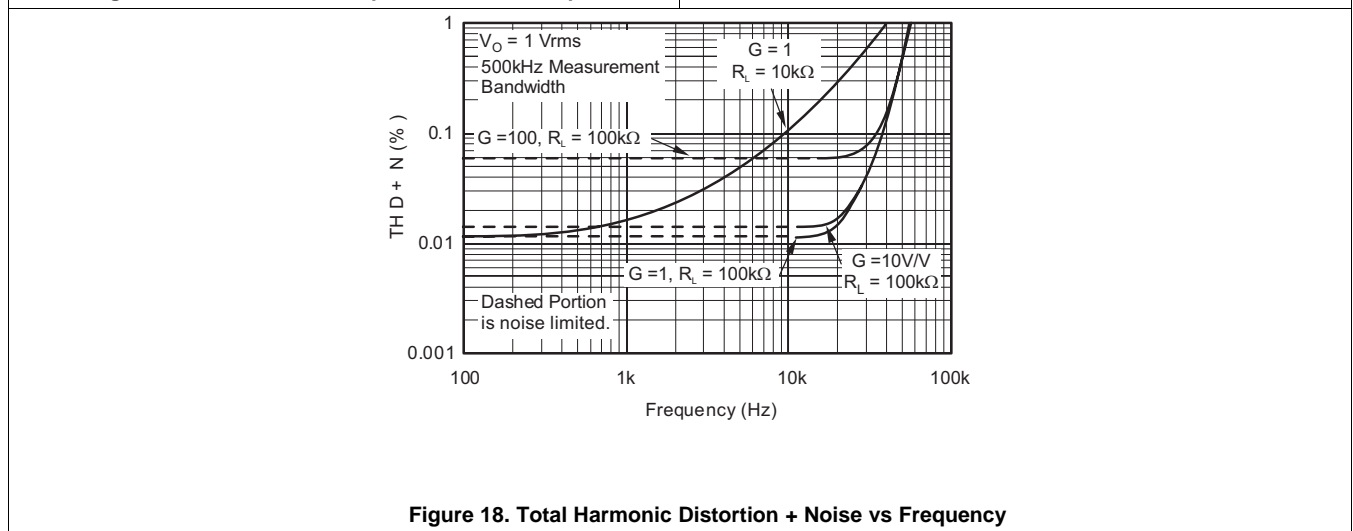


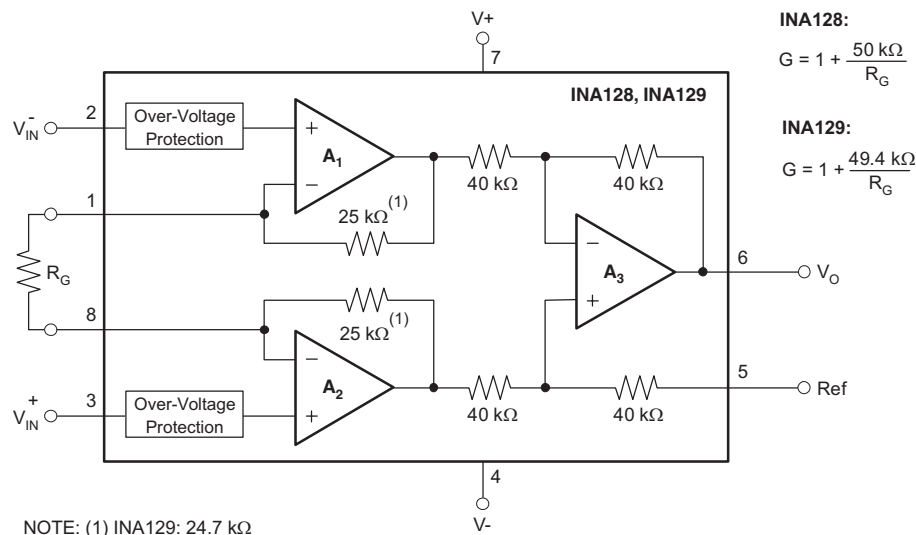
Figure 18. Total Harmonic Distortion + Noise vs Frequency

8 Detailed Description

8.1 Overview

The INA12x instrumentation amplifier is a type of differential amplifier that has been outfitted with input protection circuit and input buffer amplifiers, which eliminate the need for input impedance matching and make the amplifier particularly suitable for use in measurement and test equipment. Additional characteristics of the INA12x include a very low DC offset, low drift, low noise, very high open-loop gain, very high common-mode rejection ratio, and very high input impedances. The INA12x is used where great accuracy and stability of the circuit both short and long term are required.

8.2 Functional Block Diagram



8.3 Feature Description

The INA128-HT and INA129-HT are low power, general-purpose instrumentation amplifiers offering excellent accuracy. The versatile three-operational-amplifier design and small size make the amplifiers ideal for a wide range of applications. Current-feedback input circuitry provides wide bandwidth, even at high gain. A single external resistor sets any gain from 1 to 10,000. The INA128-HT and INA129-HT are laser trimmed for very low offset voltage (25 μV typical) and high common-mode rejection (93 dB at $G \geq 100$). These devices operate with power supplies as low as $\pm 2.25 \text{ V}$, and quiescent current of 2 mA, typically. The internal input protection can withstand up to $\pm 40 \text{ V}$ without damage.

8.4 Device Functional Modes

8.4.1 Noise Performance

The INA128-HT and INA129-HT provide very low noise in most applications. Low-frequency noise is approximately 2 μ VPP measured from 0.1 Hz to 10 Hz ($G \geq 100$). This provides dramatically improved noise when compared to state-of-the-art, chopper-stabilized amplifiers.

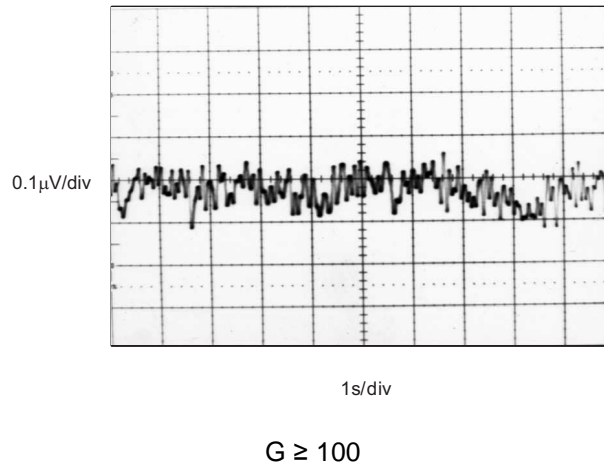


Figure 19. 0.1-Hz to 10-Hz Input-Referred Voltage Noise

8.4.2 Input Common-Mode Range

The linear input voltage ranges of the input circuitry of the INA128-HT and INA129-HT are from approximately 1.4 V below the positive supply voltage to 1.7 V above the negative supply. As a differential input voltage causes the output voltage increase, however, the linear input range will be limited by the output voltage swing of amplifiers A1 and A2. So the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage (see [Figure 6](#) and [Figure 7](#)).

Input-overload can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to their positive output swing limit, the difference voltage measured by the output amplifier will be near zero. The output of A3 will be near 0 V even though both inputs are overloaded.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The INA12x measures small differential voltage with high common-mode voltage developed between the non-inverting and inverting input. The high-input voltage protection circuit in conjunction with high input impedance make the INA12x suitable for a wide range of applications. The ability to set the reference pin to adjust the functionality of the output signal offers additional flexibility that is practical for multiple configurations.

9.2 Typical Application

Figure 20 shows the basic connections required for operation of the INA128-HT and INA129-HT. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) pin that is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 8 Ω in series with the Ref pin will cause a typical device to degrade.

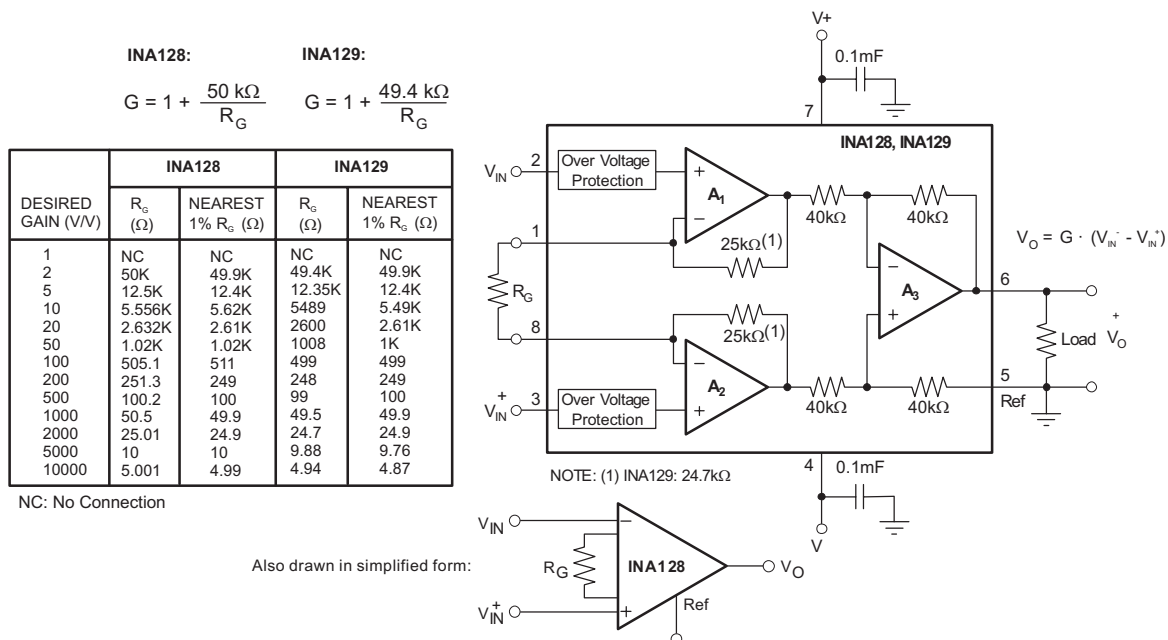


Figure 20. Basic Connections

9.2.1 Design Requirements

The device can be configured to monitor the input differential voltage when the gain of the input signal is set by the external resistor R_G. The output signal references to the Ref pin. The most common application is where the output is referenced to ground when no input signal is present by connecting the Ref pin to ground, as Figure 20 shows. When the input signal increases, the output voltage at the OUT pin increases, too.

Typical Application (continued)

9.2.2 Detailed Design Procedure

9.2.2.1 Setting the Gain

Gain is set by connecting a single external resistor, R_G , between pins 1 and 8.

INA128-HT:

$$G = 1 + \frac{50 \text{ k}\Omega}{R_G} \quad (1)$$

INA129-HT:

$$G = 1 + \frac{49.4 \text{ k}\Omega}{R_G} \quad (2)$$

Commonly used gains and resistor values are shown in [Figure 20](#).

The 50-k Ω term in [Equation 1](#) (49.4-k Ω in [Equation 2](#)) comes from the sum of the two internal feedback resistors of A1 and A2. These on-chip metal film resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these internal resistors are included in the gain accuracy and drift specifications of the INA128-HT and INA129-HT.

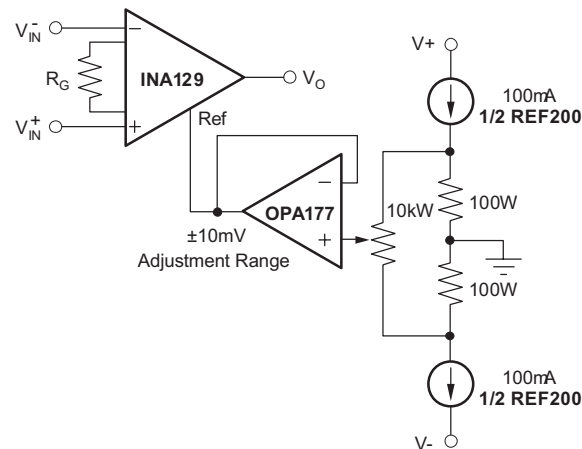
The stability and temperature drift of the external gain setting resistor, R_G , also affects gain. The R_G contribution to gain accuracy and drift can be directly inferred from [Equation 2](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

9.2.2.2 Dynamic Performance

[Figure 2](#) shows that, despite its low quiescent current, the INA128-HT and INA129-HT achieve wide bandwidth, even at high gain. This is due to the current-feedback topology of the input stage circuitry. Settling time also remains excellent at high gain.

9.2.2.3 Offset Trimming

The INA128-HT and INA129-HT are laser trimmed for low offset voltage and offset voltage drift. Most applications require no external offset adjustment. [Figure 21](#) shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed with the output. The operational amplifier buffer provides low impedance at the Ref terminal to preserve good common-mode rejection.



(1) [OPA177](#) and [REF200](#) are not tested or characterized at 210°C.

Figure 21. Optional Trimming of Output Offset Voltage

Typical Application (continued)

9.2.2.4 Input Bias Current Return Path

The input impedances of the INA128-HT and INA129-HT are extremely high (approximately $10^{10} \Omega$). However, a path must be provided for the input bias current of both inputs. This input bias current is approximately $\pm 50 \text{ nA}$. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. [Figure 22](#) shows various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential which exceeds the common-mode range, and the input amplifiers will saturate.

If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in [Figure 22](#)). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better high-frequency common-mode rejection.

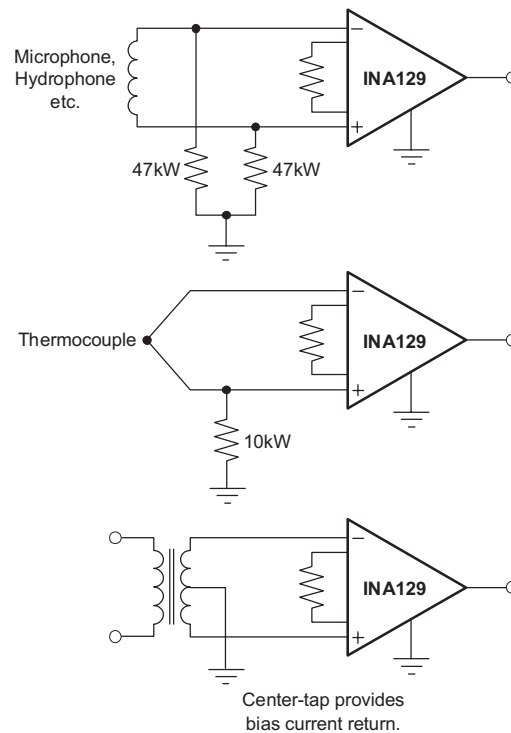


Figure 22. Providing an Input Common-Mode Current Path

Typical Application (continued)

9.2.3 Application Curves

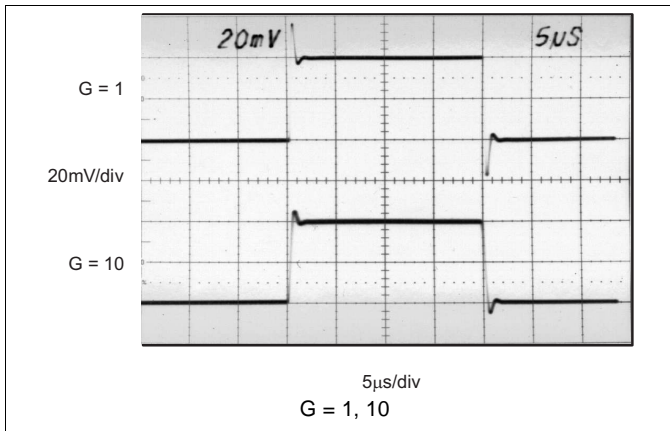


Figure 23. Small Signal

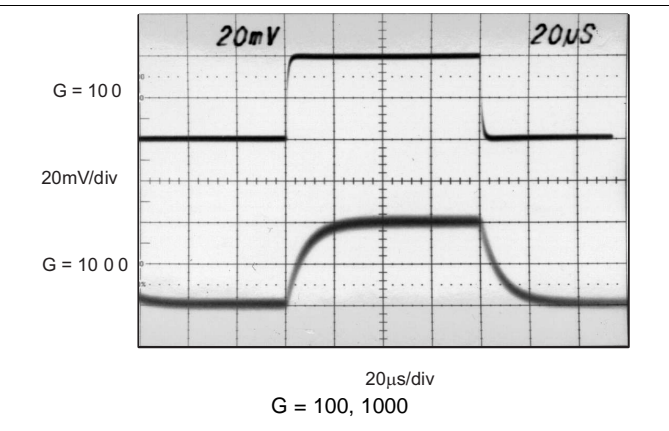


Figure 24. Small Signal

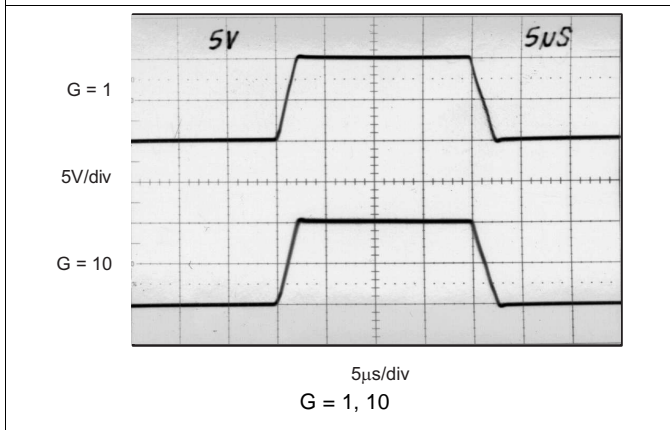


Figure 25. Large Signal

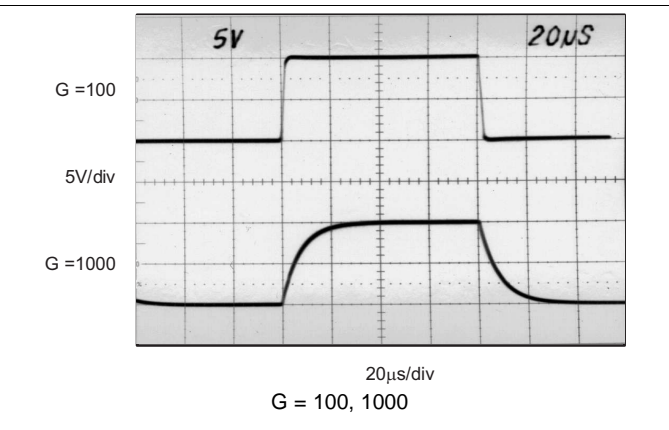


Figure 26. Large Signal

10 Power Supply Recommendations

The minimum power supply voltage for INA12x is ± 2.25 V and the maximum power supply voltage is ± 18 V. This minimum and maximum range covers a wide range of power supplies; but for optimum performance, ± 15 V is recommended. TI recommends adding a bypass capacitor at the input to compensate for the layout and power supply source impedance.

10.1 Low Voltage Operation

The INA128-HT and INA129-HT can be operated on power supplies as low as ± 2.25 V. Performance remains excellent with power supplies ranging from ± 2.25 V to ± 18 V. Most parameters vary only slightly throughout this supply voltage range.

Operation at very low supply voltage requires careful attention to assure that the input voltages remain within their linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power supply voltage. Figure 6 and Figure 7 show the range of linear operation for ± 15 V, ± 5 V, and ± 2.5 V supplies.

(1) OPA130 is not tested or characterized at 210°C.

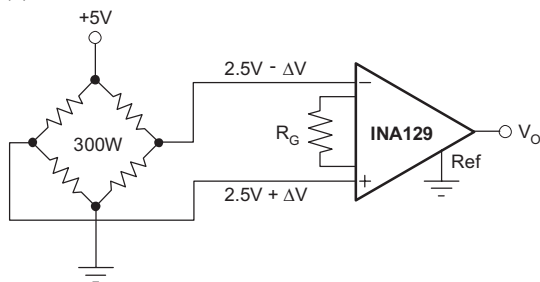


Figure 27. Bridge Amplifier

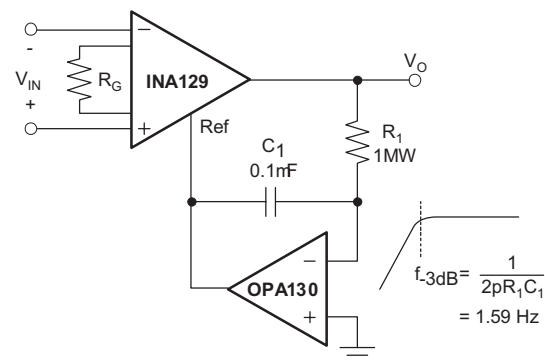
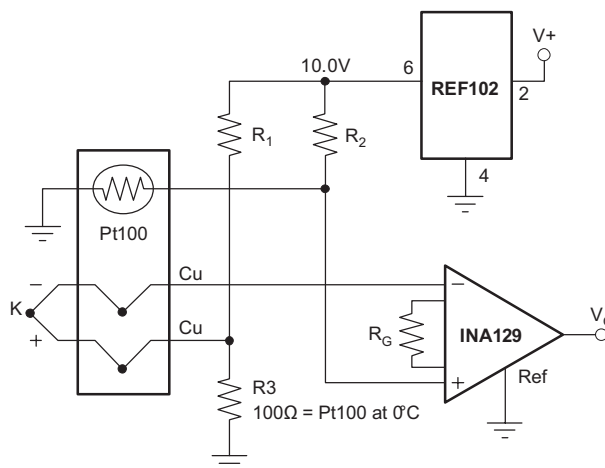


Figure 28. AC-Coupled Instrumentation Amplifier

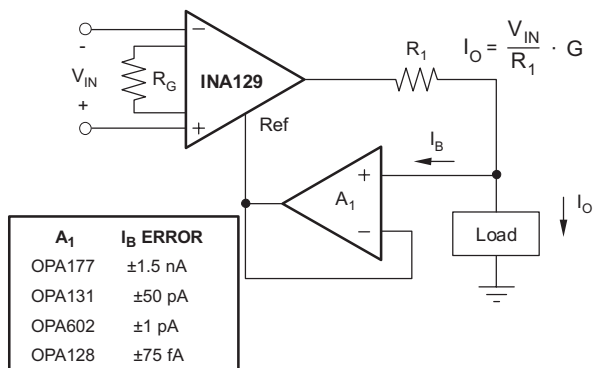


| ISA TYPE | MATERIAL | SEEBECK COEFFICIENT (mV/°C) | R ₁ , R ₂ |
|----------|-------------------------|-----------------------------|---------------------------------|
| E | +Chromel -Constantan | 58.5 | 66.5kW |
| J | +Iron -Constantan | 50.2 | 76.8kW |
| K | +Chromel -Alumel | 39.4 | 97.6kW |
| T | +Copper -Constantan | 38 | 102kW |

(1) REF102 is not tested or characterized at 210°C.

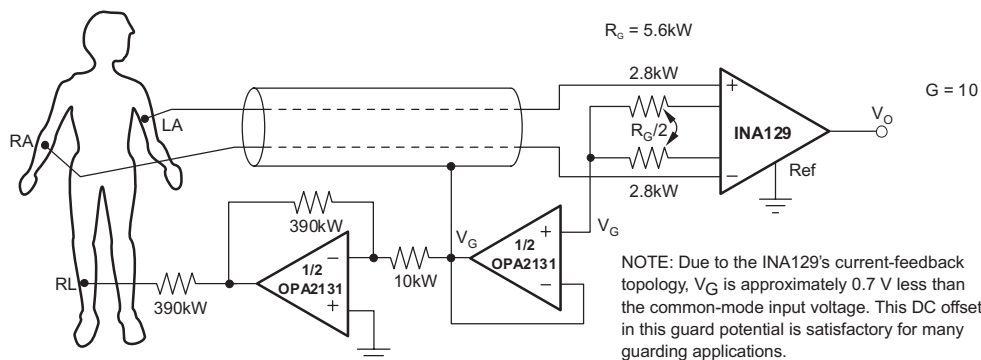
Figure 29. Thermocouple Amplifier With RTD Cold-Junction Compensation

Low Voltage Operation (continued)



(1) OPA177, OPA131, OPA602, and OPA128 are not tested or characterized at 210°C.

Figure 30. Differential Voltage-to-Current Converter



(1) OPA2131 is not tested or characterized at 210°C.

Figure 31. ECG Amplifier With Right-Leg Drive

11 Layout

11.1 Layout Guidelines

Place the power-supply bypass capacitor as closely as possible to the supply and ground pins. The recommended value of this bypass capacitor is 0.1 μF to 1 μF . If necessary, additional decoupling capacitance can be added to compensate for noisy or high-impedance power supplies. These decoupling capacitors must be placed between the power supply and INA12x device.

The gain resistor must be placed close to pin 1 and pin 8. This placement limits the layout loop and minimizes any noise coupling into the part.

11.2 Layout Example

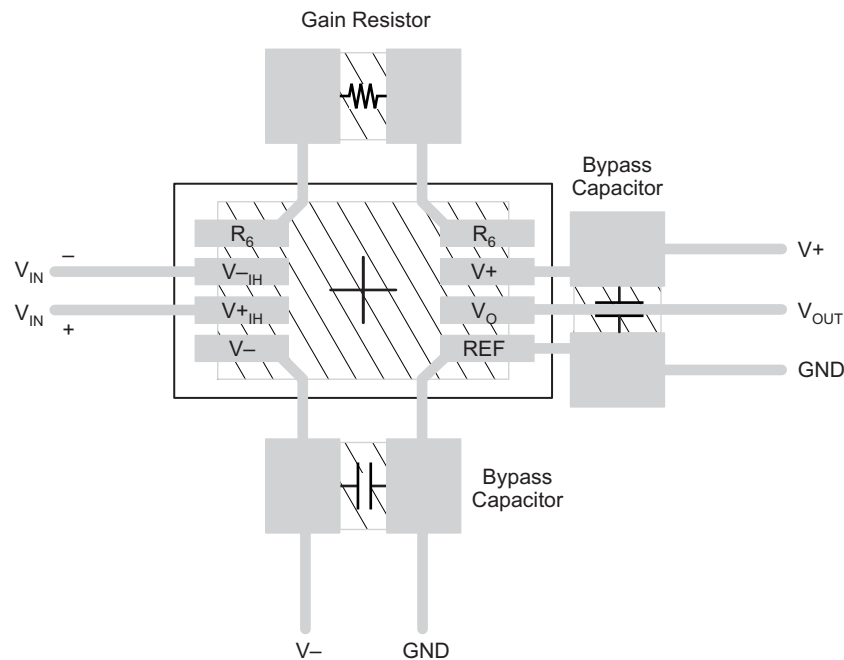


Figure 32. Recommended Layout

12 Device and Documentation Support

12.1 Device Support

12.1.1 Development Support

Table 1. Design Kits and Evaluation Modules

| NAME | PART NUMBER | TYPE |
|---|-----------------|-------------------------------|
| DIP Adapter Evaluation Module | DIP-ADAPTER-EVM | Evaluation Modules and Boards |
| Universal Instrumentation Amplifier Evaluation Module | INAEVM | Evaluation Modules and Boards |

Table 2. Development Tools

| NAME | PART NUMBER | TYPE |
|---|--------------|-------------------------------|
| Calculate Input Common-Mode Range of Instrumentation Amplifiers | INA-CMV-CALC | Calculation Tools |
| SPICE-Based Analog Simulation Program | TINA-TI | Circuit Design and Simulation |

12.2 Related Links

[Table 3](#) lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|-----------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| INA128-HT | Click here | Click here | Click here | Click here | Click here |
| INA129-HT | Click here | Click here | Click here | Click here | Click here |

12.3 Trademarks

All trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| INA128HD | ACTIVE | SOIC | D | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -55 to +175 | 128HD | Samples |
| INA129SHKJ | ACTIVE | CFP | HKJ | 8 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 210 | INA129S HKJ | Samples |
| INA129SHKQ | ACTIVE | CFP | HKQ | 8 | 1 | TBD | AU | N / A for Pkg Type | -55 to 210 | INA129S HKQ | Samples |
| INA129SJD | ACTIVE | CDIP SB | JDJ | 8 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 210 | INA129SJD | Samples |
| INA129SKGD1 | ACTIVE | XCEPT | KGD | 0 | 80 | Green (RoHS & no Sb/Br) | Call TI | N / A for Pkg Type | -55 to 210 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF INA128-HT, INA129-HT :

- Catalog: [INA128](#), [INA129](#)
- Enhanced Product: [INA129-EP](#)

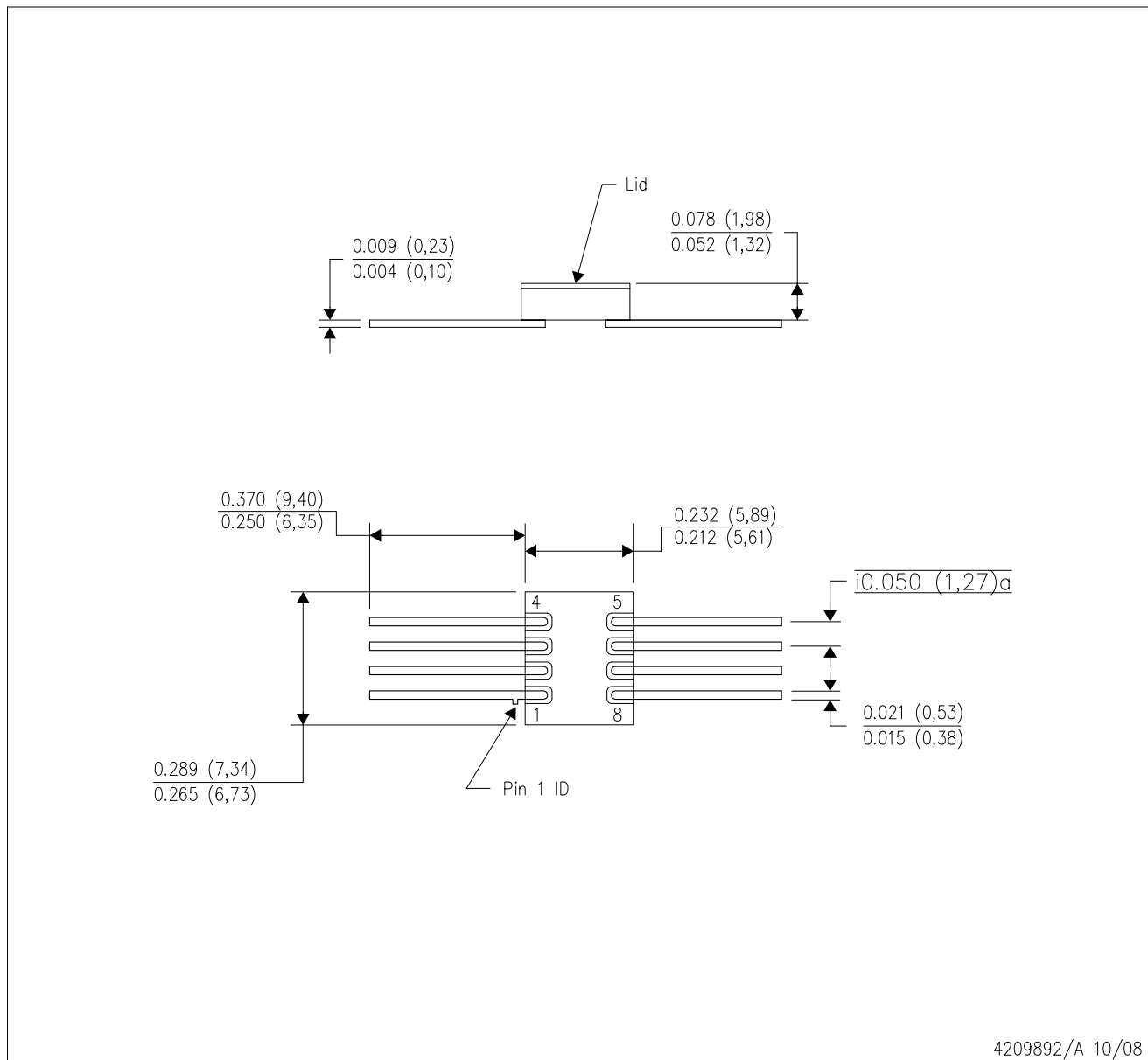
NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

MECHANICAL DATA

HKJ (R-CDFP-F8)

CERAMIC DUAL FLATPACK

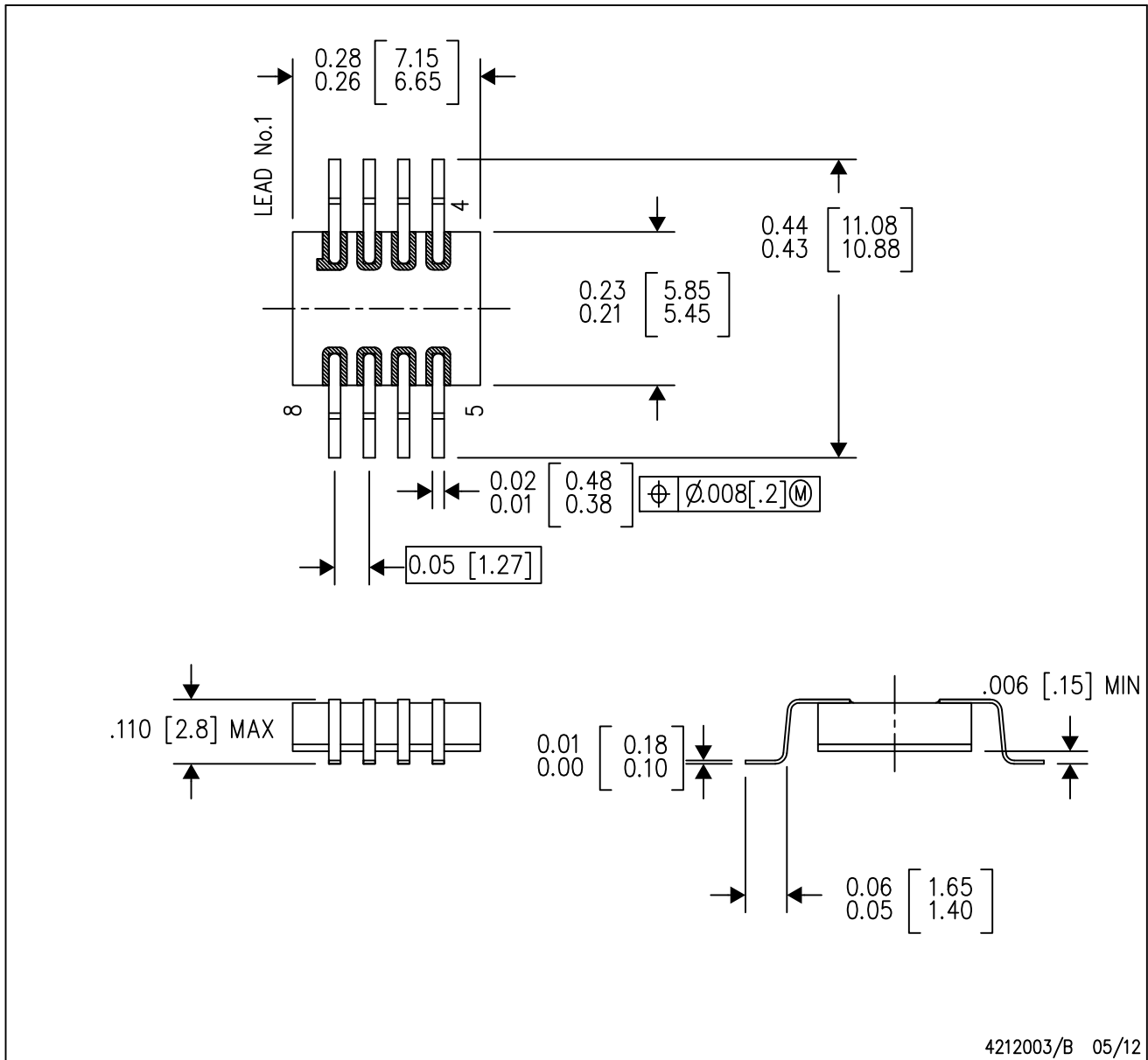


- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals will be gold plated.

MECHANICAL DATA

HKQ (R-CDFP-G8)

CERAMIC GULL WING



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package can be hermetically sealed with a metal lid.
 - The terminals will be gold plated.
 - Lid is not connected to any lead.



D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

- Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
- This dimension does not include interlead flash.
- Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
 EXPOSED METAL SHOWN
 SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

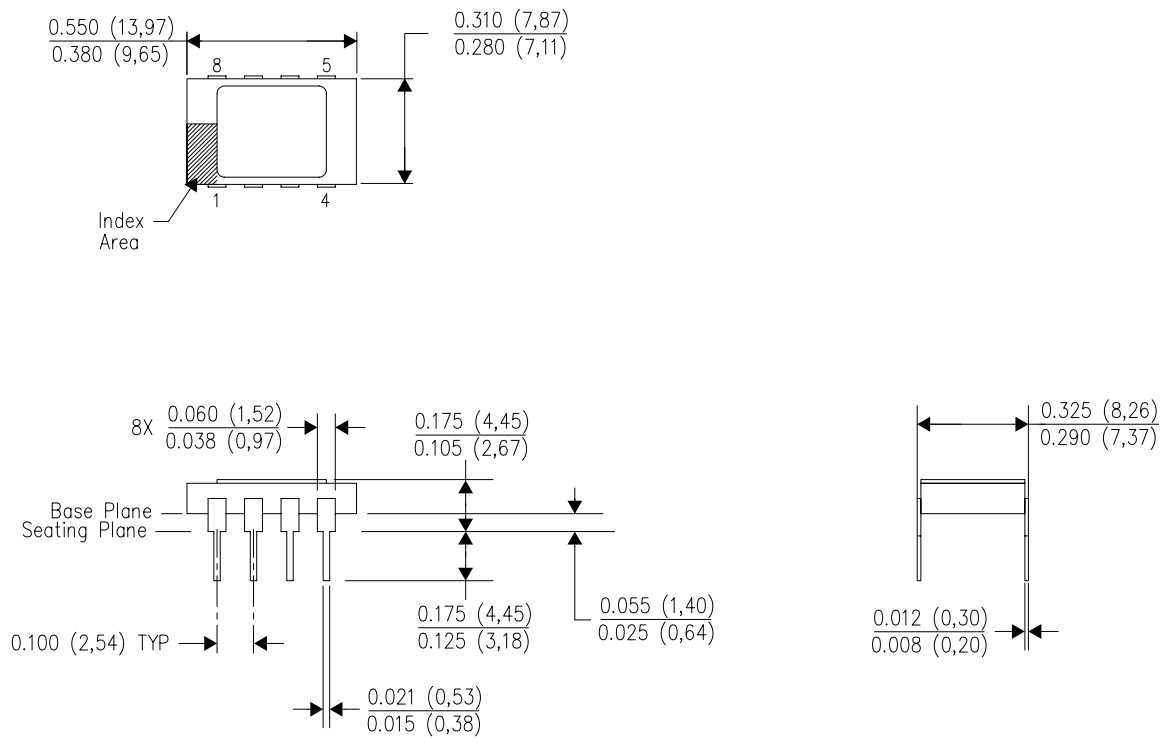
4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

JDJ (R-CDIP-T8)

CERAMIC DUAL IN-LINE PACKAGE



4202646-2/B 07/10

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Ceramic quad flatpack with flat leads brazed to non-conductive tie bar carrier.
 - This package is hermetically sealed with a metal lid.
 - The leads are gold plated and can be solderdipped.
 - Leads not shown for clarity purposes.
 - Lid and heat sink are connected to GND leads.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View INA129SHKJ](#) on WIN SOURCE

 [Texas Instruments](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management