

2SK4177

Electrical Characteristics at Ta=25°C

Parameter	Symbol	Conditions	Ratings			Unit	
			min	typ	max		
Drain-to-Source Breakdown Voltage	V(BR)DSS	I _D =1mA, V _{GS} =0V	1500			V	
Zero-Gate Voltage Drain Current	I _{DSS}	V _{DS} =1200V, V _{GS} =0V			100	μA	
Gate-to-Source Leakage Current	I _{GSS}	V _{GS} =±16V, V _{DS} =0V			±10	μA	
Cutoff Voltage	V _{GS(off)}	V _{DS} =10V, I _D =1mA	2.5		3.5	V	
Forward Transfer Admittance	y _{fs}	V _{DS} =20V, I _D =1A	0.7	1.4		S	
Static Drain-to-Source On-State Resistance	R _{DS(on)}	I _D =1A, V _{GS} =10V		10	13	Ω	
Input Capacitance	C _{iss}	V _{DS} =30V, f=1MHz		380		pF	
Output Capacitance	C _{oss}				70		pF
Reverse Transfer Capacitance	C _{rss}				40		pF
Turn-ON Delay Time	t _{d(on)}	See Fig.2		12		ns	
Rise Time	t _r			37		ns	
Turn-OFF Delay Time	t _{d(off)}			152		ns	
Fall Time	t _f			59		ns	
Total Gate Charge	Q _g	V _{DS} =200V, V _{GS} =10V, I _D =2A		37.5		nC	
Gate-to-Source Charge	Q _{gs}			2.7		nC	
Gate-to-Drain "Miller" Charge	Q _{gd}			20		nC	
Diode Forward Voltage	V _{SD}	I _S =2A, V _{GS} =0V		0.88	1.2	V	

Fig.1 Unclamped Inductive Switching Test Circuit

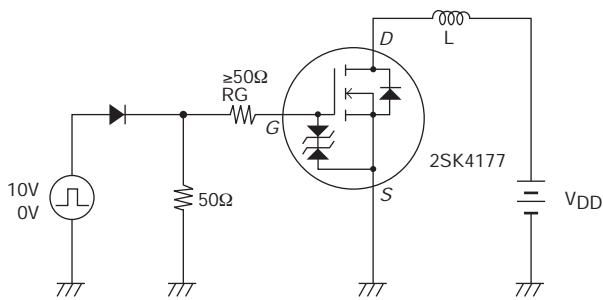
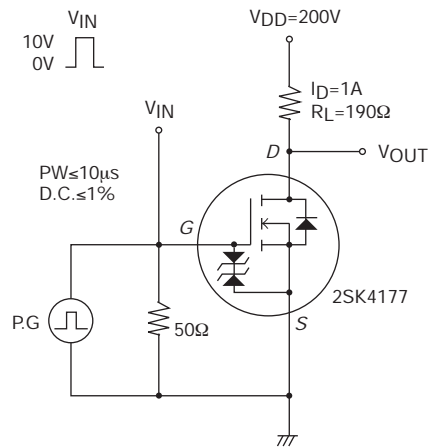
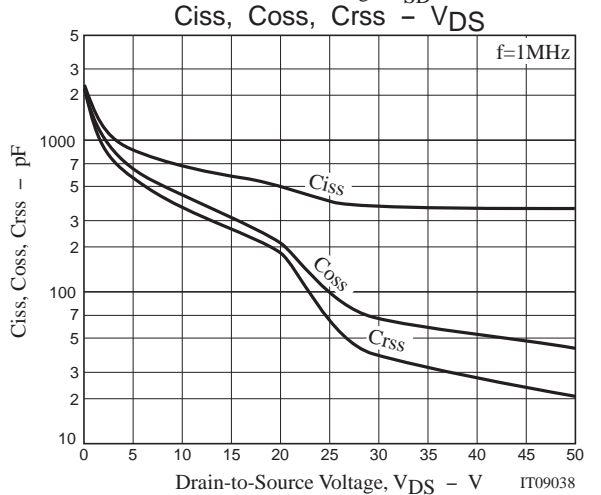
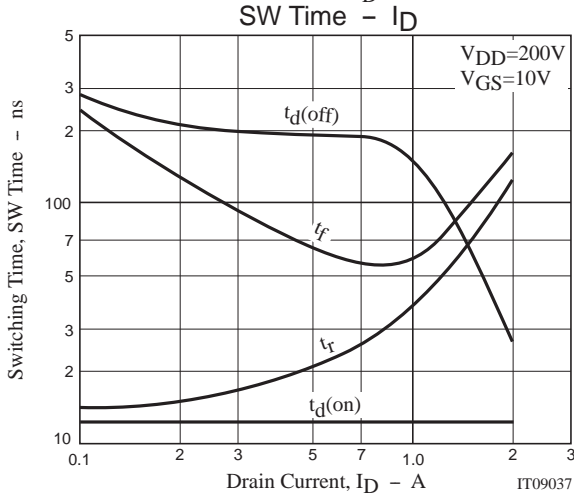
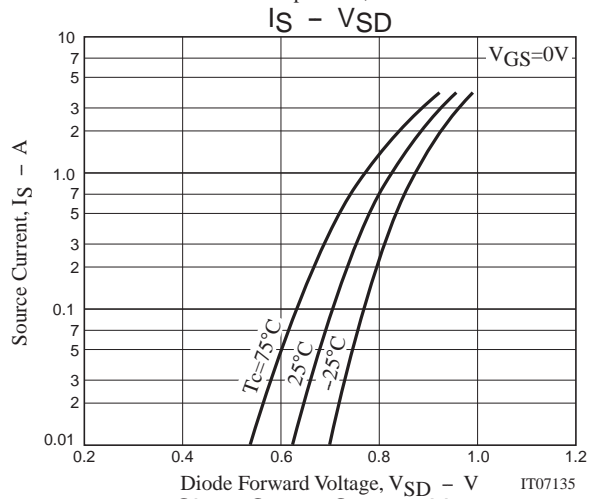
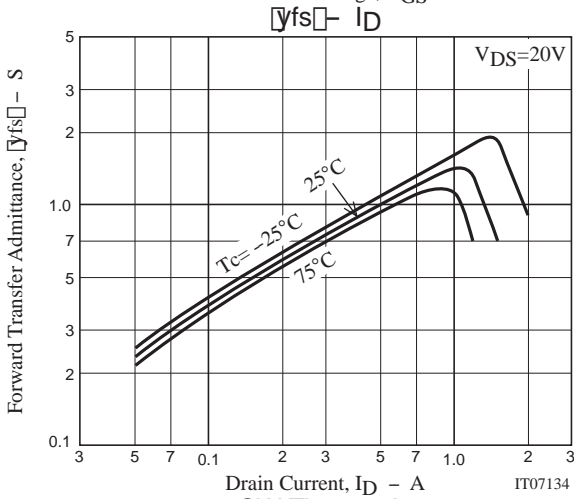
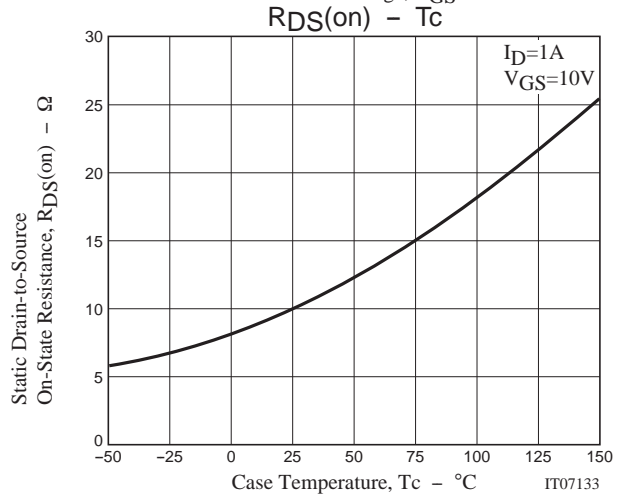
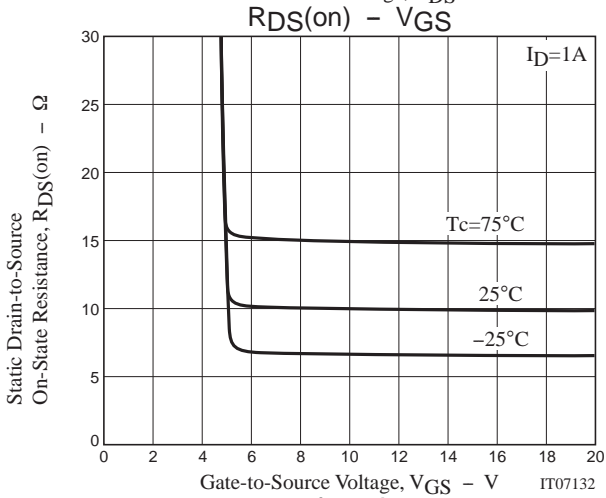
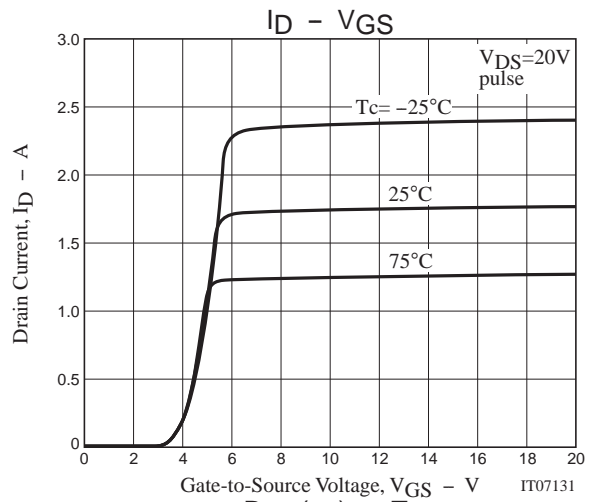
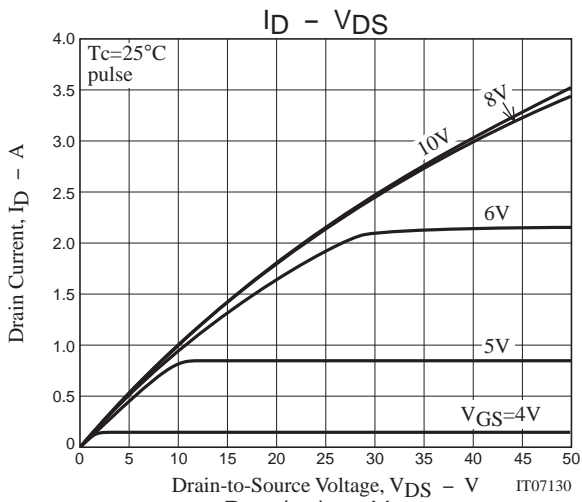


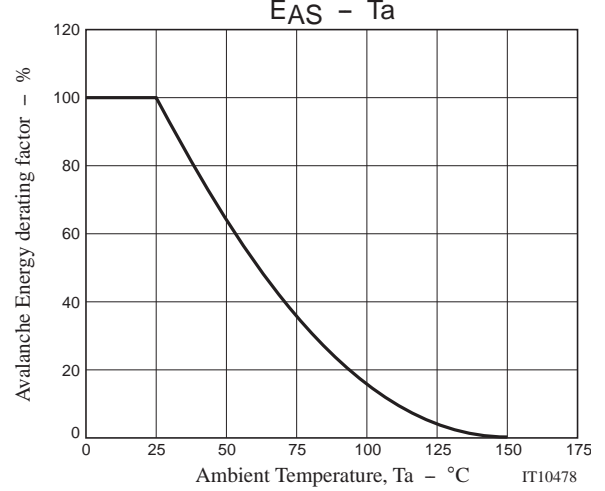
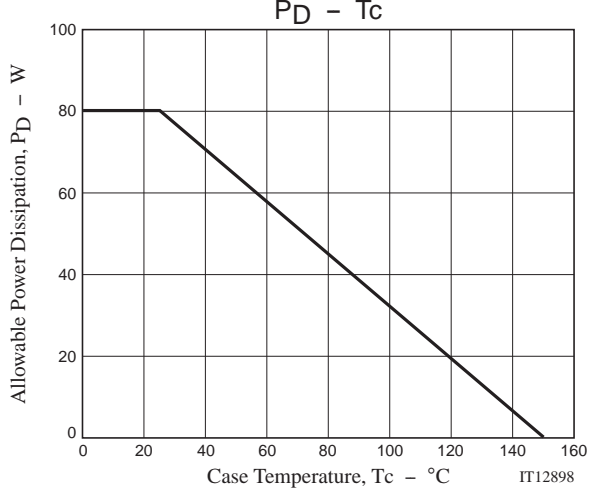
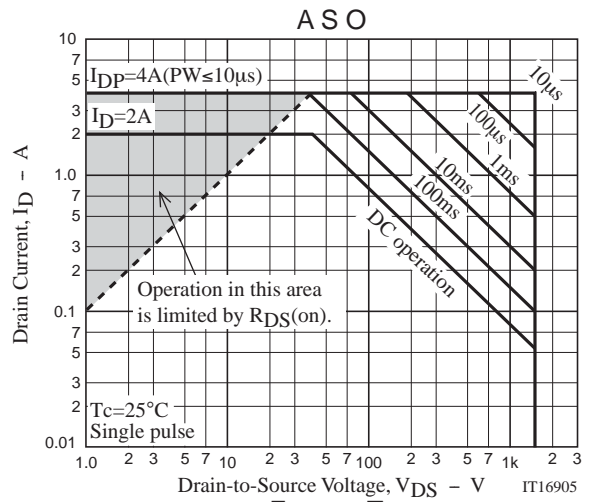
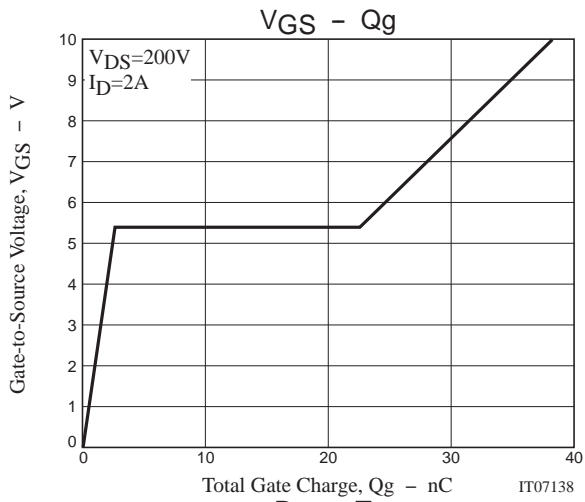
Fig.2 Switching Time Test Circuit



Ordering Information

Device	Package	Shipping	memo
2SK4177-DL-1E	TO-263-2L	800pcs./reel	Pb Free





Taping Specification

2SK4177-DL-1E

1. Packing Format

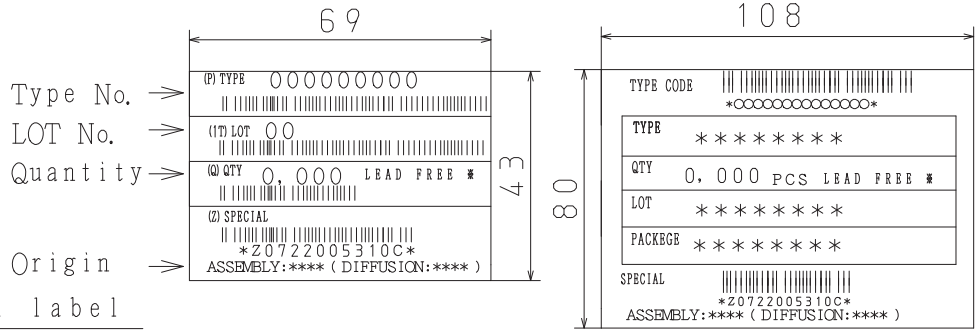
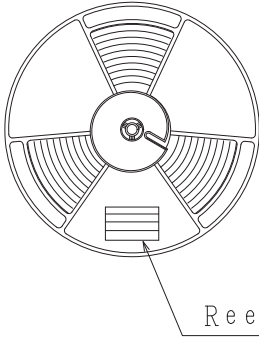
Package Name	Maximum Number of devices contained (pcs)			Packing format	
	Reel	Inner box	Outer box	Inner BOX	Outer BOX
TO-263-2L	800	1600	6400	SPD-0V0011 2 reel contained Dimensions:mm (external) 351×340×68	SPD-0V0009 4 inner boxes contained Dimensions:mm (external) 390×370×318

Reel label, Inner box label
(unit:mm)

Outer box label

Packing method

It is a label at the time of factory shipments.
The form of a label may change in physical distribution process.



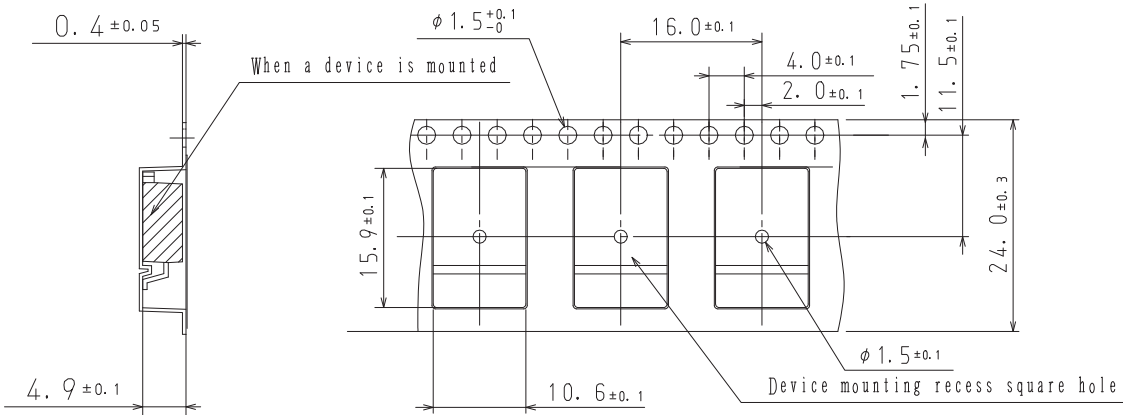
NOTE (1)

The LEAD FREE * description shows that the surface treatment of the terminal is lead free.

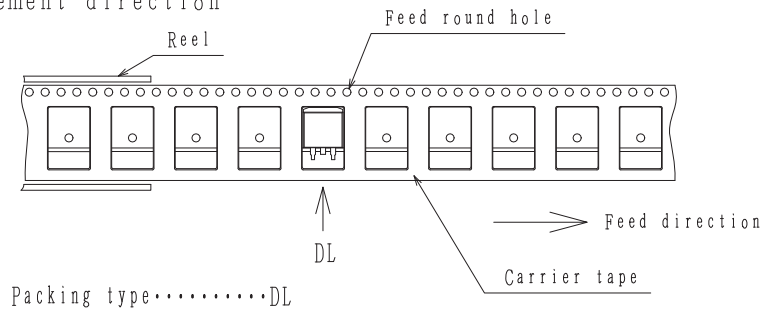
Label	JEITA Phase
LEAD FREE 3	JEITA Phase 3A

2. Taping configuration

2-1. Carrier tape size (unit:mm)



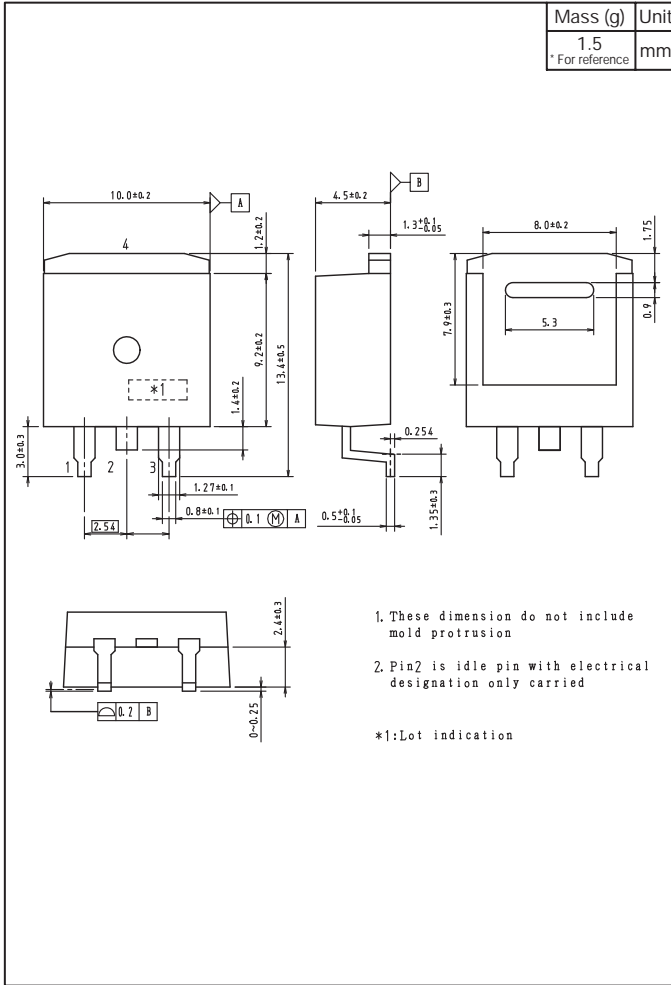
2-2. Device placement direction



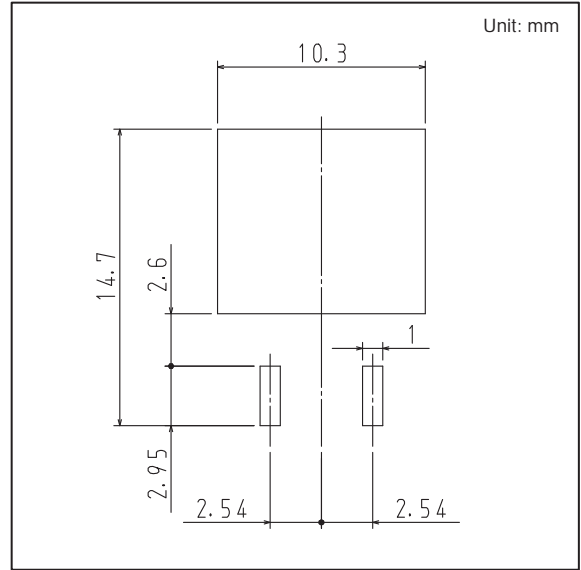
2SK4177

Outline Drawing

2SK4177-DL-1E



Land Pattern Example





Note on usage : Since the 2SK4177 is a MOSFET product, please avoid using this device in the vicinity of highly charged objects.

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