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FDBL0240N100

N-Channel PowerTrench[®] MOSFET

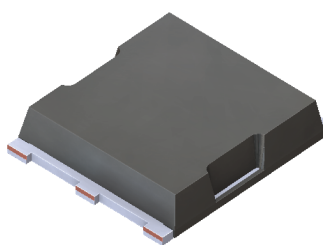
100 V, 210 A, 2.8 mΩ

Features

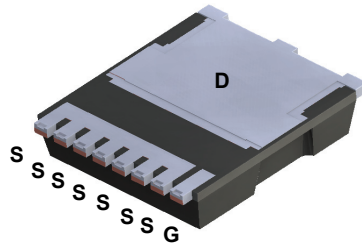
- Max $R_{DS(on)}$ = 2.8 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- Max $Q_{g(tot)}$ = 111 nC at $V_{GS} = 10\text{ V}$, $I_D = 80\text{ A}$
- UIS Capability
- RoHS Compliant

Applications

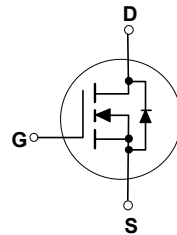
- Industrial Motor Drive
- Industrial Power Supply
- Industrial Automation
- Battery Operated tools
- Battery Protection
- Solar Inverters
- UPS and Energy Inverters
- Energy Storage
- Load Switch



TOP



BOTTOM



MO-299A

MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Conditions	Rated Value	Units
V_{DS}	Drain to Source Voltage		100	V
V_{GS}	Gate to Source Voltage		±20	V
I_D	Drain Current	-Continuous $T_C = 25^\circ\text{C}$ (Note 5)	210	A
		-Continuous $T_C = 100^\circ\text{C}$ (Note 5)	150	
		-Pulsed (Note 4)	910	
E_{AS}	Single Pulse Avalanche Energy	(Note 3)	821	mJ
P_D	Power Dissipation	$T_C = 25^\circ\text{C}$	300	W
	Power Dissipation	$T_A = 25^\circ\text{C}$ (Note 1a)	3.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +175	$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	(Note 1)	0.5	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	43	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL0240N100	FDBL0240N100	MO-299A	-	-	-

FDBL0240N100 N-Channel PowerTrench[®] MOSFET

Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	100			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		58		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80\ \text{V}, V_{GS} = 0\ \text{V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\ \text{V}, V_{DS} = 0\ \text{V}$			± 100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	2	2.9	4	V
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 80\ \text{A}$		2.2	2.8	m Ω
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, referenced to $25\text{ }^\circ\text{C}$		-13		mV/ $^\circ\text{C}$
g_{FS}	Forward Transconductance	$V_{DS} = 10\ \text{V}, I_D = 80\ \text{A}$		162		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 50\ \text{V}, V_{GS} = 0\ \text{V},$ $f = 1\ \text{MHz}$		5835	8755	pF
C_{oss}	Output Capacitance			1235	1855	pF
C_{rss}	Reverse Transfer Capacitance			41	65	pF
R_g	Gate Resistance	$V_{GS} = 0.5\ \text{V}, f = 1\ \text{MHz}$		2.5		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\ \text{V}, I_D = 80\ \text{A},$ $V_{GS} = 10\ \text{V}, R_{GEN} = 6\ \Omega$		26	42	ns
t_r	Rise Time			32	51	ns
$t_{d(off)}$	Turn-Off Delay Time			44	70	ns
t_f	Fall Time			17	30	ns
$Q_{g(TOT)}$	Total Gate Charge	$V_{GS} = 0\ \text{to}\ 10\ \text{V}$	$V_{DD} = 50\ \text{V},$ $I_D = 80\ \text{A}$	79	111	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0\ \text{to}\ 2\ \text{V}$		11	15	nC
Q_{gs}	Gate to Source Gate Charge			27		nC
Q_{gd}	Gate to Drain "Miller" Charge			16		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	210	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	910	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_S = 80\ \text{A}$ (Note 2)		0.8	1.3	V
		$V_{GS} = 0\ \text{V}, I_S = 40\ \text{A}$ (Note 2)		0.8	1.2	
t_{rr}	Reverse Recovery Time	$I_F = 80\ \text{A}, di/dt = 100\ \text{A}/\mu\text{s}$		82	131	ns
Q_{rr}	Reverse Recovery Charge			151	242	nC

Notes:

1. $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) $43\text{ }^\circ\text{C}/\text{W}$ when mounted on a $1\ \text{in}^2$ pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs , Duty cycle < 2.0 %.

3. E_{AS} of 821 mJ is based on starting $T_J = 25\text{ }^\circ\text{C}$, $L = 0.3\ \text{mH}$, $I_{AS} = 74\ \text{A}$, $V_{DD} = 90\ \text{V}$, $V_{GS} = 10\ \text{V}$. 100% test at $L = 0.1\ \text{mH}$, $I_{AS} = 106\ \text{A}$.

4. Pulsed I_D please refer to Figure "Forward Bias Safe Operating Area" for more details.

5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

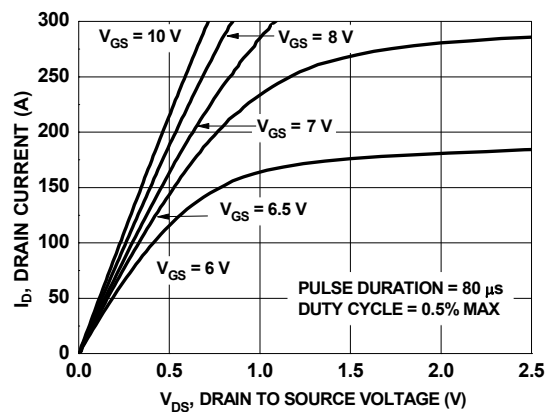


Figure 1. On Region Characteristics

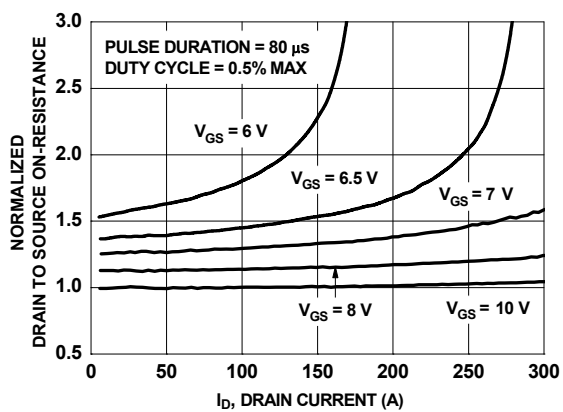


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

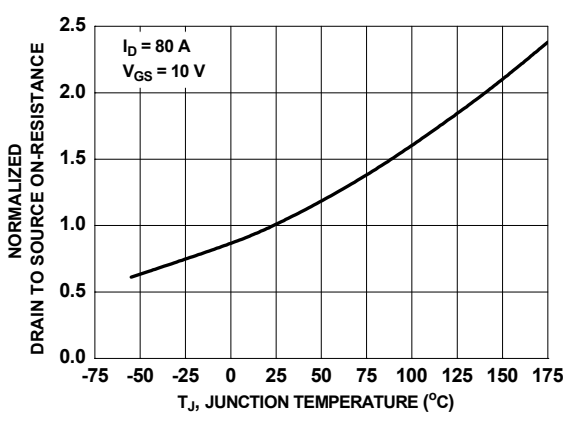


Figure 3. Normalized On Resistance vs. Junction Temperature

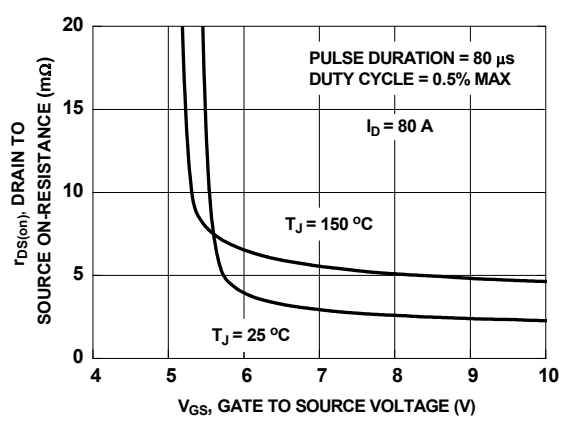


Figure 4. On-Resistance vs. Gate to Source Voltage

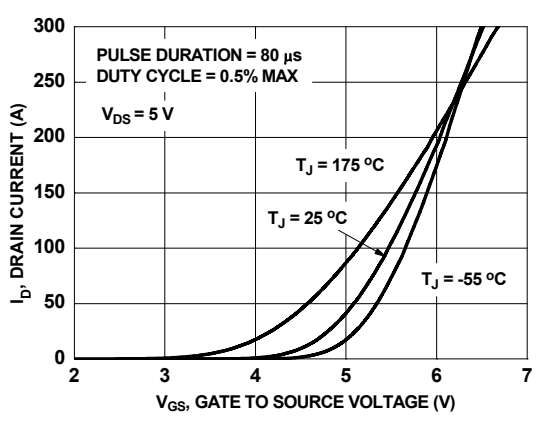


Figure 5. Transfer Characteristics

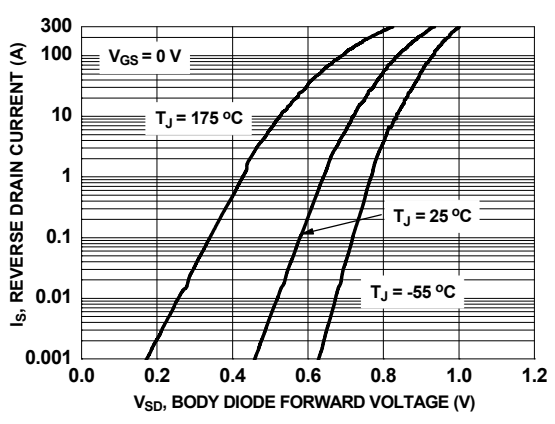


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted.

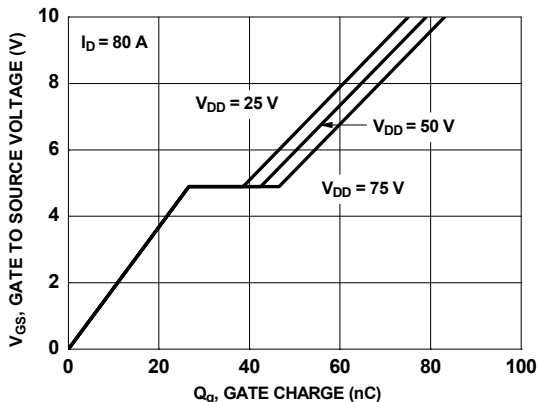


Figure 7. Gate Charge Characteristics

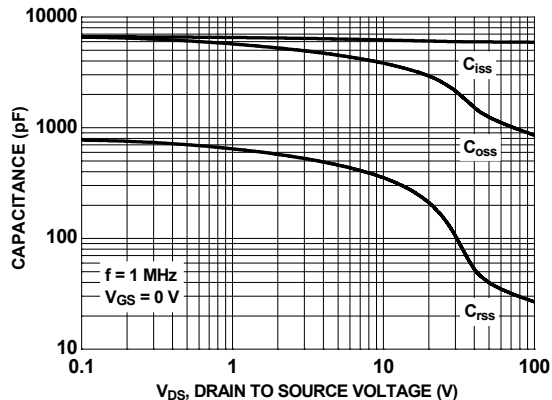


Figure 8. Capacitance vs. Drain to Source Voltage

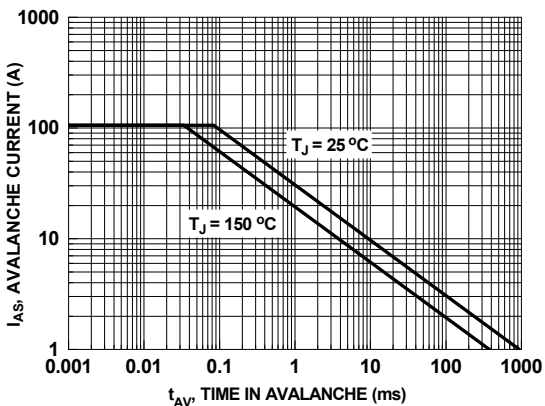


Figure 9. Unclamped Inductive Switching Capability

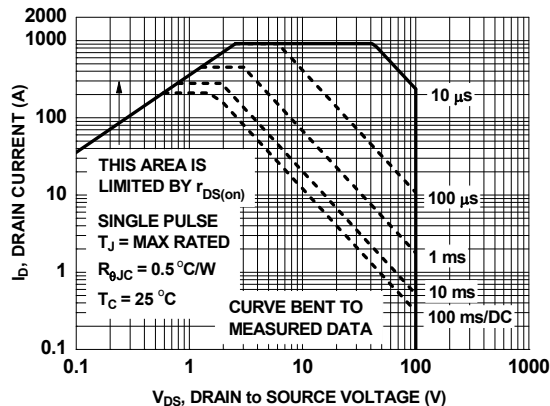


Figure 10. Forward Bias Safe Operating Area

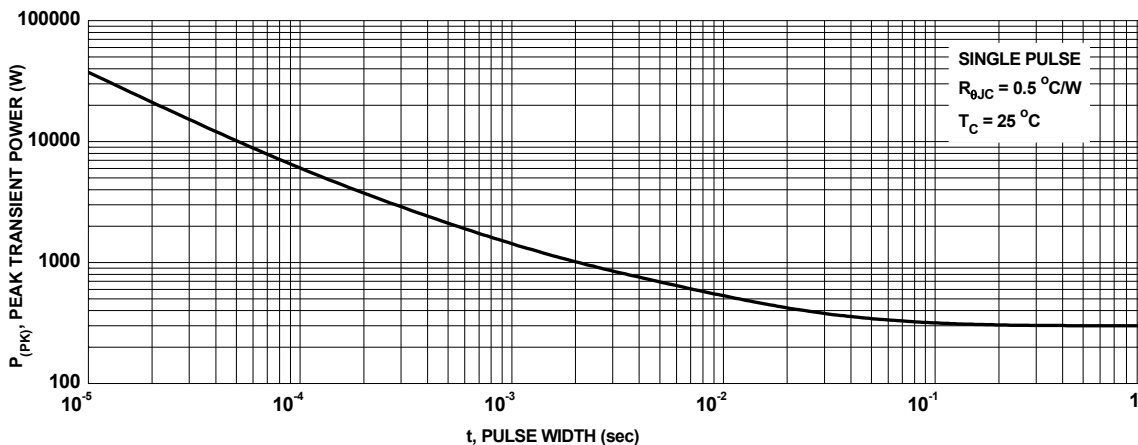


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

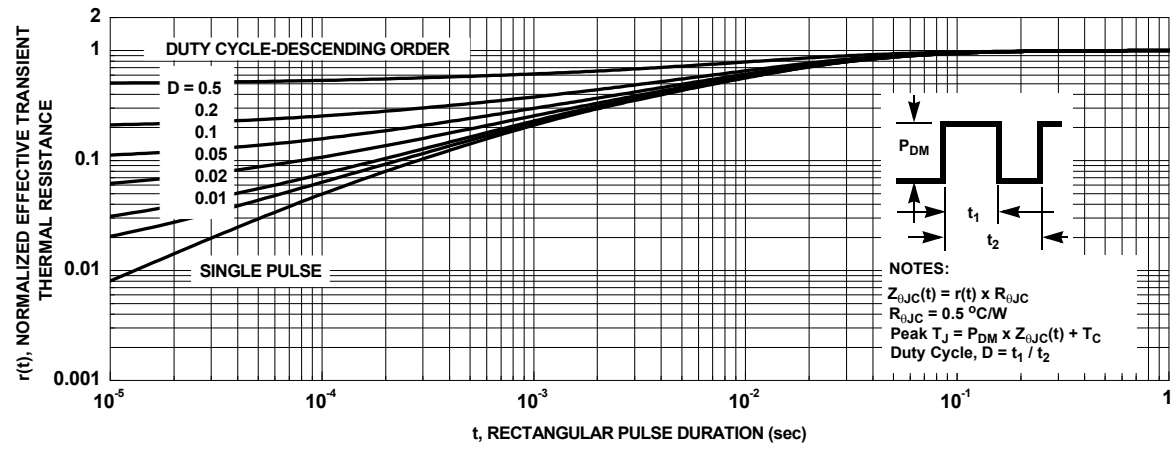
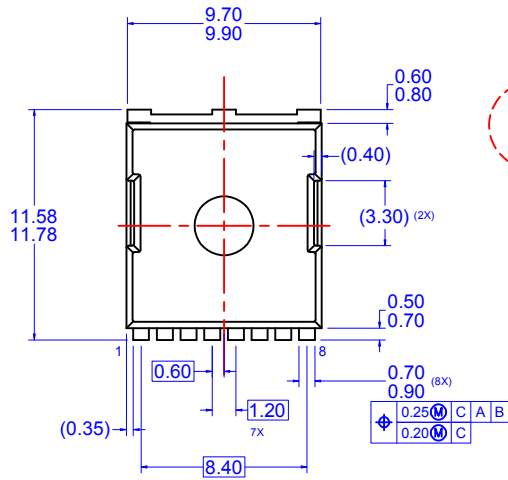
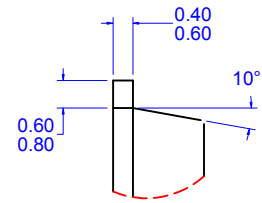
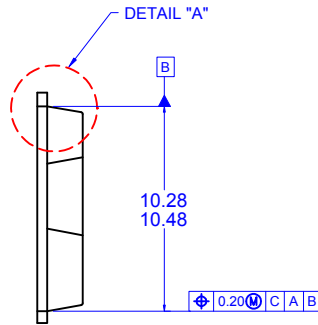


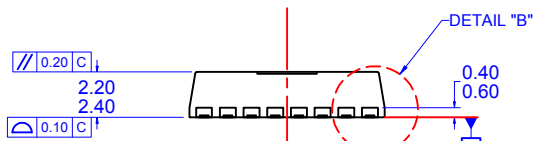
Figure 12. Junction-to-Case Transient Thermal Response Curve



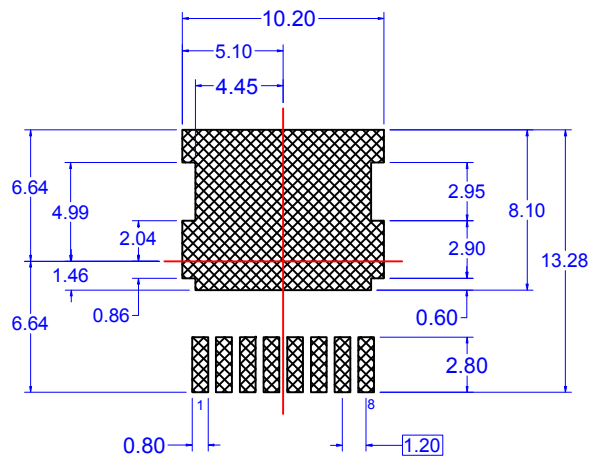
TOP VIEW



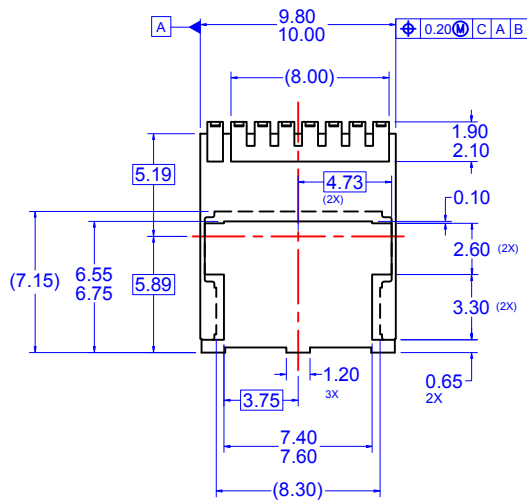
DETAIL "A"



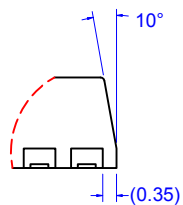
SIDE VIEW



LAND PATTERN RECOMMENDATION



BOTTOM VIEW



DETAIL "B"

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- A) PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE A, DATED NOVEMBER 2009.
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
 - D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
 - E) DRAWING FILE NAME: MKT-PSOF08AREV3

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