



**THE DATASHEET OF
74ALVC162245TX**



74ALVC162245

Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in A Port Outputs

General Description

The ALVC162245 contains sixteen non-inverting bidirectional buffers with 3-STATE outputs and is intended for bus oriented applications. The device is byte controlled. Each byte has separate 3-STATE control inputs which can be shorted together for full 16-bit operation. The T/R inputs determine the direction of data flow through the device. The OE inputs disable both the A and B Ports by placing them in a high impedance state.

The 74ALVC162245 is designed for low voltage (1.65V to 3.6V) V_{CC} applications with I/O compatibility up to 3.6V.

The 74ALVC162245 is also designed with 26Ω series resistance in the A Port outputs. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The 74ALVC162245 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

Features

- 1.65V–3.6V V_{CC} supply operation
- 3.6V tolerant inputs and outputs
- 26Ω series resistors in A Port outputs
- t_{PD}
 - 3.9 ns max for 3.0V to 3.6V V_{CC}
 - 4.8 ns max for 2.3V to 2.7V V_{CC}
 - 8.6 ns max for 1.65V to 1.95V V_{CC}
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
 - Human body model > 2000V
 - Machine model >200V

Note 1: To ensure the high-impedance state during power up or power down, OE should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

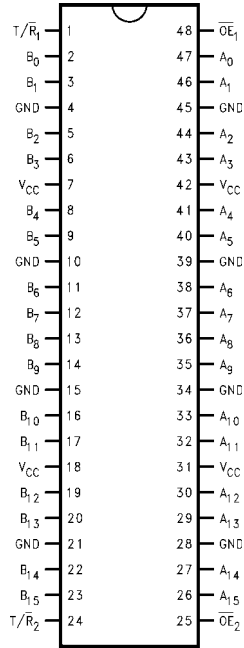
Ordering Code:

Order Number	Package Number	Package Description
74ALVC162245T	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

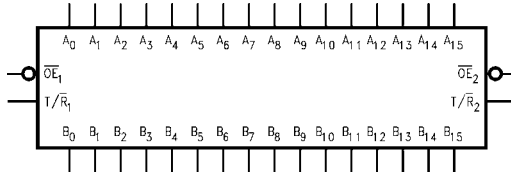
Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

74ALVC162245 Low Voltage 16-Bit Bidirectional Transceiver with 3.6V Tolerant Inputs and Outputs and 26Ω Series Resistors in A Port Outputs

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
T/\overline{R}_n	Transmit/Receive Input
A_0-A_{15}	Side A Inputs or 3-STATE Outputs
B_0-B_{15}	Side B Inputs or 3-STATE Outputs

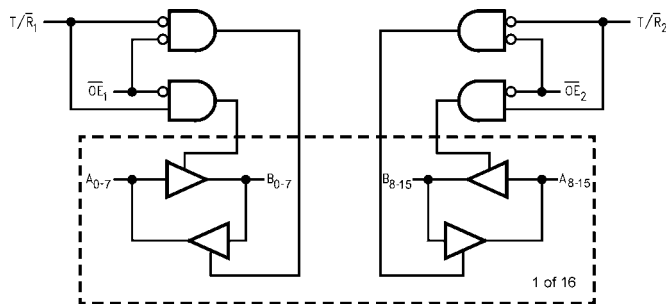
Truth Tables

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B_0-B_7 Data to Bus A_0-A_7
L	H	Bus A_0-A_7 Data to Bus B_0-B_7
H	X	HIGH Z State on A_0-A_7, B_0-B_7

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B_8-B_{15} Data to Bus A_8-A_{15}
L	H	Bus A_8-A_{15} Data to Bus B_8-B_{15}
H	X	HIGH Z State on A_8-A_{15}, B_8-B_{15}

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial (HIGH or LOW, inputs and I/O's may not float)
 Z = High Impedance

Logic Diagram



Absolute Maximum Ratings(Note 2)

Supply Voltage (V_{CC})	-0.5V to +4.6V
DC Input Voltage (V_I)	-0.5V to 4.6V
Output Voltage (V_O) (Note 3)	-0.5V to $V_{CC} + 0.5V$
DC Input Diode Current (I_{IK})	
$V_I < 0V$	-50 mA
DC Output Diode Current (I_{OK})	
$V_O < 0V$	-50 mA
DC Output Source/Sink Current (I_{OH}/I_{OL})	±50 mA
DC V_{CC} or GND Current per Supply Pin (I_{CC} or GND)	±100 mA
Storage Temperature Range (T_{STG})	-65°C to +150°C

Recommended Operating Conditions (Note 4)

Power Supply	
Operating	1.65V to 3.6V
Input Voltage	0V to V_{CC}
Output Voltage (V_O)	0V to V_{CC}
Free Air Operating Temperature (T_A)	-40°C to +85°C
Minimum Input Edge Rate ($\Delta t/\Delta V$)	
$V_{IN} = 0.8V$ to 2.0V, $V_{CC} = 3.0V$	10 ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Floating or unused control inputs must be held HIGH or LOW.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	Min	Max	Units	
V_{IH}	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	$0.65 \times V_{CC}$ 1.7 2.0		V	
V_{IL}	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		$0.35 \times V_{CC}$ 0.7 0.8	V	
V_{OH}	HIGH Level Output Voltage A Outputs	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V	
		$I_{OH} = -2 \text{ mA}$	1.65	1.2			
		$I_{OH} = -4 \text{ mA}$	2.3	1.9			
		$I_{OH} = -6 \text{ mA}$	2.3	1.7			
		$I_{OH} = -8 \text{ mA}$	3.0	2.4			
		$I_{OH} = -12 \text{ mA}$	2.7	2			
	HIGH Level Output Voltage B Outputs	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$			
		$I_{OH} = -4 \text{ mA}$	1.65	1.2			
		$I_{OH} = -6 \text{ mA}$	2.3	2.0			
		$I_{OH} = -12 \text{ mA}$	2.3	1.7			
			2.7	2.2			
			3.0	2.4			
V_{OL}	LOW Level Output Voltage A Outputs	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V	
		$I_{OL} = 2 \text{ mA}$	1.65		0.45		
		$I_{OL} = 4 \text{ mA}$	2.3		0.4		
		$I_{OL} = 6 \text{ mA}$	2.3		0.55		
			3.0		0.55		
		$I_{OL} = 8 \text{ mA}$	2.7		0.6		
		$I_{OL} = 12 \text{ mA}$	3.0		0.8		
	LOW Level Output Voltage B Outputs	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2		
		$I_{OL} = 4 \text{ mA}$	1.65		0.45		
		$I_{OL} = 6 \text{ mA}$	2.3		0.4		
		$I_{OL} = 12 \text{ mA}$	2.3		0.7		
			2.7		0.4		
			3.0		0.55		
			3.0		0.55		
I_I	Input Leakage Current	$0 \leq V_I \leq 3.6V$	1.65 - 3.6		±5.0	μA	
I_{OZ}	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V, V_I = V_{IH}$ or V_{IL}	1.65 - 3.6		±10	μA	

DC Electrical Characteristics (Continued)										
Symbol	Parameter	Conditions	V _{CC} (V)	Min	Max	Units				
I _{OFF}	Power Off Leakage Current	0V ≤ (V _I , V _O) ≤ 3.6V	0		10	mA				
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND, I _O = 0	3.6		40	μA				
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		750	μA				
AC Electrical Characteristics										
Symbol	Parameter	T _A = -40°C to +85°C, R _L = 500Ω								Units
		C _L = 50 pF				C _L = 30 pF				
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		V _{CC} = 2.5 ± 0.2V		V _{CC} = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t _{PHL} , t _{PLH}	Propagation Delay A to B	1.3	3.0	1.5	3.5	1	3.0	1.5	6.0	ns
	Propagation Delay B to A	1.3	3.9	1.5	4.8	1	4.3	1.5	8.6	
t _{PZL} , t _{PZH}	Output Enable Time A to B	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.3	ns
	Output Enable Time B to A	1.3	4.7	1.5	6.2	1.0	5.7	1.5	9.8	
t _{PLZ} , t _{PHZ}	Output Disable Time A to B	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns
	Output Disable Time B to A	1.3	4.6	1.5	5.3	1.0	4.8	1.5	8.6	
Capacitance										
Symbol	Parameter	Conditions	T _A = +25°C		Units					
			V _{CC}	Typical						
C _{IN}	Input Capacitance	V _I = 0V or V _{CC}	3.3	6	pF					
C _{IO}	Input, Output Capacitance	V _O = 0V or V _{CC}	3.3	7	pF					
C _{PD}	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C _L = 50 pF		pF					
			3.3	20						
			2.5	20						

AC Loading and Waveforms

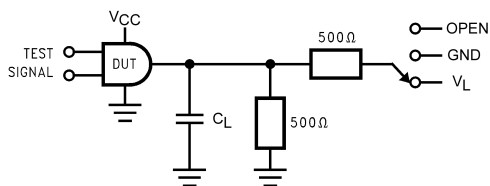


FIGURE 1. AC Test Circuit

TABLE 1. Values for Figure 1

TEST	SWITCH
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	V_L
t_{PZH} , t_{PHZ}	GND

TABLE 2. Variable Matrix
(Input Characteristics: $f = 1\text{MHz}$; $t_r = t_f = 2\text{ns}$; $Z_0 = 50\Omega$)

Symbol	V_{CC}			
	$3.3\text{V} \pm 0.3\text{V}$	2.7V	$2.5 \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
V_{mi}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_{mo}	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
V_X	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
V_Y	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
V_L	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$

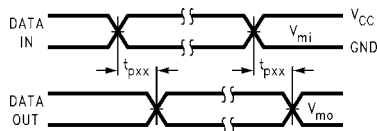


FIGURE 2. Waveform for Inverting and Non-inverting Functions

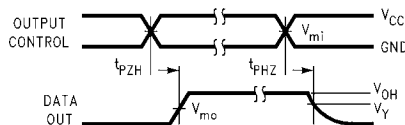


FIGURE 3. 3-STATE Output High Enable and Disable Times for Low Voltage Logic

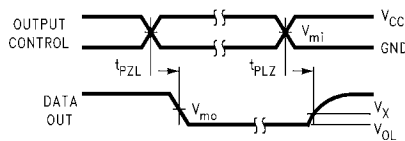
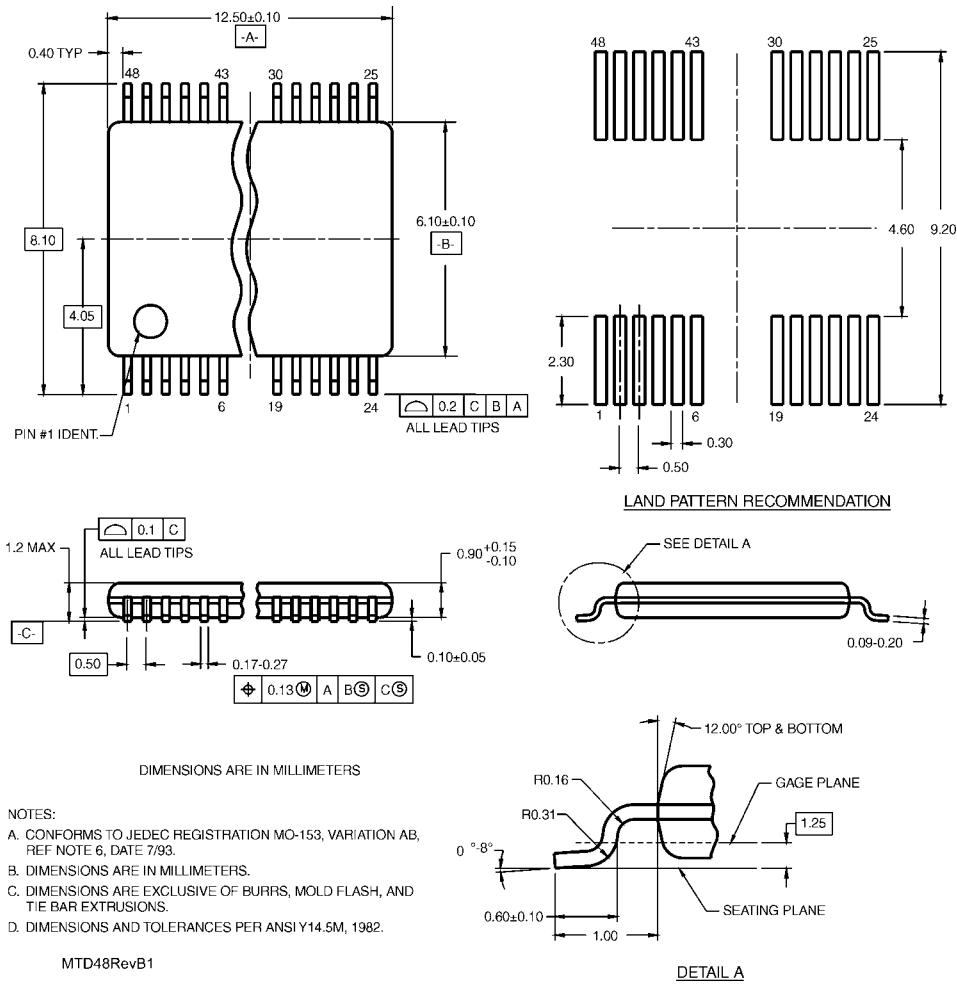


FIGURE 4. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic

Physical Dimensions inches (millimeters) unless otherwise noted



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