



**THE DATASHEET OF
74ALVC16244DL,118**



74ALVC16244; 74ALVCH16244

2.5 V / 3.3 V 16-bit buffer/line driver; 3-state

Rev. 5 — 15 January 2019

Product data sheet

1. General description

The 74ALVC16244; 74ALVCH16244 is a 16-bit non-inverting buffer/line driver with 3-state outputs. The device can be used as four 4-bit buffers, two 8-bit buffers or one 16-bit buffer. The 3-state outputs are controlled by the output enable inputs 1OE, 2OE, 3OE and 4OE. A HIGH on nOE causes the outputs to assume a high-impedance OFF-state.

The 74ALVCH16244 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

The 74ALVC16244 has 5 V tolerant inputs.

2. Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on data inputs (74ALVCH16244 only)
- Output drive capability 50 Ω transmission lines at 85 °C
- Current drive ±24 mA at 3.0 V
- Complies with JEDEC standard no. 8-1A
- ESD protection:
 - HBM JESD22-A114-A exceeds 2000 V
 - MM JESD22-A115-A exceeds 200 V

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74ALVC16244DL	-40 °C to +85 °C	SSOP48	plastic shrink small outline package; 48 leads; body width 7.5 mm	SOT370-1
74ALVC16244DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1
74ALVCH16244DGG				

4. Functional diagram

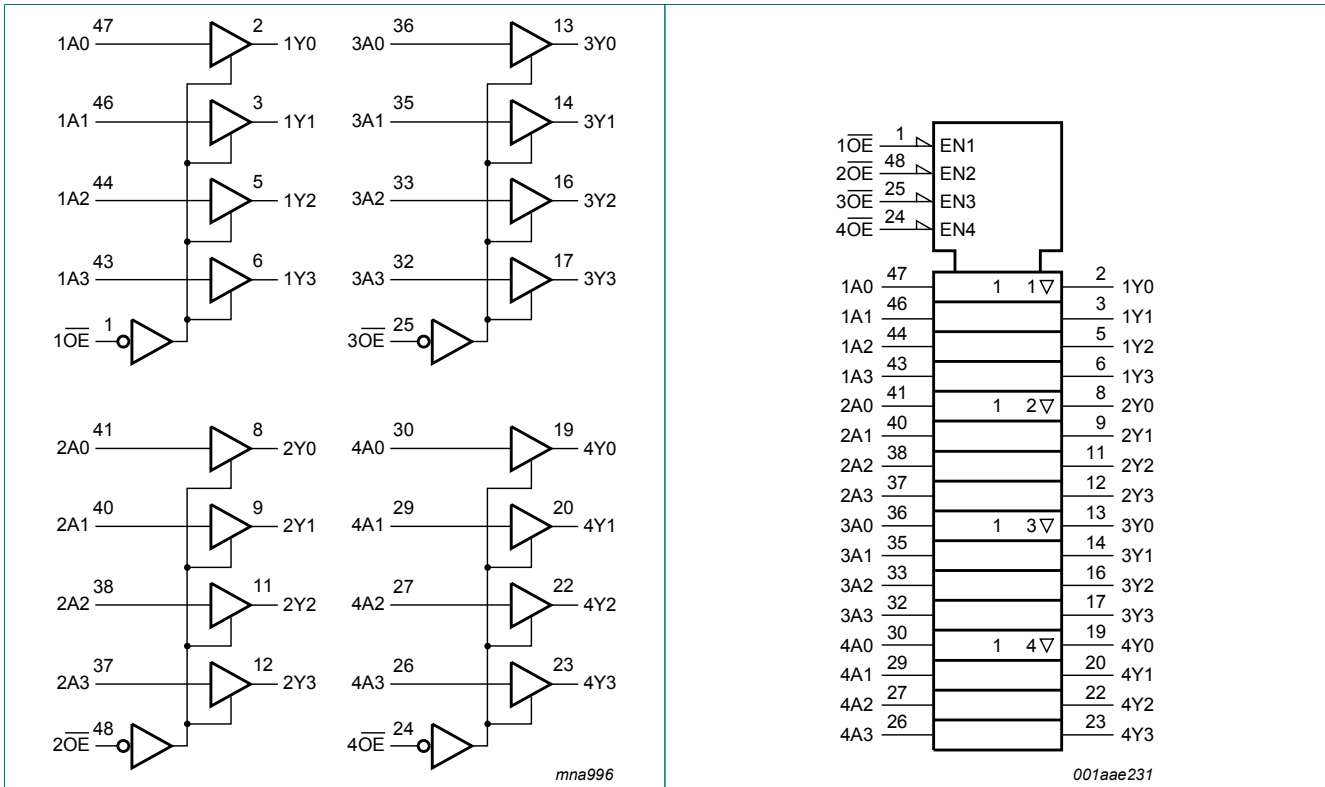


Fig. 1. Logic symbol

Fig. 2. IEC logic symbol

Fig. 3. Bus hold circuit

5. Pinning information

5.1. Pinning

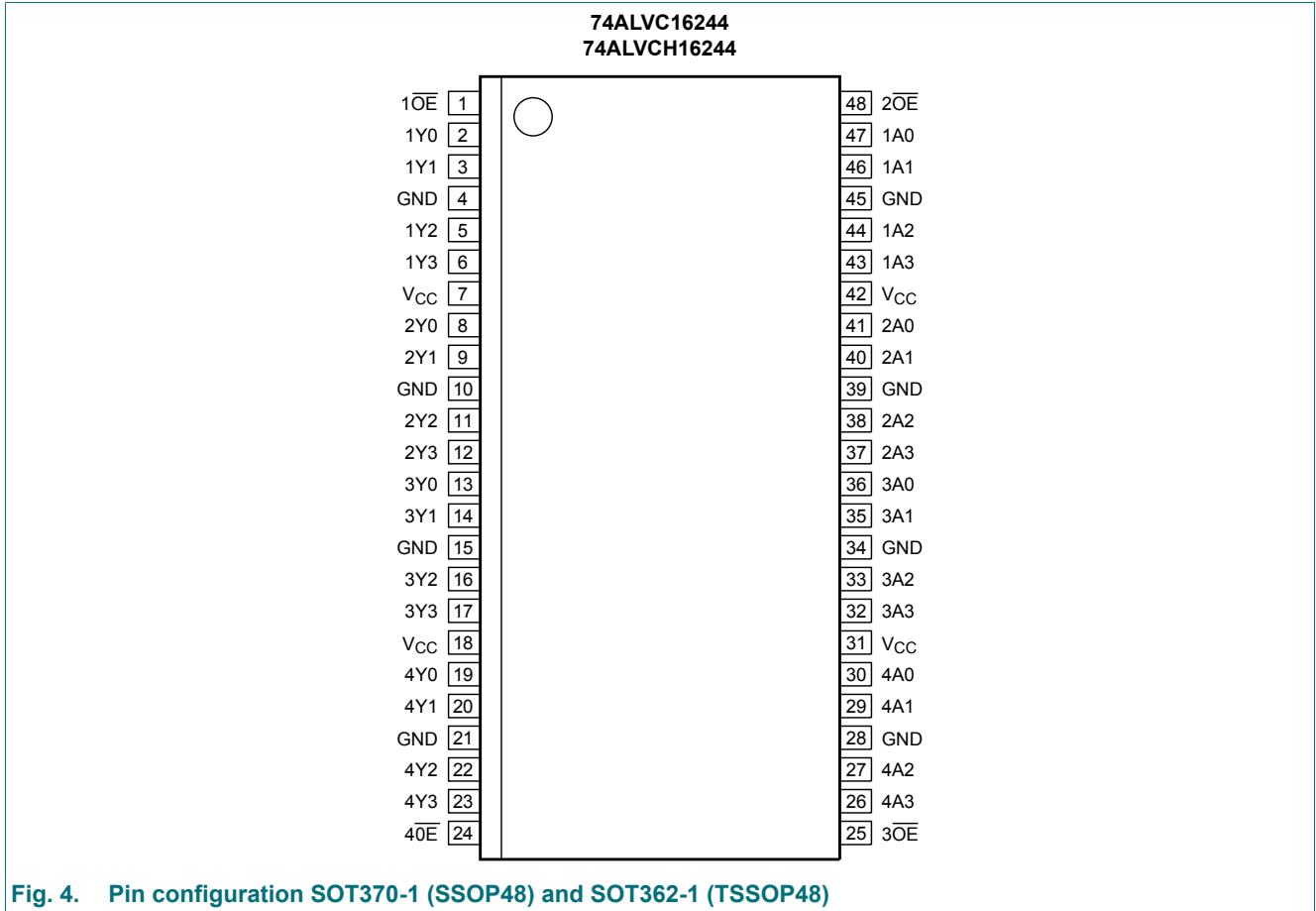


Fig. 4. Pin configuration SOT370-1 (SSOP48) and SOT362-1 (TSSOP48)

5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
$1\overline{OE}$, $2\overline{OE}$, $3\overline{OE}$, $4\overline{OE}$	1, 48, 25, 24	output enable inputs (active LOW)
1A0, 1A1, 1A2, 1A3	47, 46, 44, 43	data inputs
2A0, 2A1, 2A2, 2A3	41, 40, 38, 37	data inputs
3A0, 3A1, 3A2, 3A3	36, 35, 33, 32	data inputs
4A0, 4A1, 4A2, 4A3	30, 29, 27, 26	data inputs
1Y0, 1Y1, 1Y2, 1Y3	2, 3, 5, 6	data outputs
2Y0, 2Y1, 2Y2, 2Y3	8, 9, 11, 12	data outputs
3Y0, 3Y1, 3Y2, 3Y3	13, 14, 16, 17	data outputs
4Y0, 4Y1, 4Y2, 4Y3	19, 20, 22, 23	data outputs
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
V_{CC}	7, 18, 31, 42	supply voltage

6. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

Input		Output
nOE	nAn	nYn
L	L	L
L	H	H
H	X	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	supply voltage		-0.5	+4.6	V
V_I	input voltage	74ALVCH16244; data inputs; [1]	-0.5	$V_{CC} + 0.5$	V
		74ALVC16244; data inputs; [1]	-0.5	+5.5	V
		control inputs [1]	-0.5	+5.5	V
V_O	output voltage	[1]	-0.5	$V_{CC} + 0.5$	V
I_{IK}	input clamping current	$V_I < 0$ V	-50	-	mA
I_{OK}	output clamping current	$V_O > V_{CC}$ or $V_O < 0$ V	-	± 50	mA
I_O	output current	$V_O = 0$ V to V_{CC}	-	± 50	mA
I_{CC}	supply current		-	100	mA
I_{GND}	ground current		-100	-	mA
T_{stg}	storage temperature		-65	+150	°C
P_{tot}	total power dissipation	$T_{amb} = -40$ °C to +85 °C [2]			
		SSOP48 package	-	850	mW
		TSSOP48 package	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SSOP48 packages: above 55 °C derate linearly with 11.3 mW/K.
For TSSOP48 packages: above 55 °C derate linearly with 8 mW/K.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	maximum speed performance			
		V _{CC} = 2.5 V; C _L = 30 pF	2.3	2.7	V
		V _{CC} = 3.3 V; C _L = 50 pF	3.0	3.6	V
		LOW-voltage applications	1.2	3.6	V
V _I	input voltage	74ALVCH16244; data inputs;	0	V _{CC}	V
		74ALVC16244; data inputs;	0	5.5	V
		control inputs	0	5.5	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	0	10	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V). T_{amb} = -40 °C to +85 °C

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
V _{IH}	HIGH-level input voltage	V _{CC} = 1.2 V	V _{CC}	-	-	V
		V _{CC} = 1.8 V	0.7 × V _{CC}	0.9	-	V
		V _{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 1.2 V	-	-	GND	V
		V _{CC} = 1.8 V	-	0.9	0.2 × V _{CC}	V
		V _{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μA; V _{CC} = 1.8 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -6 mA; V _{CC} = 1.8 V	V _{CC} - 0.4	V _{CC} - 0.10	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.3	V _{CC} - 0.08	-	V
		I _O = -12 mA; V _{CC} = 2.3 V	V _{CC} - 0.5	V _{CC} - 0.17	-	V
		I _O = -18 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.26	-	V
		I _O = -12 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.14	-	V
		I _O = -24 mA; V _{CC} = 3.0 V	V _{CC} - 1.0	V _{CC} - 0.28	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μA; V _{CC} = 1.8 V to 3.6 V	-	GND	0.20	V
		I _O = 6 mA; V _{CC} = 1.8 V	-	0.09	0.30	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.07	0.20	V
		I _O = 12 mA; V _{CC} = 2.3 V	-	0.15	0.40	V
		I _O = 18 mA; V _{CC} = 2.3 V	-	0.23	0.60	V
		I _O = 12 mA; V _{CC} = 2.7 V	-	0.14	0.40	V
		I _O = 24 mA; V _{CC} = 3.0 V	-	0.27	0.55	V

Symbol	Parameter	Conditions	Min	Typ [1]	Max	Unit
I_I	input leakage current	74ALVCH16244; data inputs; $V_I = V_{CC}$ or GND; $V_{CC} = 1.8$ V to 3.6 V	-	0.1	5	μ A
		74ALVC16244; data inputs; $V_I = 5.5$ V or GND; $V_{CC} = 1.8$ V to 3.6 V	-	0.1	5	μ A
		control inputs; $V_I = 5.5$ V or GND; $V_{CC} = 1.8$ V to 3.6 V	-	0.1	5	μ A
I_{BHL}	bus hold LOW current	$V_{CC} = 2.3$ V; $V_I = 0.7$ V [2]	45	-	-	μ A
		$V_{CC} = 3.0$ V; $V_I = 0.8$ V [2]	75	150	-	μ A
I_{BHH}	bus hold HIGH current	$V_{CC} = 2.3$ V; $V_I = 1.7$ V [2]	-45	-	-	μ A
		$V_{CC} = 3.0$ V; $V_I = 2.0$ V [2]	-75	-175	-	μ A
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 2.7$ V [2]	300	-	-	μ A
		$V_{CC} = 3.6$ V [2]	450	-	-	μ A
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 2.7$ V [2]	-300	-	-	μ A
		$V_{CC} = 3.6$ V [2]	-450	-	-	μ A
I_{OZ}	OFF-state output current	$V_{CC} = 1.8$ to 2.7 V; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	-	0.1	5	μ A
		$V_{CC} = 3.6$ V; $V_I = V_{IH}$ or V_{IL} ; $V_O = V_{CC}$ or GND	-	0.1	10	μ A
I_{CC}	supply current	$V_{CC} = 1.8$ to 2.7 V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	0.1	20	μ A
		$V_{CC} = 2.3$ to 3.6 V; $V_I = V_{CC}$ or GND; $I_O = 0$ A	-	0.2	40	μ A
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 0.6$ V; $I_O = 0$ A; $V_{CC} = 2.7$ V to 3.6 V				
		74ALVCH16244	-	150	750	μ A
		74ALVC16244	-	5	500	μ A
		control pin	-	5	500	μ A
C_I	input capacitance		-	5.0	-	pF

[1] All typical values are measured at $T_{amb} = 25$ °C.

[2] Valid for data inputs of bus hold parts.

10. Dynamic characteristics

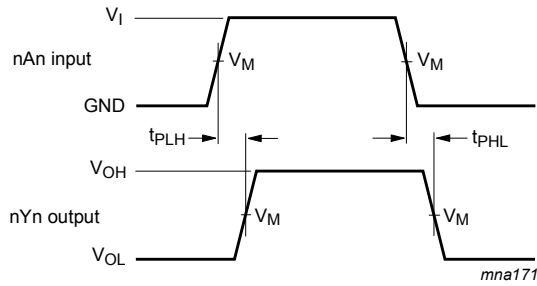
Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit, see Fig. 7.

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ [1]	Max	
t _{pd}	propagation delay	nAn to nYn; see Fig. 5 [2]				
		V _{CC} = 1.2 V	-	5.8	-	ns
		V _{CC} = 1.8 V	1.5	2.8	5.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	1.9	3.7	ns
		V _{CC} = 2.7 V	1.0	2.1	3.6	ns
	V _{CC} = 3.0 V to 3.6 V	1.0	1.9	3.0	ns	
t _{en}	enable time	nOE to nYn; see Fig. 6 [3]				
		V _{CC} = 1.2 V	-	8.4	-	ns
		V _{CC} = 1.8 V	1.5	3.8	7.1	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	4.9	ns
		V _{CC} = 2.7 V	1.0	2.9	4.9	ns
	V _{CC} = 3.0 V to 3.6 V	1.0	2.3	4.0	ns	
t _{dis}	disable time	nOE to nYn; see Fig. 6 [4]				
		V _{CC} = 1.2 V	-	5.9	-	ns
		V _{CC} = 1.8 V	1.5	3.1	5.4	ns
		V _{CC} = 2.3 V to 2.7 V	1.0	2.1	4.1	ns
		V _{CC} = 2.7 V	1.0	3.0	4.5	ns
	V _{CC} = 3.0 V to 3.6 V	1.0	2.7	4.1	ns	
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} [5]				
		outputs enabled	-	25	-	pF
		outputs disabled	-	4	-	pF

- [1] Typical values are measured at T_{amb} = 25 °C
 Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
 Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V
- [2] t_{pd} is the same as t_{PHL} and t_{PLH}.
- [3] t_{en} is the same as t_{PZH} and t_{PZL}.
- [4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \Sigma(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz
 f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = total load switching outputs
 Σ(C_L × V_{CC}² × f_o) = sum of the outputs

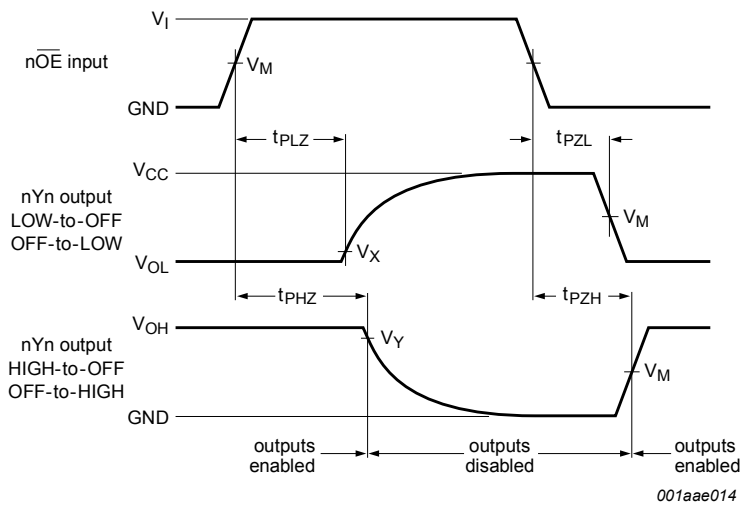
10.1. Waveforms and test circuit



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 5. Inputs nAn to output nYn propagation delays



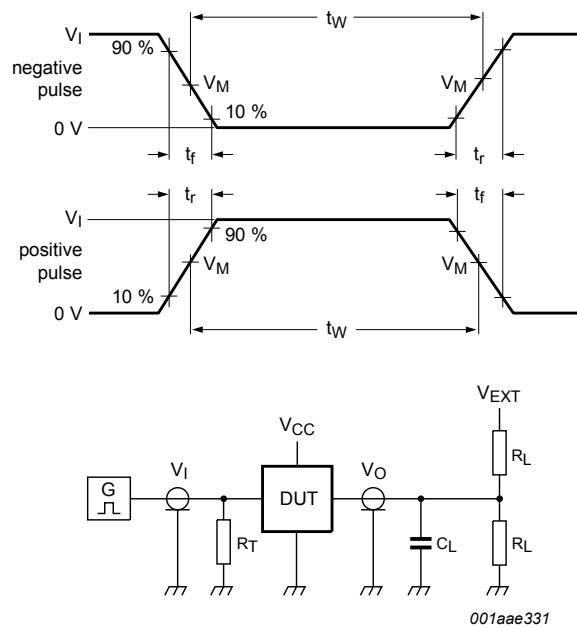
Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig. 6. OFF-state to HIGH or LOW and HIGH or LOW to OFF-state propagation delays

Table 8. Measurement points

Supply voltage	Input		Output		
	V_I	V_M	V_M	V_X	V_Y
1.2	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
1.8 V	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig. 7. Test circuit for measuring switching times

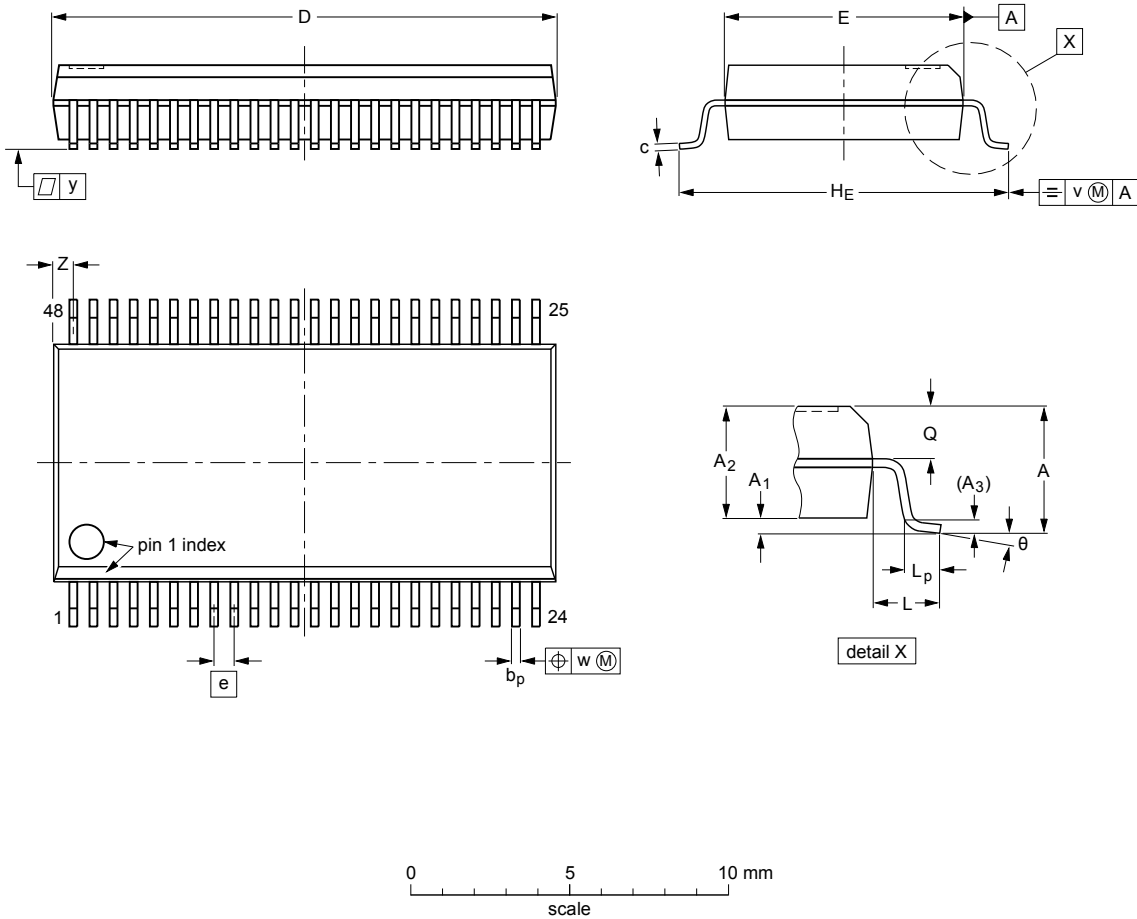
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
1.2 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
1.8 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11. Package outline

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5 mm

SOT370-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	Z ⁽¹⁾	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	16.00 15.75	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

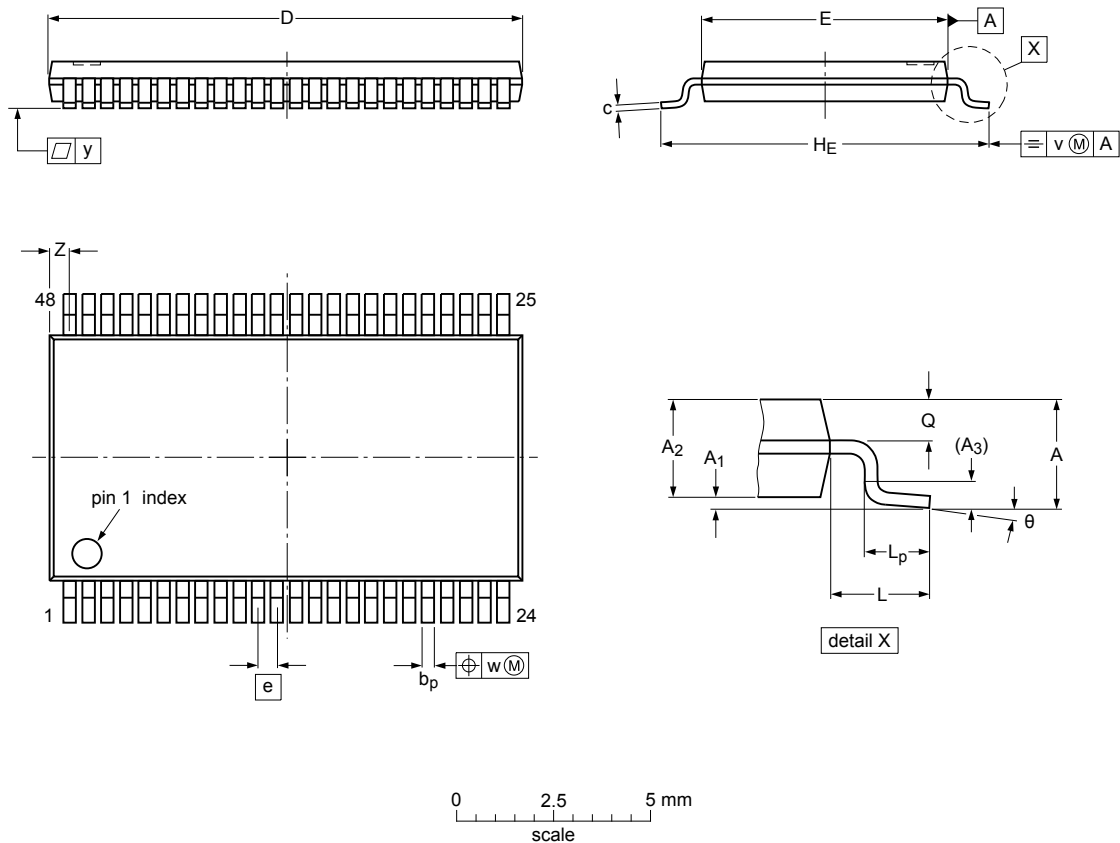
1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT370-1		MO-118				99-12-27 03-02-19

Fig. 8. Package outline SSOP48 (SOT370-1)

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
mm	max	0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
	nom	1.2		0.25				0.5			1			0.25	0.08	0.1		
	min		0.05	0.85	0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT362-1		MO-153				03-02-19- 13-08-05

Fig. 9. Package outline TSSOP48 (SOT362-1)

12. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MM	Machine Model
TTL	Transistor-Transistor Logic

13. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVC_ALVCH16244 v.5	20190115	Product data sheet	-	74ALVC_ALVCH16244 v.4
Modifications:	<ul style="list-style-type: none"> Type number 74ALVCH16244DL (SOT370-1) removed. 			
74ALVC_ALVCH16244 v.4	20170612	Product data sheet	-	74ALVC_ALVCH16244 v.3
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. 			
74ALVC_ALVCH16244 v.3	20030514	Product specification	-	74ALVC_ALVCH16244 v.2
74ALVC_ALVCH16244 v.2	19980629	Product specification	-	74ALVCH16244 v.1
74ALVCH16244 v.1	19970321	Product specification	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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