



**THE DATASHEET OF
74ALVCH162245DL,11**



74ALVCH162245

16-bit bus transceiver with direction pin and
30 Ω termination resistor; 3-state

Rev. 3 — 16 January 2018

Product data sheet

1 General description

The 74ALVCH162245 is a 16-bit transceiver featuring non-inverting 3-state bus compatible outputs in both send and receive directions.

The 74ALVCH162245 features two output enable ($\overline{\text{nOE}}$) inputs for easy cascading and two send/receive ($\overline{\text{nDIR}}$) inputs for direction control. $\overline{\text{nOE}}$ controls the outputs so that the buses are effectively isolated. This device can be used as two 8-bit transceivers or one 16-bit transceiver.

The 74ALVCH162245 is designed with 30 Ω series resistors in both HIGH and LOW output states.

The 74ALVCH162245 has active bus hold circuitry which is provided to hold unused or floating data inputs at a valid logic level. This feature eliminates the need for external pull-up or pull-down resistors.

2 Features and benefits

- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- MultiByte flow-through standard pin-out architecture
- Low inductance multiple V_{CC} and GND pins for minimum noise and ground bounce
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Bus hold on all data inputs
- Integrated 30 Ω termination resistor
- Complies with JEDEC standards:
 - JESD8-5 (2.3 V to 2.7 V)
 - JESD8B/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM ANSI/ESDA/JEDEC JS-001 exceeds 2000 V
 - CDM JESD22-C101E exceeds 1000 V

3 Ordering information

Table 1. Ordering information

Type number	Package			Version
	Temperature range	Name	Description	
74ALVCH162245DGG	-40 °C to +85 °C	TSSOP48	plastic thin shrink small outline package; 48 leads; body width 6.1 mm	SOT362-1

4 Functional diagram

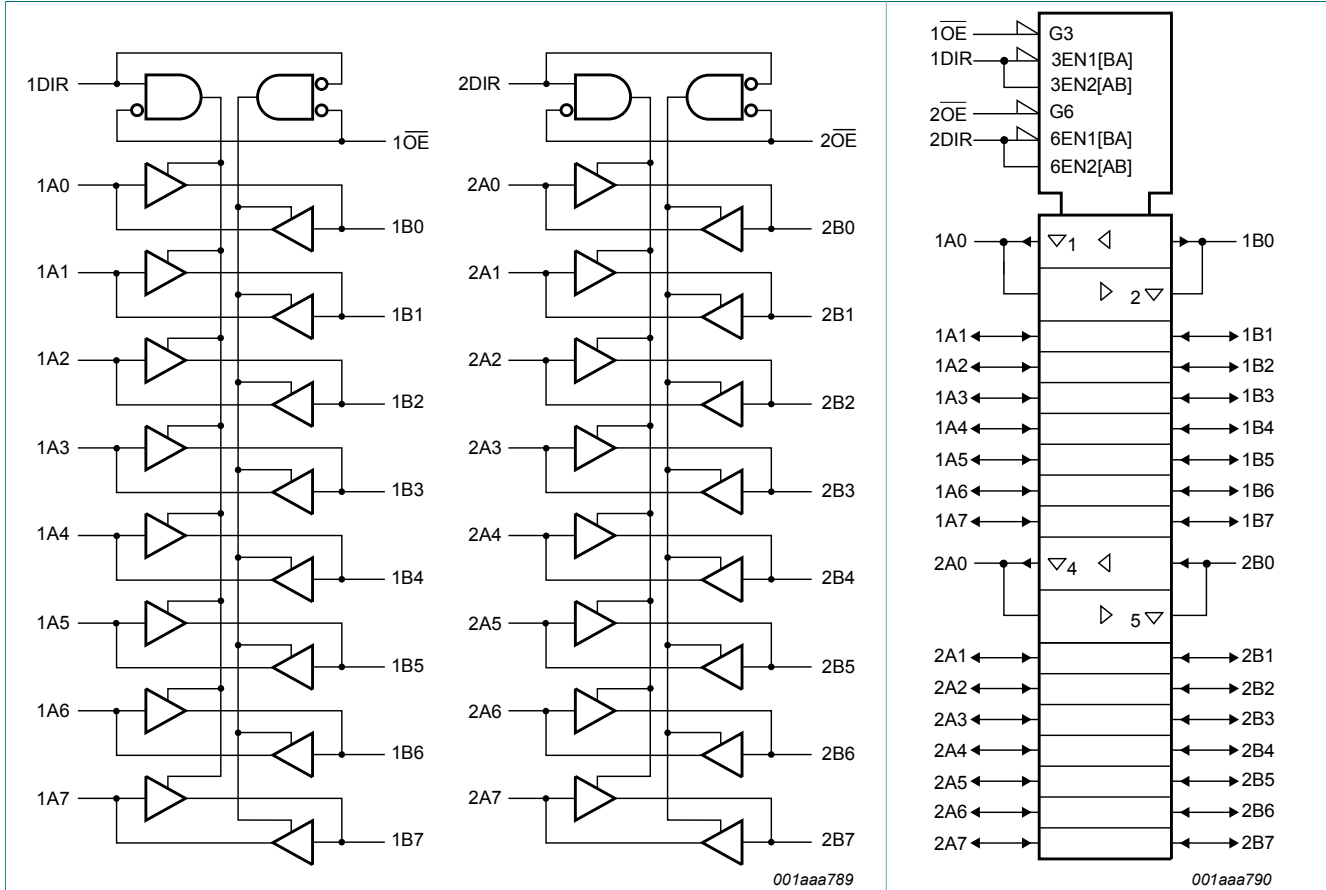


Figure 1. Logic symbol

Figure 2. IEC logic symbol

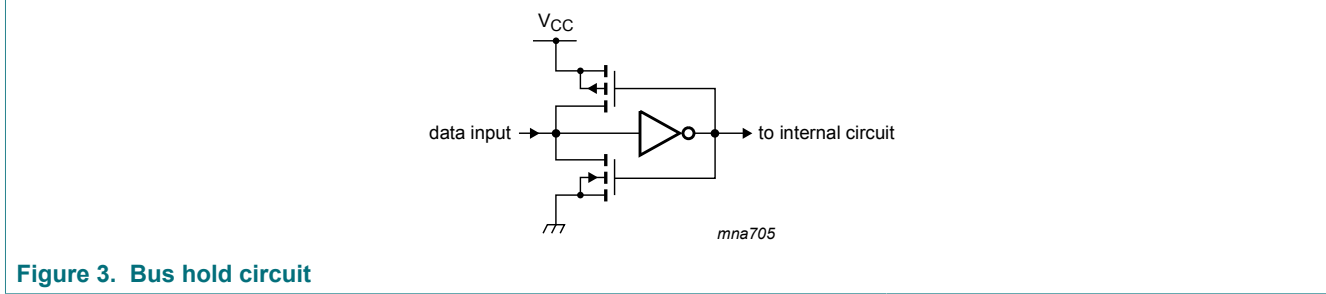


Figure 3. Bus hold circuit

5 Pinning information

5.1 Pinning

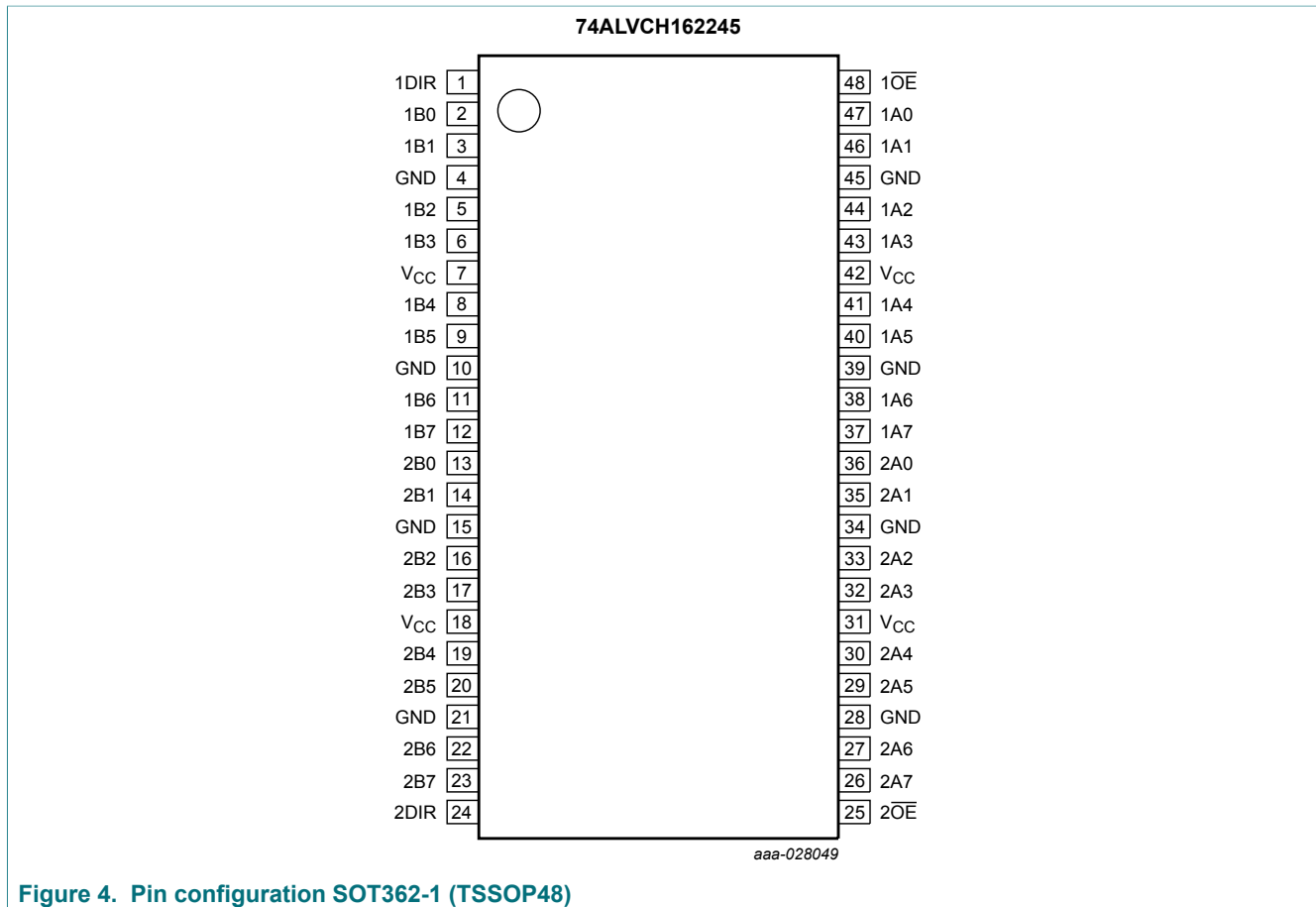


Figure 4. Pin configuration SOT362-1 (TSSOP48)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
1DIR, 2DIR	1, 24	direction control input
1A0, 1A1, 1A2, 1A3, 1A4, 1A5, 1A6, 1A7	47, 46, 44, 43, 41, 40, 38, 37	data input/output
2A0, 2A1, 2A2, 2A3, 2A4, 2A5, 2A6, 2A7	36, 35, 33, 32, 30, 29, 27, 26	data input/output
GND	4, 10, 15, 21, 28, 34, 39, 45	ground (0 V)
1B0, 1B1, 1B2, 1B3, 1B4, 1B5, 1B6, 1B7	2, 3, 5, 6, 8, 9, 11, 12	data input/output
2B0, 2B1, 2B2, 2B3, 2B4, 2B5, 2B6, 2B7	13, 14, 16, 17, 19, 20, 22, 23	data input/output
1 \overline{OE} , 2 \overline{OE}	48, 25	output enable input (active-LOW)
V _{CC}	7, 18, 31, 42	supply voltage

6 Functional description

Table 3. Function table ^[1]

Control		Input/output	
nOE	nDIR	nAn	nBn
L	L	output nAn = nBn	input
L	H	input	output nBn = nAn
H	X	Z	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7 Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	data inputs ^[1]	-0.5	V _{CC} + 0.5	V
		control inputs ^[1]	-0.5	+4.6	V
V _O	output voltage	^[1]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _I < 0 V	-50	-	mA
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0 V	-	±50	mA
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C			
		TSSOP48 package ^[2]	-	600	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For TSSOP48 packages: above 55 °C derate linearly with 8 mW/K.

8 Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage	V _{CC} = 2.5 V: for maximum speed performance at C _L = 30 pF	2.3	2.7	V
		V _{CC} = 3.3 V: for maximum speed performance at C _L = 50 pF	3.0	3.6	V
V _I	input voltage		0	V _{CC}	V
V _O	output voltage		0	V _{CC}	V
T _{amb}	ambient temperature	in free air	-40	+85	°C
$\Delta t/\Delta V$	input transition rise and fall rate	V _{CC} = 2.3 V to 3.0 V	0	20	ns/V
		V _{CC} = 3.0 V to 3.6 V	0	10	ns/V

9 Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
V _{IH}	HIGH-level input voltage	V _{CC} = 2.3 to 2.7 V	1.7	1.2	-	V
		V _{CC} = 2.7 to 3.6 V	2.0	1.5	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.3 to 2.7 V	-	1.2	0.7	V
		V _{CC} = 2.7 to 3.6 V	-	1.5	0.8	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -100 μ A; V _{CC} = 2.3 V to 3.6 V	V _{CC} - 0.2	V _{CC}	-	V
		I _O = -4 mA; V _{CC} = 2.3 V	V _{CC} - 0.4	V _{CC} - 0.11	-	V
		I _O = -6 mA; V _{CC} = 2.3 V	V _{CC} - 0.6	V _{CC} - 0.17	-	V
		I _O = -4 mA; V _{CC} = 2.7 V	V _{CC} - 0.5	V _{CC} - 0.09	-	V
		I _O = -8 mA; V _{CC} = 2.7 V	V _{CC} - 0.7	V _{CC} - 0.19	-	V
		I _O = -6 mA; V _{CC} = 3.0 V	V _{CC} - 0.6	V _{CC} - 0.13	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 100 μ A; V _{CC} = 2.3 V to 3.6 V	-	GND	0.20	V
		I _O = 4 mA; V _{CC} = 2.3 V	-	0.07	0.40	V
		I _O = 6 mA; V _{CC} = 2.3 V	-	0.11	0.55	V
		I _O = 4 mA; V _{CC} = 2.7 V	-	0.06	0.40	V
		I _O = 8 mA; V _{CC} = 2.7 V	-	0.13	0.60	V
		I _O = 6 mA; V _{CC} = 3.0 V	-	0.09	0.55	V
	I _O = 12 mA; V _{CC} = 3.0 V	-	0.19	0.80	V	

Symbol	Parameter	Conditions	Min	Typ ^[1]	Max	Unit
I_I	input leakage current	per data input; $V_I = V_{CC}$ or GND; $V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}$	-	0.1	5	μA
I_{BHL}	bus hold LOW current	$V_{CC} = 2.3 \text{ V}; V_I = 0.7 \text{ V}$	45	-	-	μA
		$V_{CC} = 3.0 \text{ V}; V_I = 0.8 \text{ V}$	75	150	-	μA
I_{BHH}	bus hold HIGH current	$V_{CC} = 2.3 \text{ V}; V_I = 1.7 \text{ V}$	-45	-	-	μA
		$V_{CC} = 3.0 \text{ V}; V_I = 2.0 \text{ V}$	-75	-175	-	μA
I_{BHLO}	bus hold LOW overdrive current	$V_{CC} = 3.6 \text{ V}$	500	-	-	μA
I_{BHHO}	bus hold HIGH overdrive current	$V_{CC} = 3.6 \text{ V}$	-500	-	-	μA
I_{OZ}	OFF-state output current	$V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}; V_I = V_{IH}$ or $V_{IL};$ $V_O = V_{CC}$ or GND	-	0.1	10	μA
I_{CC}	supply current	$V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}; V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}$	-	0.2	40	μA
ΔI_{CC}	additional supply current	$V_{CC} = 2.3 \text{ V to } 3.6 \text{ V}; V_I = V_{CC} - 0.6 \text{ V};$ $I_O = 0 \text{ A}$	-	150	750	μA
C_I	input capacitance		-	4.0	-	pF
$C_{I/O}$	input/output capacitance		-	8.0	-	pF

[1] All typical values are measured at $T_{amb} = 25 \text{ }^\circ\text{C}$.

10 Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); For test circuit, see [Figure 7](#).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ ^[1]	Max	
t _{pd}	propagation delay	nAn to nBn or nBn to nAn; see Figure 5 ^[2]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.5	4.9	ns
		V _{CC} = 2.7 V	1.0	2.7	4.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.4	4.2	ns
t _{en}	enable time	n $\overline{O}E$ to nAn or n $\overline{O}E$ to nBn; see Figure 6 ^[3]				
		V _{CC} = 2.3 V to 2.7 V	1.0	2.9	6.8	ns
		V _{CC} = 2.7 V	1.0	3.9	6.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	3.0	5.6	ns
t _{dis}	disable time	n $\overline{O}E$ to nAn or n $\overline{O}E$ to nBn; see Figure 6 ^[4]				
		V _{CC} = 2.3 V to 2.7 V	1.0	3.0	6.3	ns
		V _{CC} = 2.7 V	1.0	2.9	5.7	ns
		V _{CC} = 3.0 V to 3.6 V	1.0	2.6	5.5	ns
C _{PD}	power dissipation capacitance	per buffer; V _I = GND to V _{CC} ^[5]				
		outputs enabled	-	27	-	pF
		outputs disabled	-	4	-	pF

[1] Typical values are measured at T_{amb} = 25 °C
 Typical values for V_{CC} = 2.3 V to 2.7 V are measured at V_{CC} = 2.5 V
 Typical values for V_{CC} = 3.0 V to 3.6 V are measured at V_{CC} = 3.3 V

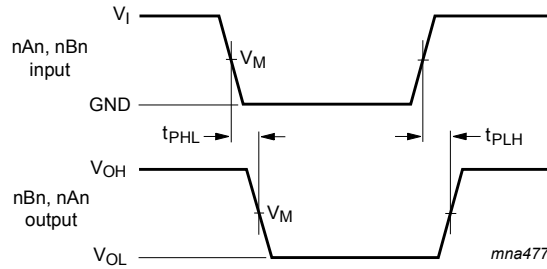
[2] t_{pd} is the same as t_{PHL} and t_{PLH}.

[3] t_{en} is the same as t_{PZH} and t_{PZL}.

[4] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

[5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz
 f_o = output frequency in MHz
 C_L = output load capacitance in pF
 V_{CC} = supply voltage in Volts
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of the outputs

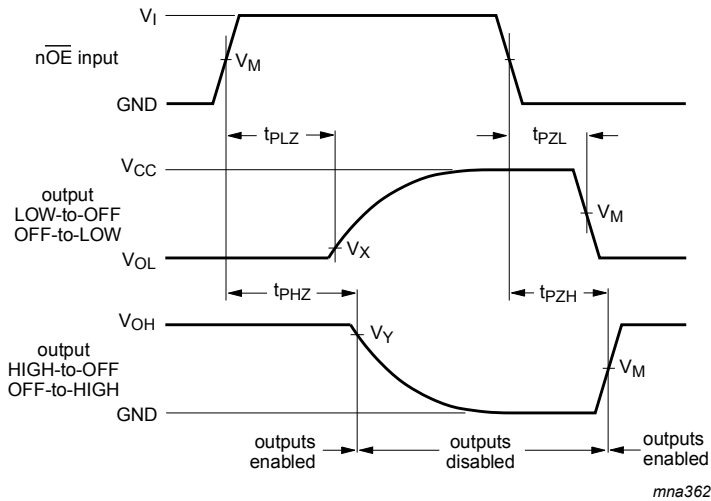
10.1 Waveforms and test circuit



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Figure 5. Input (nAn or nBn) to output (nBn or nAn) propagation delays



Measurement points are given in [Table 8](#).

V_{OL} and V_{OH} are typical output voltage levels that occur with the output load.

Figure 6. 3-state enable and disable times

Table 8. Measurement points

Supply voltage	Input		Output		
V_{CC}	V_I	V_M	V_M	V_X	V_Y
2.3 V to 2.7 V	V_{CC}	$0.5 \times V_{CC}$	$0.5V_{CC}$	$V_{OL} + 0.15 \text{ V}$	$V_{OH} - 0.15 \text{ V}$
2.7 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$
3.0 V to 3.6 V	2.7 V	1.5 V	1.5 V	$V_{OL} + 0.3 \text{ V}$	$V_{OH} - 0.3 \text{ V}$

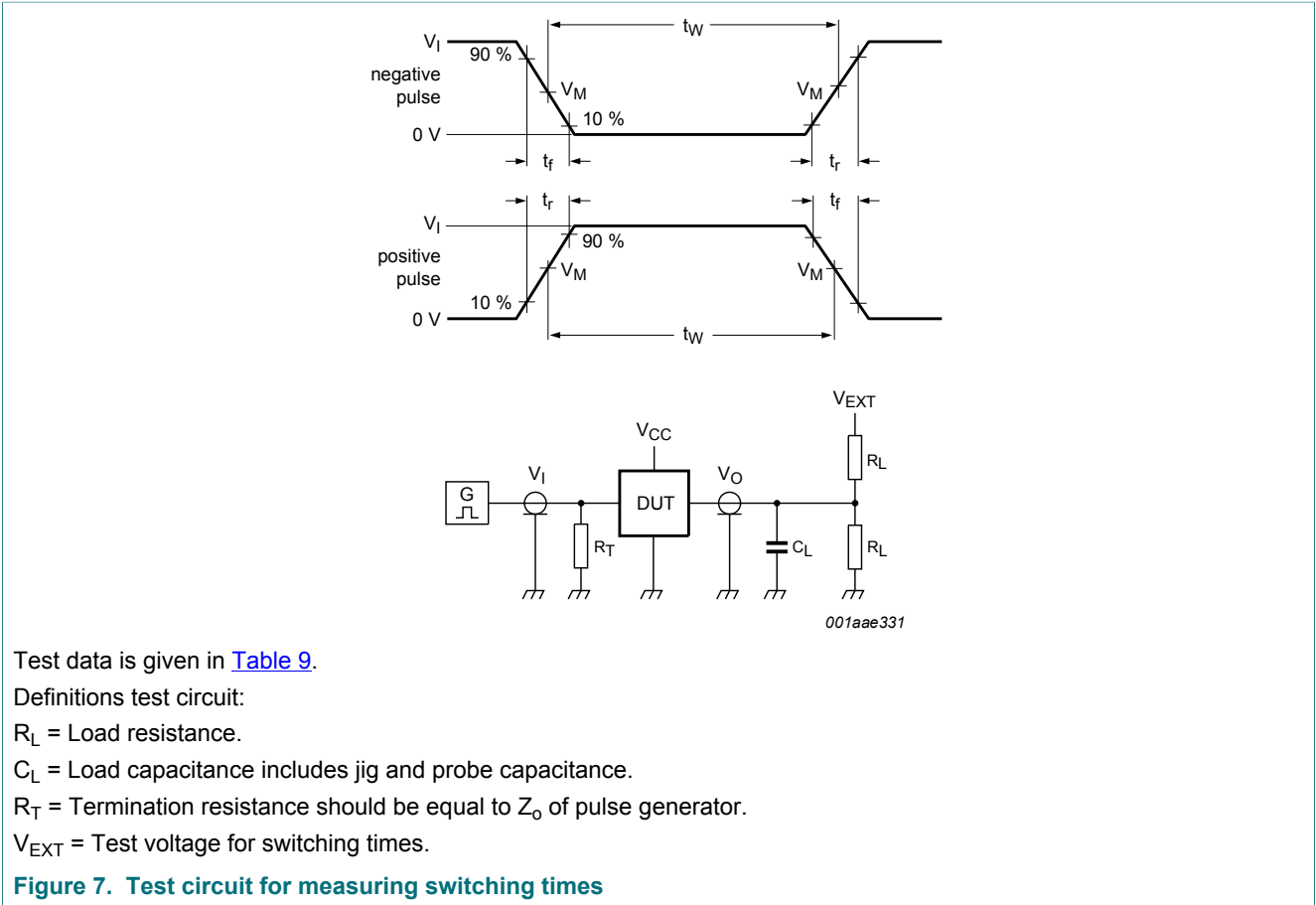


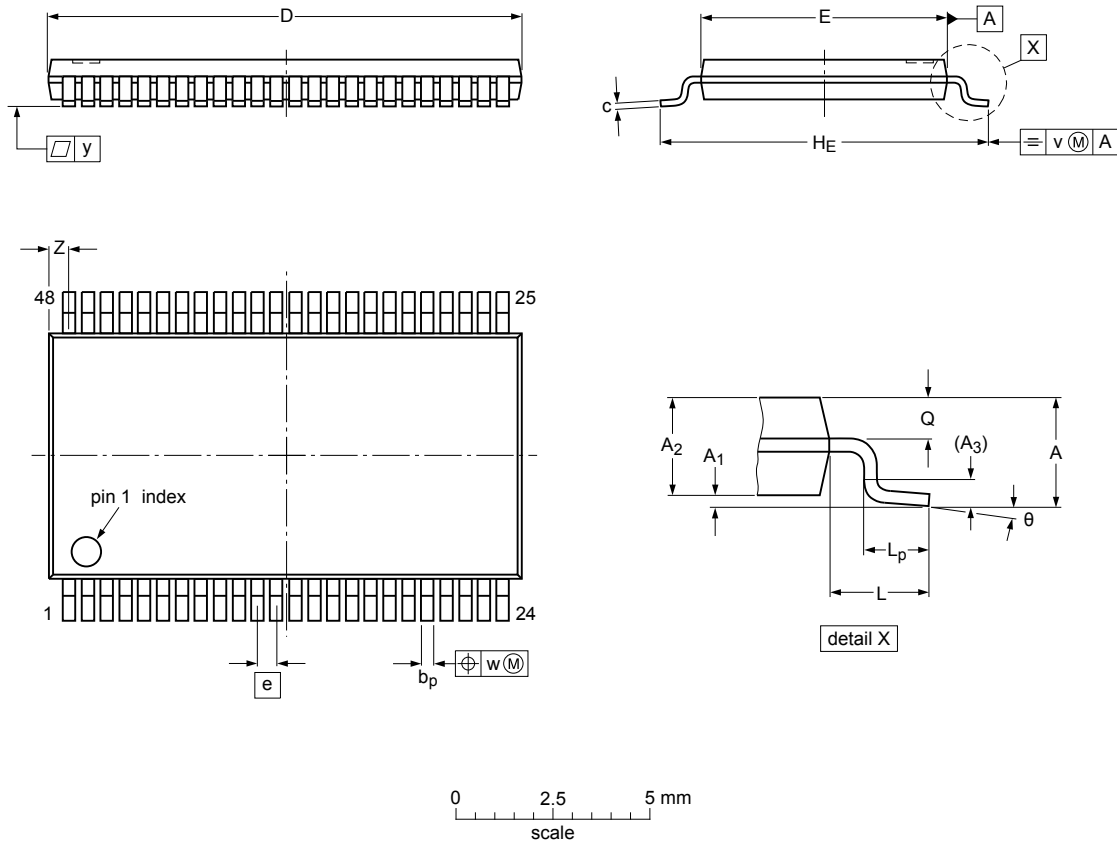
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}		
V_{CC}	V_I	t_r, t_f	C_L	R_L	t_{PLH}, t_{PHL}	t_{PLZ}, t_{PZL}	t_{PHZ}, t_{PZH}
2.3 V to 2.7 V	V_{CC}	≤ 2.0 ns	30 pF	500 Ω	open	$2 \times V_{CC}$	GND
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω	open	$2 \times V_{CC}$	GND

11 Package outline

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1 mm

SOT362-1



Dimensions (mm are the original dimensions)

Unit	A	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽²⁾	e	H _E	L	L _p	Q	v	w	y	Z	θ
max		0.15	1.05		0.28	0.2	12.6	6.2		8.3		0.8	0.50				0.8	8°
nom	1.2			0.25					0.5		1			0.25	0.08	0.1		
min		0.05	0.85		0.17	0.1	12.4	6.0		7.9		0.4	0.35				0.4	0°

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

sot362-1_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT362-1		MO-153			03-02-19 13-08-05

Figure 8. Package outline SOT362-1 (TSSOP48)

12 Abbreviations

Table 10. Abbreviations

Acronym	Description
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
TTL	Transistor-Transistor Logic

13 Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74ALVCH162245 v.3	20180116	Product data sheet	-	74ALVCH162245 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Type number 74ALVCH162245DL (SOT370-1 / SSOP48) removed. 			
74ALVCH162245 v.2	19980629	Product specification	-	74ALVCH162245 v.1
74ALVCH162245 v.1	19980504	Product specification	-	-

14 Legal information

14.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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