



## 74F620 • 74F623 Inverting Octal Bus Transceiver with 3-STATE Outputs

### General Description

These devices are octal bus transceivers designed for asynchronous two-way data flow between the A and B busses. Both busses are capable of sinking 64 mA and have 3-STATE outputs. Dual enable pins (GAB,  $\bar{G}BA$ ) allow data transmission from the A bus to the B bus or from the B bus to the A bus. The 74F620 is an inverting option of the 74F623.

### Features

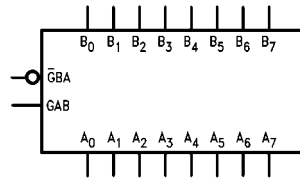
- Designed for asynchronous two-way data flow between busses
- Outputs sink 64 mA
- Dual enable inputs control direction of data flow
- Guaranteed 4000V minimum ESD protection
- 74F620 is an inverting option of the 74F623

### Ordering Code:

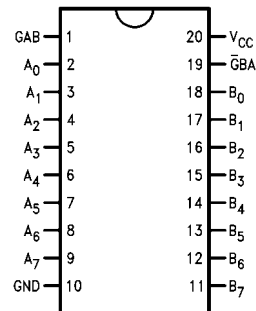
Order Number	Package Number	Package Description
74F620PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
74F623SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F623PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Unit Loading/Fan Out

Pin Names	Description	U.L. HIGH/LOW	Input $I_{IH}/I_{IL}$ Output $I_{OH}/I_{OL}$
$\overline{G}BA, GAB$	Enable Inputs	1.0/1.0	20 $\mu A$ / -0.6 mA
$A_0-A_7$	A Inputs or 3-STATE Outputs	3.5/1.083	70 $\mu A$ / -0.4 mA
$B_0-B_7$	B Inputs or 3-STATE Outputs	150/40	-3 mA / 64 mA

### Functional Description

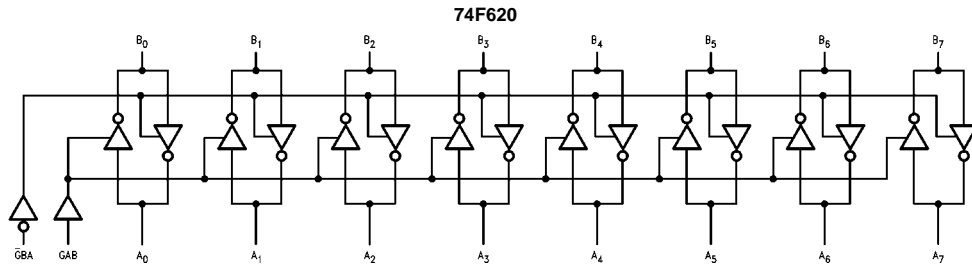
The enable inputs  $GAB$  and  $\overline{G}BA$  control whether data is transmitted from the A bus to the B bus or from the B bus to the A bus. If both  $\overline{G}BA$  and  $GAB$  are disabled ( $\overline{G}BA$  HIGH and  $GAB$  LOW), the outputs are in the high impedance state and data is stored at the A and B busses. When  $\overline{G}BA$  is active LOW, B data is sent to the A bus. When  $GAB$  is active HIGH, data from the A bus is sent to the B bus. If both enable inputs are active ( $\overline{G}BA$  LOW and  $GAB$  HIGH) B data is sent to the A bus while A data is sent to the B bus.

### Function Table

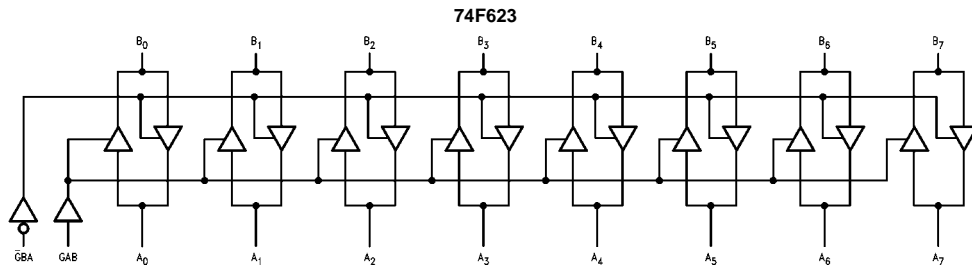
Enable Inputs		Operation	
$\overline{G}BA$	$GAB$	74F620	74F623
L	L	$\overline{B}$ Data to A Bus	B Data to A Bus
H	H	$\overline{A}$ Data to B Bus	A Data to B Bus
H	L	Z	Z
L	H	$\overline{B}$ Data to A Bus, $\overline{A}$ Data to B Bus	B Data to A Bus, A Data to B Bus

H = HIGH Voltage Level  
L = LOW Voltage Level  
Z = High Impedance

### Logic Diagrams



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.



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**Absolute Maximum Ratings**(Note 1)

Storage Temperature	-65°C to +150°C
Ambient Temperature under Bias	-55°C to +125°C
Junction Temperature under Bias	-55°C to +150°C
V <sub>CC</sub> Pin Potential to Ground Pin	-0.5V to +7.0V
Input Voltage (Note 2)	-0.5V to +7.0V
Input Current (Note 2)	-30 mA to +5.0 mA
Voltage Applied to Output in HIGH State (with V <sub>CC</sub> = 0V)	
Standard Output	-0.5V to V <sub>CC</sub>
3-STATE Output	-0.5V to +5.5V
Current Applied to Output in LOW State (Max)	twice the rated I <sub>OL</sub> (mA)
ESD Last Passing Voltage (Min)	4000V

**Recommended Operating Conditions**

Free Air Ambient Temperature	0°C to +70°C
Supply Voltage	+4.5V to +5.5V

**Note 1:** Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

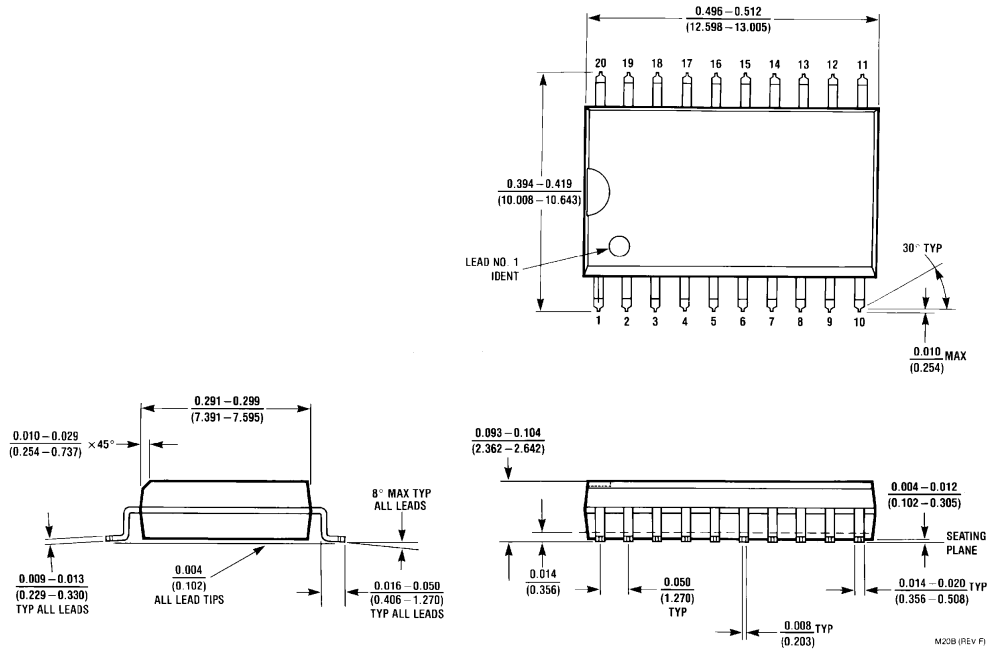
**Note 2:** Either voltage limit or current limit is sufficient to protect inputs.

**DC Electrical Characteristics**

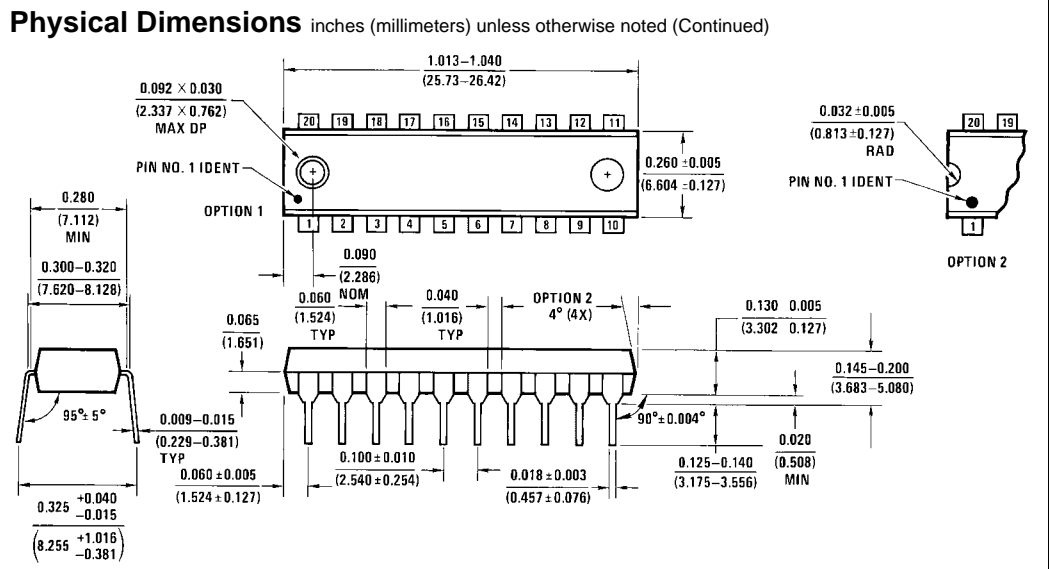
Symbol	Parameter	Min	Typ	Max	Units	V <sub>CC</sub>	Conditions
V <sub>IH</sub>	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V <sub>IL</sub>	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V <sub>CD</sub>	Input Clamp Diode Voltage			-1.2	V	Min	I <sub>IN</sub> = -18 mA (Non I/O Pins)
V <sub>OH</sub>	Output HIGH Voltage 10% V <sub>CC</sub>	2.0			V	Min	I <sub>OH</sub> = -15 mA (A <sub>n</sub> , B <sub>n</sub> )
V <sub>OL</sub>	Output LOW Voltage 10% V <sub>CC</sub>			0.55	V	Min	I <sub>OL</sub> = 64 mA (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IH</sub>	Input HIGH Current			5.0	μA	Max	V <sub>IN</sub> = 2.7V
I <sub>BVI</sub>	Input HIGH Current Breakdown Test			7.0	μA	Max	V <sub>IN</sub> = 7.0V (GBA, GAB)
I <sub>BVIT</sub>	Input HIGH Current Breakdown (I/O)			0.5	mA	Max	V <sub>IN</sub> = 5.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>CEX</sub>	Output HIGH Leakage Current			50	μA	Max	V <sub>OUT</sub> = V <sub>CC</sub>
V <sub>ID</sub>	Input Leakage Test	4.75			V	0.0	I <sub>ID</sub> = 1.9 μA All Other Pins Grounded
I <sub>OD</sub>	Output Leakage Circuit Current			3.75	μA	0.0	V <sub>IOD</sub> = 150 mV All Other Pins Grounded
I <sub>IL</sub>	Input LOW Current			-0.6	mA	Max	V <sub>IN</sub> = 0.5V (Non I/O Pins)
I <sub>IH</sub> + I <sub>OZH</sub>	Output Leakage Current			70	μA	Max	V <sub>OUT</sub> = 2.7V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>IL</sub> + I <sub>OZL</sub>	Output Leakage Current			-650	μA	Max	V <sub>OUT</sub> = 0.5V (A <sub>n</sub> , B <sub>n</sub> )
I <sub>OS</sub>	Output Short-Circuit Current	-100		-225	mA	Max	V <sub>OUT</sub> = 0V
I <sub>ZZ</sub>	Bus Drainage Test			500	μA	0.0V	V <sub>OUT</sub> = 5.25V
I <sub>CCH</sub>	Power Supply Current (74F620)			82	mA	Max	V <sub>O</sub> = HIGH, V <sub>IN</sub> = 0.2V
I <sub>CCL</sub>	Power Supply Current (74F620)			82	mA	Max	V <sub>O</sub> = LOW
I <sub>CCZ</sub>	Power Supply Current (74F620)			95	mA	Max	V <sub>O</sub> = HIGH Z
I <sub>CCH</sub>	Power Supply Current (74F623)			65	mA	Max	V <sub>O</sub> = HIGH
I <sub>CCL</sub>	Power Supply Current (74F623)			82	mA	Max	V <sub>O</sub> = LOW, V <sub>IN</sub> = 0.2V
I <sub>CCZ</sub>	Power Supply Current (74F623)			85	mA	Max	V <sub>O</sub> = HIGH Z

AC Electrical Characteristics							
Symbol	Parameter	T <sub>A</sub> = +25°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF			T <sub>A</sub> = 0°C to +70°C V <sub>CC</sub> = +5.0V C <sub>L</sub> = 50 pF		Units
		Min	Typ	Max	Min	Max	
t <sub>PLH</sub>	Propagation Delay	2.5		7.5	2.0	8.0	ns
t <sub>PHL</sub>	A Input to B Output (74F620)	2.0		7.0	2.0	7.0	
t <sub>PLH</sub>	Propagation Delay	2.5		7.5	2.0	8.0	ns
t <sub>PHL</sub>	B Input to A Output (74F620)	2.0		7.0	2.0	7.0	
t <sub>PLH</sub>	Propagation Delay	1.5		6.5	1.5	7.5	ns
t <sub>PHL</sub>	A Input to B Output (74F623)	2.0		7.0	2.0	7.5	
t <sub>PLH</sub>	Propagation Delay	1.5		6.5	1.5	7.5	ns
t <sub>PHL</sub>	B Input to A Output (74F623)	2.0		7.0	2.0	7.5	
t <sub>PZH</sub>	Enable Time	2.0		7.0	2.0	8.0	ns
t <sub>PZL</sub>	GBA Input to A Output	2.5		8.0	2.0	8.5	
t <sub>PHZ</sub>	Disable Time	1.5		6.5	1.5	7.5	
t <sub>PLZ</sub>	GBA Input to A Output	1.0		5.5	1.0	5.5	
t <sub>PZH</sub>	Enable Time	2.0		7.5	2.0	8.5	ns
t <sub>PZL</sub>	GAB Input to B Output (74F620)	3.0		8.0	2.0	8.5	
t <sub>PHZ</sub>	Disable Time	2.5		8.0	2.0	9.0	
t <sub>PLZ</sub>	GAB Input to B Output (74F620)	2.0		7.5	2.0	8.0	
t <sub>PZH</sub>	Enable Time	2.0		7.5	2.0	8.5	ns
t <sub>PZL</sub>	GAB Input to B Output (74F623)	2.5		8.0	2.0	8.5	
t <sub>PHZ</sub>	Disable Time	2.0		8.0	2.0	9.0	
t <sub>PLZ</sub>	GAB Input to B Output (74F623)	2.0		8.0	2.0	8.0	

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide  
Package Number M20B**



20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide Package Number N20A

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