THE DATASHEET OF

74HCT7541N,112

www.win-source.net 0086-755-83957316

74HC7541; 74HCT7541

Octal Schmitt trigger buffer/line driver; 3-state

Rev. 6 — 16 December 2013 Product data sheet

1. General description

The 74HC7541; 74HCT7541 is an 8-bit buffer/line driver with Schmitt-trigger inputs and 3-state outputs. The device features two output enables ($\overline{OE}1$ and $\overline{OE}2$). A HIGH on $\overline{OE}n$ causes the outputs to assume a high-impedance OFF-state. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC}. Schmitt trigger inputs transform slowly changing input signals into sharply defined jitter-free output signals.

2. Features and benefits

- Non-inverting outputs
- Low-power dissipation
- Input levels:
  - For 74HC7541: CMOS level
  - For 74HCT7541: TTL level
- Complies with JEDEC standard no. 7A
- ESD protection:
  - HBM JESD22-A114F exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Multiple package options
- Specified from −40 °C to +85 °C and from −40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74HC7541N	−40 °C to +125 °C	DIP20	plastic dual in-line package; 20 leads (300 mil)	SOT146-1
74HCT7541N				
74HC7541D	−40 °C to +125 °C	SO20	plastic small outline package; 20 leads; body width 7.5 mm	SOT163-1
74HCT7541D				
74HC7541DB	−40 °C to +125 °C	SSOP20	plastic shrink small outline package; 20 leads; body width 5.3 mm	SOT339-1
74HC7541PW	−40 °C to +125 °C	TSSOP20	plastic thin shrink small outline package; 20 leads; body width 4.4 mm	SOT360-1
74HCT7541PW				

4. Functional diagram

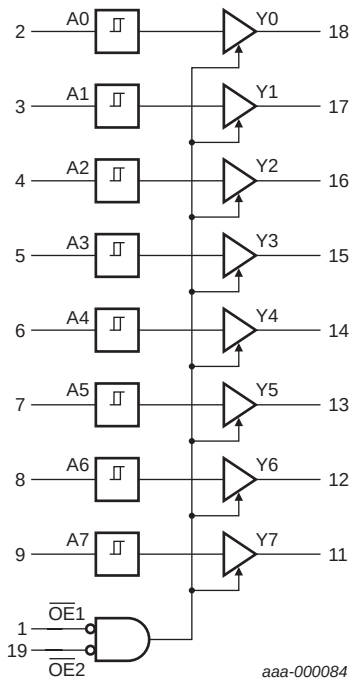


Fig 1. Logic symbol

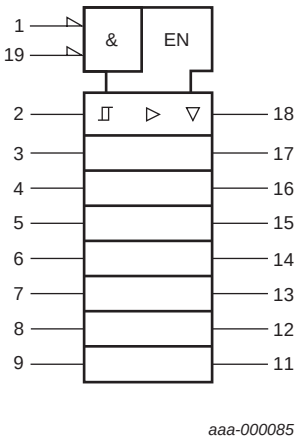


Fig 2. IEC logic symbol

5. Pinning information

5.1 Pinning

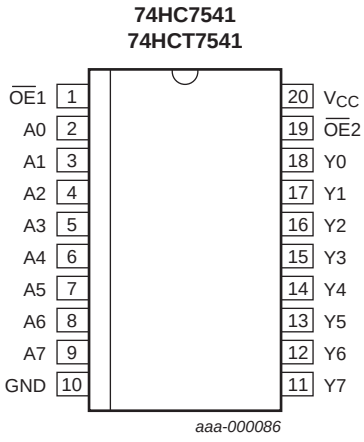


Fig 3. Pin configuration DIP20, SO20

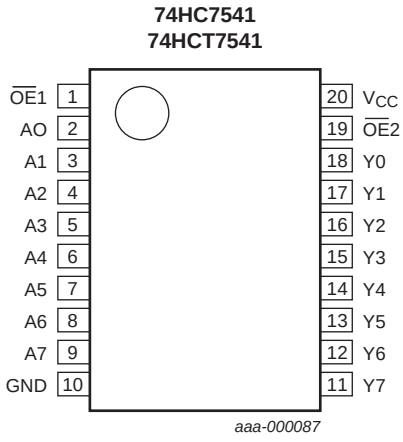


Fig 4. Pin configuration SSOP20, TSSOP20

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
$\overline{OE}1$	1	output enable input (active LOW)
A0 to A7	2, 3, 4, 5, 6, 7, 8, 9	data input
GND	10	ground (0 V)
Y0 to Y7	18, 17, 16, 15, 14, 13, 12, 11	data output
$\overline{OE}2$	19	output enable input (active LOW)
V_{CC}	20	supply voltage

6. Functional description

Table 3. Functional table[1]

Control		Input	Output
$\overline{OE}1$	$\overline{OE}2$	An	Yn
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{CC}	supply voltage			−0.5	+7	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{CC} + 0.5$ V	[1]	-	±20	mA
I_O	output current	-0.5 V $< V_O < V_{CC} + 0.5$ V		-	±35	mA
I_{CC}	supply current			-	70	mA
I_{GND}	ground current			−70	-	mA
T_{stg}	storage temperature			−65	+150	°C
P_{tot}	total power dissipation		[2]			
	DIP20			-	750	mW
	SO20, SSOP20, TSSOP20			-	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For DIP20 packages: above 70 °C the value of P_{tot} derates linearly with 12 mW/K.
For SO20 packages: above 70 °C the value of P_{tot} derates linearly with 8 mW/K.
For SSOP20 and TSSOP20 packages: above 60 °C the value of P_{tot} derates linearly with 5.5 mW/K.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	74HC7541			74HCT7541			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		–40	+25	+125	–40	+25	+125	°C

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC7541										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = –20 μA; V_{CC} = 2.0 V	1.9	2.0	-	1.9	-	1.9	-	V
		I_O = –20 μA; V_{CC} = 4.5 V	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –20 μA; V_{CC} = 6.0 V	5.9	6.0	-	5.9	-	5.9	-	V
		I_O = –6.0 mA; V_{CC} = 4.5 V	3.98	4.32	-	3.84	-	3.7	-	V
		I_O = –7.8 mA; V_{CC} = 6.0 V	5.48	5.81	-	5.34	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}								
		I_O = 20 μA; V_{CC} = 2.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 4.5 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 20 μA; V_{CC} = 6.0 V	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA; V_{CC} = 4.5 V	-	0.15	0.26	-	0.33	-	0.4	V
		I_O = 7.8 mA; V_{CC} = 6.0 V	-	0.16	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 6.0 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{T+}$ or V_{T-}; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; V_{CC} = 6.0 V; I_O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 6.0 V	-	-	8.0	-	80	-	160	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF
74HCT7541										
V_{OH}	HIGH-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = –20 μA	4.4	4.5	-	4.4	-	4.4	-	V
		I_O = –6.0 mA	3.98	4.32	-	3.84	-	3.7	-	V

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 6. Static characteristics *…continued*

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
V_{OL}	LOW-level output voltage	$V_I = V_{T+}$ or V_{T-}; V_{CC} = 4.5 V								
		I_O = 20 μA;	-	0	0.1	-	0.1	-	0.1	V
		I_O = 6.0 mA;	-	0.15	0.26	-	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; V_{CC} = 5.5 V	-	-	±0.1	-	±1.0	-	±1.0	μA
I_{OZ}	OFF-state output current	per input pin; $V_I = V_{T+}$ or V_{T-}; $V_O = V_{CC}$ or GND; other inputs at V_{CC} or GND; V_{CC} = 5.5 V; I_O = 0 A	-	-	±0.5	-	±5.0	-	±10	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; I_O = 0 A; V_{CC} = 5.5 V	-	-	8.0	-	80	-	160	μA
ΔI_{CC}	additional supply current	per input pin; I_O = 0 A; $V_I = V_{CC}$ – 2.1 V; other inputs at V_{CC} or GND; V_{CC} = 4.5 V to 5.5 V								
		An input	-	20	72	-	90	-	98	μA
		$\overline{OE}$n input	-	130	468	-	585	-	637	μA
C_I	input capacitance		-	3.5	-	-	-	-	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Figure 7.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
74HC7541									
t_{pd}	propagation delay	An to Yn; see Figure 5	[1]						
		V_{CC} = 2.0 V		-	39	120	150	180	ns
		V_{CC} = 4.5 V		-	14	24	30	36	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	10	-	-	-	ns
		V_{CC} = 6.0 V		-	11	20	26	32	ns
t_{en}	enable time	$\overline{OE}$n to Yn; see Figure 6	[1]						
		V_{CC} = 2.0 V		-	44	160	200	240	ns
		V_{CC} = 4.5 V		-	16	32	40	48	ns
		V_{CC} = 6.0 V		-	13	27	34	41	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Figure 6	[1]						
		V_{CC} = 2.0 V		-	58	160	200	240	ns
		V_{CC} = 4.5 V		-	21	32	40	48	ns
		V_{CC} = 6.0 V		-	17	27	34	41	ns

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Table 7. Dynamic characteristics

GND = 0 V; C_L = 50 pF; for test circuit see Figure 7.

Symbol	Parameter	Conditions		T_{amb} = 25 °C			T_{amb} = –40 °C to +125 °C		Unit
				Min	Typ	Max	Max (85 °C)	Max (125 °C)	
t_t	transition time	see Figure 5	[2]						
		V_{CC} = 2.0 V		-	14	60	75	90	ns
		V_{CC} = 4.5 V		-	5	12	15	18	ns
		V_{CC} = 6.0 V		-	4	10	13	15	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC}	[3]	-	30	-	-	-	pF
74HCT7541									
t_{pd}	propagation delay	An to Yn; see Figure 5	[1]						
		V_{CC} = 4.5 V		-	19	32	40	48	ns
		V_{CC} = 5.0 V; C_L = 15 pF		-	16	-	-	-	ns
t_{en}	enable time	$\overline{OE}$n to Yn; see Figure 6	[1]						
		V_{CC} = 4.5 V		-	18	32	40	48	ns
t_{dis}	disable time	$\overline{OE}$n to Yn; see Figure 6	[1]						
		V_{CC} = 4.5 V		-	20	32	40	48	ns
t_t	transition time	V_{CC} = 4.5 V; see Figure 5	[2]	-	5	12	15	18	ns
C_{PD}	power dissipation capacitance	per package; V_I = GND to V_{CC} – 1.5 V	[3]	-	32	-	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL}.
t_{en} is the same as t_{PZL} and t_{PZH}.
t_{dis} is the same as t_{PLZ} and t_{PHZ}.

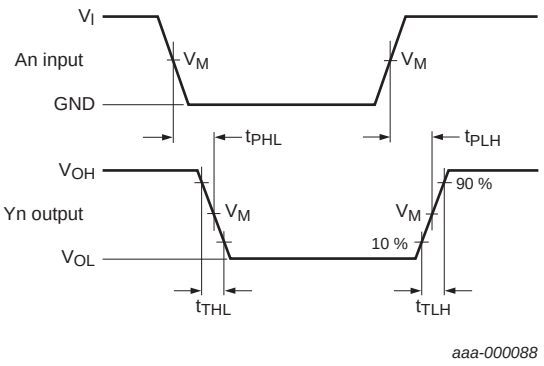
[2] t_t is the same as t_{THL} and t_{TLH}.

[3] C_{PD} is used to determine the dynamic power dissipation (P_D in µW):
$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
f_i = input frequency in MHz;
f_o = output frequency in MHz;
C_L = output load capacitance in pF;
V_{CC} = supply voltage in V;
N = number of inputs switching;
$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

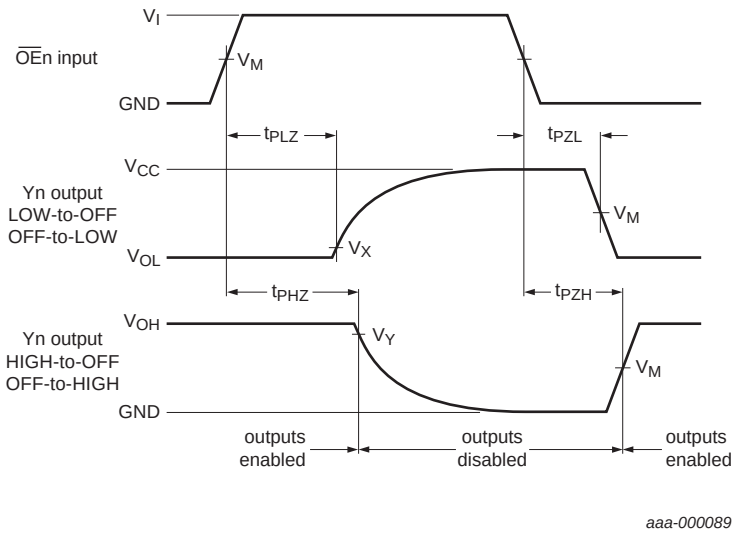
11. Waveforms



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 5. Input to output propagation delays



Measurement points are given in Table 8.

V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

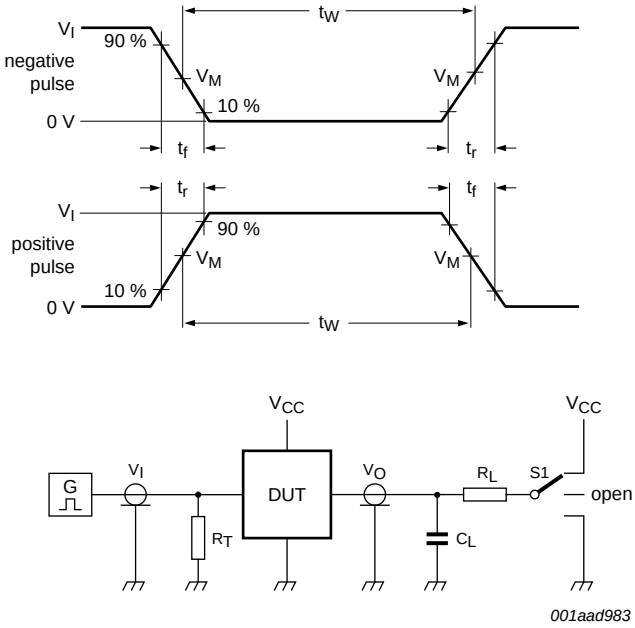
Fig 6. 3-state enable and disable times

Table 8. Measurement points

Type	Input	Output		
	V_M	V_M	V_X	V_Y
74HC7541	$0.5V_{CC}$	$0.5V_{CC}$	$0.1V_{CC}$	$0.9V_{CC}$
74HCT7541	1.3 V	1.3 V	$0.1V_{CC}$	$0.9V_{CC}$

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.



Test data is given in Table 9.

Definitions test circuit:

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator

C_L = Load capacitance including jig and probe capacitance

R_L = Load resistance

S1 = Test selection switch

Fig 7. Test circuit for measuring switching times

Table 9. Test data

Type	Input		Load		S1 position		
	V_I	t_r, t_f	C_L	R_L	t_{PHL}, t_{PLH}	t_{PZH}, t_{PHZ}	t_{PZL}, t_{PLZ}
74HC7541	V_{CC}	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}
74HCT7541	3 V	6 ns	15 pF, 50 pF	1 kΩ	open	GND	V_{CC}

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

12. Transfer characteristics

Table 10. Transfer characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); see Figure 8 and Figure 9.

Symbol	Parameter	Conditions	T_{amb} = 25 °C			T_{amb} = –40 °C to +85 °C		T_{amb} = –40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	Min	Max	
74HC7541										
V_{T+}	positive-going threshold voltage	V_{CC} = 2.0 V	-	-	1.5	-	1.5	-	1.5	V
		V_{CC} = 4.5 V	-	-	3.15	-	3.15	-	3.15	V
		V_{CC} = 6.0 V	-	-	4.2	-	4.2	-	4.2	V
V_{T-}	negative-going threshold voltage	V_{CC} = 2.0 V	0.3	-	-	0.3	-	0.3	-	V
		V_{CC} = 4.5 V	1.35	-	-	1.35	-	1.35	-	V
		V_{CC} = 6.0 V	1.8	-	-	1.8	-	1.8	-	V
V_H	hysteresis voltage	V_{CC} = 2.0 V	0.1	0.20	-	0.1	-	0.1	-	V
		V_{CC} = 4.5 V	0.25	0.40	-	0.25	-	0.25	-	V
		V_{CC} = 6.0 V	0.3	0.5	-	0.3	-	0.3	-	V
74HCT7541										
V_{T+}	positive-going threshold voltage	V_{CC} = 4.5 V	-	-	2.0	-	2.0	-	2.0	V
		V_{CC} = 5.5 V	-	-	2.1	-	2.1	-	2.1	V
V_{T-}	negative-going threshold voltage	V_{CC} = 4.5 V	0.7	-	-	0.64	-	0.6	-	V
		V_{CC} = 5.5 V	0.8	-	-	0.74	-	0.7	-	V
V_H	hysteresis voltage	V_{CC} = 4.5 V	0.17	0.23	-	-	-	-	-	V
		V_{CC} = 5.5 V	0.17	0.23	-	-	-	-	-	V

13. Transfer characteristics waveforms

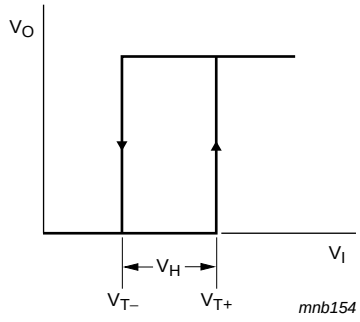


Fig 8. Transfer characteristics

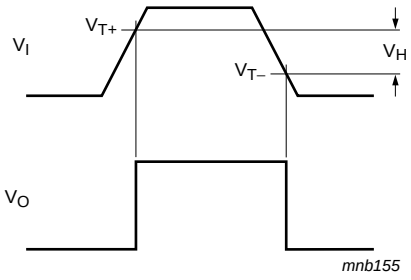


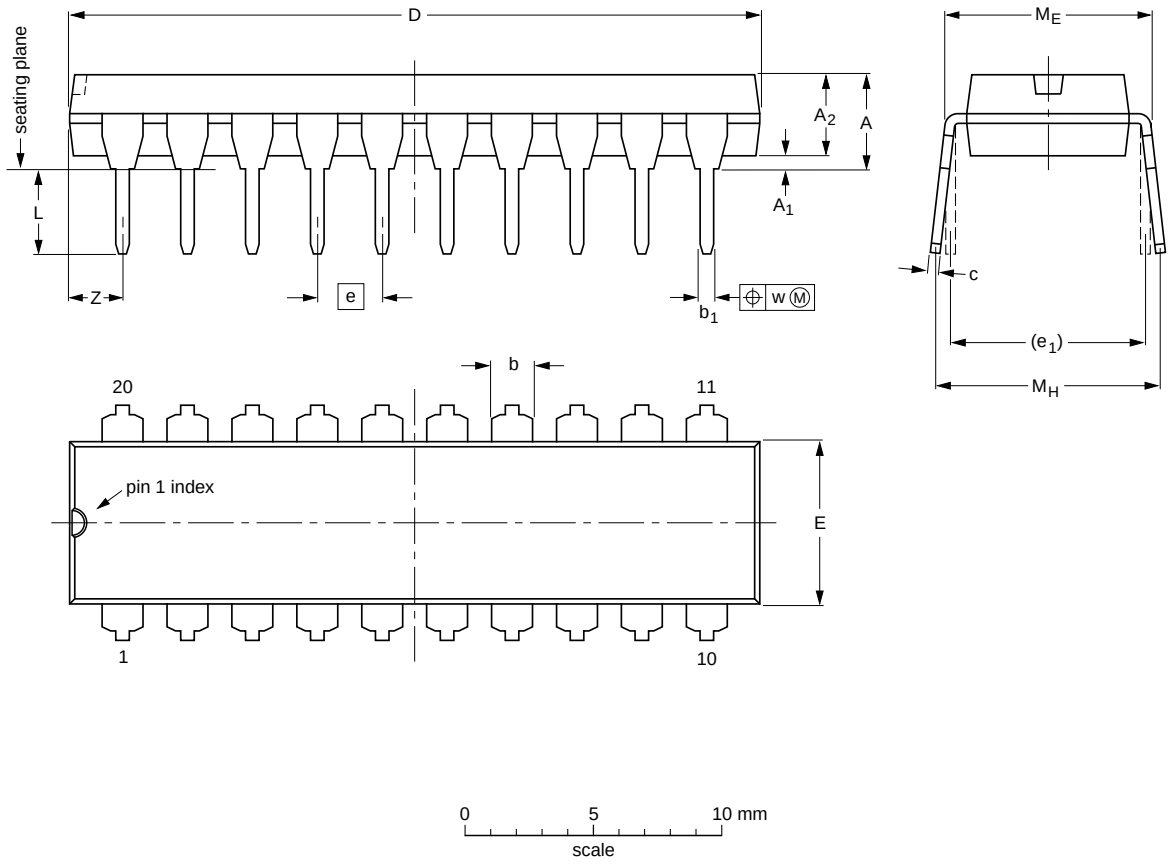
Fig 9. Transfer characteristics definitions

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

14. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil) **SOT146-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

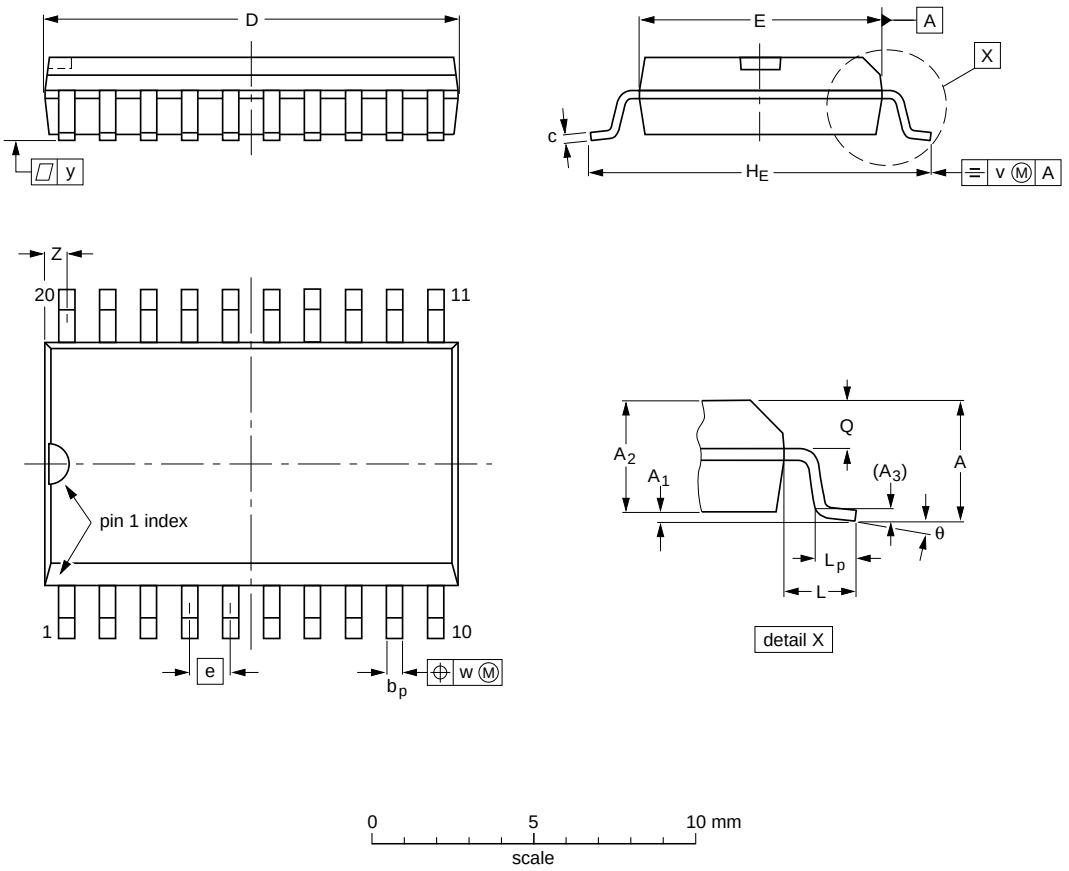
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT146-1		MS-001	SC-603			~~99-12-27~~ 03-02-13

Fig 10. Package outline SOT146-1 (DIP20)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.3 0.1	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.1	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.05	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

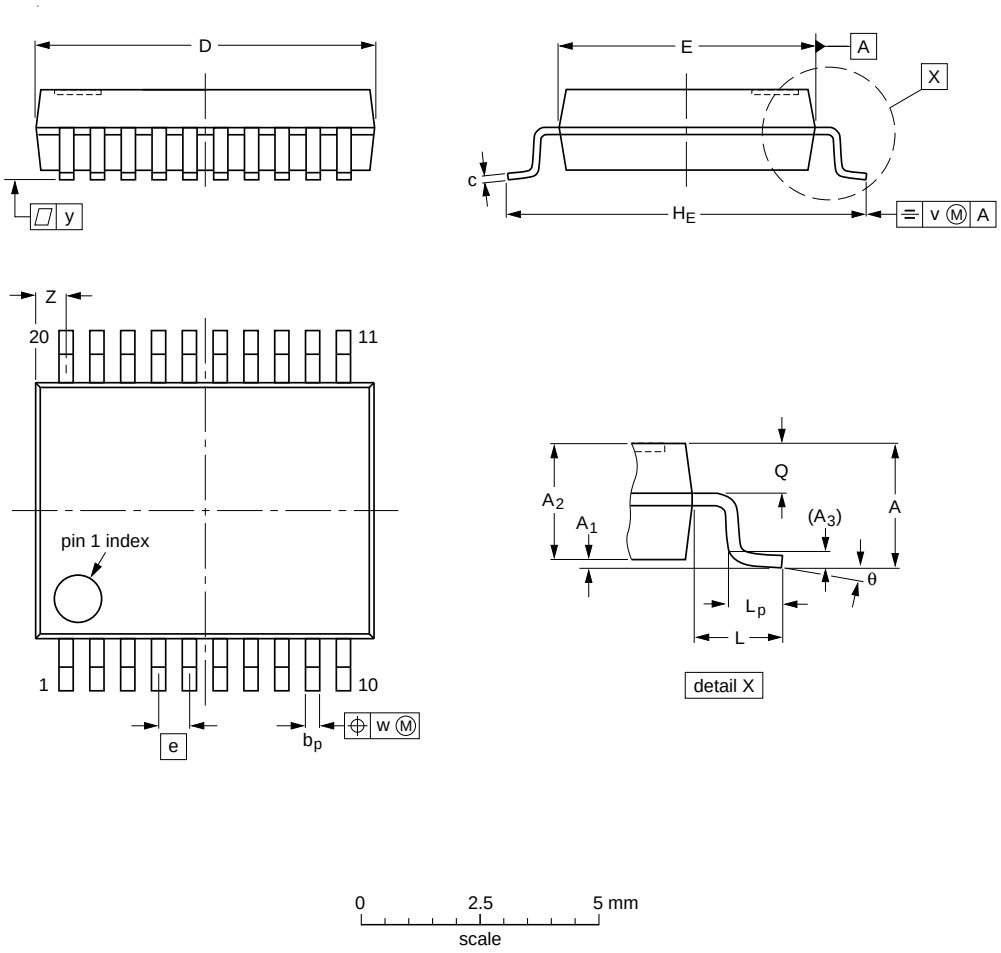
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT163-1	075E04	MS-013				~~99-12-27~~ 03-02-19

Fig 11. Package outline SOT163-1 (SO20)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8^o 0^o

Note

1. Plastic or metal protrusions of 0.2 mm maximum per side are not included.

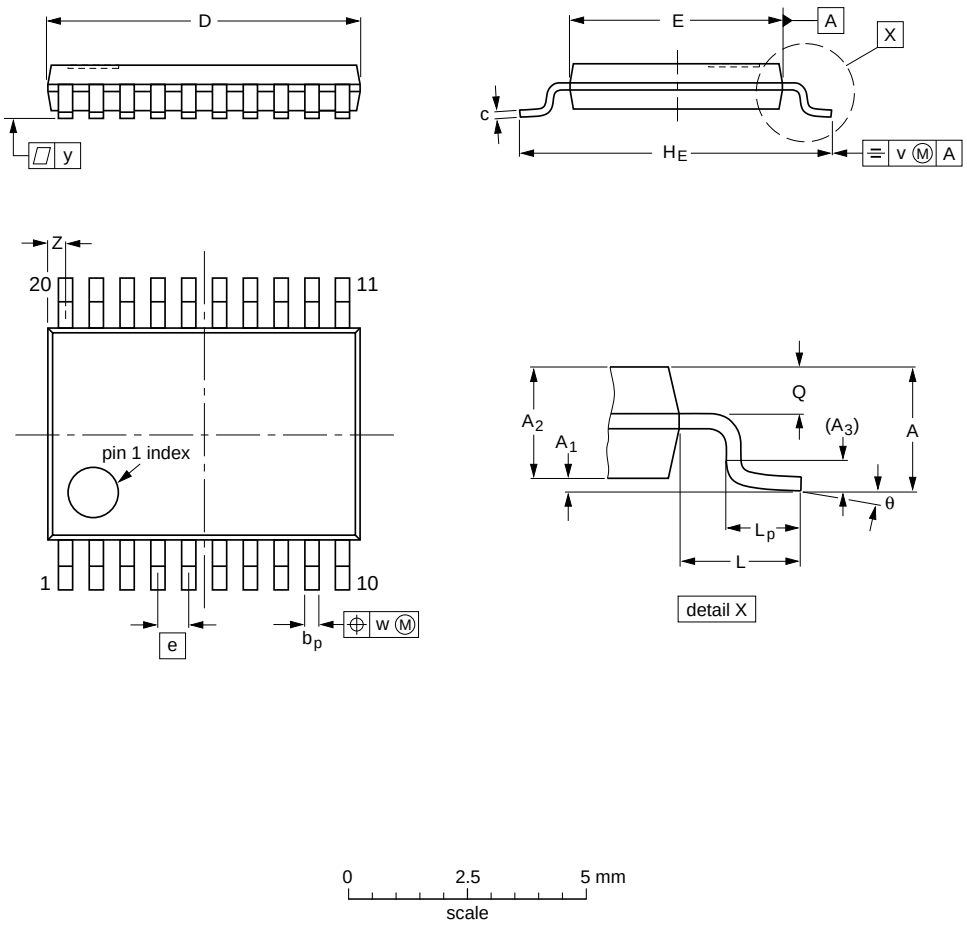
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT339-1		MO-150				~~99-12-27~~ 03-02-19

Fig 12. Package outline SOT339-1 (SSOP20)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm **SOT360-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT360-1		MO-153				~~99-12-27~~ 03-02-19

Fig 13. Package outline SOT360-1 (TSSOP20)

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

15. Abbreviations

Table 11. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
LSTTL	Low-power Schottky Transistor-Transistor Logic
MM	Machine Model

16. Revision history

Table 12. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT7541 v.6	20131216	Product data sheet	-	74HC_HCT7541 v.5
Modifications:	• New general description (errata).			
74HC_HCT7541 v.5	20121231	Product data sheet	-	74HC_HCT7541 v.4
Modifications:	• I_{OZ} added to static characteristics table.			
74HC_HCT7541 v.4	20111219	Product data sheet	-	74HC_HCT7541 v.3
Modifications:	• Legal pages updated.			
74HC_HCT7541 v.3	20110725	Product data sheet	-	74HC_HCT7541_CNV v.2
74HC_HCT7541_CNV v.2	19970917	Product specification	-	-

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between NXP Semiconductors and its customer, unless NXP Semiconductors and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the NXP Semiconductors product is deemed to offer functions and qualities beyond those described in the Product data sheet.

17.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. NXP Semiconductors takes no responsibility for the content in this document if provided by an information source outside of NXP Semiconductors.

In no event shall NXP Semiconductors be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, NXP Semiconductors' aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of NXP Semiconductors.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors and its suppliers accept no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using NXP Semiconductors products, and NXP Semiconductors accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the NXP Semiconductors product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

NXP Semiconductors does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using NXP Semiconductors products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). NXP does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. NXP Semiconductors hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of NXP Semiconductors products by customer.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Non-automotive qualified products — Unless this data sheet expressly states that this specific NXP Semiconductors product is automotive qualified, the product is not suitable for automotive use. It is neither qualified nor tested in accordance with automotive testing or application requirements. NXP Semiconductors accepts no liability for inclusion and/or use of non-automotive qualified products in automotive equipment or applications.

In the event that customer uses the product for design-in and use in automotive applications to automotive specifications and standards, customer (a) shall use the product without NXP Semiconductors' warranty of the product for such automotive applications, use and specifications, and (b) whenever customer uses the product for automotive applications beyond NXP Semiconductors' specifications such use shall be solely at customer's own risk, and (c) customer fully indemnifies NXP Semiconductors for any liability, damages or failed product claims resulting from customer design and use of the product for automotive applications beyond NXP Semiconductors' standard warranty and NXP Semiconductors' product specifications.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

All information provided in this document is subject to legal disclaimers.

© NXP B.V. 2013. All rights reserved.

19. Contents

1	**General description**	**1**
2	**Features and benefits**	**1**
3	**Ordering information**	**1**
4	**Functional diagram**	**2**
5	**Pinning information**	**2**
5.1	Pinning	2
5.2	Pin description	3
6	**Functional description**	**3**
7	**Limiting values**	**3**
8	**Recommended operating conditions**	**4**
9	**Static characteristics**	**4**
10	**Dynamic characteristics**	**5**
11	**Waveforms**	**7**
12	**Transfer characteristics**	**9**
13	**Transfer characteristics waveforms**	**9**
14	**Package outline**	**10**
15	**Abbreviations**	**14**
16	**Revision history**	**14**
17	**Legal information**	**15**
17.1	Data sheet status	15
17.2	Definitions	15
17.3	Disclaimers	15
17.4	Trademarks	16
18	**Contact information**	**16**
19	**Contents**	**17**

Please be aware that important notices concerning this document and the product(s) described herein, have been included in section 'Legal information'.

© NXP B.V. 2013. **All rights reserved.**

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 16 December 2013
Document identifier: 74HC_HCT7541

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View 74HCT7541N,112 on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management