



**THE DATASHEET OF  
74LVT16652ADL,512**



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Kind regards,

Team Nexperia

# 74LVT16652A

3.3 V 16-bit bus transceiver/register; 3-state

Rev. 03 — 12 January 2005

Product data sheet

## 1. General description

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The 74LVT16652A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3 V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output enable (OEAB and  $\overline{OEBA}$ ) inputs are provided to control the transceiver functions. Select control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A LOW input level selects real-time data, and a HIGH input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by LOW-to-HIGH transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select control or output enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high-impedance, each set of bus lines remains at its last level configuration.

## 2. Features

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- 16-bit bus interface
- 3-state buffers
- Output capability: +64 mA and -32 mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5 V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion and extraction permitted
- Power-up reset
- Power-up 3-state
- No bus current loading when output is tied to 5 V bus
- Latch-up protection exceeds 500 mA per JESD78
- ESD protection:
  - ◆ MIL STD 883 method 3015: exceeds 2000 V
  - ◆ Machine model: exceeds 200 V

**PHILIPS**

### 3. Quick reference data

**Table 1: Quick reference data**

$T_{amb} = 25^{\circ}\text{C}$ .

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PLH}$	propagation delay nAx to nBx or nBx to nAx	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	-	2.1	-	ns
$t_{PHL}$	propagation delay nAx to nBx or nBx to nAx	$C_L = 50\text{ pF}$ ; $V_{CC} = 3.3\text{ V}$	-	2.4	-	ns
$C_I$	input capacitance control pins	$V_I = 0\text{ V}$ or $3.0\text{ V}$	-	3	-	pF
$C_{I/O}$	I/O pin capacitance	outputs disabled; $V_I = 0\text{ V}$ or $3.0\text{ V}$	-	9	-	pF
$I_{CC}$	quiescent supply current	outputs disabled; $V_{CC} = 3.6\text{ V}$	-	70	-	$\mu\text{A}$

### 4. Ordering information

**Table 2: Ordering information**

Type number	Package			
	Temperature range	Name	Description	Version
74LVT16652ADGG	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	TSSOP56	plastic thin shrink small outline package; 56 leads; body width 6.1 mm	SOT364-1
74LVT16652ADL	$-40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$	SSOP56	plastic shrink small outline package; 56 leads; body width 7.5 mm	SOT371-1

5. Functional diagram

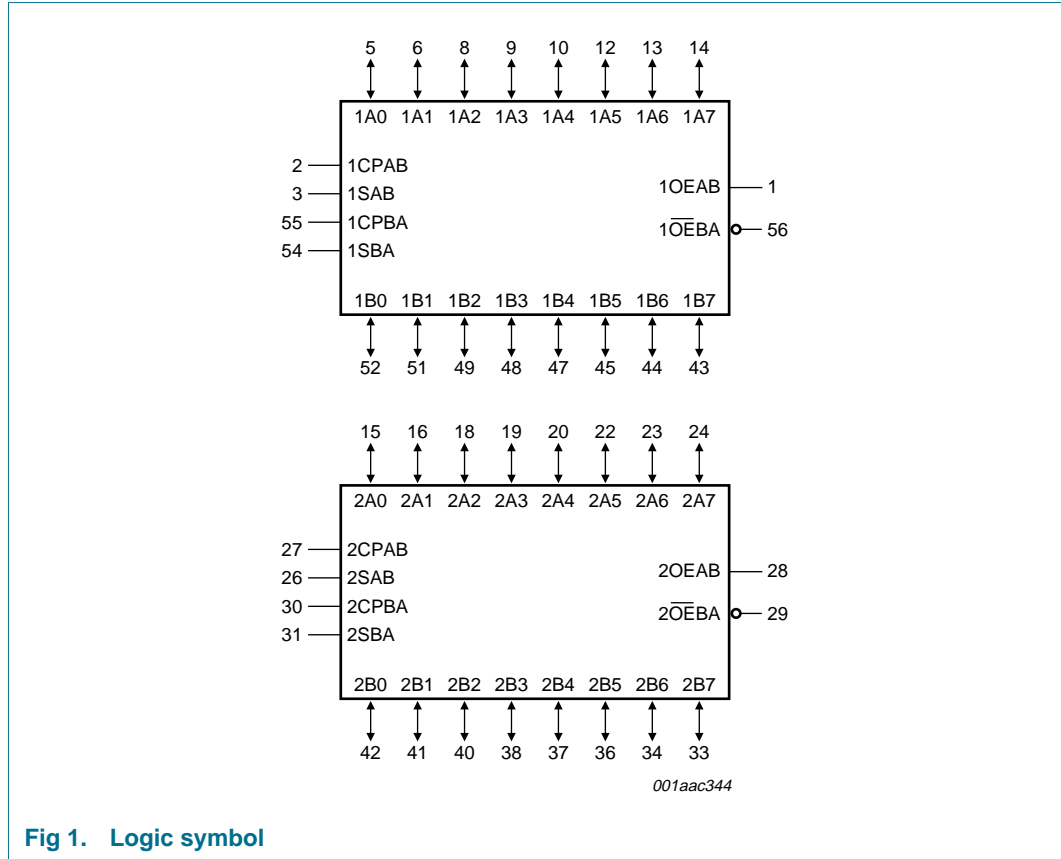


Fig 1. Logic symbol

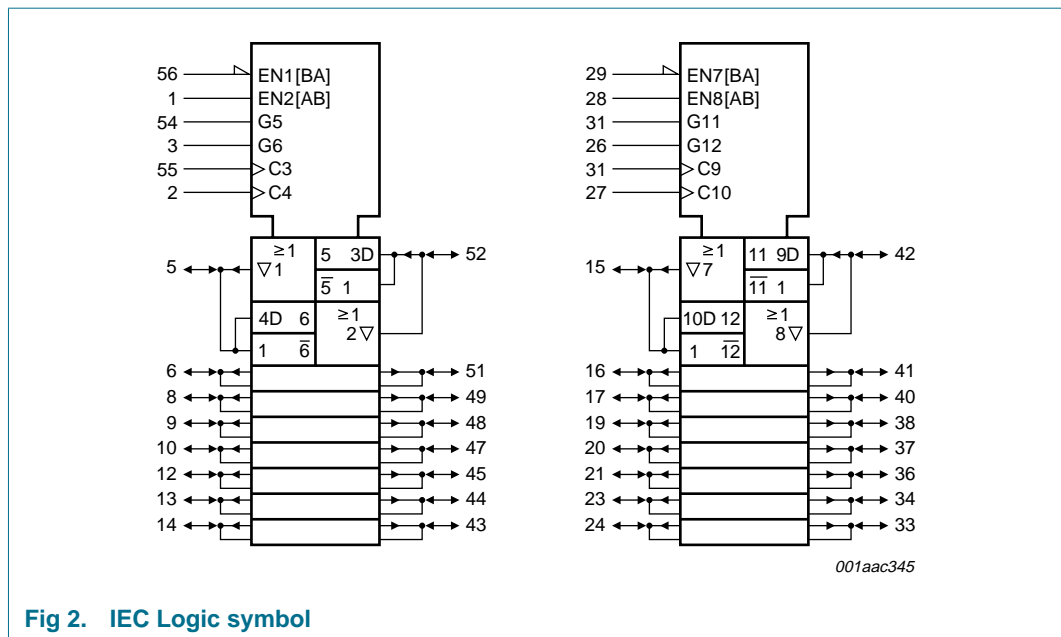


Fig 2. IEC Logic symbol

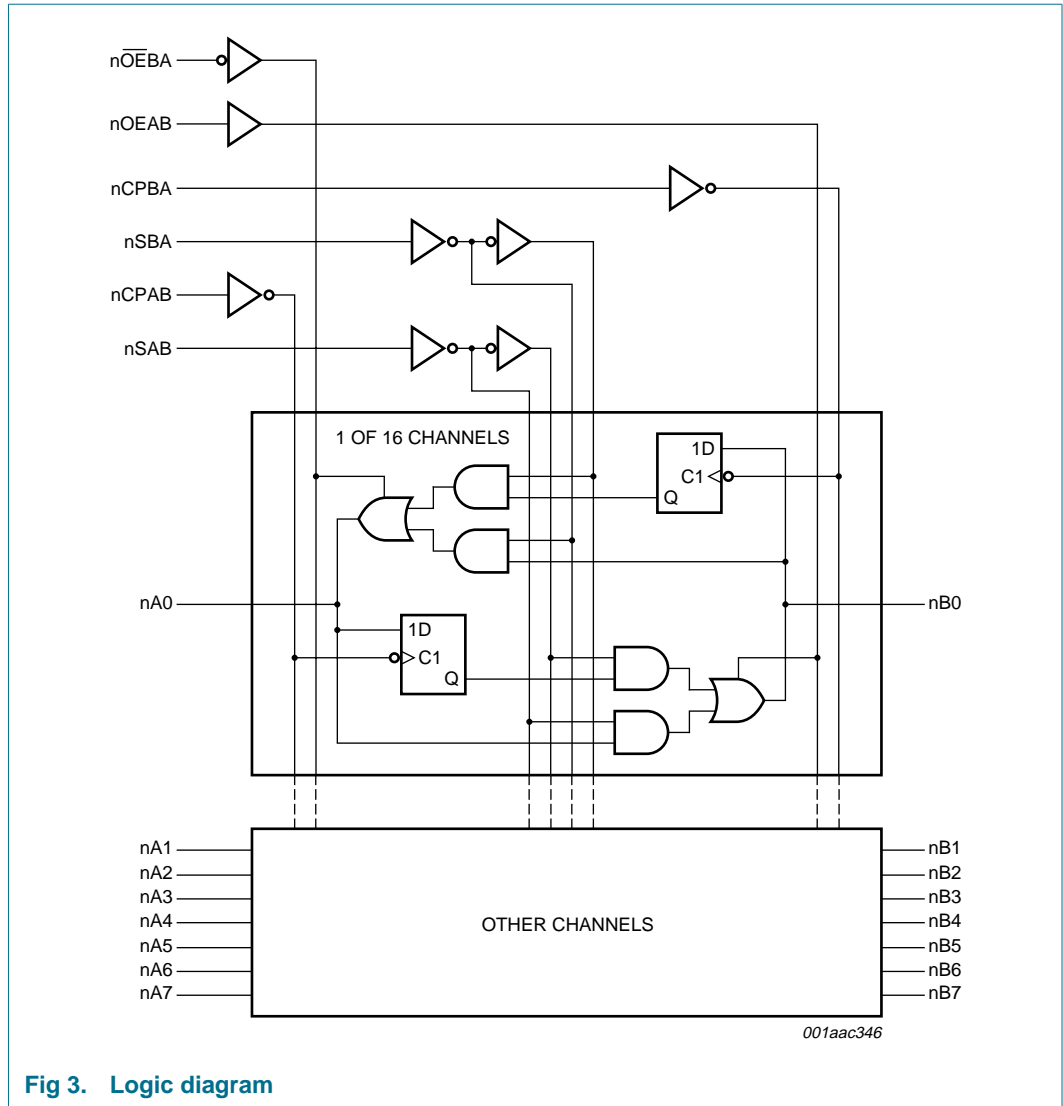
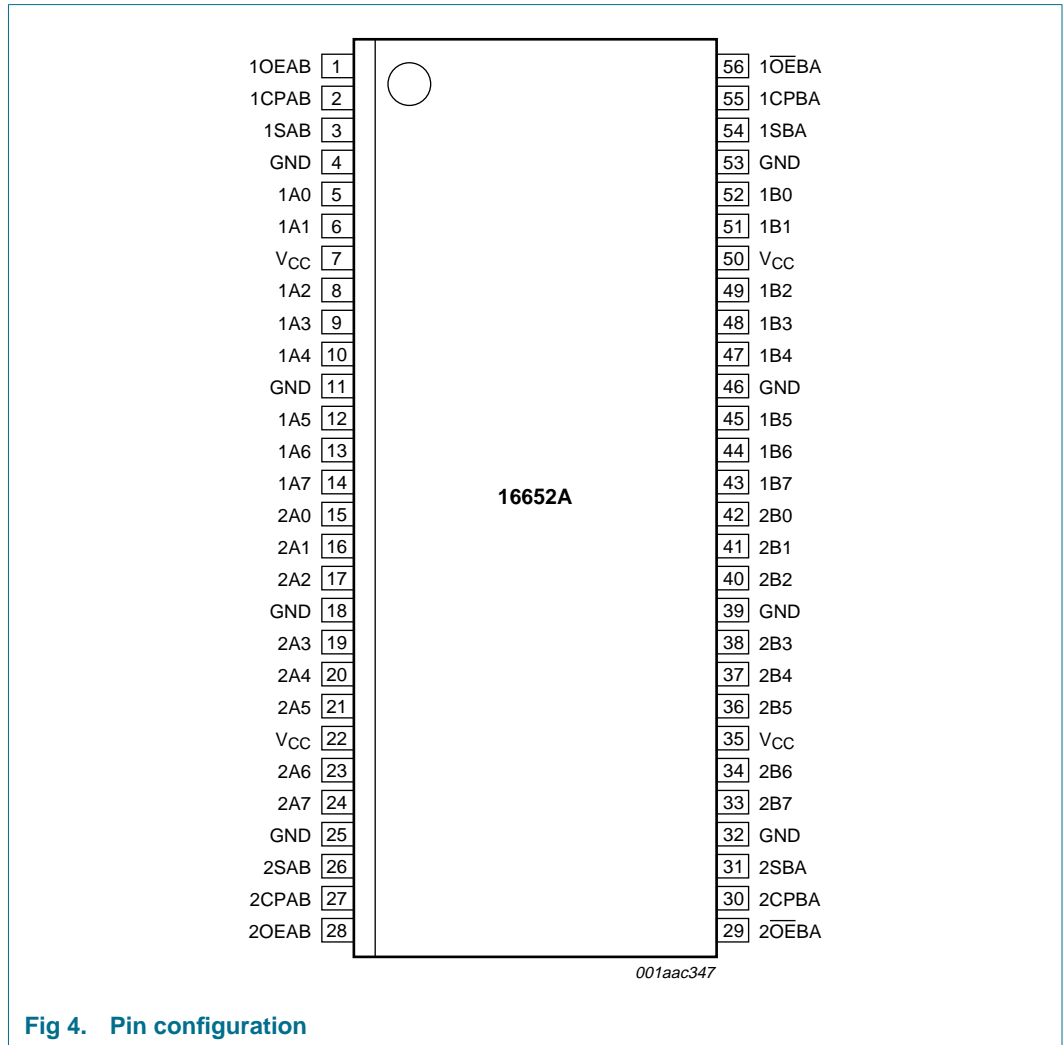


Fig 3. Logic diagram

## 6. Pinning information

### 6.1 Pinning



### 6.2 Pin description

**Table 3: Pin description**

Symbol	Pin	Description
1OEAB	1	A to B output enable input
1CPAB	2	A to B clock input
1SAB	3	A to B select input
GND	4	ground (0 V)
1A0	5	data input or output (A-side)
1A1	6	data input or output (A-side)
V <sub>CC</sub>	7	supply voltage
1A2	8	data input or output (A-side)

Table 3: Pin description ...continued

Symbol	Pin	Description
1A3	9	data input or output (A-side)
1A4	10	data input or output (A-side)
GND	11	ground (0 V)
1A5	12	data input or output (A-side)
1A6	13	data input or output (A-side)
1A7	14	data input or output (A-side)
2A0	15	data input or output (A-side)
2A1	16	data input or output (A-side)
2A2	17	data input or output (A-side)
GND	18	ground (0 V)
2A3	19	data input or output (A-side)
2A4	20	data input or output (A-side)
2A5	21	data input or output (A-side)
V <sub>CC</sub>	22	positive supply voltage
2A6	23	data input or output (A-side)
2A7	24	data input or output (A-side)
GND	25	ground (0 V)
2SAB	26	A to B select input
2CPAB	27	A to B clock input
2OEAB	28	A to B output enable input
2 $\overline{O}$ EBA	29	B to A output enable input
2CPBA	30	B to A clock input
2SBA	31	B to A select input
GND	32	ground (0 V)
2B7	33	data input or output (B-side)
2B6	34	data input or output (B-side)
V <sub>CC</sub>	35	supply voltage
2B5	36	data input or output (B-side)
2B4	37	data input or output (B-side)
2B3	38	data input or output (B-side)
GND	39	ground (0 V)
2B2	40	data input or output (B-side)
2B1	41	data input or output (B-side)
2B0	42	data input or output (B-side)
1B7	43	data input or output (B-side)
1B6	44	data input or output (B-side)
1B5	45	data input or output (B-side)
GND	46	ground (0 V)
1B4	47	data input or output (B-side)
1B3	48	data input or output (B-side)
1B2	49	data input or output (B-side)

Table 3: Pin description ...continued

Symbol	Pin	Description
V <sub>CC</sub>	50	supply voltage
1B1	51	data input or output (B-side)
1B0	52	data input or output (B-side)
GND	53	ground (0 V)
1SBA	54	B to A select input
1CPBA	55	B to A clock input
1 $\overline{\text{OE}}$ BA	56	B to A output enable input

## 7. Functional description

### 7.1 Function table

Table 4: Function table [1]

Operating mode	Input						Data I/O	
	nOEAB	n $\overline{\text{OE}}$ BA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx
Isolation	L	H	H or L	H or L	X	X	input	input
Store A and B data	L	H	↑	↑	X	X	input	input
Store A, hold B	X	H	↑	H or L	X	X	input	unspecified output [2]
Store A in both registers	H	H	↑	↑	[3]	X	input	unspecified output [2]
Hold A, store B	L	X	H or L	↑	X	X	unspecified output [2]	input
Store B in both registers	L	L	↑	↑	X	[3]	unspecified output [2]	input
Real-time B data to A bus	L	L	X	X	X	L	output	input
Store B data to A bus	L	L	X	H or L	X	H	output	input
Real-time A data to B bus	H	H	X	X	L	X	input	output
Store A data to B bus	H	H	H or L	X	H	X	input	output
Stored A data to B bus and stored B data to A bus	H	L	H or L	H or L	H	H	output	output

- [1] H = HIGH voltage level;  
L = LOW voltage level;  
X = don't care;  
↑ = LOW-to-HIGH clock transition.

- [2] The data output function may be enabled or disabled by various signals at the n $\overline{\text{OE}}$ BA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every LOW-to-HIGH transition of the clock.

- [3] If both select controls (nSAB and nSBA) are LOW, then clocks can occur simultaneously. If either select control is HIGH, the clocks must be staggered in order to load both registers.

7.2 Bus management function

Figure 5 demonstrates the four fundamental bus management functions that can be performed with the 74LVT16652A. The select pins determine whether data is stored or transferred through the device in real time. The output enable pins determine the direction of the data flow.

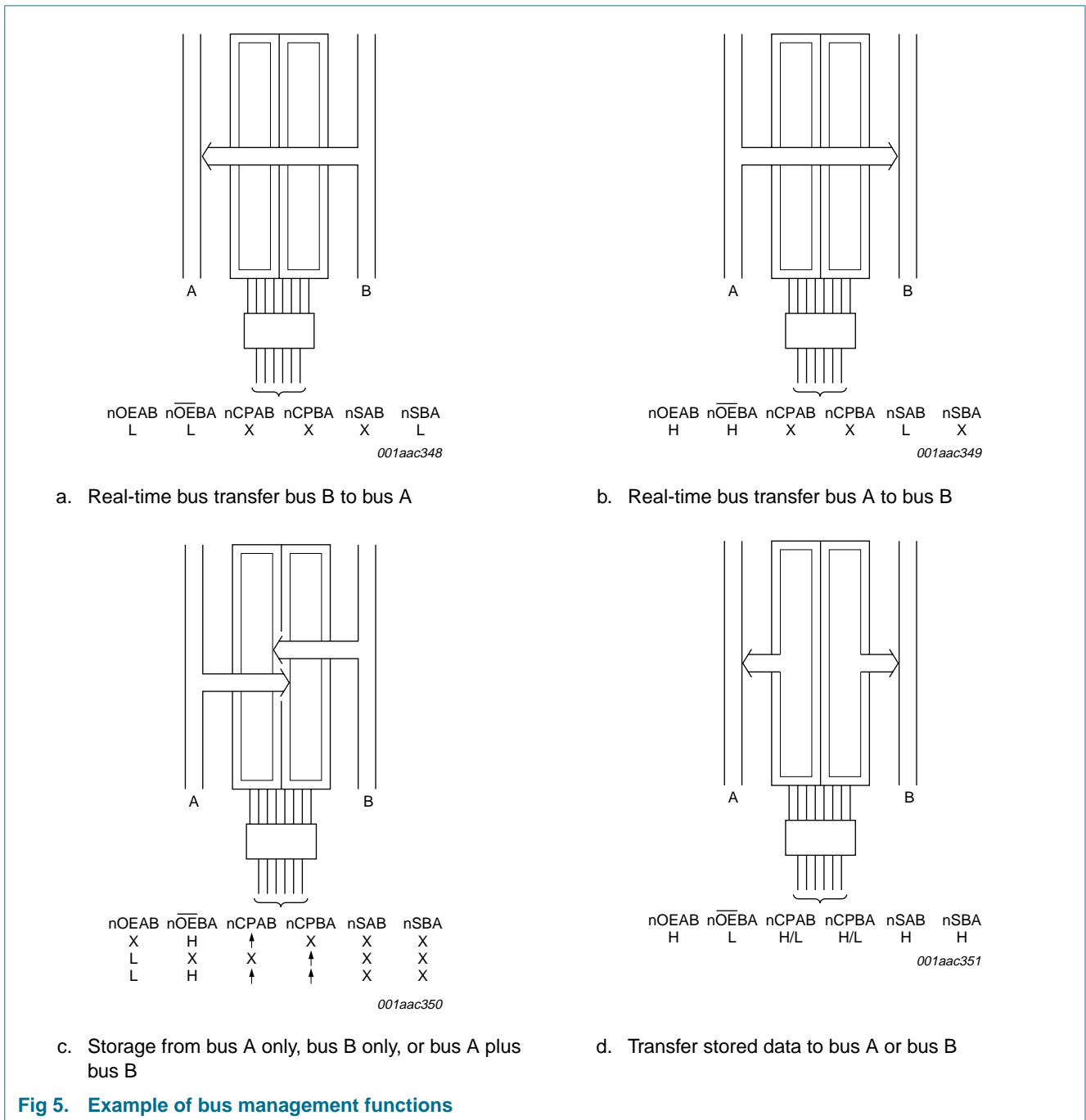


Fig 5. Example of bus management functions

## 8. Limiting values

**Table 5: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{CC}$	DC supply voltage		-0.5	+4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$ V	-50	-	mA
$V_I$	DC input voltage		[2] -0.5	+7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$ V	-50	-	mA
$V_O$	DC output voltage	output in OFF or HIGH-state	[2] -0.5	+7.0	V
$I_O$	DC output current	output in LOW-state	-	128	mA
		output in HIGH-state	-64	-	mA
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		[1] -	150	°C

[1] The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability.

[2] The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

## 9. Recommended operating conditions

**Table 6: Recommended operating conditions**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{CC}$	supply voltage		2.7	-	3.6	V
$V_I$	input voltage		0	-	5.5	V
$V_{IH}$	HIGH-level input voltage		2.0	-	-	V
$V_{IL}$	LOW-level input voltage		-	-	0.8	V
$I_{OH}$	HIGH-level output current		-	-	-32	mA
$I_{OL}$	LOW-level output current		-	-	32	mA
		duty cycle $\leq 50$ %; $f \geq 1$ kHz	-	-	64	mA
$\Delta t/\Delta V$	input transition rise or fall rate	outputs enabled	-	-	10	ns/V
$T_{amb}$	ambient temperature		-40	-	+85	°C

## 10. Static characteristics

**Table 7: Static characteristics**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>T<sub>amb</sub> = -40 °C to +85 °C [1]</b>							
V <sub>IK</sub>	input clamp voltage	V <sub>CC</sub> = 2.7 V; I <sub>IK</sub> = -18 mA	-	-0.85	-1.2	V	
V <sub>OH</sub>	HIGH-level output voltage	V <sub>CC</sub> = 2.7 V to 3.6 V; I <sub>OH</sub> = -100 μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>	-	V	
		V <sub>CC</sub> = 2.7 V; I <sub>OH</sub> = -8 mA	2.4	2.5	-	V	
		V <sub>CC</sub> = 3.0 V; I <sub>OH</sub> = -32 mA	2.0	2.3	-	V	
V <sub>OL</sub>	LOW-level output voltage	V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 100 μA	-	0.07	0.2	V	
		V <sub>CC</sub> = 2.7 V; I <sub>OL</sub> = 24 mA	-	0.3	0.5	V	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 16 mA	-	0.25	0.4	V	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 32 mA	-	0.3	0.5	V	
		V <sub>CC</sub> = 3.0 V; I <sub>OL</sub> = 64 mA	-	0.4	0.55	V	
V <sub>RST</sub>	power-up output low voltage	V <sub>CC</sub> = 3.6 V; I <sub>O</sub> = 1 mA; V <sub>I</sub> = GND or V <sub>CC</sub>	[2] -	0.11	0.55	V	
I <sub>LI</sub>	input leakage current	control pins	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub> or GND	-	0.1	±1	μA
			V <sub>CC</sub> = 0 V or 3.6 V; V <sub>I</sub> = 5.5 V	-	0.1	10	μA
	I/O data pins	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 5.5 V	[3] -	0.1	20	μA	
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = V <sub>CC</sub>	[3] -	0.1	10	μA	
		V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = 0 V	[3] -	+0.1	-5	μA	
I <sub>OFF</sub>	output off current	V <sub>CC</sub> = 0 V; V <sub>I</sub> or V <sub>O</sub> = 0 V to 4.5 V	-	0.1	±100	μA	
I <sub>HOLD</sub>	bus-hold current A or B outputs	V <sub>CC</sub> = 3 V; V <sub>I</sub> = 0.8 V	[4] 75	135	-	μA	
		V <sub>CC</sub> = 3 V; V <sub>I</sub> = 2.0 V	[4] -75	-140	-	μA	
		V <sub>CC</sub> = 0 V to 3.6 V; V <sub>I</sub> = 3.6 V	[4] ±500	-	-	μA	
I <sub>EX</sub>	current into an output in the HIGH-state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5 V; V <sub>CC</sub> = 3.0 V	-	45	125	μA	
I <sub>PU</sub> , I <sub>PD</sub>	power-up or down 3-state output current	V <sub>CC</sub> ≤ 1.2 V; V <sub>O</sub> = 0.5 V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; pins nOEAB and nOEBA are don't care	[5] -	35	±100	μA	
I <sub>CC</sub>	quiescent supply current	V <sub>CC</sub> = 3.6 V; V <sub>I</sub> = GND or V <sub>CC</sub> and I <sub>O</sub> = 0 A					
		outputs HIGH	-	0.07	0.12	mA	
		outputs LOW	[6] -	4.9	6	mA	
	outputs disabled	[7] -	0.07	0.12	mA		

**Table 7: Static characteristics ...continued**

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta I_{CC}$	additional supply current per input pin	$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ ; one input at $V_{CC} - 0.6 \text{ V}$ ; other inputs at $V_{CC}$ or GND	[8] -	0.1	0.2	mA
$C_I$	input capacitance control pins	$V_I = 0 \text{ V}$ or $3.0 \text{ V}$	-	3	-	pF
$C_{I/O}$	I/O pin capacitance	outputs disabled; $V_I = 0 \text{ V}$ or $3.0 \text{ V}$	-	9	-	pF

- [1] All typical values are measured at  $V_{CC} = 3.3 \text{ V}$  and  $T_{amb} = 25 \text{ }^\circ\text{C}$ .
- [2] For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
- [3] Unused pins at  $V_{CC}$  or GND.
- [4] This is the bus-hold overdrive current required to force the input to the opposite logic state.
- [5] This parameter is valid for any  $V_{CC}$  between 0 V and 1.2 V with a transition time of up to 10 ms. From  $V_{CC} = 1.2 \text{ V}$  to  $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$  a transition time of 100  $\mu\text{s}$  is permitted. This parameter is valid for  $T_{amb} = 25 \text{ }^\circ\text{C}$  only.
- [6]  $I_{CC}$  is measured with 16 outputs LOW.
- [7]  $I_{CC}$  is measured with outputs pulled to  $V_{CC}$  or GND.
- [8] This is the increase in supply current for each input at the specified voltage level other than  $V_{CC}$  or GND.

## 11. Dynamic characteristics

**Table 8: Dynamic characteristics**

$GND = 0 \text{ V}$ ;  $t_r = t_f = 2.5 \text{ ns}$ ;  $C_L = 50 \text{ pF}$ ;  $R_L = 500 \text{ } \Omega$ ; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40 \text{ }^\circ\text{C}</math> to <math>+85 \text{ }^\circ\text{C}</math> [1]</b>						
$f_{max}$	maximum clock frequency	$V_{CC} = 2.7 \text{ V}$ or $3.3 \text{ V} \pm 0.3 \text{ V}$ ; see <a href="#">Figure 6</a>	150	180	-	MHz
$t_{PLH}$	propagation delay nAx to nBx or nBx to nAx	see <a href="#">Figure 7</a>				
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	0.5	2.1	3.4	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	3.9	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.5	2.5	4.2	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	4.7	ns
	propagation delay nSAB to nBx or nSBA to nAx	see <a href="#">Figure 8</a>				
		$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$	1.0	2.3	4.5	ns
		$V_{CC} = 2.7 \text{ V}$	-	-	5.4	ns

**Table 8: Dynamic characteristics ...continued**

$GND = 0\text{ V}$ ;  $t_r = t_f = 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 500\ \Omega$ ; test circuit see [Figure 12](#).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{PHL}$	propagation delay nAx to nBx or nBx to nAx	see <a href="#">Figure 7</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	0.5	2.4	3.4	ns
		$V_{CC} = 2.7\text{ V}$	-	-	3.9	ns
	propagation delay nCPAB to nBx or nCPBA to nAx	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.5	2.7	4.2	ns
		$V_{CC} = 2.7\text{ V}$	-	-	4.7	ns
propagation delay nSAB to nBx or nSBA to nAx	see <a href="#">Figure 8</a>					
	$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.5	4.5	ns	
	$V_{CC} = 2.7\text{ V}$	-	-	5.4	ns	
$t_{PZH}$	output enable time nOEBA to nAx	see <a href="#">Figure 9</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	2.7	4.3	ns
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
	output enable time nOEAB to nBx	see <a href="#">Figure 10</a>				
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		1.0	2.6	4.2	ns	
	$V_{CC} = 2.7\text{ V}$	-	-	4.9	ns	
$t_{PZL}$	output enable time nOEBA to nAx	see <a href="#">Figure 10</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	3.1	4.3	ns
		$V_{CC} = 2.7\text{ V}$	-	-	5.0	ns
	output enable time nOEAB to nBx	see <a href="#">Figure 9</a>				
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		1.0	2.9	4.2	ns	
	$V_{CC} = 2.7\text{ V}$	-	-	4.9	ns	
$t_{PHZ}$	output disable time nOEBA to nAx	see <a href="#">Figure 9</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.5	3.1	4.9	ns
		$V_{CC} = 2.7\text{ V}$	-	-	5.3	ns
	output disable time nOEAB to nBx	see <a href="#">Figure 9</a>				
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		1.5	3.4	5.2	ns	
	$V_{CC} = 2.7\text{ V}$	-	-	5.8	ns	
$t_{PLZ}$	output disable time nOEBA to nAx	see <a href="#">Figure 10</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.5	2.8	4.4	ns
		$V_{CC} = 2.7\text{ V}$	-	-	4.6	ns
	output disable time nOEAB to nBx	see <a href="#">Figure 10</a>				
$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		1.5	3.0	4.4	ns	
	$V_{CC} = 2.7\text{ V}$	-	-	4.6	ns	

[1] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

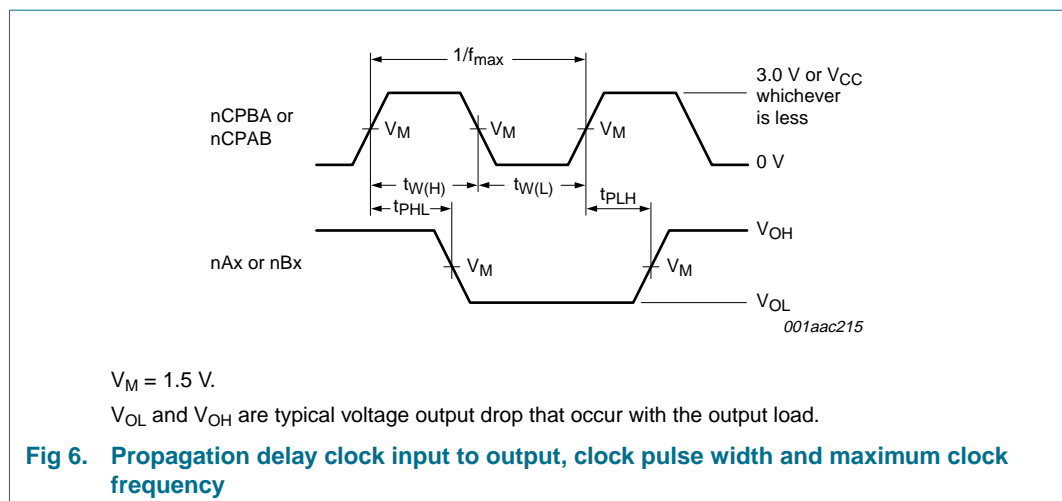
**Table 9: Dynamic characteristics setup requirements**

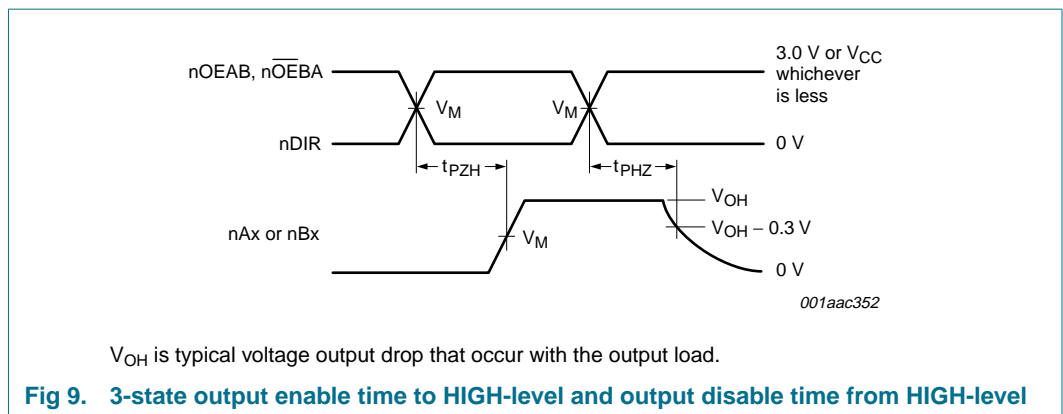
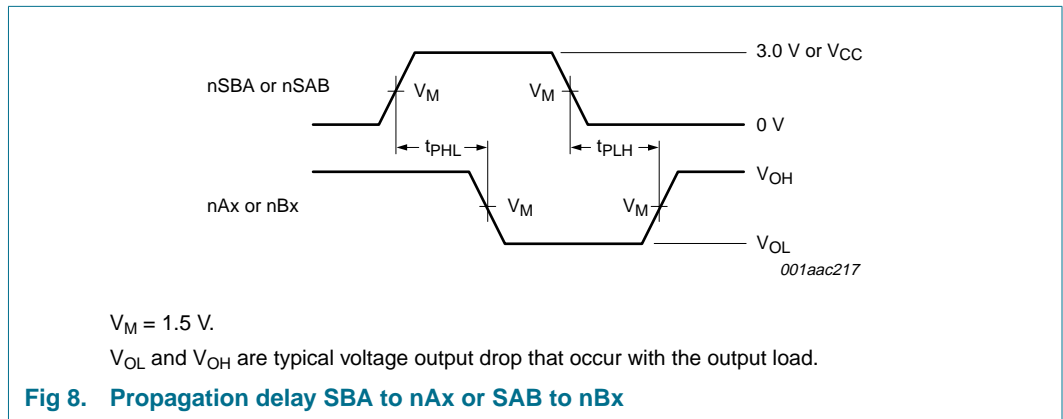
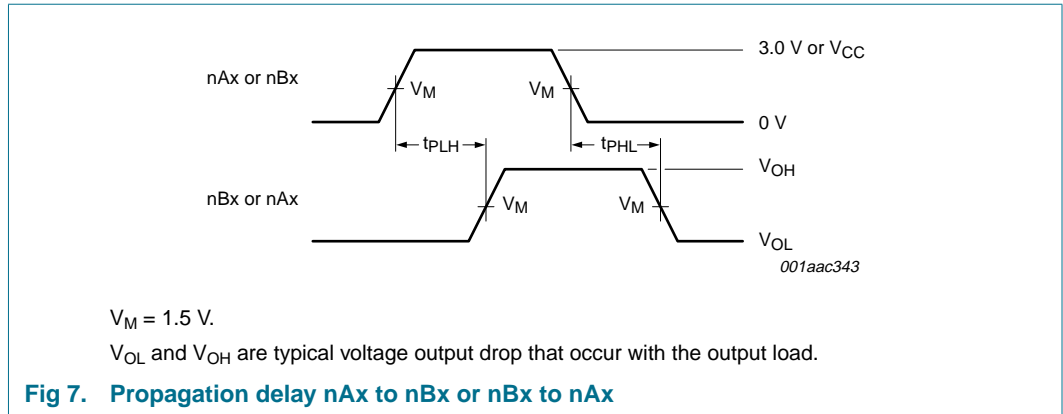
$GND = 0\text{ V}$ ;  $t_r = t_f = 2.5\text{ ns}$ ;  $C_L = 50\text{ pF}$ ;  $R_L = 500\ \Omega$ .

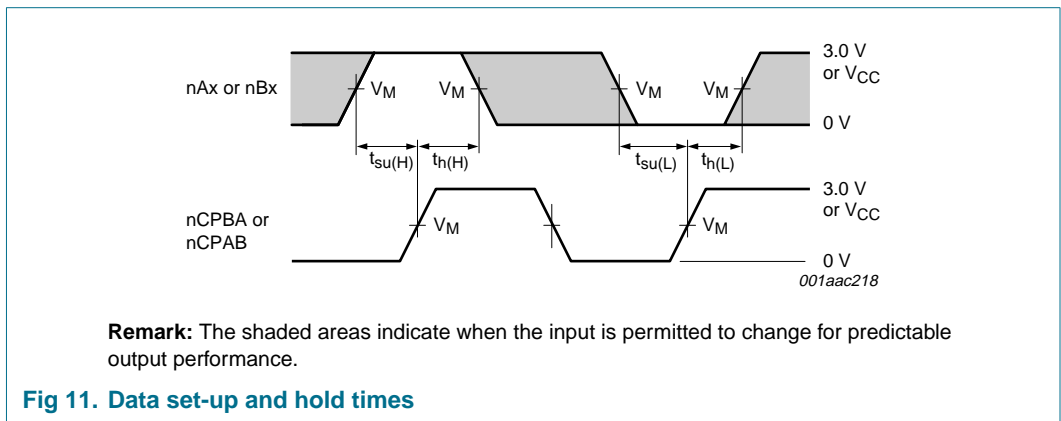
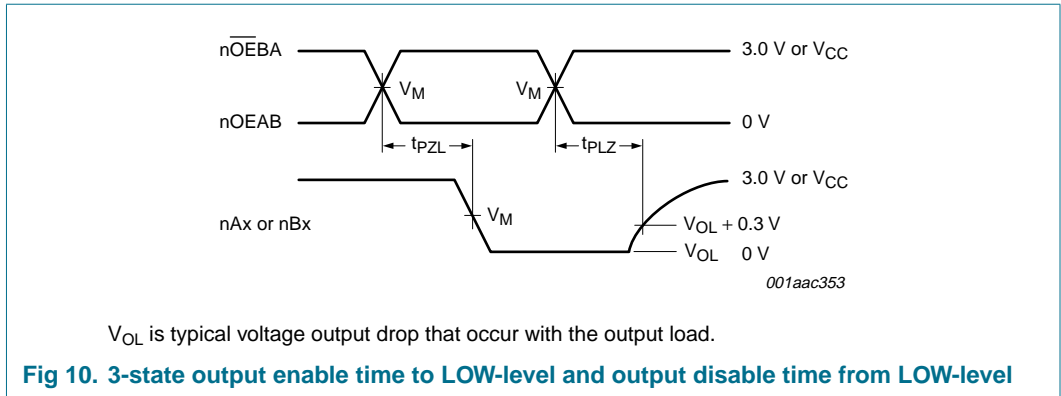
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b><math>T_{amb} = -40\text{ }^\circ\text{C to } +85\text{ }^\circ\text{C}</math> [1]</b>						
$t_{su(H)}$	set-up time HIGH nAx to nCPAB or nBx to nCPBA	see <a href="#">Figure 11</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	0.6	-	ns
		$V_{CC} = 2.7\text{ V}$	1.1	-	-	ns
$t_{su(L)}$	set-up time LOW nAx to nCPAB or nBx to nCPBA	see <a href="#">Figure 11</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.9	0.5	-	ns
		$V_{CC} = 2.7\text{ V}$	2.4	-	-	ns
$t_{h(H)}$	hold time HIGH nAx to nCPAB or nBx to nCPBA	see <a href="#">Figure 11</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	0.4	-	ns
		$V_{CC} = 2.7\text{ V}$	1.0	-	-	ns
$t_{h(L)}$	hold time LOW nAx to nCPAB or nBx to nCPBA	see <a href="#">Figure 11</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	1.0	0.5	-	ns
		$V_{CC} = 2.7\text{ V}$	1.0	-	-	ns
$t_{W(H)}$	pulse width HIGH nCPAB or nCPBA	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2.6	2.2	-	ns
		$V_{CC} = 2.7\text{ V}$	2.6	-	-	ns
$t_{W(L)}$	pulse width LOW nCPAB or nCPBA	see <a href="#">Figure 6</a>				
		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	2.8	2.4	-	ns
		$V_{CC} = 2.7\text{ V}$	2.8	-	-	ns

[1] All typical values are measured at  $V_{CC} = 3.3\text{ V}$  and  $T_{amb} = 25\text{ }^\circ\text{C}$ .

## 12. Waveforms







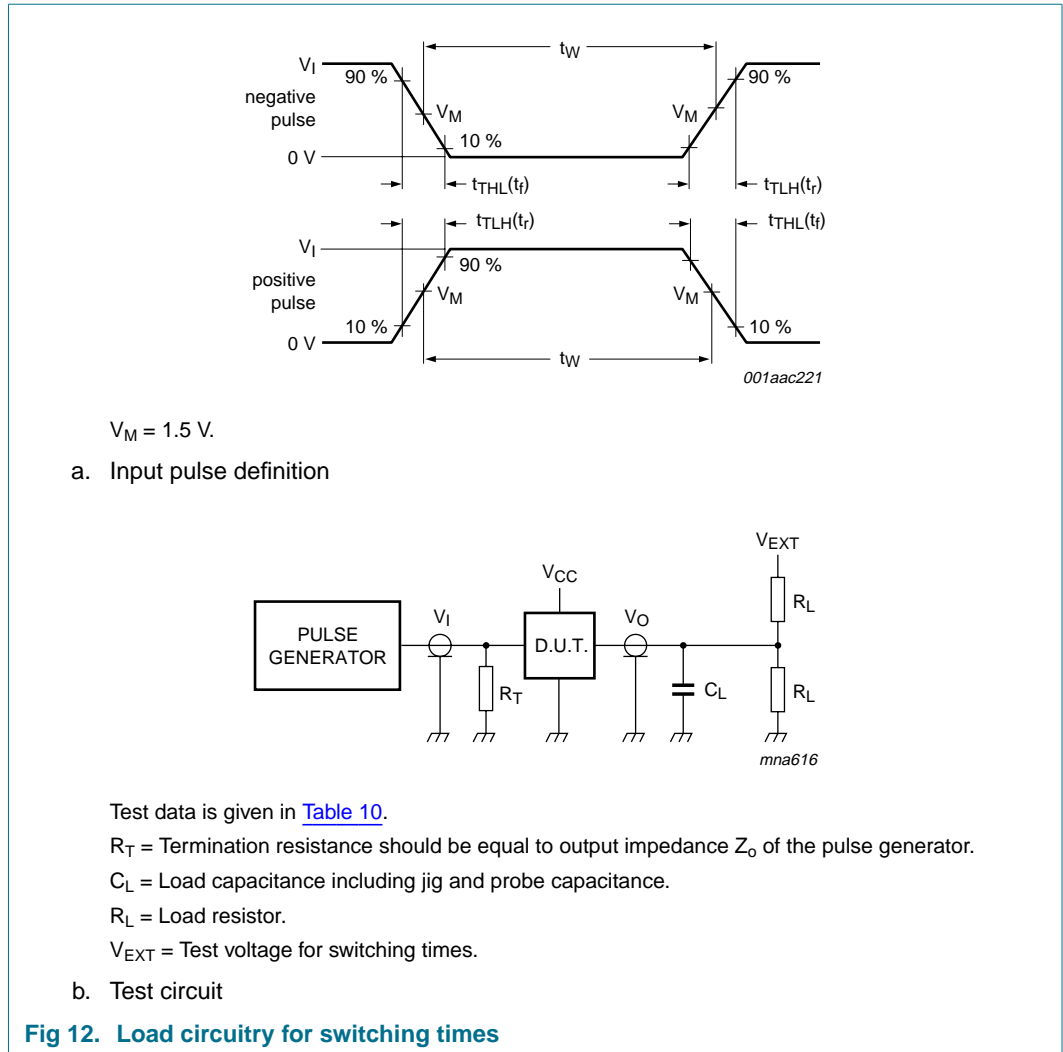


Table 10: Test data

Input				Load		$V_{EXT}$		
$V_I$	Repetition rate	$t_W$	$t_r, t_f$	$C_L$	$R_L$	$t_{PHZ}, t_{PZH}$	$t_{PLZ}, t_{PZL}$	$t_{PLH}, t_{PHL}$
2.7 V	$\leq 10$ MHz	500 ns	$\leq 2.5$ ns	50 pF	500 $\Omega$	GND	6 V	open

13. Package outline

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1 mm

SOT364-1

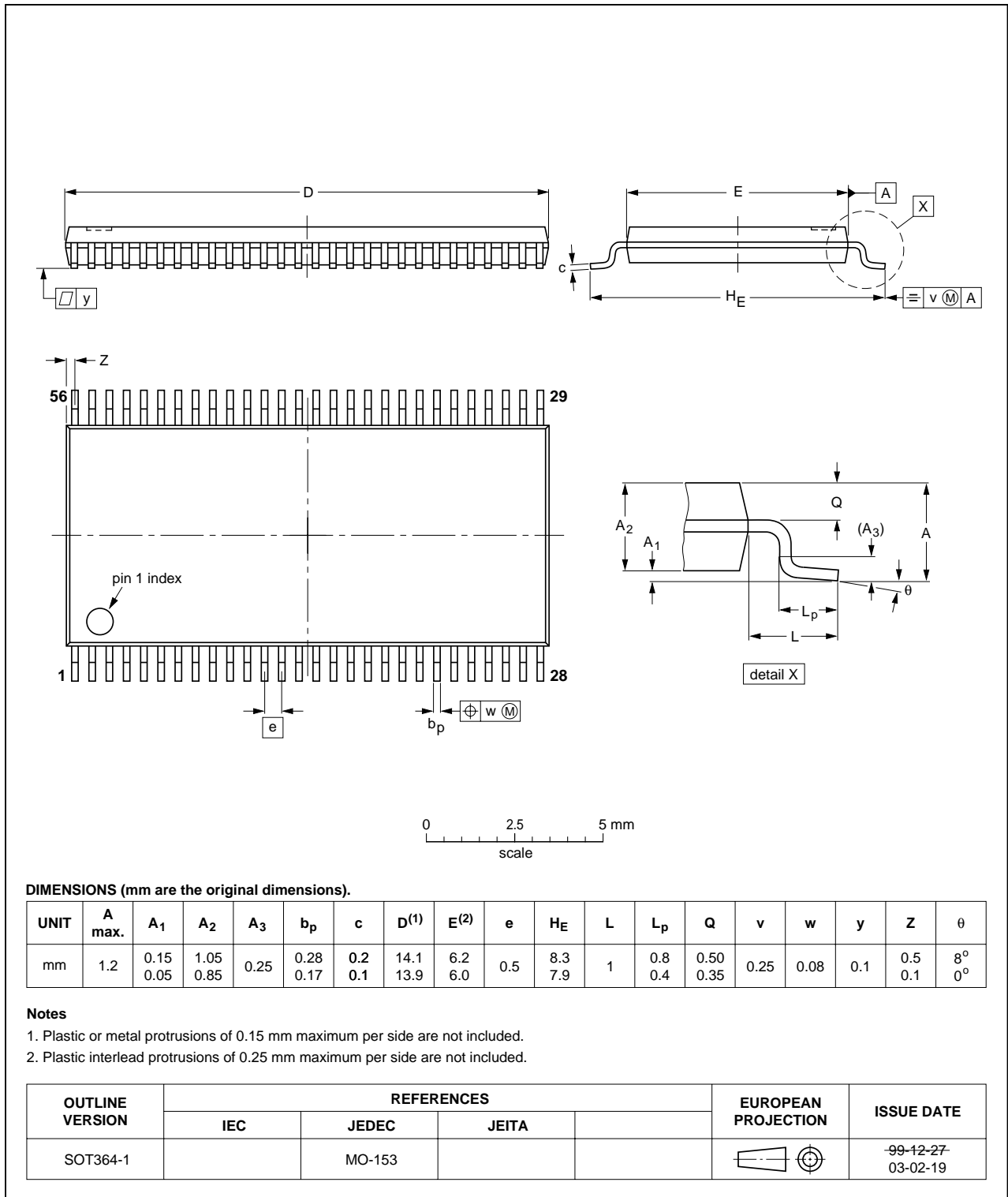


Fig 13. Package outline SOT364-1 (TSSOP56)

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1

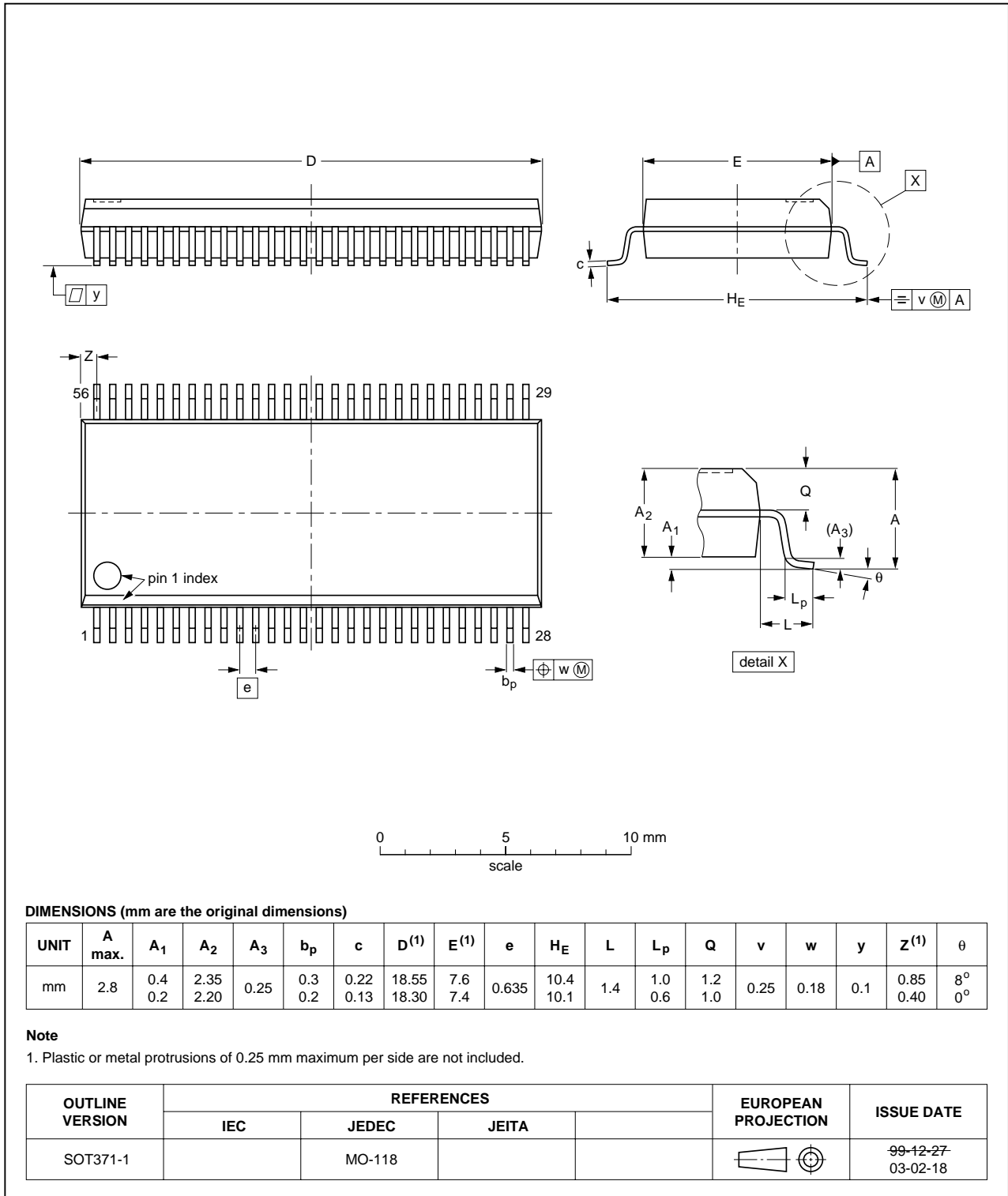


Fig 14. Package outline SOT371-1 (SSOP56)

## 14. Revision history

Table 11: Revision history

Document ID	Release date	Data sheet status	Change notice	Doc. number	Supersedes
74LVT16652A_3	20050112	Product data sheet	-	9397 750 14402	74LVT16652A_2
Modifications:					
					<ul style="list-style-type: none"><li>• The format of this data sheet has been redesigned to comply with the new presentation and information standard of Philips Semiconductors.</li><li>• Product title modified</li><li>• <a href="#">Section 2 “Features”</a>: modified JEDEC Std 17 into JESD78</li><li>• <a href="#">Section 3 “Quick reference data”</a>: modified values for <math>t_{PLH}</math> and <math>t_{PHL}</math></li><li>• <a href="#">Section 11 “Dynamic characteristics”</a>: modified various timing values.</li></ul>
74LVT16652A_2	19980219	Product specification	-	9397 750 03561	74LVT16652A_1
74LVT16652A_1	1994	Product specification	-	-	-

## 15. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup> <sup>[3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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