



**THE DATASHEET OF
74LVTH32245GX**



74LVT32245 • 74LVTH32245

Low Voltage 32-Bit Transceiver with 3-STATE Outputs

General Description

The LVT32245 and LVTH32245 contain thirty-two non-inverting bidirectional buffers with 3-STATE outputs and are intended for bus oriented applications. The devices are byte controlled. Each byte has separate control inputs which can be shorted together for full 32-bit operation. The T/\bar{R} inputs determine the direction of data flow through the device. The OE inputs disable both the A and B ports by placing them in a high impedance state.

The LVTH32245 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These non-inverting transceivers are designed for low voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT32245 and LVTH32245 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH32245), also available without bushold feature (74LVT32245).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Outputs source/sink -32 mA/+64 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V
- Packaged in plastic Fine-Pitch Ball Grid Array (FBGA)

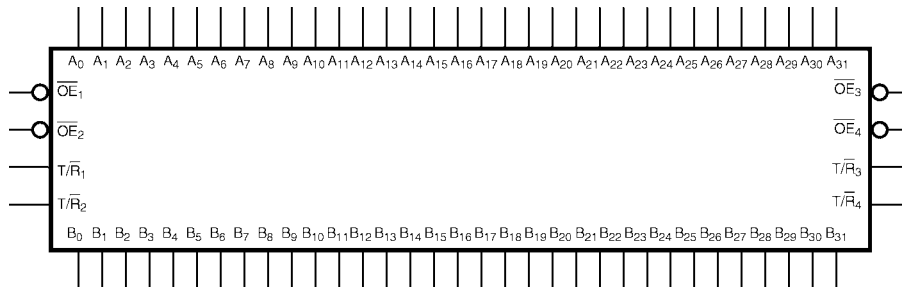
Ordering Code:

Order Number	Package Number	Package Description
74LVT32245G (Note 1)(Note 2)	BGA96A (Preliminary)	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
74LVTH32245G (Note 1)(Note 2)	BGA96A	96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide

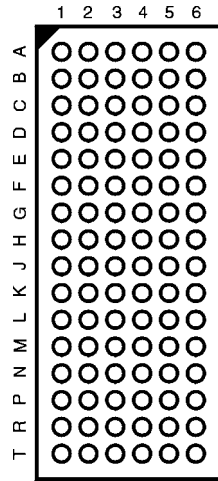
Note 1: Ordering code "G" indicates Trays.

Note 2: Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol



Connection Diagram



(Top Thru View)

Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Input (Active LOW)
T/\overline{R}_n	Transmit/Receive Input
A_0 – A_{31}	Side A Inputs/3-STATE Outputs
B_0 – B_{31}	Side B Inputs/3-STATE Outputs

FBGA Pin Assignments

	1	2	3	4	5	6
A	B ₁	B ₀	T/\overline{R}_1	\overline{OE}_1	A ₀	A ₁
B	B ₃	B ₂	GND	GND	A ₂	A ₃
C	B ₅	B ₄	V _{CC1}	V _{CC1}	A ₄	A ₅
D	B ₇	B ₆	GND	GND	A ₆	A ₇
E	B ₉	B ₈	GND	GND	A ₈	A ₉
F	B ₁₁	B ₁₀	V _{CC1}	V _{CC1}	A ₁₀	A ₁₁
G	B ₁₃	B ₁₂	GND	GND	A ₁₂	A ₁₃
H	B ₁₄	B ₁₅	T/\overline{R}_2	\overline{OE}_2	A ₁₅	A ₁₄
J	B ₁₇	B ₁₆	T/\overline{R}_3	\overline{OE}_3	A ₁₆	A ₁₇
K	B ₁₉	B ₁₈	GND	GND	A ₁₈	A ₁₉
L	B ₂₁	B ₂₀	V _{CC2}	V _{CC2}	A ₂₀	A ₂₁
M	B ₂₃	B ₂₂	GND	GND	A ₂₂	A ₂₃
N	B ₂₅	B ₂₄	GND	GND	A ₂₄	A ₂₅
P	B ₂₇	B ₂₆	V _{CC2}	V _{CC2}	A ₂₆	A ₂₇
R	B ₂₉	B ₂₈	GND	GND	A ₂₈	A ₂₉
T	B ₃₀	B ₃₁	T/\overline{R}_4	\overline{OE}_4	A ₃₁	A ₃₀

Truth Tables

Inputs		Outputs
\overline{OE}_1	T/\overline{R}_1	
L	L	Bus B ₀ –B ₇ Data to Bus A ₀ –A ₇
L	H	Bus A ₀ –A ₇ Data to Bus B ₀ –B ₇
H	X	HIGH–Z State on A ₀ –A ₇ , B ₀ –B ₇

Inputs		Outputs
\overline{OE}_3	T/\overline{R}_3	
L	L	Bus B ₁₆ –B ₂₃ Data to Bus A ₁₆ –A ₂₃
L	H	Bus A ₁₆ –A ₂₃ Data to Bus B ₁₆ –B ₂₃
H	X	HIGH–Z State on A ₁₆ –A ₂₃ , B ₁₆ –B ₂₃

Inputs		Outputs
\overline{OE}_2	T/\overline{R}_2	
L	L	Bus B ₈ –B ₁₅ Data to Bus A ₈ –A ₁₅
L	H	Bus A ₈ –A ₁₅ Data to Bus B ₈ –B ₁₅
H	X	HIGH–Z State on A ₈ –A ₁₅ , B ₈ –B ₁₅

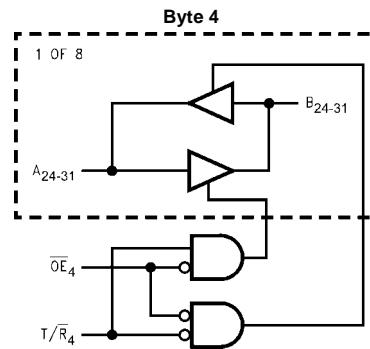
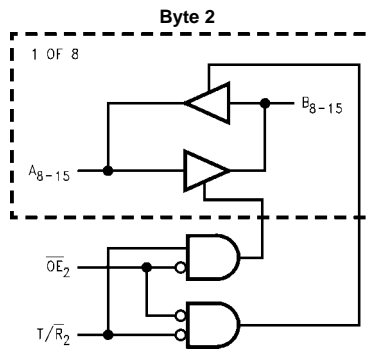
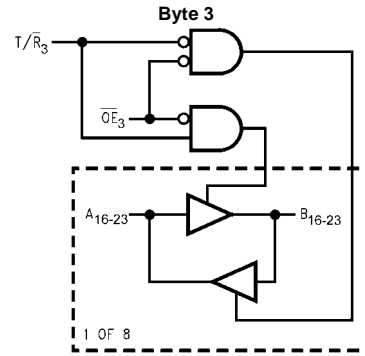
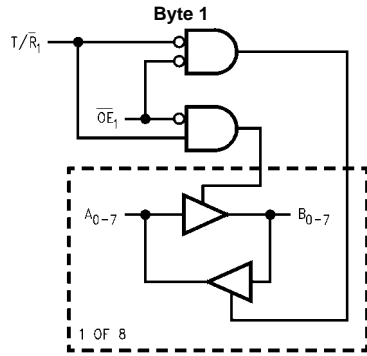
Inputs		Outputs
\overline{OE}_4	T/\overline{R}_4	
L	L	Bus B ₂₄ –B ₃₁ Data to Bus A ₂₄ –A ₃₁
L	H	Bus B ₂₄ –A ₃₁ Data to Bus B ₂₄ –B ₃₁
H	X	HIGH–Z State on A ₂₄ –A ₃₁ , B ₂₄ –B ₃₁

H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The LVT32245 and LVTH32245 contain thirty-two non-inverting bidirectional buffers with 3-STATE outputs. The device is byte controlled with each byte functioning identically, but independent of the other. The control pins can be shorted together to obtain 16-bit or full 32-bit operation.

Logic Diagrams



V_{CC1} is associated with Bytes 1 and 2.

V_{CC2} is associated with Bytes 3 and 4.

Note: Please note that these diagrams are provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings(Note 3)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	-0.5 to +4.6		V
V_I	DC Input Voltage	-0.5 to +7.0		V
V_O	Output Voltage	-0.5 to +7.0	Output in 3-STATE	V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)	
I_{IK}	DC Input Diode Current	-50	$V_I < \text{GND}$	mA
I_{OK}	DC Output Diode Current	-50	$V_O < \text{GND}$	mA
I_O	DC Output Current	64	Output at HIGH State, $V_O > V_{CC}$	mA
		128	Output at LOW State, $V_O > V_{CC}$	
I_{CC}	DC Supply Current per Supply Pin	± 64		mA
I_{GND}	DC Ground Current per Ground Pin	± 128		mA
T_{STG}	Storage Temperature Range	-65 to +150		$^{\circ}\text{C}$

Recommended Operating Conditions

Symbol	Parameter	Min	Max	Units
V_{CC}	Supply Voltage	2.7	3.6	V
V_I	Input Voltage	0	5.5	V
I_{OH}	HIGH-Level Output Current		-32	mA
I_{OL}	LOW-Level Output Current		64	mA
T_A	Free-Air Operating Temperature	-40	+85	$^{\circ}\text{C}$
$\Delta t/\Delta V$	Input Edge Rate, $V_{IN} = 0.8\text{V}-2.0\text{V}$, $V_{CC} = 3.0\text{V}$	0	10	ns/V

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

Note 4: I_O Absolute Maximum Ratings must be observed.

DC Electrical Characteristics

Symbol	Parameter	V_{CC} (V)	$T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$		Units	Conditions	
			Min	Max			
V_{IK}	Input Clamp Diode Voltage	2.7		-1.2	V	$I_I = -18\text{ mA}$	
V_{IH}	Input HIGH Voltage	2.7-3.6	2.0		V	$V_O \leq 0.1\text{V}$ or $V_O \geq V_{CC} - 0.1\text{V}$	
V_{IL}	Input LOW Voltage	2.7-3.6		0.8	V		
V_{OH}	Output HIGH Voltage	2.7-3.6	$V_{CC} - 0.2$		V	$I_{OH} = -100\ \mu\text{A}$	
		2.7	2.4			$I_{OH} = -8\text{ mA}$	
		3.0	2.0			$I_{OH} = -32\text{ mA}$	
V_{OL}	Output LOW Voltage	2.7		0.2	V	$I_{OL} = 100\ \mu\text{A}$	
		2.7		0.5		$I_{OL} = 24\text{ mA}$	
		3.0		0.4		$I_{OL} = 16\text{ mA}$	
		3.0		0.5		$I_{OL} = 32\text{ mA}$	
		3.0		0.55		$I_{OL} = 64\text{ mA}$	
$I_{I(\text{HOLD})}$ (Note 5)	Bushold Input Minimum Drive	3.0	75		μA	$V_I = 0.8\text{V}$	
			-75			$V_I = 2.0\text{V}$	
$I_{I(\text{OD})}$ (Note 5)	Bushold Input Over-Drive Current to Change State	3.0	500		μA	(Note 6)	
			-500			(Note 7)	
I_I	Input Current	3.6		10	μA	$V_I = 5.5\text{V}$	
		Control Pins	3.6			± 1	$V_I = 0\text{V}$ or V_{CC}
			Data Pins	3.6			-5
				1		$V_I = V_{CC}$	
I_{OFF}	Power Off Leakage Current	0		± 100	μA	$0\text{V} \leq V_I$ or $V_O \leq 5.5\text{V}$	
$I_{PU/PD}$	Power Up/Down 3-STATE Output Current	0-1.5		± 100	μA	$V_O = 0.5\text{V}$ to 3.0V $V_I = \text{GND}$ or V_{CC}	
I_{OZL}	3-STATE Output Leakage Current	3.6		-5	μA	$V_O = 0.5\text{V}$	
I_{OZL} (Note 5)	3-STATE Output Leakage Current	3.6		-5	μA	$V_O = 0.0\text{V}$	
I_{OZH}	3-STATE Output Leakage Current	3.6		5	μA	$V_O = 3.0\text{V}$	

DC Electrical Characteristics (Continued)

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C		Units	Conditions
			Min	Max		
I _{OZH} (Note 5)	3-STATE Output Leakage Current	3.6		5	μA	V _O = 3.6V
I _{OZH+}	3-STATE Output Leakage Current	3.6		10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current V _{CC1} or V _{CC2}	3.6		0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current V _{CC1} or V _{CC2}	3.6		5.0	mA	Outputs LOW
I _{CCZ}	Power Supply Current V _{CC1} or V _{CC2}	3.6		0.19	mA	Outputs Disabled
I _{CCZ+}	Power Supply Current V _{CC1} or V _{CC2}	3.6		0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 8) V _{CC1} or V _{CC2}	3.6		0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND

Note 5: Applies to bushold versions only (74LVTH32245).

Note 6: An external driver must source at least the specified current to switch from LOW-to-HIGH.

Note 7: An external driver must sink at least the specified current to switch from HIGH-to-LOW.

Note 8: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

Dynamic Switching Characteristics (Note 9)

Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 10)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 10)

Note 9: Characterized in SSOP package. Guaranteed parameter, but not tested.

Note 10: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.

AC Electrical Characteristics

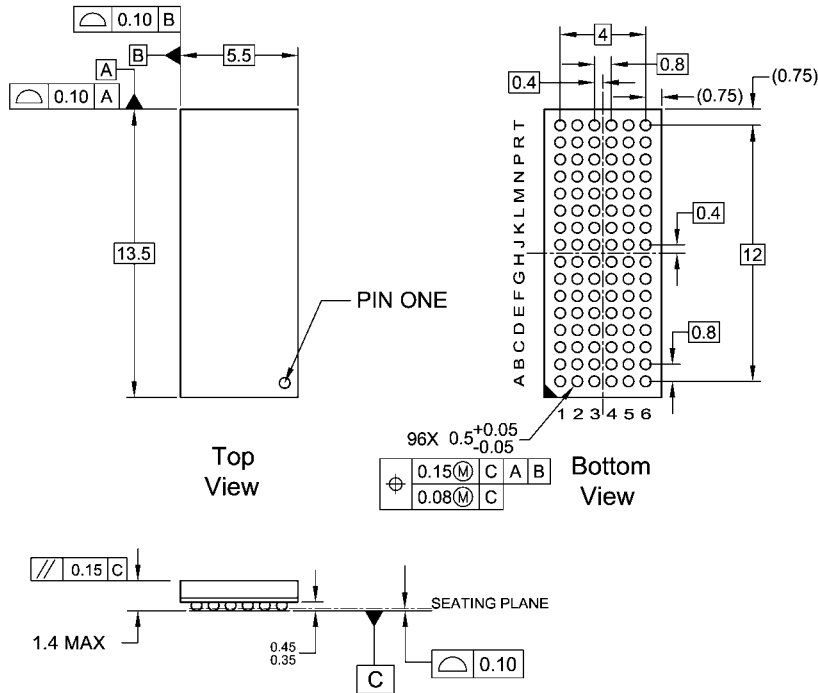
Symbol	Parameter	T _A = -40°C to +85°C C _L = 50 pF, R _L = 500Ω				Units
		V _{CC} = 3.3V ± 0.3V		V _{CC} = 2.7V		
		Min	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	1.5	3.5	1.5	3.9	ns
t _{PHL}		1.3	3.5	1.3	3.9	
t _{PZH}	Output Enable Time	1.5	4.5	1.5	5.3	ns
t _{PZL}		1.6	5.3	1.6	6.9	
t _{PHZ}	Output Disable Time	2.3	5.4	2.3	6.1	ns
t _{PLZ}		2.2	5.1	2.2	5.4	

Capacitance (Note 11)

Symbol	Parameter	Conditions	Typical	Units
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}	4	pF
C _{I/O}	Input/Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}	8	pF

Note 11: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.

Physical Dimensions inches (millimeters) unless otherwise noted



NOTES:

- A. THIS PACKAGE CONFORMS TO JEDEC MO-205
- B. ALL DIMENSIONS IN MILLIMETERS
- C. LAND PATTERN RECOMMENDATION: NSMD (Non Solder Mask Defined)
.35MM DIA PADS WITH A SOLDERMASK OPENING OF .45MM CONCENTRIC TO PADS
- D. DRAWING CONFORMS TO ASME Y14.5M-1994

BGA96ArevE

**96-Ball Fine-Pitch Ball Grid Array (FBGA), JEDEC MO-205, 5.5mm Wide
Package Number BGA96A**

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