





# ICS8633-01

## 1-TO-3 DIFFERENTIAL-TO-3.3V LVPECL ZERO DELAY BUFFER

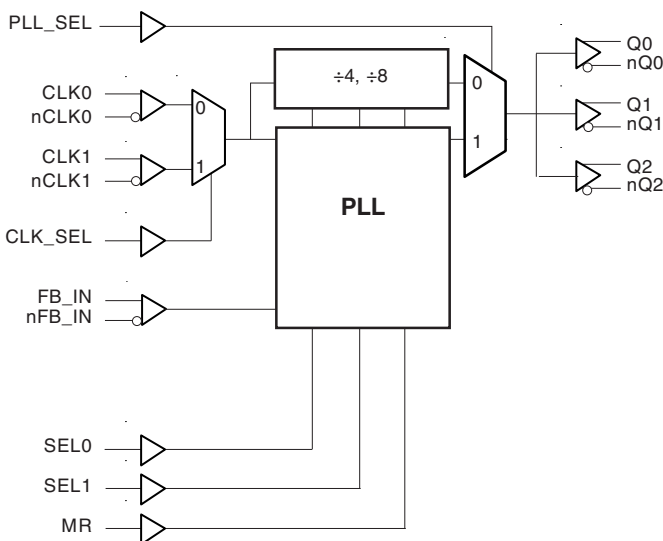
### GENERAL DESCRIPTION

The ICS8633-01 is a high performance 1-to-3 Differential-to-3.3V LVPECL Zero Delay Buffer. The ICS8633-01 has two selectable clock inputs. The CLKx, nCLKx pairs can accept most standard differential input levels. Utilizing one of the outputs as feedback to the PLL, output frequencies up to 700MHz can be regenerated with zero delay with respect to the input. Dual reference clock inputs support redundant clock or multiple reference applications.

### FEATURES

- Three differential 3.3V LVPECL outputs
- Selectable differential clock inputs
- CLKx, nCLKx pairs can accept the following differential input levels: LVPECL, LVDS, LVHSTL, HCSL, SSTL
- Output frequency range: 31.25MHz to 700MHz
- Input frequency range: 31.25MHz to 700MHz
- VCO range: 250MHz to 700MHz
- External feedback for “zero delay” clock regeneration
- Cycle-to-cycle jitter: 25ps (maximum)
- Output skew: 25ps (maximum)
- PLL reference zero delay: 50ps ± 100ps
- 3.3V operating supply
- 0°C to 70°C ambient operating temperature
- Industrial temperature information available upon request
- Available in both standard and lead-free RoHS-compliant packages

### BLOCK DIAGRAM



### PIN ASSIGNMENT

PLL_SEL	1	28	VCCA
Vcc	2	27	VEE
SEL0	3	26	VEE
SEL1	4	25	Vcco
CLK0	5	24	Vcco
nCLK0	6	23	Q2
CLK1	7	22	nQ2
nCLK1	8	21	Q1
CLK_SEL	9	20	nQ1
MR	10	19	Vcco
Vcc	11	18	Vcco
nFB_IN	12	17	Q0
FB_IN	13	16	nQ0
VEE	14	15	VEE

**ICS8633-01**  
**28-Lead, 209-MIL SSOP**  
 5.3mm x 10.2mm x 1.75mm body package  
**F Package**  
 Top View



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## 1-TO-3 DIFFERENTIAL-TO-3.3V LVPECL ZERO DELAY BUFFER

**TABLE 1. PIN DESCRIPTIONS**

Number	Name	Type		Description
1	PLL_SEL	Input	Pullup	Selects between the PLL and the reference clock as the input to the dividers. When HIGH, selects PLL. When LOW, selects reference clock. LVCMOS / LVTTTL interface levels.
2, 11	V <sub>CC</sub>	Power		Core supply pins.
3	SEL0	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
4	SEL1	Input	Pulldown	Determines output divider values in Table 3. LVCMOS / LVTTTL interface levels.
5	CLK0	Input	Pulldown	Non-inverting differential clock input.
6	nCLK0	Input	Pullup	Inverting differential clock input.
7	CLK1	Input	Pulldown	Non-inverting differential clock input.
8	nCLK1	Input	Pullup	Inverting differential clock input.
9	CLK_SEL	Input	Pulldown	Clock select input. When LOW, selects CLK0, nCLK0. When HIGH, selects CLK1, nCLK1. LVCMOS / LVTTTL interface levels.
10	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS / LVTTTL interface levels.
12	nFB_IN	Input	Pullup	Feedback input to phase detector for regenerating clocks with "zero delay".
13	FB_IN	Input	Pulldown	Feedback input to phase detector for regenerating clocks with "zero delay".
14, 15, 26, 27	V <sub>EE</sub>	Power		Negative supply pins.
16, 17	nQ0, Q0	Output		Differential output pair. LVPECL interface levels.
18, 19, 24, 25	V <sub>CC0</sub>	Power		Output supply pins.
20, 21	nQ1, Q1	Output		Differential output pair. LVPECL interface levels.
22, 23	nQ2, Q2	Output		Differential output pair. LVPECL interface levels.
28	V <sub>CCA</sub>	Power		Analog supply pin.

NOTE: *Pullup* and *Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

**TABLE 2. PIN CHARACTERISTICS**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C <sub>IN</sub>	Input Capacitance			4		pF
R <sub>PULLUP</sub>	Input Pullup Resistor			51		kΩ
R <sub>PULLDOWN</sub>	Input Pulldown Resistor			51		kΩ

**TABLE 3A. CONTROL INPUT FUNCTION TABLE**

Inputs			Outputs PLL_SEL = 1 PLL Enable Mode
SEL1	SEL0	Reference Frequency Range (MHz)*	Q0:Q2, nQ0:nQ2
0	0	250 - 700	÷ 1
0	1	125 - 350	÷ 1
1	0	62.5 - 175	÷ 1
1	1	31.25 - 87.5	÷ 1

**TABLE 3B. PLL BYPASS FUNCTION TABLE**

Inputs		Outputs PLL_SEL = 0 PLL Bypass Mode
SEL1	SEL0	Q0:Q2, nQ0:nQ2
0	0	÷ 4
0	1	÷ 4
1	0	÷ 4
1	1	÷ 8

\*NOTE: VCO frequency range for all configurations above is 250MHz to 700MHz.



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## 1-TO-3 DIFFERENTIAL-TO-3.3V LVPECL

### ZERO DELAY BUFFER

#### ABSOLUTE MAXIMUM RATINGS

Supply Voltage, $V_{CC}$	4.6V
Inputs, $V_i$	-0.5V to $V_{CC} + 0.5V$
Outputs, $I_o$	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, $\theta_{JA}$	49°C/W (0 lfpm)
Storage Temperature, $T_{STG}$	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

**TABLE 4A. POWER SUPPLY DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{CC}$	Core Supply Voltage		3.135	3.3	3.465	V
$V_{CCA}$	Analog Supply Voltage		3.135	3.3	3.465	V
$V_{CCO}$	Output Supply Voltage		3.135	3.3	3.465	V
$I_{EE}$	Power Supply Current				150	mA
$I_{CCA}$	Analog Supply Current				15	mA

**TABLE 4B. LVCMOS/LVTTL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{IH}$	Input High Voltage		2		$V_{CC} + 0.3$	V
$V_{IL}$	Input Low Voltage		-0.3		0.8	V
$I_{IH}$	Input High Current	SEL0, SEL1, CLK_SEL, MR	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		PLL_SEL	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	SEL0, SEL1, CLK_SEL, MR	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		PLL_SEL	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$

**TABLE 4C. DIFFERENTIAL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$I_{IH}$	Input High Current	CLK0, CLK1, FB_IN	$V_{CC} = V_{IN} = 3.465V$		150	$\mu A$
		nCLK0, nCLK1, nFB_IN	$V_{CC} = V_{IN} = 3.465V$		5	$\mu A$
$I_{IL}$	Input Low Current	CLK0, CLK1, FB_IN	$V_{CC} = 3.465V, V_{IN} = 0V$	-5		$\mu A$
		nCLK0, nCLK1, nFB_IN	$V_{CC} = 3.465V, V_{IN} = 0V$	-150		$\mu A$
$V_{PP}$	Peak-to-Peak Input Voltage		0.15		1.3	V
$V_{CMR}$	Common Mode Input Voltage; NOTE 1, 2		$V_{EE} + 0.5$		$V_{CC} - 0.85$	V

NOTE 1: For single ended applications, the maximum input voltage for CLK0, nCLK0 and CLK1, nCLK1 is  $V_{CC} + 0.3V$ .

NOTE 2: Common mode voltage is defined as  $V_{IH}$ .



# ICS8633-01

## 1-TO-3 DIFFERENTIAL-TO-3.3V LVPECL

### ZERO DELAY BUFFER

**TABLE 4D. LVPECL DC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$V_{OH}$	Output High Voltage; NOTE 1		$V_{CCO} - 1.4$		$V_{CCO} - 0.9$	V
$V_{OL}$	Output Low Voltage; NOTE 1		$V_{CCO} - 2.0$		$V_{CCO} - 1.7$	V
$V_{SWING}$	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with  $50\Omega$  to  $V_{CCO} - 2V$ .

**TABLE 5. INPUT FREQUENCY CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{IN}$	Input Frequency	CLK0, nCLK0, CLK1, nCLK1	PLL_SEL = 1	31.25	700	MHz
			PLL_SEL = 0		700	MHz

**TABLE 6. AC CHARACTERISTICS,  $V_{CC} = V_{CCA} = V_{CCO} = 3.3V \pm 5\%$ ,  $T_A = 0^\circ C$  TO  $70^\circ C$**

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
$f_{MAX}$	Output Frequency				700	MHz
$t_{PD}$	Propagation Delay; NOTE 1	PLL_SEL = 0V, $f \leq 700MHz$	2.8		4.9	ns
$t(\emptyset)$	PLL Reference Zero Delay; NOTE 2, 4	PLL_SEL = 3.3V	-50	50	150	ps
$t_{sk(o)}$	Output Skew; NOTE 3, 4				25	ps
$f_{jit(cc)}$	Cycle-to-Cycle Jitter; NOTE 4, 6				25	ps
$f_{jit(\theta)}$	Phase Jitter; NOTE 4, 5, 6				$\pm 50$	ps
$t_L$	PLL Lock Time				1	ms
$t_R / t_F$	Output Rise/Fall Time	20% to 80% @ 50MHz	300		700	ps
odc	Output Duty Cycle		47		53	%

All parameters measured at  $f_{MAX}$  unless noted otherwise.

NOTE 1: Measured from the differential input crossing point to the differential output crossing point.

NOTE 2: Defined as the time difference between the input reference clock and the average feedback input signal when the PLL is locked and the input reference frequency is stable.

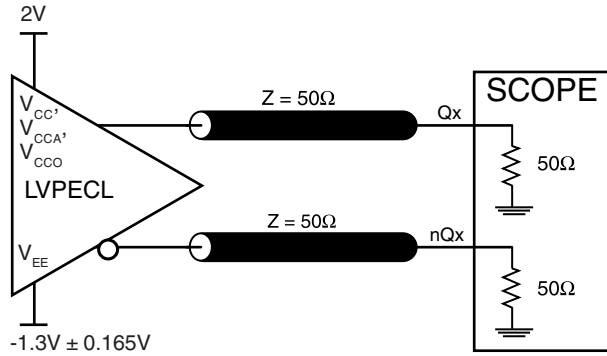
NOTE 3: Defined as skew between outputs at the same supply voltage and with equal load conditions. Measured at the output differential cross points.

NOTE 4: This parameter is defined in accordance with JEDEC Standard 65.

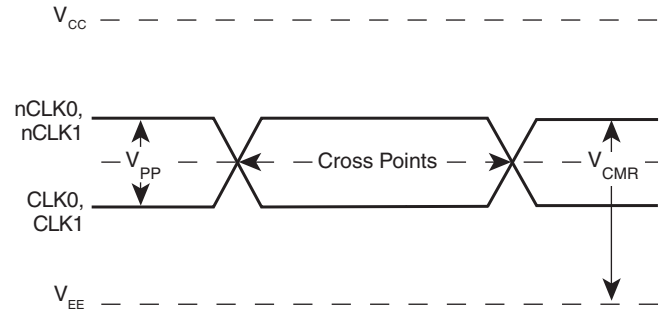
NOTE 5: Phase jitter is dependent on the input source used.

NOTE 6: Characterized at VCO frequency of 622MHz.

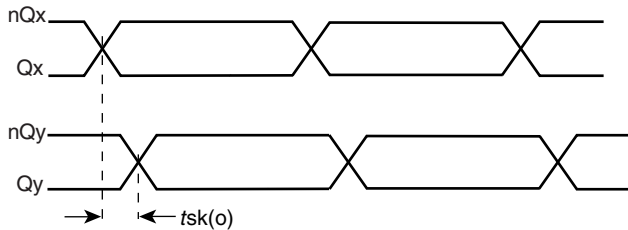
## PARAMETER MEASUREMENT INFORMATION



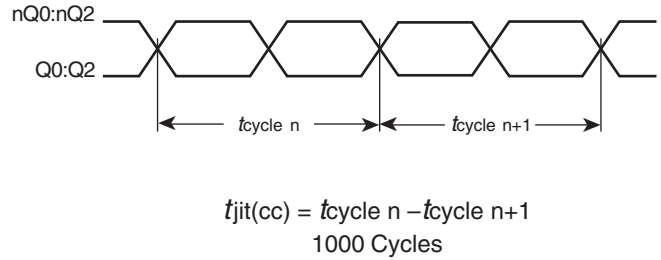
**3.3V OUTPUT LOAD AC TEST CIRCUIT**



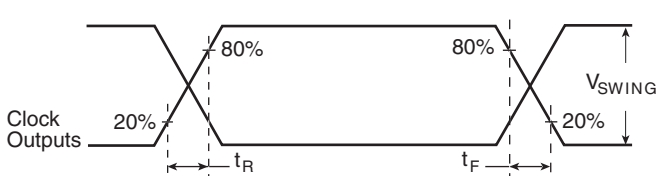
**DIFFERENTIAL INPUT LEVEL**



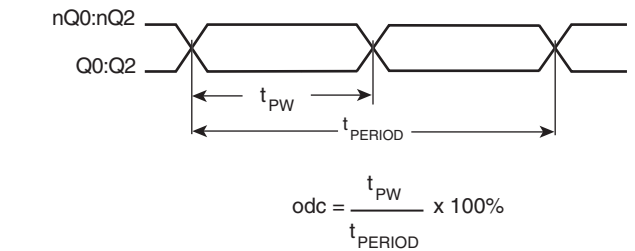
**OUTPUT SKEW**



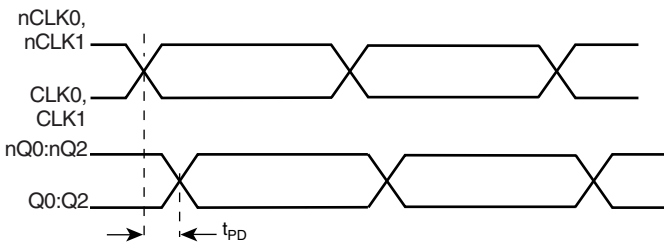
**CYCLE-TO-CYCLE JITTER**



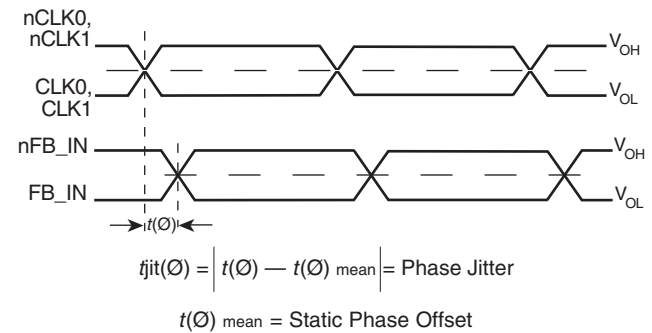
**OUTPUT RISE/FALL TIME**



**OUTPUT DUTY CYCLE/PULSE WIDTH/PERIOD**



**PROPAGATION DELAY**

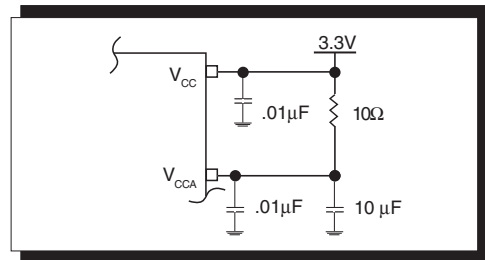


**PHASE JITTER & STATIC PHASE OFFSET**

## APPLICATION INFORMATION

### POWER SUPPLY FILTERING TECHNIQUES

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. The ICS8633-01 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL.  $V_{CC}$ ,  $V_{CCA}$ , and  $V_{CCO}$  should be individually connected to the power supply plane through vias, and bypass capacitors should be used for each pin. To achieve optimum jitter performance, power supply isolation is required. *Figure 1* illustrates how a  $10\Omega$  resistor along with a  $10\mu F$  and a  $.01\mu F$  bypass capacitor should be connected to each  $V_{CCA}$  pin.

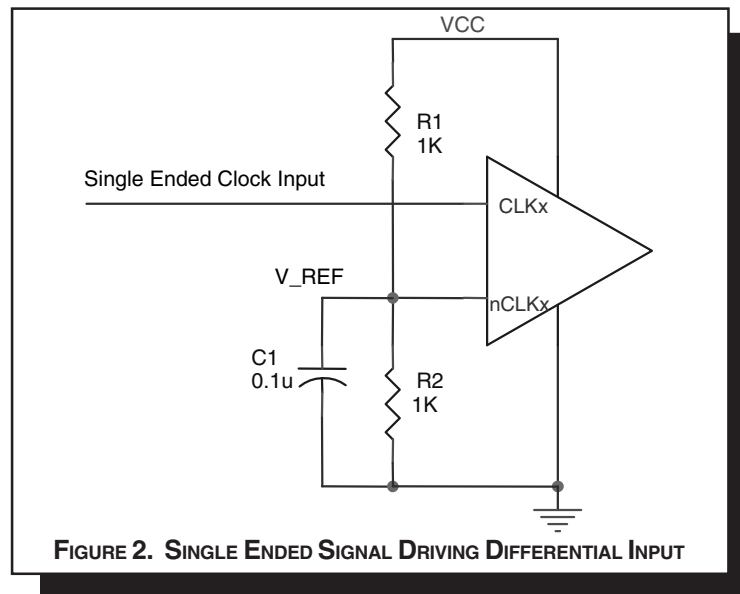


**FIGURE 1. POWER SUPPLY FILTERING**

### WIRING THE DIFFERENTIAL INPUT TO ACCEPT SINGLE ENDED LEVELS

*Figure 2* shows how the differential input can be wired to accept single ended levels. The reference voltage  $V_{REF} \approx V_{CC}/2$  is generated by the bias resistors R1, R2 and C1. This bias circuit should be located as close as possible to the input pin. The ratio

of R1 and R2 might need to be adjusted to position the  $V_{REF}$  in the center of the input voltage swing. For example, if the input clock swing is only 2.5V and  $V_{CC} = 3.3V$ ,  $V_{REF}$  should be 1.25V and  $R2/R1 = 0.609$ .



**FIGURE 2. SINGLE ENDED SIGNAL DRIVING DIFFERENTIAL INPUT**

### RECOMMENDATIONS FOR UNUSED INPUT AND OUTPUT PINS

#### INPUTS:

##### CLK/nCLK INPUT:

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

##### LVCOS CONTROL PINS:

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

#### OUTPUTS:

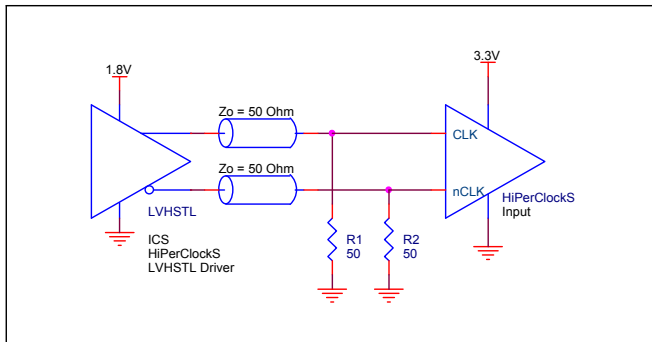
##### LVPECL OUTPUT

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

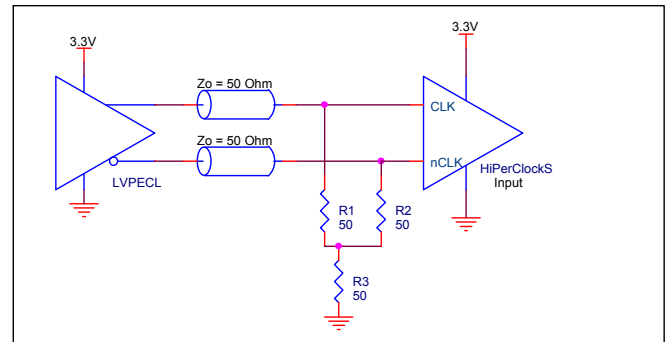
### DIFFERENTIAL CLOCK INPUT INTERFACE

The CLK/nCLK accepts LVDS, LVPECL, LVHSTL, SSTL, HCSL and other differential signals. Both  $V_{SWING}$  and  $V_{OH}$  must meet the  $V_{PP}$  and  $V_{CMR}$  input requirements. Figures 3A to 3D show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are

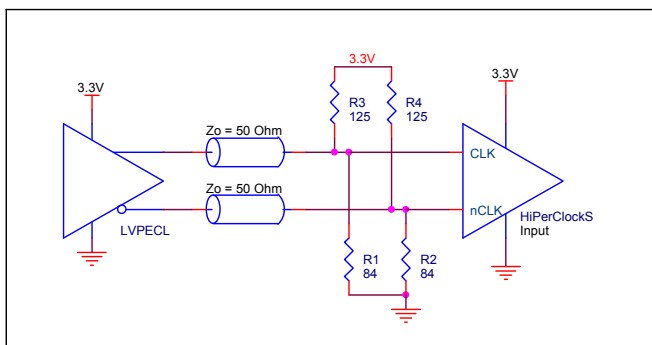
examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example in *Figure 3A*, the input termination applies for LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.



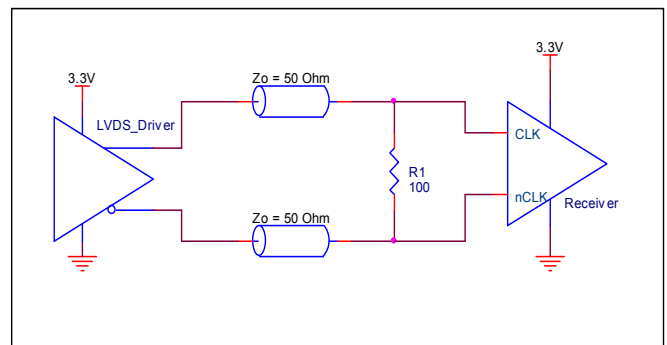
**FIGURE 3A. CLK/nCLK INPUT DRIVEN BY LVHSTL DRIVER**



**FIGURE 3B. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3C. CLK/nCLK INPUT DRIVEN BY 3.3V LVPECL DRIVER**



**FIGURE 3D. CLK/nCLK INPUT DRIVEN BY 3.3V LVDS DRIVER**

### TERMINATION FOR LVPECL OUTPUTS

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive

50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

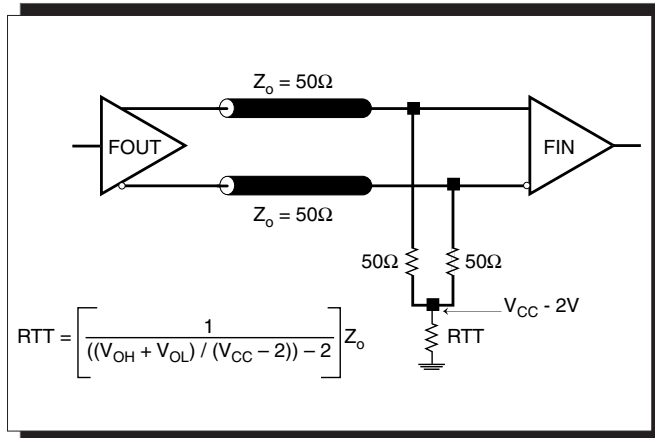


FIGURE 4A. LVPECL OUTPUT TERMINATION

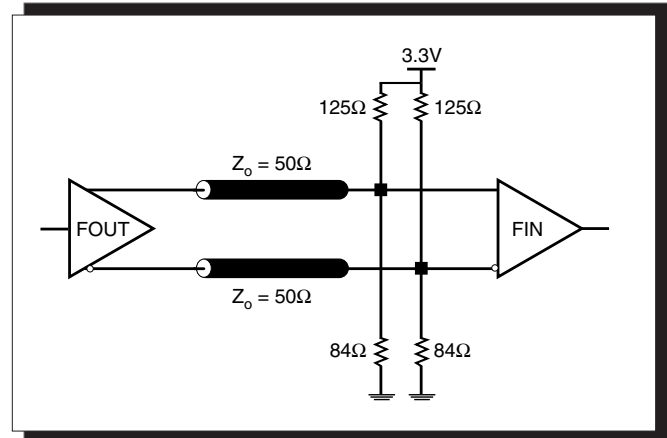
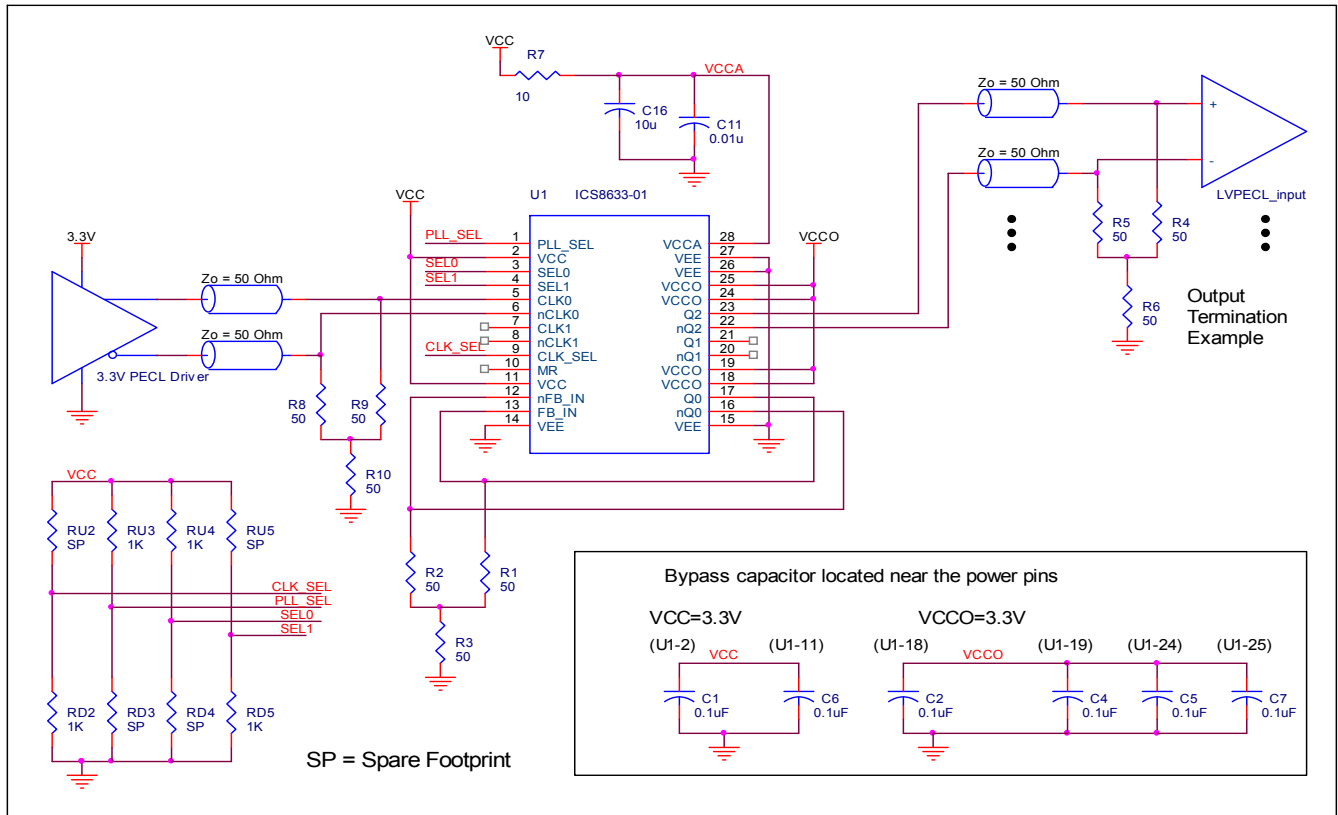


FIGURE 4B. LVPECL OUTPUT TERMINATION

### APPLICATION SCHEMATIC EXAMPLE

Figure 5 shows an example of ICS8633-01 application schematic. The CLK/nCLK input can be driven by several types of differential input levels. In this example, the input is driven by a 3.3V LVPECL driver. For the LVPECL output drivers, a

termination example is shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.



**FIGURE 5. ICS8633-01 LVPECL ZERO DELAY BUFFER SCHEMATIC EXAMPLE**



## POWER CONSIDERATIONS

This section provides information on power dissipation and junction temperature for the ICS8633-01. Equations and example calculations are also provided.

### 1. Power Dissipation.

The total power dissipation for the ICS8633-01 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for  $V_{CC} = 3.3V + 5\% = 3.465V$ , which gives worst case results.

**NOTE:** Please refer to Section 3 for details on calculating power dissipated in the load.

- Power (core)<sub>MAX</sub> =  $V_{CC\_MAX} * I_{EE\_MAX} = 3.465V * 150mA = 519.75mW$
- Power (outputs)<sub>MAX</sub> = **30mW/Loaded Output pair**  
 If all outputs are loaded, the total power is  $3 * 30mW = 90mW$

**Total Power**<sub>MAX</sub> (3.465V, with all outputs switching) =  $519.75mW + 90mW = 609.75mW$

### 2. Junction Temperature.

Junction temperature, T<sub>j</sub>, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for the devices is 125°C.

The equation for T<sub>j</sub> is as follows:  $T_j = \theta_{JA} * Pd\_total + T_A$

T<sub>j</sub> = Junction Temperature

$\theta_{JA}$  = Junction-to-Ambient Thermal Resistance

Pd<sub>total</sub> = Total Device Power Dissipation (example calculation is in section 1 above)

T<sub>A</sub> = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance  $\theta_{JA}$  must be used. Assuming a moderate air flow of 200 linear feet per minute and a multi-layer board, the appropriate value is 36°C/W per Table 7 below.

Therefore, T<sub>j</sub> for an ambient temperature of 70°C with all outputs switching is:

$70°C + 0.610W * 36°C/W = 91.96°C$ . This is well below the limit of 125°C.

This calculation is only an example. T<sub>j</sub> will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

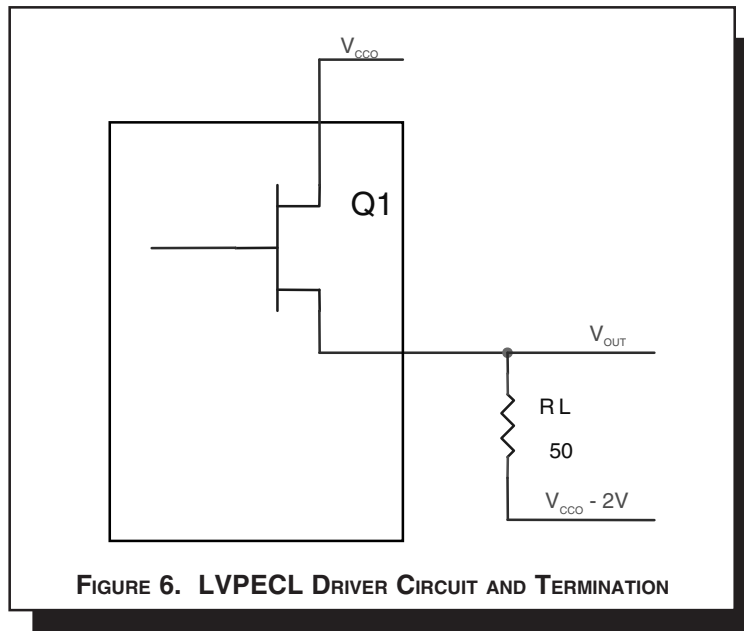
**TABLE 7. THERMAL RESISTANCE  $\theta_{JA}$  FOR 28-PIN SSOP, FORCED CONVECTION**

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	49°C/W	36°C/W	30°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in Figure 6.



**FIGURE 6. LVPECL DRIVER CIRCUIT AND TERMINATION**

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of  $V_{CCO} - 2V$ .

- For logic high,  $V_{OUT} = V_{OH\_MAX} = V_{CCO\_MAX} - 0.9V$

$$(V_{CCO\_MAX} - V_{OH\_MAX}) = 0.9V$$

- For logic low,  $V_{OUT} = V_{OL\_MAX} = V_{CCO\_MAX} - 1.7V$

$$(V_{CCO\_MAX} - V_{OL\_MAX}) = 1.7V$$

$Pd\_H$  is power dissipation when the output drives high.  
 $Pd\_L$  is the power dissipation when the output drives low.

$$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - 0.9V)/50\Omega] * 0.9V = 19.2mW$$

$$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - 1.7V)/50\Omega] * 1.7V = 10.2mW$$

Total Power Dissipation per output pair =  $Pd\_H + Pd\_L = 30mW$



## RELIABILITY INFORMATION

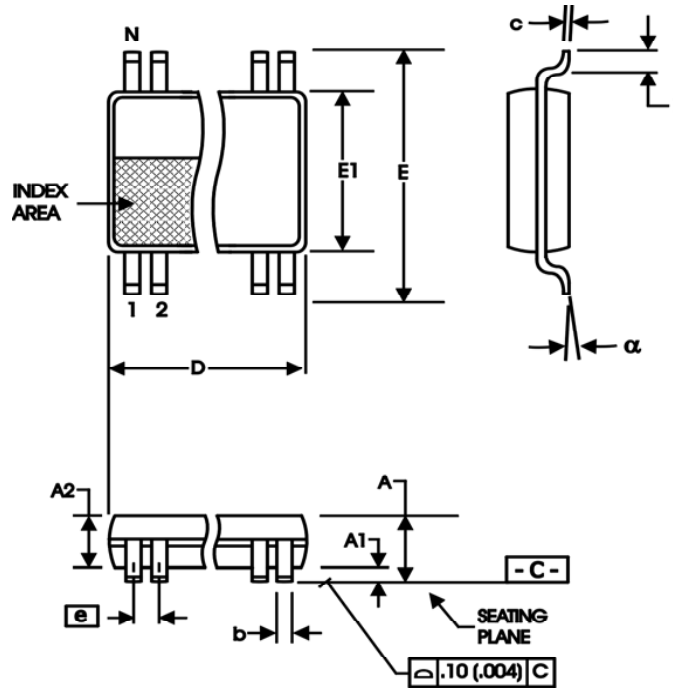
TABLE 8.  $\theta_{JA}$  VS. AIR FLOW TABLE FOR 28 LEAD SSOP

$\theta_{JA}$ by Velocity (Linear Feet per Minute)			
	0	200	500
Multi-Layer PCB, JEDEC Standard Test Boards	49°C/W	36°C/W	30°C/W

### TRANSISTOR COUNT

The transistor count for ICS8633-01 is: 2969

**PACKAGE OUTLINE - F SUFFIX FOR 28 LEAD SSOP**



**TABLE 9. PACKAGE DIMENSIONS**

SYMBOL	Millimeters	
	Minimum	Maximum
N	28	
A		2.00
A1	0.05	
A2	1.65	1.85
b	0.22	0.38
c	0.09	0.25
D	9.90	10.50
E	7.40	8.20
E1	5.00	5.60
e	0.65 BASIC	
L	0.55	0.95
α	0°	8°

Reference Document: JEDEC Publication 95, MO-150



# ICS8633-01

## 1-TO-3 DIFFERENTIAL-TO-3.3V LVPECL

### ZERO DELAY BUFFER

**TABLE 10. ORDERING INFORMATION**

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
8633AF-01	ICS8633AF-01	28 Lead SSOP	Tube	0°C to 70°C
8633AF-01T	ICS8633AF-01	28 Lead SSOP	1000 Tape & Reel	0°C to 70°C
8633AF-01LF	ICS8633AF-01LF	28 Lead "Lead-Free" SSOP	Tube	0°C to 70°C
8633AF-01LFT	ICS8633AF-01LF	28 Lead "Lead-Free" SSOP	1000 Tape & Reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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REVISION HISTORY SHEET				
Rev	Table	Page	Description of Change	Date
B	T10	14 16	Updated datasheet's header/footer with IDT from ICS. Removed ICS prefix from Part/Order Number column. Added Contact Page.	8/2/10



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