



**THE DATASHEET OF
A6276SLW**



16-Bit Serial Input, Constant-Current Latched LED Driver

Features and Benefits

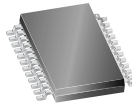
- Up to 90 mA constant-current outputs
- Undervoltage lockout
- Low-power CMOS logic and latches
- High data input rate
- Functional replacement for TB62706BN/BF

Packages

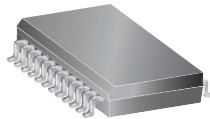
24-pin DIP
(A package)



24-pin TSSOP
with exposed thermal pad
(LP package)



24-pin SOICW
(LW package)



Not to scale

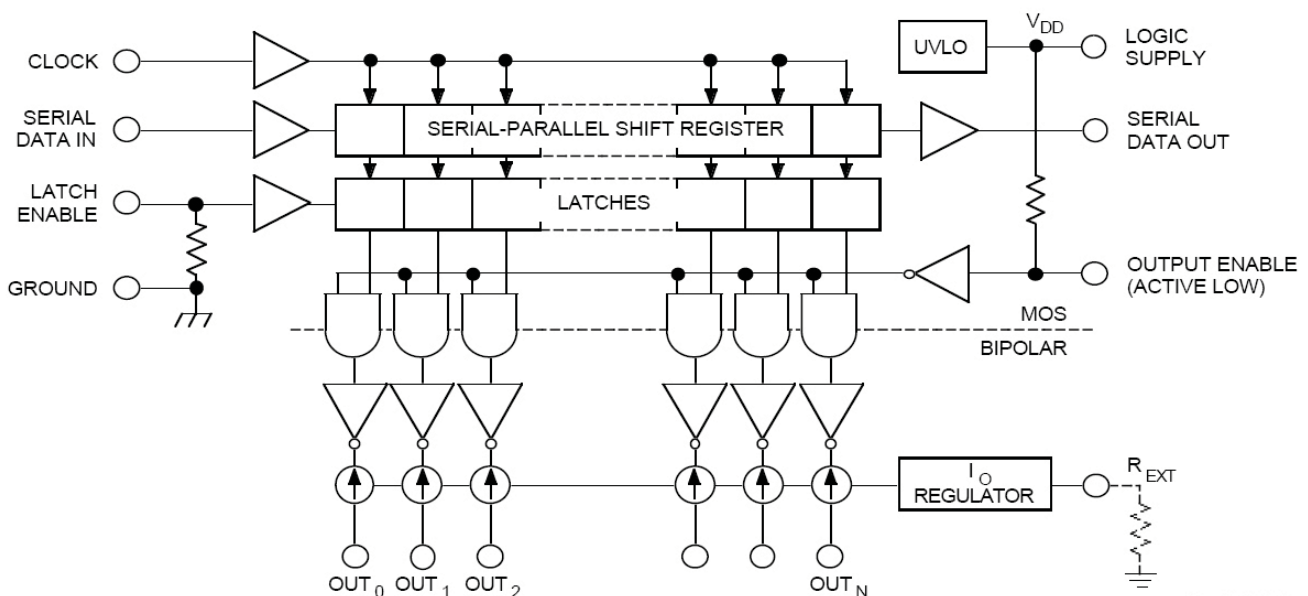
Description

The A6276 is specifically designed for LED-display applications. Each BiCMOS device includes a 16-bit CMOS shift register, accompanying data latches, and 16 NPN constant-current sink drivers. Except for package style and allowable package power dissipation, the device options are identical.

The CMOS shift register and latches allow direct interfacing with microprocessor-based systems. With a 5 V logic supply, typical serial data-input rates are up to 20 MHz. The LED drive current is determined by the user selection of a single resistor. A CMOS serial data output permits cascaded connections in applications requiring additional drive lines. For inter-digit blanking, all output drivers can be disabled with an ENABLE input high. Similar 8-bit devices are available as the A6275.

Three package styles are provided: through-hole DIP (suffix A), surface-mount SOIC (suffix LW), and TSSOP with exposed thermal pad (suffix LP). In normal applications, the copper leadframe and low logic-power dissipation of the DIP allow it to sink maximum rated current through all outputs continuously over the operating temperature range (90 mA, 0.75 V drop, 85°C). All packages are lead (Pb) free, with 100% matte tin leadframe plating.

Functional Block Diagram



Dwg. FP-013-3

Selection Guide

| Part Number | Package | Packing | Ambient Temperature (°C) |
|---------------|--------------|---------------|--------------------------|
| A6276EA-T | 24-pin DIP | 15 per tube | -40 to 85 |
| A6276ELPTR-T* | 24-pin TSSOP | 4000 per reel | -40 to 85 |
| A6276ELWTR-T | 24-pin SOICW | 1000 per reel | -40 to 85 |
| A6276SLWTR-T* | 24-pin SOICW | 1000 per reel | -20 to 85 |

*Variant is in production but has been determined to be LAST TIME BUY. This classification indicates that the variant is obsolete and notice has been given. Sale of the variant is currently restricted to existing customer applications. The variant should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available. Status date change November 1, 2008. Deadline for receipt of LAST TIME BUY orders is April 25, 2009.

Absolute Maximum Ratings*

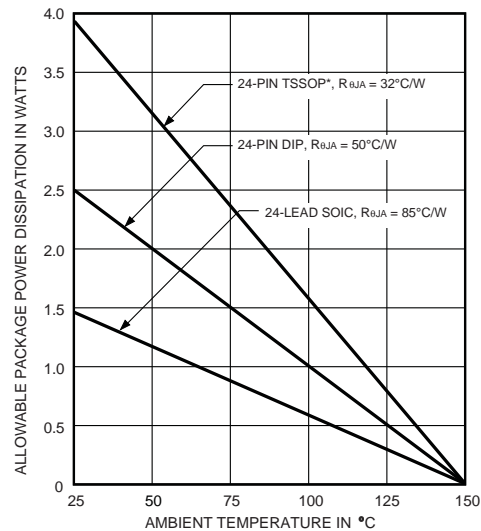
| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|------------|---------|------------------------|-------|
| Supply Voltage | V_{DD} | | 7.0 | V |
| Output Voltage | V_O | | -0.5 to 17 | V |
| Input Voltage | V_{ROUT} | | -0.4 to $V_{DD} + 0.4$ | V |
| Output Current | I_O | | 90 | mA |
| Ground Current | I_{GND} | | 1475 | mA |
| Operating Ambient Temperature | T_A | Range S | -20 to 85 | °C |
| | | Range E | -40 to 85 | °C |
| Maximum Junction Temperature | $T_J(max)$ | | 150 | °C |
| Storage Temperature | T_{stg} | | -55 to 150 | °C |

*Caution: These CMOS devices have input static protection (Class 2) but are still susceptible to damage if exposed to extremely high static electrical charges.

Thermal Characteristics may require derating at maximum conditions, see application information

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|-----------------|--|-------|-------|
| Package Thermal Resistance | $R_{\theta JA}$ | Package A, 1-layer PCB based on JEDEC standard | 50 | °C/W |
| | | Package LP, 2-layer PCB with 3.8 in ² copper area each side | 32 | °C/W |
| | | Package LW, 1-layer PCB based on JEDEC standard | 85 | °C/W |

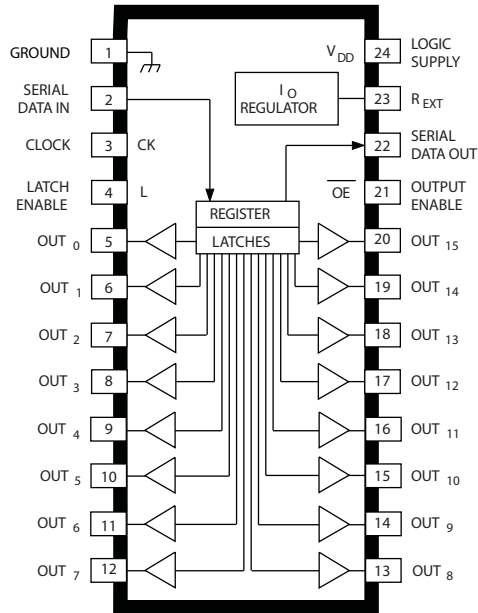
*Additional thermal information available on the Allegro website



*Mounted on single-layer, two-sided PCB, with 3.8 in² copper each side; additional information on Allegro Web site

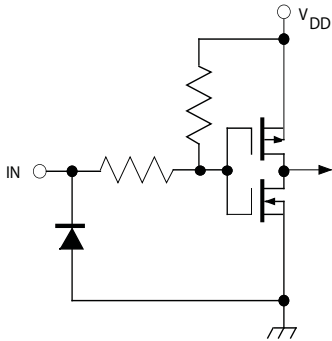
Pin-out Diagram

(A, LP, and LW packages)



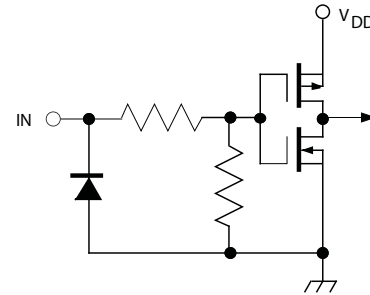
Terminal Description

| Terminal No. | Terminal Name | Function |
|--------------|---------------------|--|
| 1 | GND | Reference terminal for control logic. |
| 2 | SERIAL DATA IN | Serial-data input to the shift-register. |
| 3 | CLOCK | Clock input terminal for data shift on rising edge. |
| 4 | LATCH ENABLE | Data strobe input terminal; serial data is latched with high-level input. |
| 5-20 | OUT ₀₋₁₅ | The 16 current-sinking output terminals. |
| 21 | OUTPUT ENABLE | When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked). |
| 22 | SERIAL DATA OUT | CMOS serial-data output to the following shift-register. |
| 23 | R _{EXT} | An external resistor at this terminal establishes the output current for all sink drivers. |
| 24 | SUPPLY | (V _{DD}) The logic supply voltage (typically 5 V). |



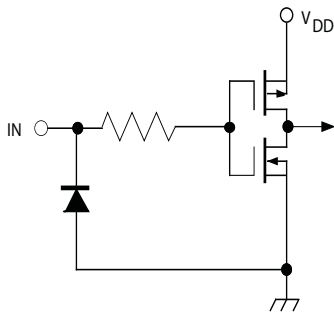
Dwg. EP-010-11

OUTPUT ENABLE (active low)



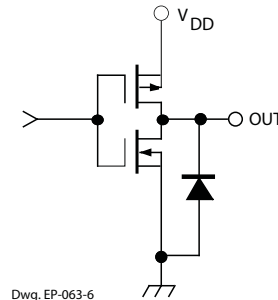
Dwg. EP-010-12

LATCH ENABLE



Dwg. EP-010-13

CLOCK and SERIAL DATA IN



Dwg. EP-063-6

SERIAL DATA OUT

TRUTH TABLE

| Serial Data Input | Clock Input | Shift Register Contents | | | | | | Serial Data Output | Latch Enable Input | Latch Contents | | | | | | Output Enable Input | Output Contents | | | | | |
|-------------------|-------------|-------------------------|----------------|----------------|-----|------------------|------------------|--------------------|--------------------|----------------|----------------|----------------|-----|------------------|----------------|---------------------|-----------------|----------------|----------------|-----|------------------|----------------|
| | | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N | | | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N | | I ₁ | I ₂ | I ₃ | ... | I _{N-1} | I _N |
| H | | H | R ₁ | R ₂ | ... | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | | |
| L | | L | R ₁ | R ₂ | ... | R _{N-2} | R _{N-1} | R _{N-1} | | | | | | | | | | | | | | |
| X | | R ₁ | R ₂ | R ₃ | ... | R _{N-1} | R _N | R _N | | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | X | L | R ₁ | R ₂ | R ₃ | ... | R _{N-1} | R _N | | | | | | | |
| | | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N | P _N | H | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N | L | P ₁ | P ₂ | P ₃ | ... | P _{N-1} | P _N |
| | | | | | | | | | | X | X | X | ... | X | X | H | H | H | ... | H | H | |

L = Low Logic (Voltage) Level H = High Logic (Voltage) Level X = Irrelevant P = Present State R = Previous State

ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$ (unless otherwise noted).

| Characteristic | Symbol | Test Conditions | Limits | | | Unit |
|---|---------------|--|-------------|-----------|-------------|------------------|
| | | | Min. | Typ. | Max. | |
| Supply Voltage Range | V_{DD} | Operating | 4.5 | 5.0 | 5.5 | V |
| Under-Voltage Lockout | $V_{DD(UV)}$ | $V_{DD} = 0\text{--}5\text{ V}$ | 3.4 | – | 4.0 | V |
| Output Current (any single output) | I_O | $V_{CE} = 0.7\text{ V}$, $R_{EXT} = 250\ \Omega$ | 64.2 | 75.5 | 86.8 | mA |
| | | $V_{CE} = 0.7\text{ V}$, $R_{EXT} = 470\ \Omega$ | 34.1 | 40.0 | 45.9 | mA |
| Output Current Matching (difference between any two outputs at same V_{CE}) | ΔI_O | $0.4\text{ V } V_{CE(A)} = V_{CE(B)}\ 0.7\text{ V}$: $R_{EXT} = 250\ \Omega$ | – | ± 1.5 | ± 6.0 | % |
| | | $R_{EXT} = 470\ \Omega$ | – | ± 1.5 | ± 6.0 | % |
| Output Leakage Current | I_{CEX} | $V_{OH} = 15\text{ V}$ | – | 1.0 | 5.0 | μA |
| Logic Input Voltage | V_{IH} | | $0.7V_{DD}$ | – | V_{DD} | V |
| | V_{IL} | | GND | – | $0.3V_{DD}$ | V |
| SERIAL DATA OUT Voltage | V_{OL} | $I_{OL} = 500\ \mu\text{A}$ | – | – | 0.4 | V |
| | V_{OH} | $I_{OH} = -500\ \mu\text{A}$ | 4.6 | – | – | V |
| Input Resistance | R_I | ENABLE Input, Pull Up | 150 | 300 | 600 | $\text{k}\Omega$ |
| | | LATCH Input, Pull Down | 100 | 200 | 400 | $\text{k}\Omega$ |
| Supply Current | $I_{DD(OFF)}$ | $R_{EXT} = \text{open}$, $V_{OE} = 5\text{ V}$ | – | 0.8 | 1.4 | mA |
| | | $R_{EXT} = 470\ \Omega$, $V_{OE} = 5\text{ V}$ | 3.5 | 6.0 | 8.0 | mA |
| | | $R_{EXT} = 250\ \Omega$, $V_{OE} = 5\text{ V}$ | 6.5 | 11 | 15 | mA |
| | $I_{DD(ON)}$ | $R_{EXT} = 470\ \Omega$, $V_{OE} = 0\text{ V}$ | 7.0 | 13 | 20 | mA |
| | | $R_{EXT} = 250\ \Omega$, $V_{OE} = 0\text{ V}$ | 10 | 22 | 32 | mA |

Typical Data is at $V_{DD} = 5\text{ V}$ and is for design information only.

SWITCHING CHARACTERISTICS at $T_A = 25^\circ\text{C}$, $V_{DD} = V_{IH} = 5\text{ V}$, $V_{CE} = 0.4\text{ V}$, $V_{IL} = 0\text{ V}$,
 $R_{EXT} = 470\ \Omega$, $I_O = 40\text{ mA}$, $V_L = 3\text{ V}$, $R_L = 65\ \Omega$, $C_L = 10.5\text{ pF}$.

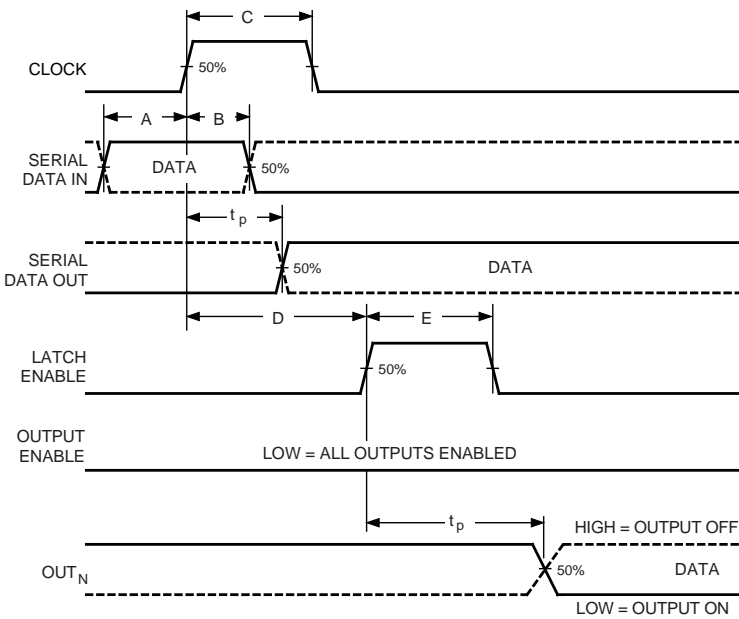
| Characteristic | Symbol | Test Conditions | Limits | | | |
|------------------------|-----------|-------------------------|--------|------|------|------|
| | | | Min. | Typ. | Max. | Unit |
| Propagation Delay Time | t_{pHL} | CLOCK-OUT _n | – | 350 | 1000 | ns |
| | | LATCH-OUT _n | – | 350 | 1000 | ns |
| | | ENABLE-OUT _n | – | 350 | 1000 | ns |
| | | CLOCK-SERIAL DATA OUT | – | 40 | – | ns |
| Propagation Delay Time | t_{pLH} | CLOCK-OUT _n | – | 300 | 1000 | ns |
| | | LATCH-OUT _n | – | 300 | 1000 | ns |
| | | ENABLE-OUT _n | – | 300 | 1000 | ns |
| | | CLOCK-SERIAL DATA OUT | – | 40 | – | ns |
| Output Fall Time | t_f | 90% to 10% voltage | 150 | 350 | 1000 | ns |
| Output Rise Time | t_r | 10% to 90% voltage | 150 | 300 | 600 | ns |

RECOMMENDED OPERATING CONDITIONS

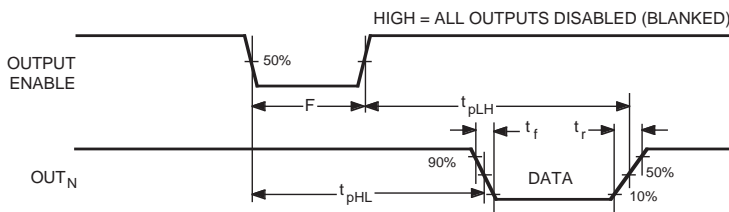
| Characteristic | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|---------------------|----------|----------------------------|-------------|------|----------------|------|
| Supply Voltage | V_{DD} | | 4.5 | 5.0 | 5.5 | V |
| Output Voltage | V_O | | – | 1.0 | 4.0 | V |
| Output Current | I_O | Continuous, any one output | – | – | 90 | mA |
| | I_{OH} | SERIAL DATA OUT | – | – | -1.0 | mA |
| | I_{OL} | SERIAL DATA OUT | – | – | 1.0 | mA |
| Logic Input Voltage | V_{IH} | | $0.7V_{DD}$ | – | $V_{DD} + 0.3$ | V |
| | V_{IL} | | -0.3 | – | $0.3V_{DD}$ | V |
| Clock Frequency | f_{CK} | Cascade operation | – | – | 10 | MHz |

TIMING REQUIREMENTS and SPECIFICATIONS

(Logic Levels are V_{DD} and Ground)



Dwg. WP-029-1



Dwg. WP-030-1A

- A. Data Active Time Before Clock Pulse (Data Set-Up Time), $t_{su(D)}$ **50 ns**
- B. Data Active Time After Clock Pulse (Data Hold Time), $t_{h(D)}$ **20 ns**
- C. Clock Pulse Width, $t_{w(CK)}$ **50 ns**
- D. Time Between Clock Activation and Latch Enable, $t_{su(L)}$ **100 ns**
- E. Latch Enable Pulse Width, $t_{w(L)}$ **100 ns**
- F. Output Enable Pulse Width, $t_{w(OE)}$ **4.5 μ s**

NOTE: Timing is representative of a 10 MHz clock. Significantly higher speeds are attainable.

Max. Clock Transition Time, t_r or t_f **10 μ s**

Serial data present at the input is transferred to the shift register on the logic 0-to-logic 1 transition of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT. The serial data must appear at the input prior to the rising edge of the CLOCK input waveform.

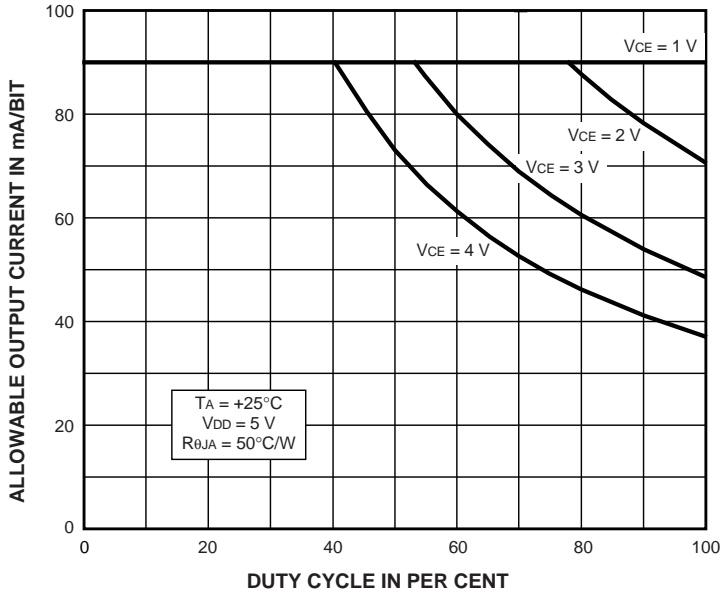
Information present at any register is transferred to the respective latch when the LATCH ENABLE is high (serial-to-parallel conversion). The latches continue to accept new data as

long as the LATCH ENABLE is held high. Applications where the latches are bypassed (LATCH ENABLE tied high) will require that the OUTPUT ENABLE input be high during serial data entry.

When the OUTPUT ENABLE input is high, the output sink drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

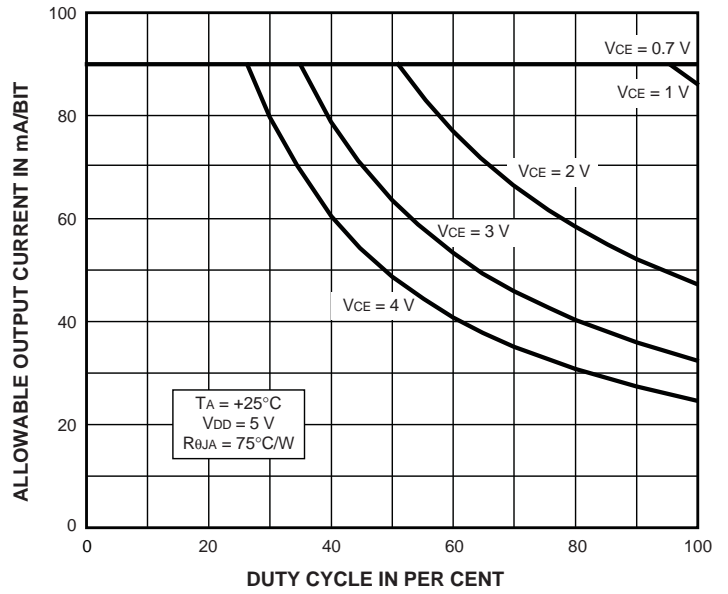
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE

A6276EA

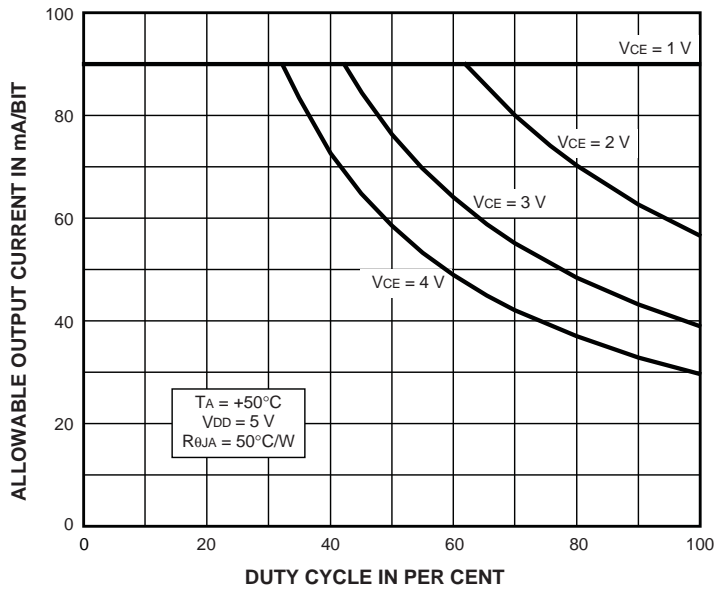


Dwg. GP-062-11

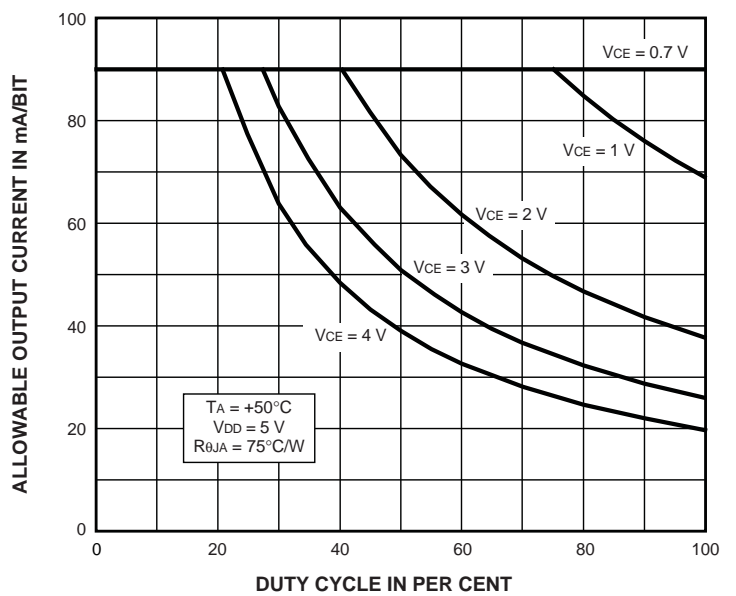
A6276ELW



Dwg. GP-062-6



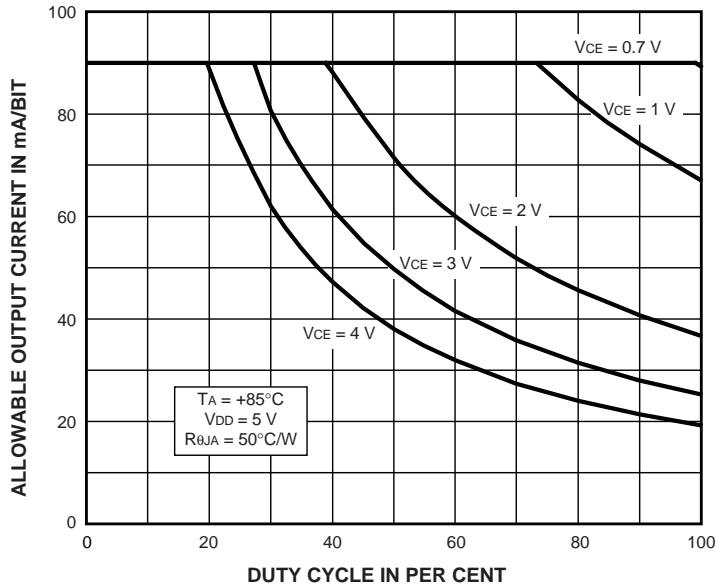
Dwg. GP-062-10



Dwg. GP-062-7

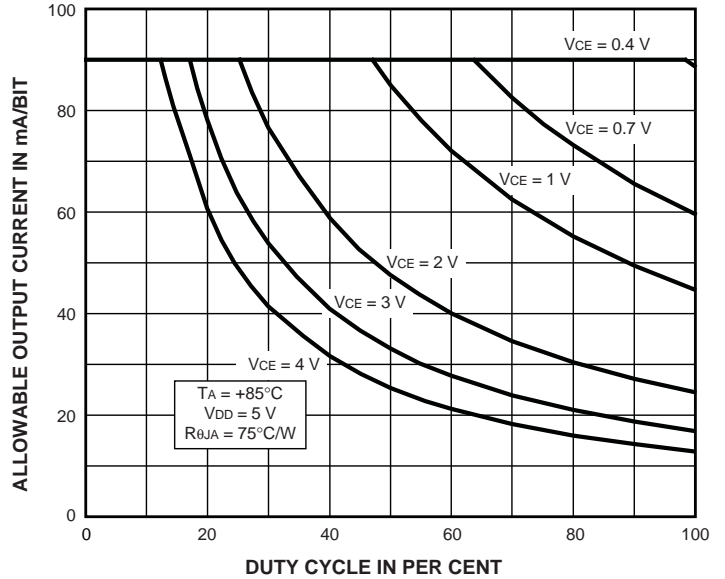
ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE (cont.)

A6276EA



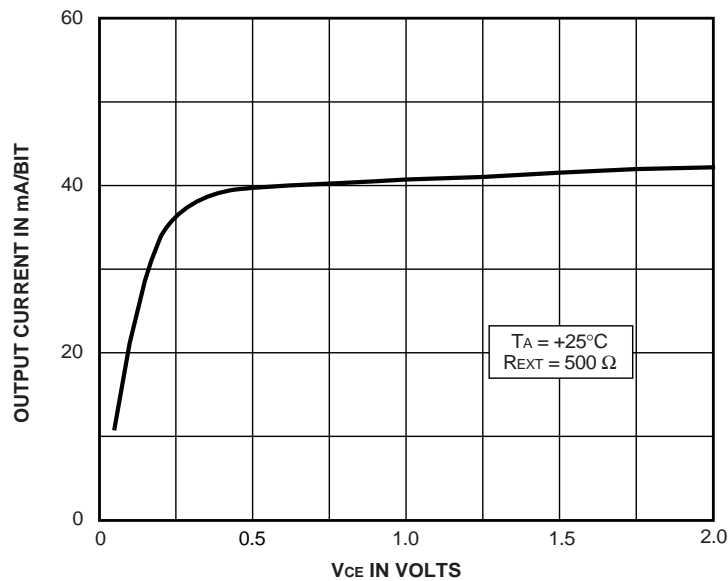
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A6276ELW



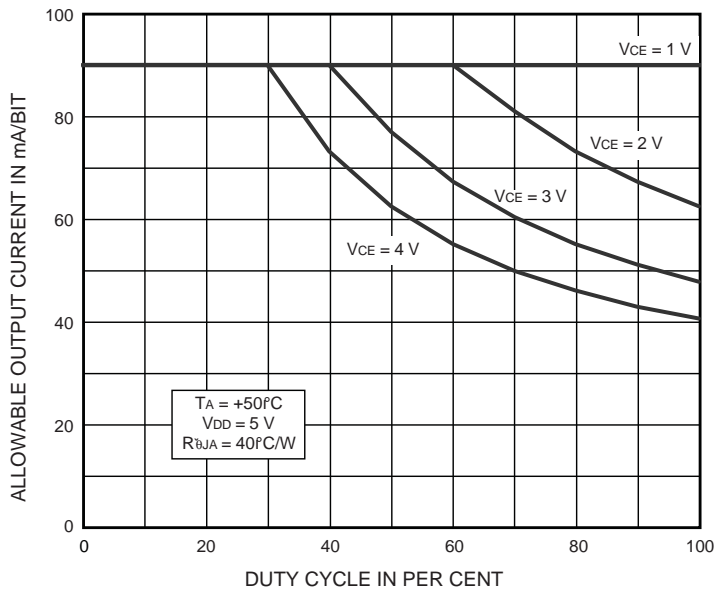
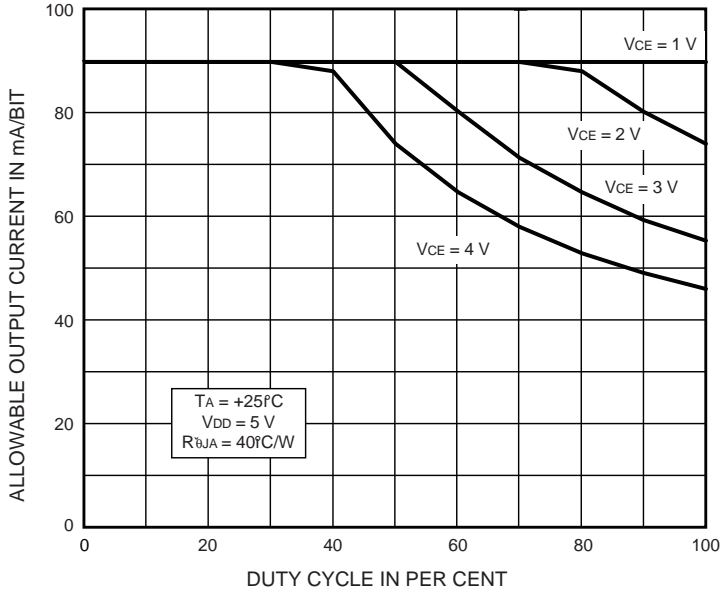
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TYPICAL CHARACTERISTICS



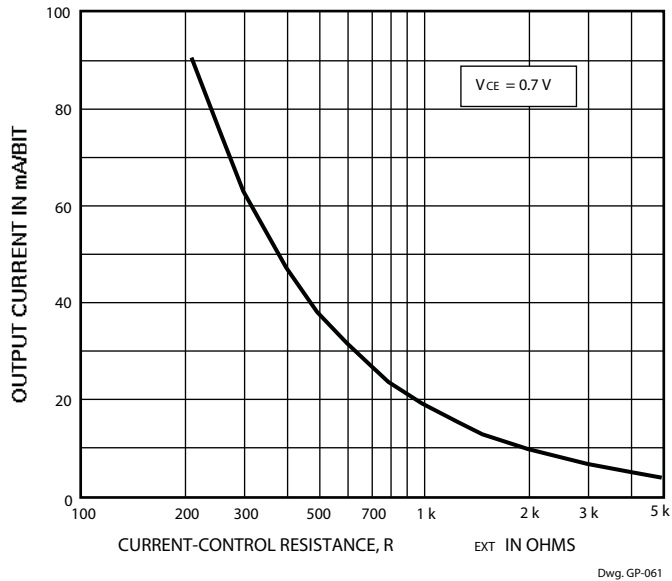
Dwg. GP-063

ALLOWABLE OUTPUT CURRENT AS A FUNCTION OF DUTY CYCLE (cont.)
A6276ELP



Applications Information

The load current per bit (I_O) is set by the external resistor (R_{EXT}) as shown in the figure below.



Package Power Dissipation (P_D). The maximum allowable package power dissipation is determined as

$$P_{D(max)} = (150 - T_A) / R_{\theta JA}$$

The actual package power dissipation is

$$P_{D(act)} = DC \cdot (V_{CE} \cdot I_O \cdot 16) + (V_{DD} \cdot I_{DD})$$

where DC is the duty cycle.

When the load supply voltage is greater than 3 V to 5 V, considering the package power dissipating limits of these devices, or if $P_{D(act)} > P_{D(max)}$, an external voltage reducer (V_{DROP}) should be used.

Load Supply Voltage (V_{LED}). These devices are designed to operate with driver voltage drops (V_{CE}) of 0.4 V to 0.7 V with LED forward voltages (V_F) of 1.2 V to 4.0 V. If higher voltages are dropped across the driver, package power dissipation will be increased significantly. To minimize package power dissipation, it is recommended to use the lowest possible load supply voltage or to set any series dropping voltage (V_{DROP}) as

$$V_{DROP} = V_{LED} - V_F - V_{CE}$$

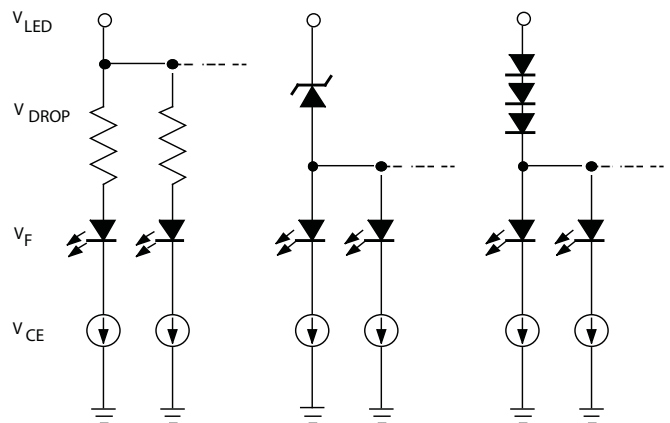
with $V_{DROP} = I_O \cdot R_{DROP}$ for a single driver, or a Zener

diode (V_Z), or a series string of diodes (approximately 0.7 V per diode) for a group of drivers. If the available voltage source will cause unacceptable dissipation and series resistors or diode(s) are undesirable, a regulator such as the Sanken Series SAI or Series SI can be used to provide supply voltages as low as 3.3 V.

For reference, typical LED forward voltages are:

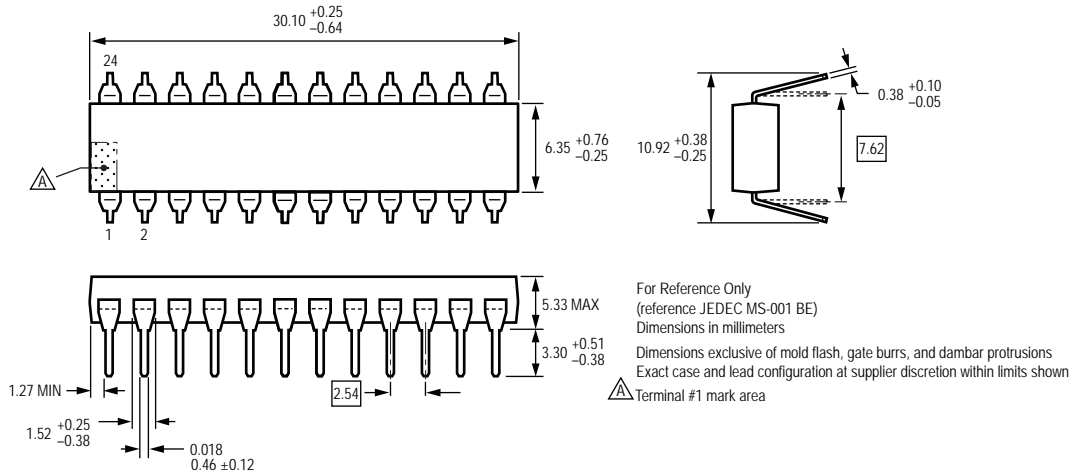
| | |
|----------|--------------|
| White | 3.5 – 4.0 V |
| Blue | 3.0 – 4.0 V |
| Green | 1.8 – 2.2 V |
| Yellow | 2.0 – 2.1 V |
| Amber | 1.9 – 2.65 V |
| Red | 1.6 – 2.25 V |
| Infrared | 1.2 – 1.5 V |

Pattern Layout. This device has a common logic-ground and power-ground terminal. If ground pattern layout contains large common-mode resistance, and the voltage between the system ground and the LATCH ENABLE or CLOCK terminals exceeds 2.5 V (because of switching noise), these devices may not operate correctly.

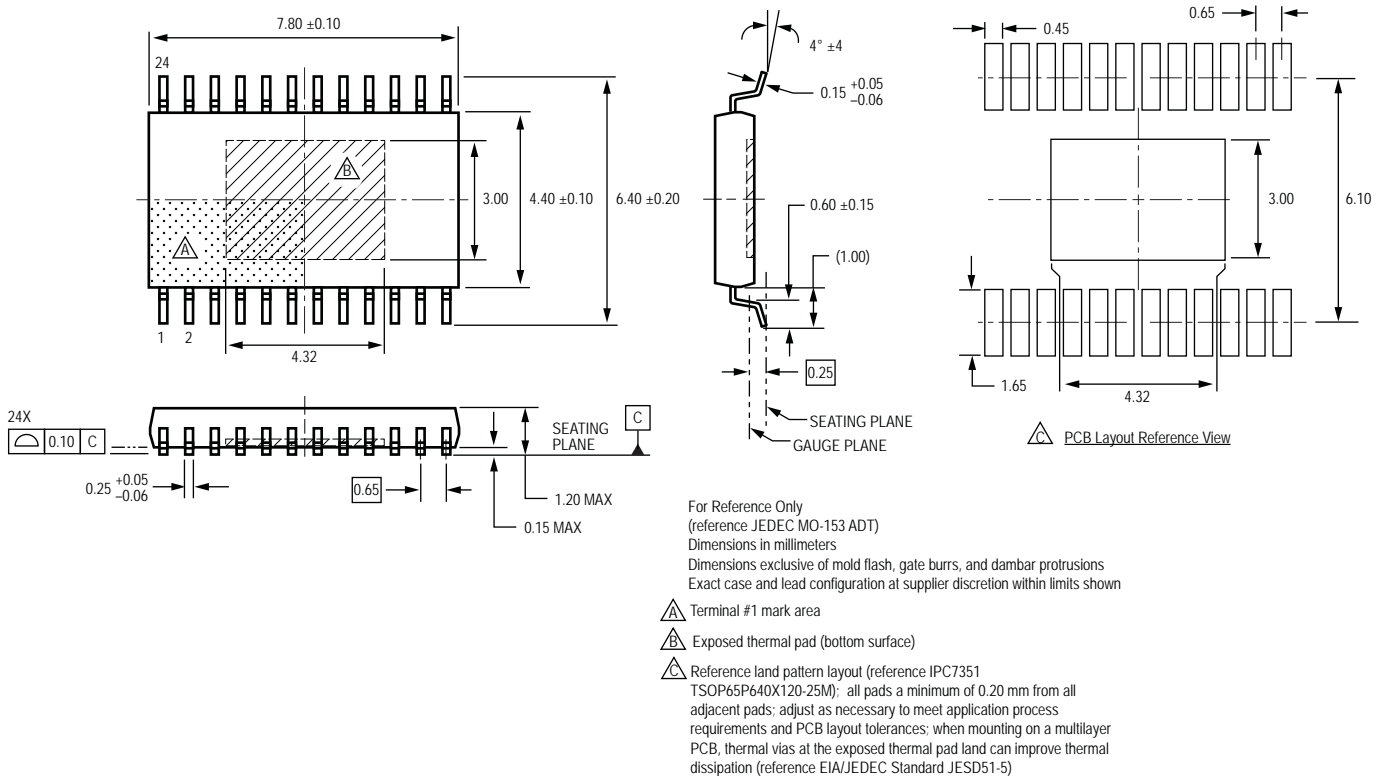


Dwg. EP-064

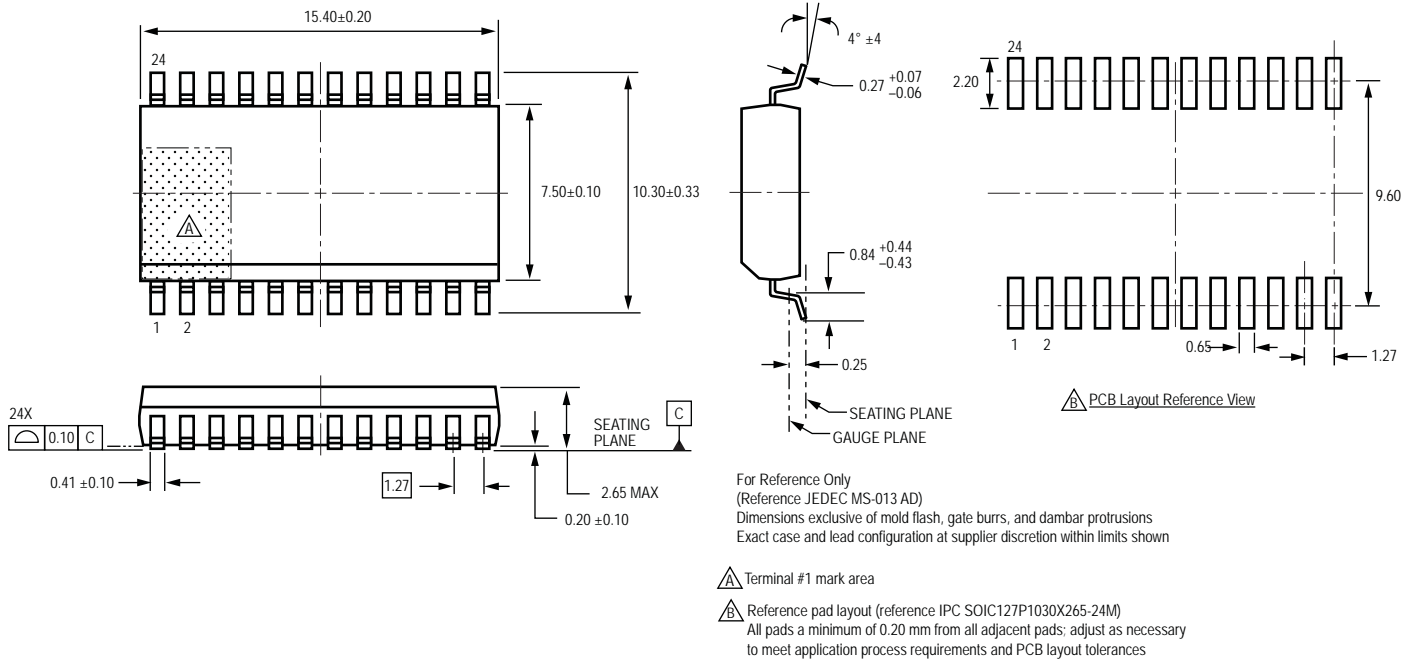
Package A, 24-pin DIP



Package A, 24-pin TSSOP with exposed thermal pad



Package LW, 24-pin SOICW



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