



**THE DATASHEET OF
A6B595KLWTR-T**



8-Bit Serial-Input DMOS Power Driver

Last Time Buy

This part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: May 3, 2010

Deadline for receipt of LAST TIME BUY orders: October 29, 2010

Recommended Substitutions:

For existing customer transition, and for new customers or new applications, contact Allegro Sales.

NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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8-Bit Serial-Input DMOS Power Driver

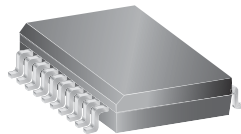
Features and Benefits

- 50 V minimum output clamp voltage
- 150 mA output current (all outputs simultaneously)
- 5 Ω typical $r_{DS(on)}$
- Low power consumption
- Replacement for TPIC6B595N and TPIC6B595DW

Packages:



18-pin DIP
(A package)



20-pin SOICW
(LW package)

Not to scale

Description

The A6B595 combines an 8-bit CMOS shift register and accompanying data latches, control circuitry, and DMOS power driver outputs. Power driver applications include relays, solenoids, and other medium-current or high-voltage peripheral power loads.

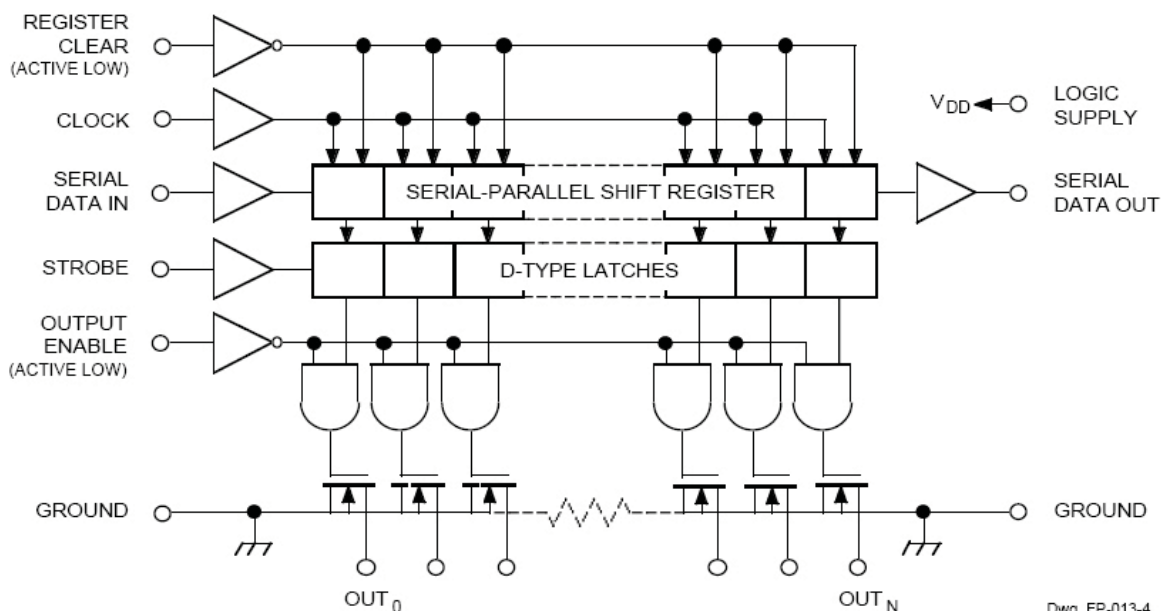
The serial-data input, CMOS shift register and latches allow direct interfacing with microprocessor-based systems. Serial-data input rates are over 5 MHz. Use with TTL may require appropriate pull-up resistors to ensure an input logic high.

A CMOS serial-data output enables cascade connections in applications requiring additional drive lines. Similar devices with reduced $r_{DS(on)}$ are available as the A6595.

The A6B595 DMOS open-drain outputs are capable of sinking up to 500 mA. All of the output drivers are disabled (the DMOS sink drivers turned off) by the OUTPUT ENABLE input high. Copper lead frames, reduced supply current requirements, and low on-state resistance allow both devices to sink 150 mA from all outputs continuously, to ambient temperatures over 85°C.

The A6B595 is furnished in a 20-pin dual in-line plastic package and a 20-pin wide-body, small-outline plastic package (SOICW) with gull-wing leads. The Pb (lead) free versions (suffix -T) have 100% matte tin leadframe plating.

Functional Block Diagram



Grounds (terminals 10, 11, and 19) must be connected together externally.

A6B595

8-Bit Serial-Input DMOS Power Driver

Selection Guide

| Part Number | Package | Packing |
|---------------|--------------|----------------------|
| A6B595KA-T | 18-pin DIP | 18 pieces per tube |
| A6B595KLWTR-T | 20-pin SOICW | 1000 pieces per reel |

Absolute Maximum Ratings

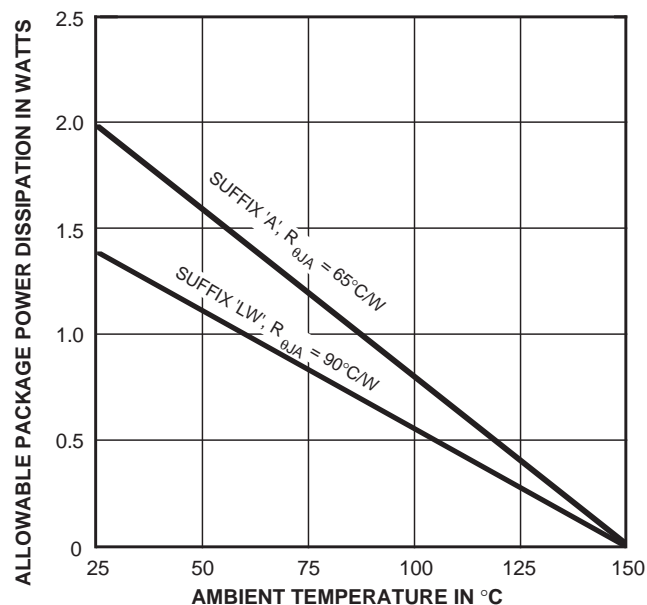
| Characteristic | Symbol | Notes | Rating | Units |
|-------------------------------|--------------|---|-------------|--------------|
| Logic Supply Voltage | V_{DD} | | 7 | V |
| Output Voltage | V_O | | 50 | V |
| Input Voltage Range | V_I | | -0.3 to 7.0 | V |
| Output Drain Current | I_O | Continuous; each output, all outputs on | 150 | mA |
| | I_{OM} | Peak; pulse duration 100 μ s, duty cycle 2% | 500 | mA |
| Single-Pulse Avalanche Energy | E_{AS} | | 30 | mJ |
| Operating Ambient Temperature | T_A | Range K | -40 to 85 | $^{\circ}$ C |
| Maximum Junction Temperature | $T_{J(max)}$ | | 150 | $^{\circ}$ C |
| Storage Temperature | T_{stg} | | -65 to 150 | $^{\circ}$ C |

Caution: These CMOS devices have input static protection (Class 3) but are still susceptible to damage if exposed to extremely high static electrical charges.

Thermal Characteristics

| Characteristic | Symbol | Test Conditions* | Value | Units |
|----------------------------|-----------------|--|-------|----------------|
| Package Thermal Resistance | $R_{\theta JA}$ | Package A, 1-layer PCB with copper limited to solder pads | 65 | $^{\circ}$ C/W |
| | | Package LW, 1-layer PCB with copper limited to solder pads | 90 | $^{\circ}$ C/W |

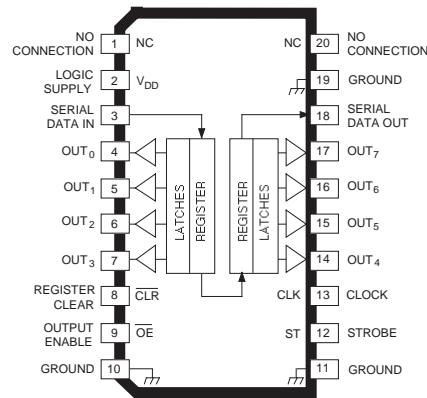
*Additional thermal information available on the Allegro website



Dwg. GS-004A



PIN-OUT DIAGRAM



Dwg. PP-029-12

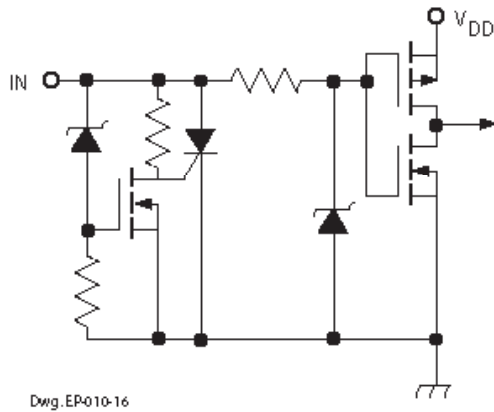
Note that the A package (DIP) and the LW package (SOIC) are electrically identical and share a common terminal number assignment.

TERMINAL DESCRIPTIONS

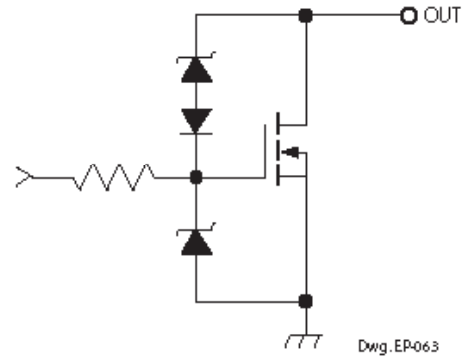
| Terminal No. | Terminal Name | Function |
|--------------|-----------------|--|
| 1 | NC | No internal connection. |
| 2 | LOGIC SUPPLY | (V_{DD}) The logic supply voltage (typically 5 V). |
| 3 | SERIAL DATA IN | Serial-data input to the shift-register. |
| 4-7 | OUT_{0-3} | Current-sinking, open-drain DMOS output terminals. |
| 8 | CLEAR | When (active) low, the registers are cleared (set low). |
| 9 | OUTPUT ENABLE | When (active) low, the output drivers are enabled; when high, all output drivers are turned OFF (blanked). |
| 10 | GROUND | Reference terminal for output voltage measurements (OUT_{0-3}). |
| 11 | GROUND | Reference terminal for output voltage measurements (OUT_{0-7}). |
| 12 | STROBE | Data strobe input terminal; shift register data is latched on rising edge. |
| 13 | CLOCK | Clock input terminal for data shift on rising edge. |
| 14-17 | OUT_{4-7} | Current-sinking, open-drain DMOS output terminals. |
| 18 | SERIAL DATA OUT | CMOS serial-data output to the following shift register. |
| 19 | GROUND | Reference terminal for input voltage measurements. |
| 20 | NC | No internal connection. |

NOTE — Grounds (terminals 10, 11, and 19) must be connected together externally.

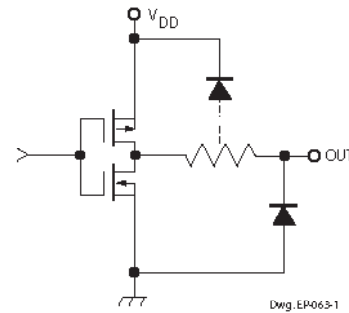
LOGIC INPUTS



DMOS POWER DRIVER OUTPUT



SERIAL DATA OUT



RECOMMENDED OPERATING CONDITIONS

over operating temperature range

- Logic Supply Voltage Range, V_{DD} 4.5 V to 5.5 V
- High-Level Input Voltage, V_{IH} $\geq 0.85V_{DD}$
- Low-level input voltage, V_{IL} $\leq 0.15V_{DD}$

TRUTH TABLE

| Data Input | Clock Input | Shift Register Contents | | | | | | Serial Data Output | Strobe | Latch Contents | | | | | | Output Enable | Output Contents | | | | | |
|------------|-------------|-------------------------|-------|-------|-----|-------|-------|--------------------|--------|----------------|-------|-------|-----|-------|-------|---------------|-----------------|-------|-------|-----|-------|-------|
| | | I_0 | I_1 | I_2 | ... | I_6 | I_7 | | | l_0 | l_1 | l_2 | ... | l_6 | l_7 | | o_0 | o_1 | o_2 | ... | o_6 | o_7 |
| H | | H | R_0 | R_1 | ... | R_5 | R_6 | R_6 | | | | | | | | | | | | | | |
| L | | L | R_0 | R_1 | ... | R_5 | R_6 | R_6 | | | | | | | | | | | | | | |
| X | | R_0 | R_1 | R_2 | ... | R_6 | R_7 | R_7 | | | | | | | | | | | | | | |
| | | X | X | X | ... | X | X | X | — | R_0 | R_1 | R_2 | ... | R_6 | R_7 | | | | | | | |
| | | P_0 | P_1 | P_2 | ... | P_6 | P_7 | P_7 | | P_0 | P_1 | P_2 | ... | P_6 | P_7 | L | | | | | | |
| | | | | | | | | | | X | X | X | ... | X | X | H | | | | | | |

L = Low Logic Level H = High Logic Level X = Irrelevant P = Present State R = Previous State

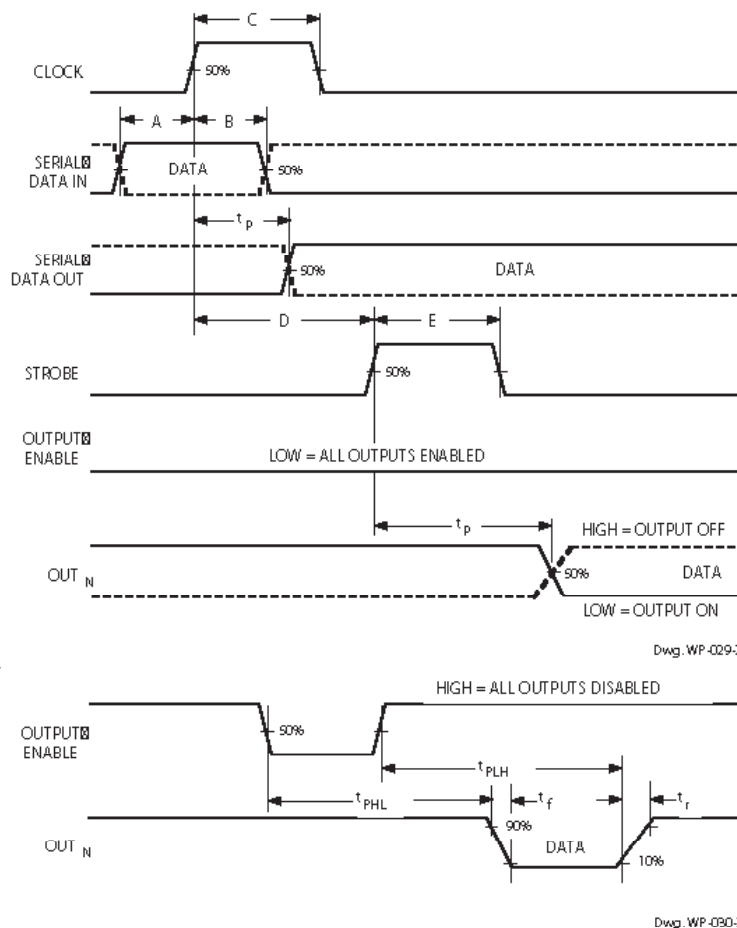
ELECTRICAL CHARACTERISTICS at $T_A = +25^\circ\text{C}$, $V_{DD} = 5\text{ V}$, $t_{ir} = t_{if} = 10\text{ ns}$ (unless otherwise specified).

| Characteristic | Symbol | Test Conditions | Limits | | | Units |
|---|----------------|---|--------|-------|------|---------------|
| | | | Min. | Typ. | Max. | |
| Output Breakdown Voltage | $V_{(BR)DSX}$ | $I_O = 1\text{ mA}$ | 50 | — | — | V |
| Off-State Output Current | I_{DSX} | $V_O = 40\text{ V}$, $V_{DD} = 5.5\text{ V}$ | — | 0.1 | 5.0 | μA |
| | | $V_O = 40\text{ V}$, $V_{DD} = 5.5\text{ V}$, $T_A = 125^\circ\text{C}$ | — | 0.15 | 8.0 | μA |
| Static Drain-Source On-State Resistance | $r_{DS(on)}$ | $I_O = 100\text{ mA}$, $V_{DD} = 4.5\text{ V}$ | — | 4.2 | 5.7 | Ω |
| | | $I_O = 100\text{ mA}$, $V_{DD} = 4.5\text{ V}$, $T_A = 125^\circ\text{C}$ | — | 6.8 | 9.5 | Ω |
| | | $I_O = 350\text{ mA}$, $V_{DD} = 4.5\text{ V}$ (see note) | — | 5.5 | 8.0 | Ω |
| Nominal Output Current | I_{ON} | $V_{DS(on)} = 0.5\text{ V}$, $T_A = 85^\circ\text{C}$ | — | 90 | — | mA |
| Logic Input Current | I_{IH} | $V_I = V_{DD} = 5.5\text{ V}$ | — | — | 1.0 | μA |
| | I_{IL} | $V_I = 0$, $V_{DD} = 5.5\text{ V}$ | — | — | -1.0 | μA |
| SERIAL-DATA Output Voltage | V_{OH} | $I_{OH} = -20\text{ }\mu\text{A}$, $V_{DD} = 4.5\text{ V}$ | 4.4 | 4.49 | — | V |
| | | $I_{OH} = -4\text{ mA}$, $V_{DD} = 4.5\text{ V}$ | 4.0 | 4.2 | — | V |
| | V_{OL} | $I_{OL} = 20\text{ }\mu\text{A}$, $V_{DD} = 4.5\text{ V}$ | — | 0.005 | 0.1 | V |
| | | $I_{OL} = 4\text{ mA}$, $V_{DD} = 4.5\text{ V}$ | — | 0.3 | 0.5 | V |
| Prop. Delay Time | t_{PLH} | $I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$ | — | 150 | — | ns |
| | t_{PHL} | $I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$ | — | 90 | — | ns |
| Output Rise Time | t_r | $I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$ | — | 200 | — | ns |
| Output Fall Time | t_f | $I_O = 100\text{ mA}$, $C_L = 30\text{ pF}$ | — | 200 | — | ns |
| Supply Current | $I_{DD(OFF)}$ | $V_{DD} = 5.5\text{ V}$, Outputs OFF | — | 20 | 100 | μA |
| | $I_{DD(ON)}$ | $V_{DD} = 5.5\text{ V}$, Outputs ON | — | 150 | 300 | μA |
| | $I_{DD(fclk)}$ | $f_{clk} = 5\text{ MHz}$, $C_L = 30\text{ pF}$, Outputs OFF | — | 0.4 | 5.0 | mA |

Typical Data is at $V_{DD} = 5\text{ V}$ and is for design information only.

NOTE — Pulse test, duration 100 μs , duty cycle 2%.

TIMING REQUIREMENTS and SPECIFICATIONS
(Logic Levels are V_{DD} and Ground)



- A.** Data Active Time Before Clock Pulse
(Data Set-Up Time), $t_{su(D)}$ **20 ns**
- B.** Data Active Time After Clock Pulse
(Data Hold Time), $t_{h(D)}$ **20 ns**
- C.** Clock Pulse Width, $t_{w(CLK)}$ **40 ns**
- D.** Time Between Clock Activation
and Strobe, $t_{su(ST)}$ **50 ns**
- E.** Strobe Pulse Width, $t_{w(ST)}$ **50 ns**
- F.** Output Enable Pulse Width, $t_{w(OE)}$ **4.5 μ s**

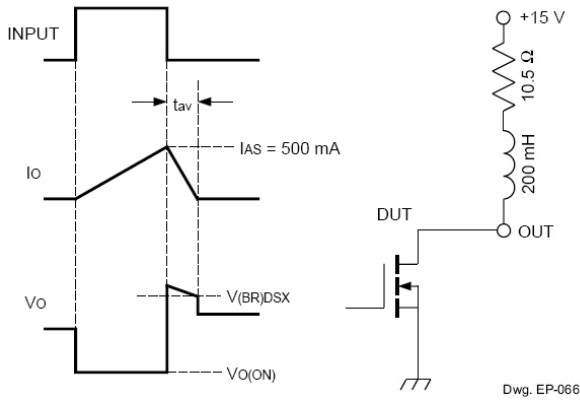
NOTE – Timing is representative of a 12.5 MHz clock.
Higher speeds are attainable.

Serial data present at the input is transferred to the shift register on the rising edge of the CLOCK input pulse. On succeeding CLOCK pulses, the registers shift data information towards the SERIAL DATA OUTPUT.

Information present at any register is transferred to the respective latch on the rising edge of the STROBE input pulse (serial-to-parallel conversion).

When the OUTPUT ENABLE input is high, the output source drivers are disabled (OFF). The information stored in the latches is not affected by the OUTPUT ENABLE input. With the OUTPUT ENABLE input low, the outputs are controlled by the state of their respective latches.

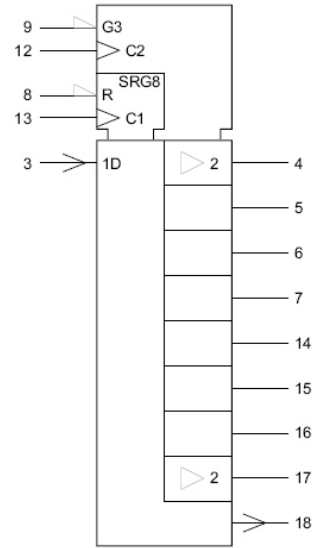
TEST CIRCUITS



$$E_{AS} = I_{AS} \times V_{(BR)DSX} \times t_{AV}/2$$

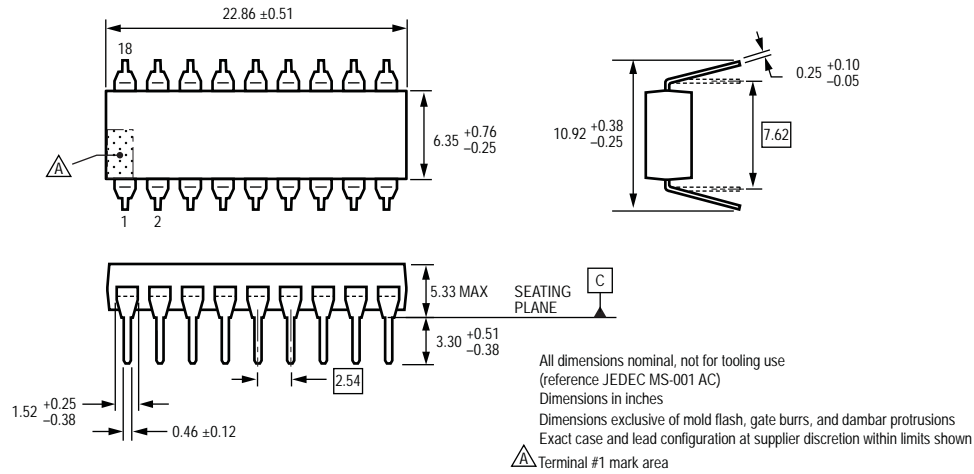
Single-Pulse Avalanche Energy Test Circuit and Waveforms

LOGIC SYMBOL

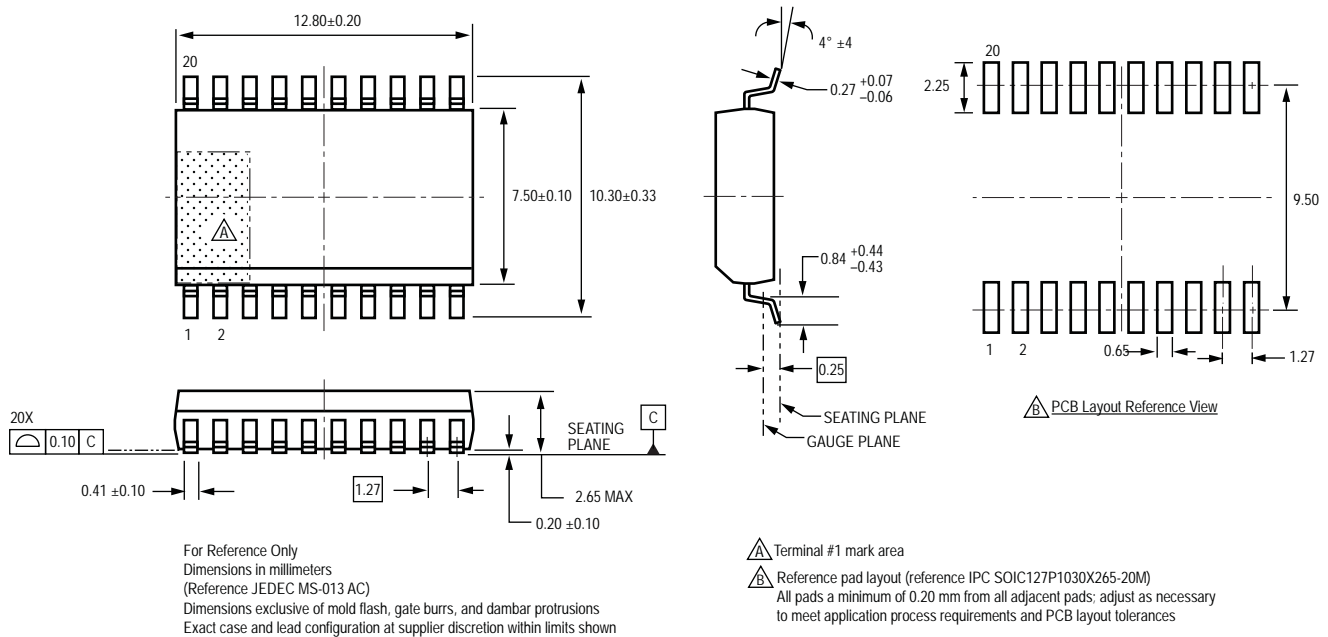


Dwg. FP-043

Package A, 18-Pin DIP



Package LW, 20-Pin SOICW



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