THE DATASHEET OF

AD5347BRUZ

2.5 V to 5.5 V, Parallel Interface Octal Voltage Output 8-/10-/12-Bit DACs

Data Sheet **AD5346/AD5347/AD5348**

FEATURES

AD5346: octal 8-bit DAC
AD5347: octal 10-bit DAC
AD5348: octal 12-bit DAC
Low power operation: 1.4 mA (max) at 3.6 V
Power-down to 120 nA at 3 V, 400 nA at 5 V
Guaranteed monotonic by design over all codes
Rail-to-rail output range: 0 V to V_{REF} or 0 V to 2 × V_{REF}
Power-on reset to 0 V
Simultaneous update of DAC outputs via $\overline{LDAC}$ pin
Asynchronous $\overline{CLR}$ facility
Readback
Buffered/unbuffered reference inputs
20 ns $\overline{WR}$ time
38-lead TSSOP/6 mm × 6 mm 40-lead LFCSP packaging
Temperature range: −40°C to +105°C

APPLICATIONS

Portable battery-powered instruments
Digital gain and offset adjustment
Programmable voltage and current sources
Optical networking
Automatic test equipment
Mobile communications
Programmable attenuators
Industrial process control

GENERAL DESCRIPTION

The AD5346/AD5347/AD5348[1] are octal 8-, 10-, and 12-bit DACs, operating from a 2.5 V to 5.5 V supply. These devices incorporate an on-chip output buffer that can drive the output to both supply rails, and also allow a choice of buffered or unbuffered reference input.

The AD5346/AD5347/AD5348 have a parallel interface. $\overline{CS}$ selects the device and data is loaded into the input registers on the rising edge of $\overline{WR}$. A readback feature allows the internal DAC registers to be read back through the digital port.

The GAIN pin on these devices allows the output range to be set at 0 V to V_{REF} or 0 V to 2 × V_{REF}.

Input data to the DACs is double-buffered, allowing simultaneous update of multiple DACs in a system using the $\overline{LDAC}$ pin.

An asynchronous $\overline{CLR}$ input is also provided, which resets the contents of the input register and the DAC register to all zeros. These devices also incorporate a power-on reset circuit that ensures that the DAC output powers on to 0 V and remains there until valid data is written to the device.

All three parts are pin compatible, which allows users to select the amount of resolution appropriate for their application without redesigning their circuit board.

FUNCTIONAL BLOCK DIAGRAM

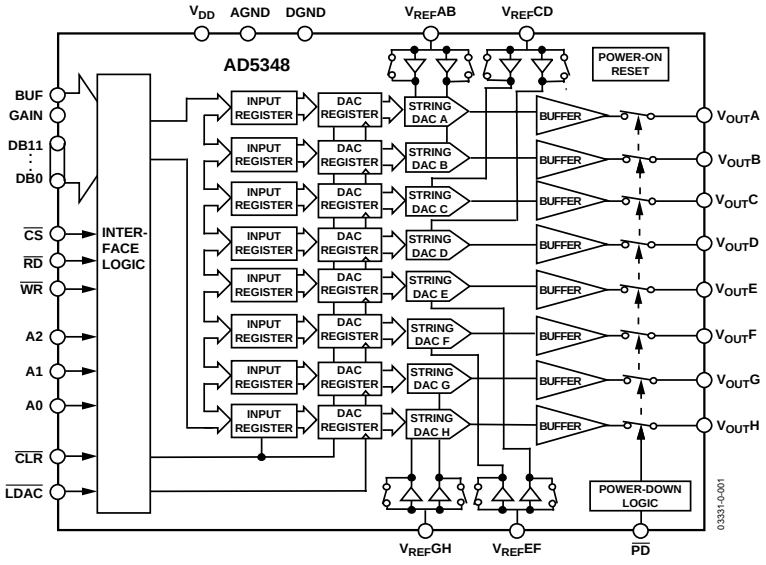

Figure 1.

[1] Protected by U.S. Patent No. 5,969,657.

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REVISION HISTORY

6/15—Rev. 0 to Rev. A

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Deleted Driving V_{DD} from the Reference Voltage Section and Figure 42; Renumbered Sequentially ... 20
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11/03—Revision 0: Initial Version

SPECIFICATIONS

VDD = 2.5 V to 5.5 V; VREF = 2 V; RL = 2 kΩ to GND; CL = 200 pF to GND; all specifications TMIN to TMAX, unless otherwise noted.

Table 1.

	B Version[1]				
Parameter[2]	**Min**	**Typ**	**Max**	**Unit**	**Test Conditions/Comments**
DC PERFORMANCE[3, 4]					
AD5346					
Resolution		8		Bits	
Relative Accuracy		±0.15	±1	LSB	
Differential Nonlinearity		±0.02	±0.25	LSB	Guaranteed monotonic by design over all codes
AD5347					
Resolution		10		Bits	
Relative Accuracy		±0.5	±4	LSB	
Differential Nonlinearity		±0.05	±0.5	LSB	Guaranteed monotonic by design over all codes
AD5348					
Resolution		12		Bits	
Relative Accuracy		±2	±16	LSB	
Differential Nonlinearity		±0.2	±1	LSB	Guaranteed monotonic by design over all codes
Offset Error		±0.4	±3	% of FSR	
Gain Error		±0.1	±1	% of FSR	
Lower Deadband[5]		10	60	mV	Lower deadband exists only if offset error is negative
Upper Deadband[5]		10	60	mV	V_{DD} = 5 V; upper deadband exists only if $V_{REF} = V_{DD}$
Offset Error Drift[6]		−12		ppm of FSR/°C	
Gain Error Drift[6]		−5		ppm of FSR/°C	
DC Power Supply Rejection Ratio[6]		−60		dB	ΔV_{DD} = ±10%
DC Crosstalk[6]		200		µV	R_L = 2 kΩ to GND, 2 kΩ to V_{DD}; C_L = 200 pF to GND; Gain = +1
DAC REFERENCE INPUT[6]					
V_{REF} Input Range	1		V_{DD}	V	Buffered reference mode
V_{REF} Input Range	0.25		V_{DD}	V	Unbuffered reference mode
V_{REF} Input Impedance		>10		MΩ	Buffered reference mode and power-down mode
		90		kΩ	Gain = +1; input impedance = R_{DAC}
		45		kΩ	Gain = +2; input impedance = R_{DAC}
Reference Feedthrough		−90		dB	Frequency = 10 kHz
Channel-to-Channel Isolation		−75		dB	Frequency = 10 kHz
OUTPUT CHARACTERISTICS[6]					
Minimum Output Voltage[4, 7]		0.001		V min	Rail-to-rail operation
Maximum Output Voltage[4, 7]		V_{DD} − 0.001		V max	
DC Output Impedance		0.5		Ω	
Short Circuit Current		25		mA	V_{DD} = 5 V
		16		mA	V_{DD} = 3 V
Power-Up Time		2.5		µs	Coming out of power-down mode; V_{DD} = 5 V
		5		µs	Coming out of power-down mode; V_{DD} = 3 V

Parameter[2]	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS[6]					
Input Current			±1	μA	
V_{IL}, Input Low Voltage			0.8	V	V_{DD} = 5 V ±10%
			0.7	V	V_{DD} = 3 V ±10%
			0.6	V	V_{DD} = 2.5 V
V_{IH}, Input High Voltage	1.7			V	V_{DD} = 2.5 V to 5.5 V
Pin Capacitance		5		pF	
LOGIC OUTPUTS[6]					
V_{DD} = 4.5 V to 5.5 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} – 1			V	I_{SOURCE} = 200 μA
V_{DD} = 2.5 V to 3.6 V					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 200 μA
Output High Voltage, V_{OH}	V_{DD} – 0.5			V	I_{SOURCE} = 200 μA
POWER REQUIREMENTS					
V_{DD}	2.5		5.5	V	
I_{DD} (Normal Mode)					$V_{IH} = V_{DD}$, V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		1	1.65	mA	All DACs in unbuffered mode. In buffered mode,
V_{DD} = 2.5 V to 3.6 V		0.8	1.4	mA	extra current is typically x μA per DAC, where x = 5 μA + V_{REF}/R_{DAC}
I_{DD} (Power-Down Mode)					$V_{IH} = V_{DD}$, V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		0.4	1	μA	
V_{DD} = 2.5 V to 3.6 V		0.12	1	μA	

[1] Temperature range: B Version: −40°C to +105°C; typical specifications are at 25°C.
[2] See the Terminology section.
[3] Linearity is tested using a reduced code range: AD5346 (Code 8 to Code 255); AD5347 (Code 28 to Code 1023); AD5348 (Code 115 to Code 4095).
[4] DC specifications tested with outputs unloaded.
[5] This corresponds to x codes. x = deadband voltage/LSB size.
[6] Guaranteed by design and characterization, not production tested.
[7] For the amplifier output to reach its minimum voltage, offset error must be negative. For the amplifier output to reach its maximum voltage, $V_{REF} = V_{DD}$ and the offset plus gain error must be positive.

AC CHARACTERISTICS

VDD = 2.5 V to 5.5 V; RL = 2 kΩ to GND; CL = 200 pF to GND; all specifications TMIN to TMAX, unless otherwise noted. Guaranteed by design and characterization, not production tested.

Table 2.

Parameter[2]	B Version[1] Min	Typ	Max	Unit	Test Conditions/Comments
Output Voltage Settling Time					V_{REF} = 2 V
AD5346		6	8	µs	1/4 scale to 3/4 scale change (40 H to C0 H)
AD5347		7	9	µs	1/4 scale to 3/4 scale change (100 H to 300 H)
AD5348		8	10	µs	1/4 scale to 3/4 scale change (400 H to C00 H)
Slew Rate		0.7		V/µs	
Major Code Transition Glitch Energy		8		nV-s	1 LSB change around major carry
Digital Feedthrough		0.5		nV-s	
Digital Crosstalk		1		nV-s	
Analog Crosstalk		1		nV-s	
DAC-to-DAC Crosstalk		3.5		nV-s	
Multiplying Bandwidth		200		kHz	V_{REF} = 2 V ±0.1 V p-p; unbuffered mode
Total Harmonic Distortion		−70		dB	V_{REF} = 2. V ±0.1 V p-p; frequency = 10 kHz; unbuffered mode

[1] Temperature range: B Version: −40°C to +105°C; typical specifications are at 25°C.
[2] See the Terminology section.

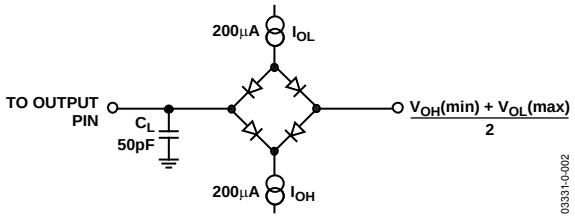


Figure 2. Load Circuit for Digital Output Timing Specifications

TIMING CHARACTERISTICS

VDD = 2.5 V to 5.5 V; all specifications TMIN to TMAX, unless otherwise noted. Guaranteed by design and characterization, not production tested. All input signals are specified with tr = tf = 5 ns (10% to 90% of V_{DD}) and timed from a voltage level of (V_{IL} + V_{IH})/2. See Figure 2.

Table 3.

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Condition/Comments
Data Write Mode (Figure 3)			
t_1	0	ns min	$\overline{CS}$ to $\overline{WR}$ setup time
t_2	0	ns min	$\overline{CS}$ to $\overline{WR}$ hold time
t_3	20	ns min	$\overline{WR}$ pulse width
t_4	5	ns min	Data, GAIN, BUF setup time
t_5	4.5	ns min	Data, GAIN, BUF hold time
t_6	5	ns min	Synchronous mode. $\overline{WR}$ falling to $\overline{LDAC}$ falling.
t_7	5	ns min	Synchronous mode. $\overline{LDAC}$ falling to $\overline{WR}$ rising.
t_8	4.5	ns min	Synchronous mode. $\overline{WR}$ rising to $\overline{LDAC}$ rising.
t_9	5	ns min	Asynchronous mode. $\overline{LDAC}$ rising to $\overline{WR}$ rising.
t_{10}	4.5	ns min	Asynchronous mode. $\overline{WR}$ rising to $\overline{LDAC}$ falling.
t_{11}	20	ns min	$\overline{LDAC}$ pulse width
t_{12}	10	ns min	$\overline{CLR}$ pulse width
t_{13}	20	ns min	Time between $\overline{WR}$ cycles
t_{14}	20	ns min	A0, A1, A2 setup time
t_{15}	0	ns min	A0, A1, A2 hold time

Parameter	Limit at T_{MIN}, T_{MAX}	Unit	Test Condition/Comments
Data Readback Mode (Figure 4)			
t_{16}	0	ns min	A0, A1, A2 to $\overline{CS}$ setup time
t_{17}	0	ns min	A0, A1, A2 to $\overline{CS}$ hold time
t_{18}	0	ns min	$\overline{CS}$ to falling edge of $\overline{RD}$
t_{19}	20	ns min	$\overline{RD}$ pulse width; V_{DD} = 3.6 V to 5.5 V
	30	ns min	$\overline{RD}$ pulse width; V_{DD} = 2.5 V to 3.6 V
t_{20}	0	ns min	$\overline{CS}$ to $\overline{RD}$ hold time
t_{21}	22	ns max	Data access time after falling edge of $\overline{RD}$; V_{DD} = 3.6 V to 5.5 V
	30	ns max	Data access time after falling edge of $\overline{RD}$ V_{DD} = 2.5 V to 3.6 V
t_{22}	4	ns min	Bus relinquish time after rising edge of $\overline{RD}$
	30	ns max	
t_{23}	22	ns max	$\overline{CS}$ falling edge to data; V_{DD} = 3.6 V to 5.5 V
	30	ns max	$\overline{CS}$ falling edge to data; V_{DD} = 2.5 V to 3.6 V
t_{24}	30	ns min	Time between $\overline{RD}$ cycles
t_{25}	30	ns min	Time from $\overline{RD}$ to $\overline{WR}$
t_{26}	30	ns min	Time from $\overline{WR}$ to $\overline{RD}$, V_{DD} = 3.6 V to 5.5 V
	50	ns min	Time from $\overline{WR}$ to $\overline{RD}$, V_{DD} = 2.5 V to 3.6 V

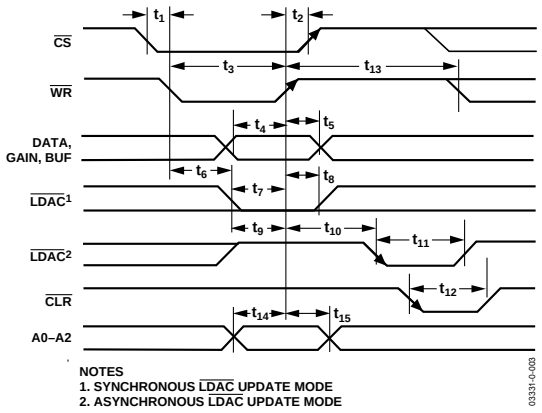


Figure 3. Parallel Interface Write Timing Diagram

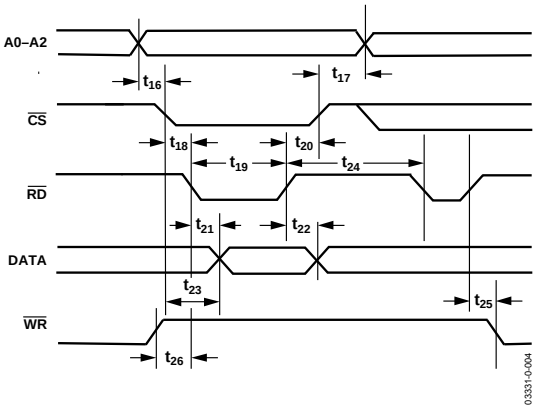


Figure 4. Parallel Interface Read Timing Diagram

ABSOLUTE MAXIMUM RATINGS

TA = 25°C, unless otherwise noted.

Table 4.

Parameter	Rating
V_{DD} to GND	–0.3 V to +7 V
Digital Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Digital Output Voltage to GND	–0.3 V to V_{DD} + 0.3 V
Reference Input Voltage to GND	–0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	–0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial (B Version)	–40°C to +105°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature	150°C
38-Lead TSSOP Package	
Power Dissipation	$(T_J \text{ max} – T_A)/ \theta_{JA}$ mW
θ_{JA} Thermal Impedance	98.3°C/W
θ_{JC} Thermal Impedance	8.9°C/W
40-Lead LFCSP Package	
Power Dissipation	$(T_J \text{ max} – T_A)/ \theta_{JA}$ mW
θ_{JA} Thermal Impedance (3-layer board)	29.6°C/W
Lead Temperature, Soldering (10 sec)	300°C
IR Reflow, Peak Temperature	220°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those listed in the operational sections of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

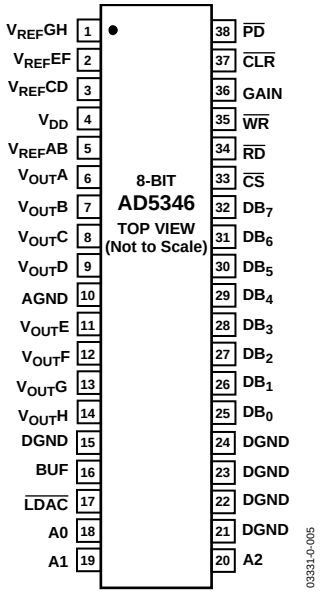
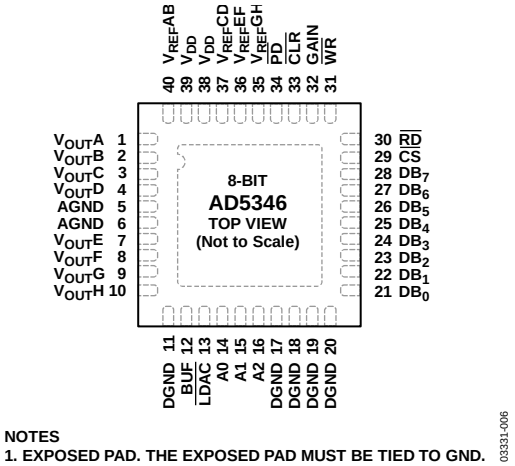


Figure 5. AD5346 Pin Configuration—TSSOP



NOTES
1. EXPOSED PAD. THE EXPOSED PAD MUST BE TIED TO GND.

Figure 6. AD5346 Pin Configuration—LFCSP

Table 5. AD5346 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	35	$V_{REF}GH$	Reference Input for DACs G and H.
2	36	$V_{REF}EF$	Reference Input for DACs E and F.
3	37	$V_{REF}CD$	Reference Input for DACs C and D.
4	38, 39	V_{DD}	Power Supply Pin(s). This part can operate from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. Both V_{DD} pins on the LFCSP package must be at the same potential.
5	40	$V_{REF}AB$	Reference Input for DACs A and B.
6 to 9, 11 to 14	1 to 4, 7 to 10	$V_{OUT}X$	Output of DAC X. Buffered output with rail-to-rail operation.
10	5, 6	AGND	Analog Ground. Ground reference for analog circuitry.
15, 21 to 24	11, 17 to 20	DGND	Digital Ground. Ground reference for digital circuitry.
16	12	BUF	Buffer Control Pin. Controls whether the reference input to the DAC is buffered or unbuffered.
17	13	$\overline{LDAC}$	Active Low Control Input. Updates the DAC registers with the contents of the input registers, which allows all DAC outputs to be simultaneously updated.
18	14	A0	LSB Address Pin. Selects which DAC is to be written to.
19	15	A1	Address Pin. Selects which DAC is to be written to.
20	16	A2	MSB Address Pin. Selects which DAC is to be written to.
25 to 32	21 to 28	DB_0 to DB_7	Eight Parallel Data Inputs. DB_7 is the MSB of these eight bits.
33	29	$\overline{CS}$	Active Low Chip Select Input. Used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to read back data from a DAC.
34	30	$\overline{RD}$	Active Low Read Input. Used in conjunction with $\overline{CS}$ to read data back from the internal DACs.
35	31	$\overline{WR}$	Active Low Write Input. Used in conjunction with $\overline{CS}$ to write data to the parallel interface.
36	32	GAIN	Gain Control Pin. Controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}.
37	33	$\overline{CLR}$	Asynchronous Active Low Control Input. Clears all input registers and DAC registers to zeros.
38	34	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
Not applicable	41	EPAD	Exposed Pad. The exposed pad must be tied to GND.

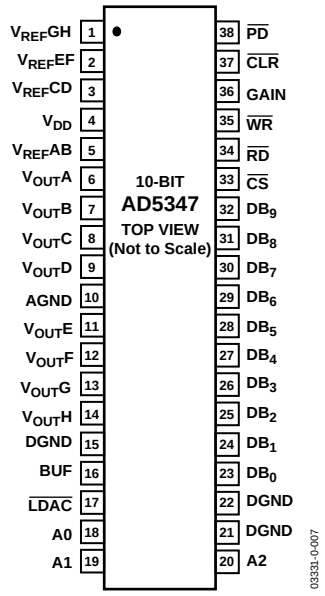


Figure 7. AD5347 Pin Configuration—TSSOP

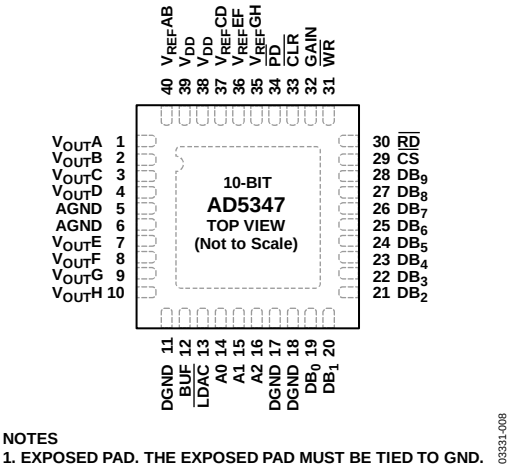


Figure 8. AD5347 Pin Configuration—LFCSP

Table 6. AD5347 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	35	$V_{REF}GH$	Reference Input for DACs G and H.
2	36	$V_{REF}EF$	Reference Input for DACs E and F.
3	37	$V_{REF}CD$	Reference Input for DACs C and D.
4	38, 39	V_{DD}	Power Supply Pin(s). This part can operate from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. Both V_{DD} pins on the LFCSP package must be at the same potential.
5	40	$V_{REF}AB$	Reference Input for DACs A and B.
6 to 9, 11 to 14	1 to 4, 7 to 10	$V_{OUT}X$	Output of DAC X. Buffered output with rail-to-rail operation.
10	5, 6	AGND	Analog Ground. Ground reference for analog circuitry.
15, 21 to 22	11, 17 to 18	DGND	Digital Ground. Ground reference for digital circuitry.
16	12	BUF	Buffer Control Pin. Controls whether the reference input to the DAC is buffered or unbuffered.
17	13	$\overline{LDAC}$	Active Low Control Input. Updates the DAC registers with the contents of the input registers, which allows all DAC outputs to be simultaneously updated.
18	14	A0	LSB Address Pin. Selects which DAC is to be written to.
19	15	A1	Address Pin. Selects which DAC is to be written to.
20	16	A2	MSB Address Pin. Selects which DAC is to be written to.
23 to 32	19 to 28	DB_0 to DB_9	Ten Parallel Data Inputs. DB_9 Is the MSB of these ten bits.
33	29	$\overline{CS}$	Active Low Chip Select Input. Used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to read back data from a DAC.
34	30	$\overline{RD}$	Active Low Read Input. Used in conjunction with $\overline{CS}$ to read data back from the internal DACs.
35	31	$\overline{WR}$	Active Low Write Input. Used in conjunction with $\overline{CS}$ to write data to the parallel interface.
36	32	GAIN	Gain Control Pin. Controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}.
37	33	$\overline{CLR}$	Asynchronous Active Low Control Input. Clears all input registers and DAC registers to zeros.
38	34	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
Not applicable	41	EPAD	Exposed Pad. The exposed pad must be tied to GND.

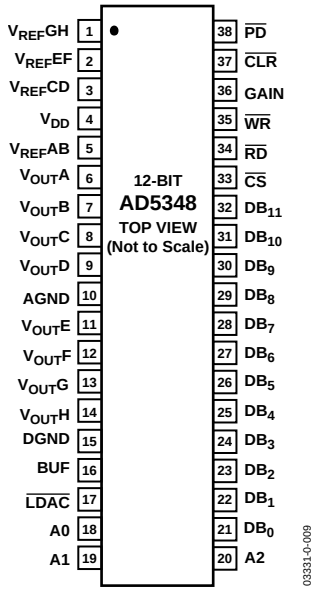


Figure 9. AD5348 Pin Configuration—TSSOP

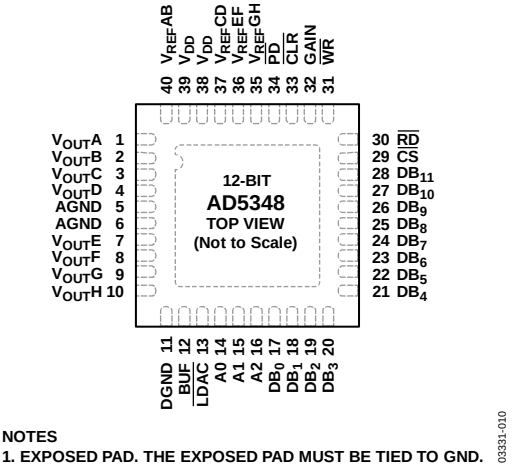


Figure 10. AD5348 Pin Configuration—LFCSP

Table 7. AD5348 Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	35	$V_{REF}GH$	Reference Input for DACs G and H.
2	36	$V_{REF}EF$	Reference Input for DACs E and F.
3	37	$V_{REF}CD$	Reference Input for DACs C and D.
4	38, 39	V_{DD}	Power Supply Pin(s). This part can operate from 2.5 V to 5.5 V, and the supply should be decoupled with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND. Both V_{DD} pins on the LFCSP package must be at the same potential.
5	40	$V_{REF}AB$	Reference Input for DACs A and B.
6 to 9, 11 to 14	1 to 4, 7 to 10	$V_{OUT}X$	Output of DAC X. Buffered output with rail-to-rail operation.
10	5, 6	AGND	Analog Ground. Ground reference for analog circuitry.
15	11	DGND	Digital Ground. Ground reference for digital circuitry.
16	12	BUF	Buffer Control Pin. Controls whether the reference input to the DAC is buffered or unbuffered.
17	13	$\overline{LDAC}$	Active Low Control Input. Updates the DAC registers with the contents of the input registers, which allows all DAC outputs to be simultaneously updated.
18	14	A0	LSB Address Pin. Selects which DAC is to be written to.
19	15	A1	Address Pin. Selects which DAC is to be written to.
20	16	A2	MSB Address Pin. Selects which DAC is to be written to.
21 to 32	17 to 28	DB_0 to DB_{11}	Twelve Parallel Data Inputs. DB_{11} is the MSB of these 12 bits.
33	29	$\overline{CS}$	Active Low Chip Select Input. Used in conjunction with $\overline{WR}$ to write data to the parallel interface, or with $\overline{RD}$ to read back data from a DAC.
34	30	$\overline{RD}$	Active Low Read Input. Used in conjunction with $\overline{CS}$ to read data back from the internal DACs.
35	31	$\overline{WR}$	Active Low Write Input. Used in conjunction with $\overline{CS}$ to write data to the parallel interface.
36	32	GAIN	Gain Control Pin. Controls whether the output range from the DAC is 0 V to V_{REF} or 0 V to 2 × V_{REF}.
37	33	$\overline{CLR}$	Asynchronous Active Low Control Input. Clears all input registers and DAC registers to zeros.
38	34	$\overline{PD}$	Power-Down Pin. This active low control pin puts all DACs into power-down mode.
Not applicable	41	EPAD	Exposed Pad. The exposed pad must be tied to GND.

TERMINOLOGY

Relative Accuracy

For the DAC, relative accuracy or integral nonlinearity (INL) is a measure of the maximum deviation, in LSBs, from a straight line passing through the actual endpoints of the DAC transfer function. Typical INL versus code plots can be seen in Figure 14, Figure 15, and Figure 16.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ± 1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Typical DNL versus code plots can be seen in Figure 17, Figure 18, and Figure 19.

Gain Error

This is a measure of the span error of the DAC, including any error in the gain of the buffer amplifier. It is the deviation in slope of the actual DAC transfer characteristic from the ideal and is expressed as a percentage of the full-scale range. This is illustrated in Figure 11.

Offset Error

This is a measure of the offset error of the DAC and the output amplifier. It is expressed as a percentage of the full-scale range.

If the offset voltage is positive, the output voltage still positive at zero input code. This is shown in Figure 12. Because the DACs operate from a single supply, a negative offset cannot appear at the output of the buffer amplifier. Instead, there is a code close to zero at which the amplifier output saturates (amplifier footroom). Below this code there is a dead band over which the output voltage does not change. This is illustrated in Figure 13.

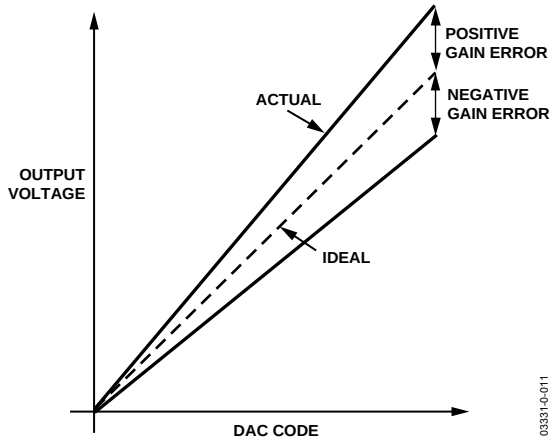


Figure 11. Gain Error

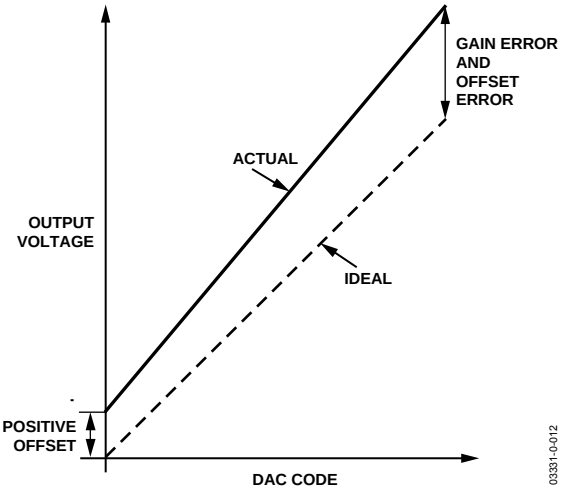


Figure 12. Positive Offset Error and Gain Error

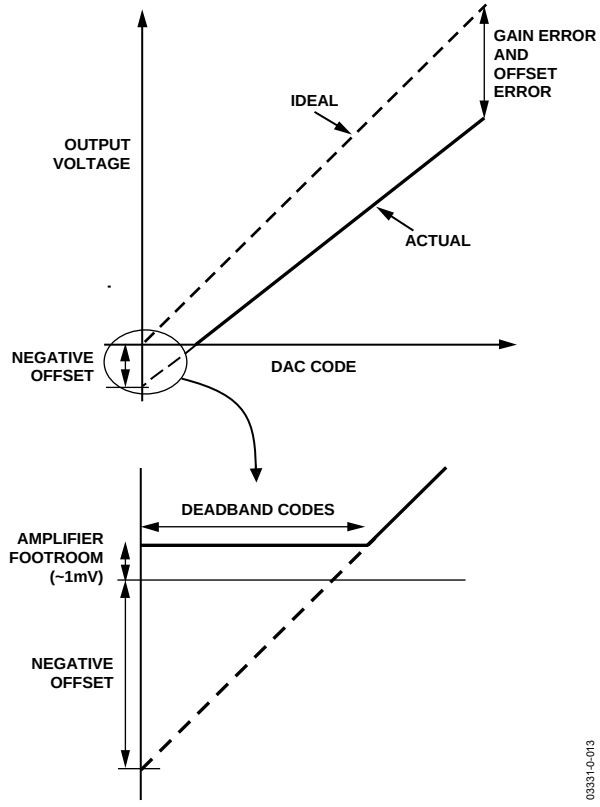


Figure 13. Negative Offset Error and Gain Error

Offset Error Drift
This is a measure of the change in offset error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Gain Error Drift
This is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

DC Power-Supply Rejection Ratio (PSRR)
This indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. It is measured in dB. V_{REF} is held at 2 V and V_{DD} is varied ±10%.

DC Crosstalk
This is the dc change in the output level of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) and output change of another DAC. It is expressed in μV.

Reference Feedthrough
This is the ratio of the amplitude of the signal at the DAC output to the reference input when the DAC output is not being updated, that is, $\overline{\text{LDAC}}$ is high. It is expressed in dB.

Channel-to-Channel Isolation
This is a ratio of the amplitude of the signal at the output of one DAC to a sine wave on the reference inputs of the other DACs. It is measured by grounding one V_{REF} pin and applying a 10 kHz, 4 V p-p sine wave to the other V_{REF} pins. It is expressed in dB.

Major-Code Transition Glitch Energy
This is the energy of the impulse injected into the analog output when the DAC changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital code is changed by 1 LSB at the major carry transition (011 . . . 11 to 100 . . . 00 or 100 . . . 00 to 011 . . . 11).

Digital Feedthrough
This is a measure of the impulse injected into the analog output of the DAC from the digital input pins of the device, but it is measured when the DAC is not being written to, $\overline{\text{CS}}$ held high. It is specified in nV-s and is measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s and vice versa.

Digital Crosstalk
This is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s and vice versa) in the input register of another DAC. It is expressed in nV-s.

Analog Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s and vice versa) while keeping $\overline{\text{LDAC}}$ high. Then pulse $\overline{\text{LDAC}}$ low and monitor the output of the DAC whose digital code was not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
This is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s and vice versa) with the $\overline{\text{LDAC}}$ pin set low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
This is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in dB.

TYPICAL PERFORMANCE CHARACTERISTICS

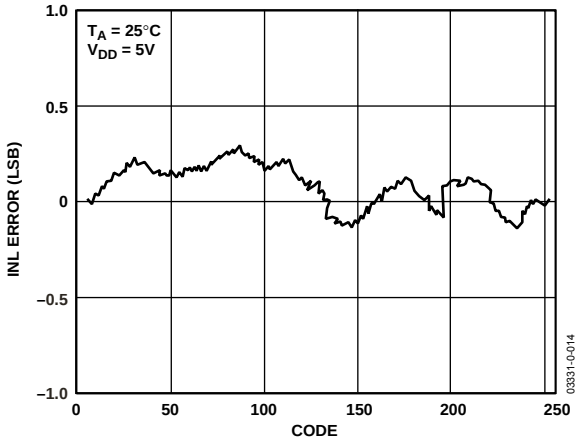


Figure 14. AD5346 Typical INL Plot

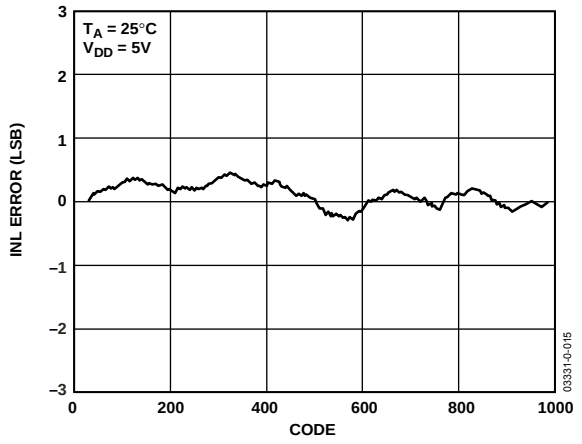


Figure 15. AD5347 Typical INL Plot

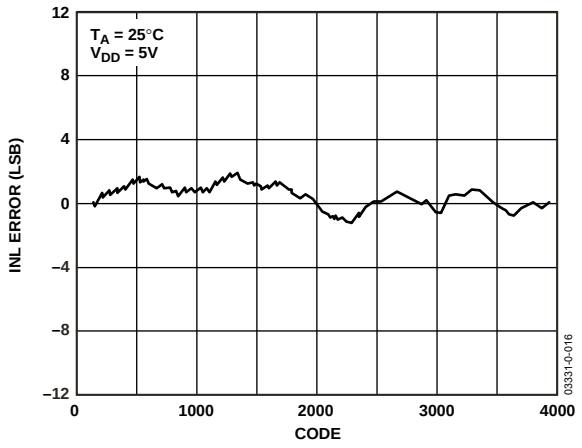


Figure 16. AD5348 Typical INL Plot

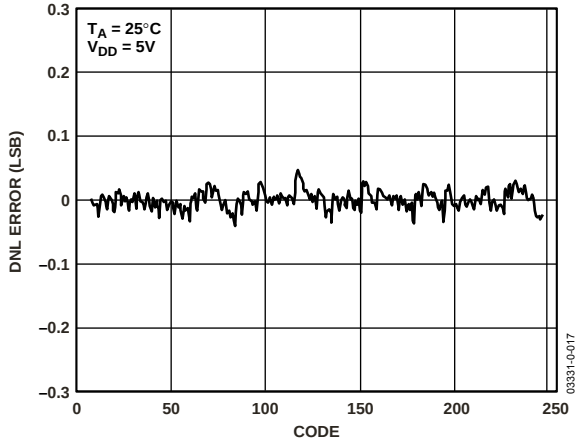


Figure 17. AD5346 Typical DNL Plot

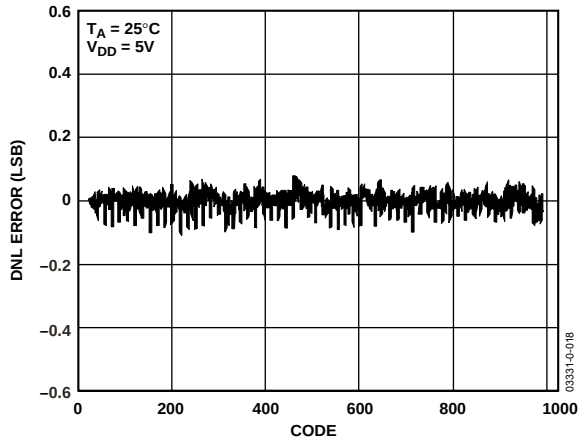


Figure 18. AD5347 Typical DNL Plot

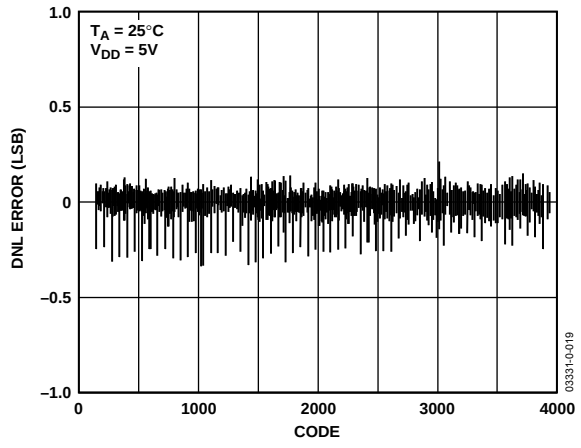


Figure 19. AD5348 Typical DNL Plot

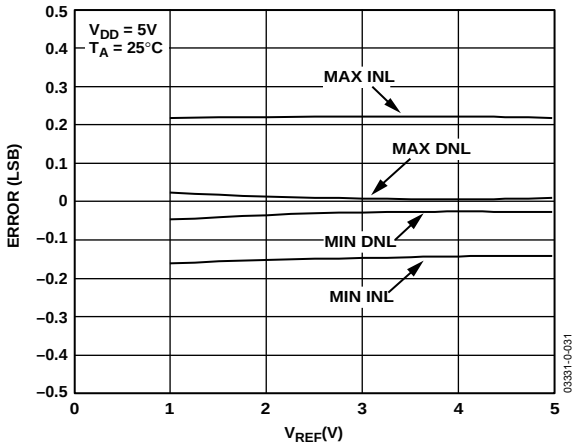


Figure 20. AD5346 INL and DNL Error vs. V_{REF}

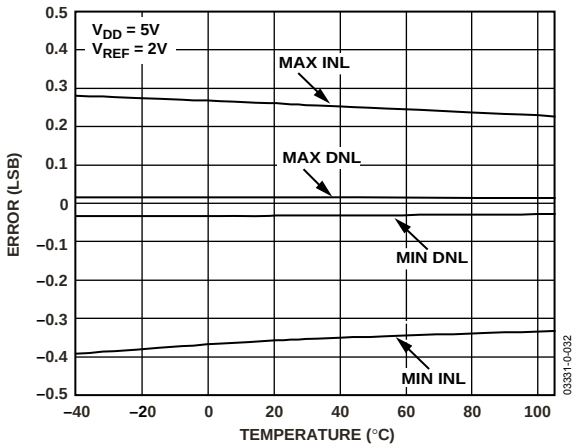


Figure 21. AD5346 INL and DNL Error vs. Temperature

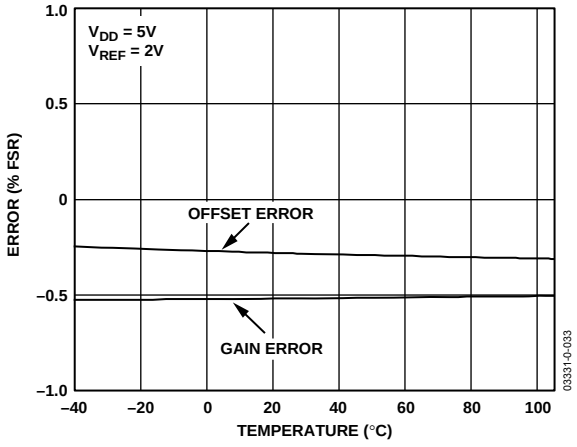


Figure 22. AD5346 Offset Error and Gain Error vs. Temperature

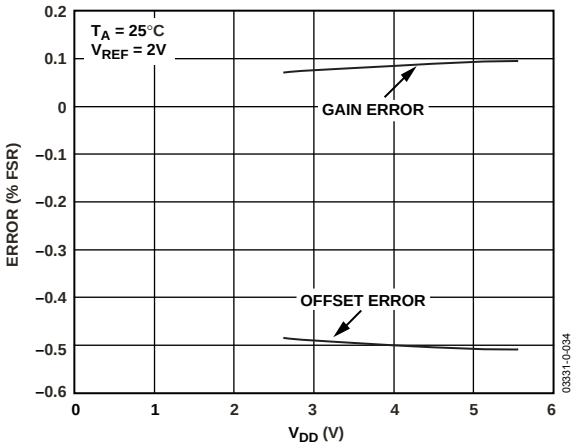


Figure 23. Offset Error and Gain Error vs. V_{DD}

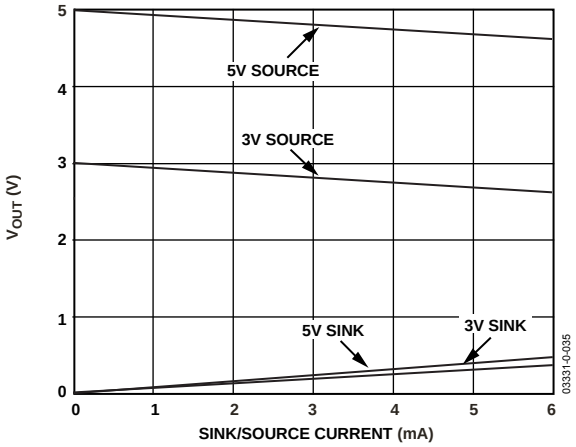


Figure 24. V_{OUT} Source and Sink Current Capability

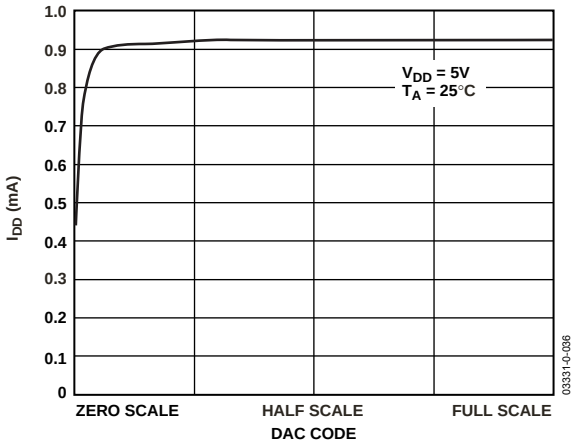


Figure 25. Supply Current vs. DAC Code

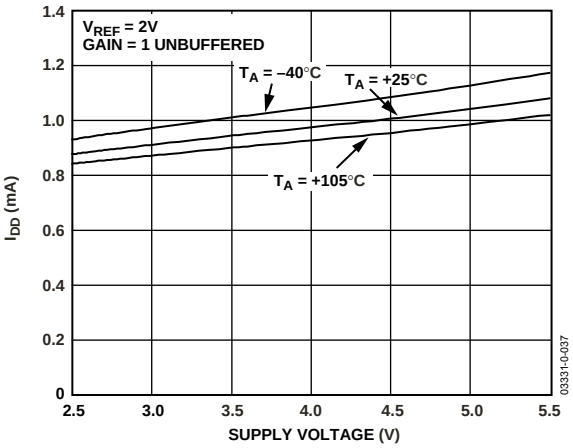


Figure 26. Supply Current vs. Supply Voltage

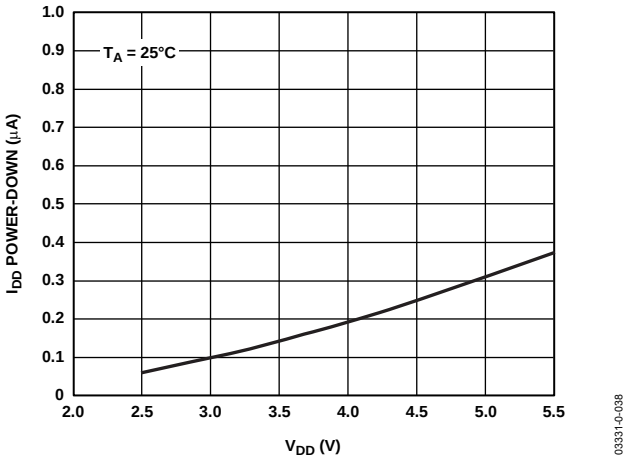


Figure 27. Power-Down Current vs. Supply Voltage

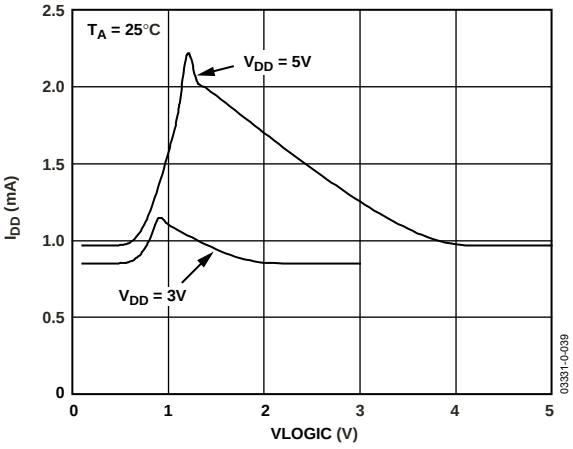


Figure 28. Supply Current vs. Logic Input Voltage

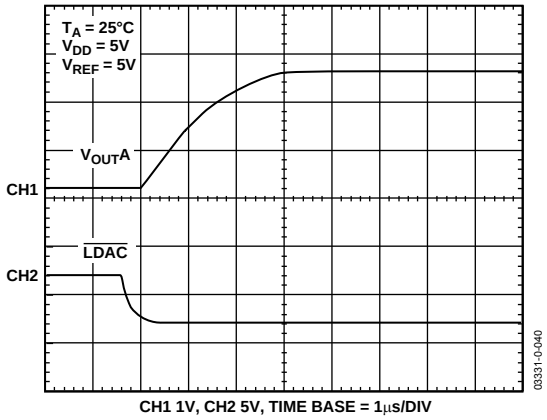


Figure 29. Half-Scale Settling (¼ to ¾ Scale Code)

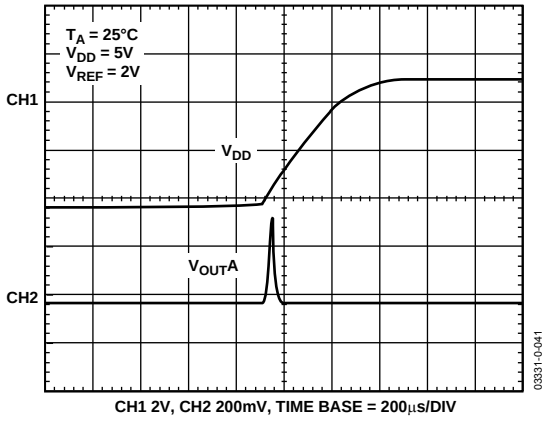


Figure 30. Power-On Reset to 0 V

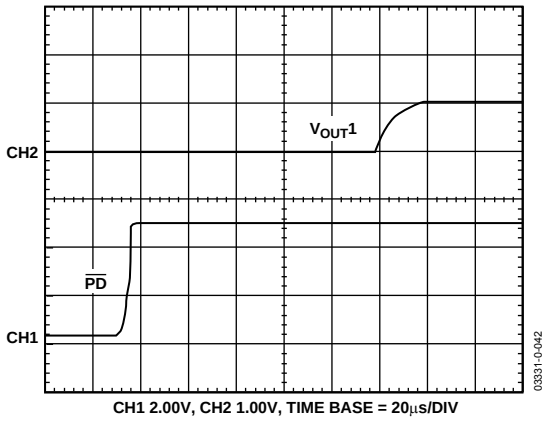


Figure 31. Exiting Power-Down to Midscale

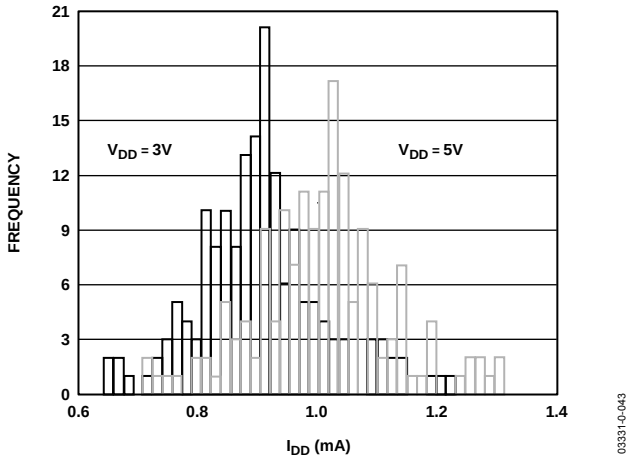


Figure 32. I_{DD} Histogram with V_{DD} = 3 V and V_{DD} = 5 V

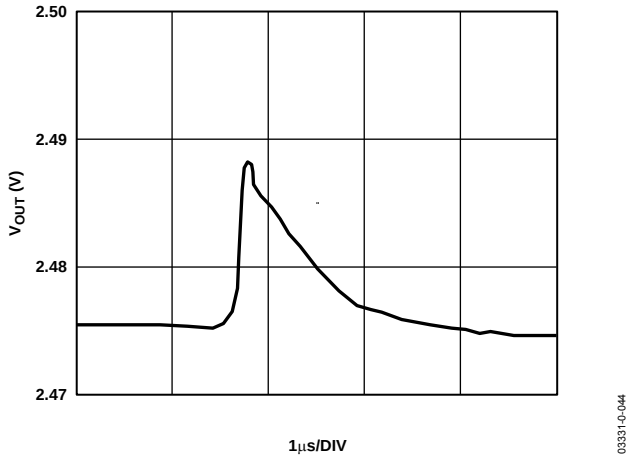


Figure 33. AD5348 Major Code Transition Glitch Energy

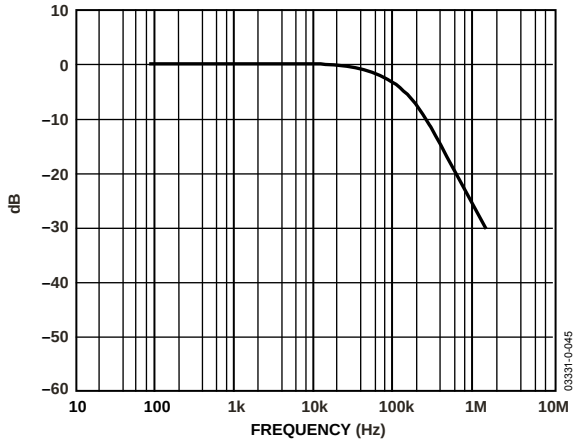


Figure 34. Multiplying Bandwidth (Small Signal Frequency Response)

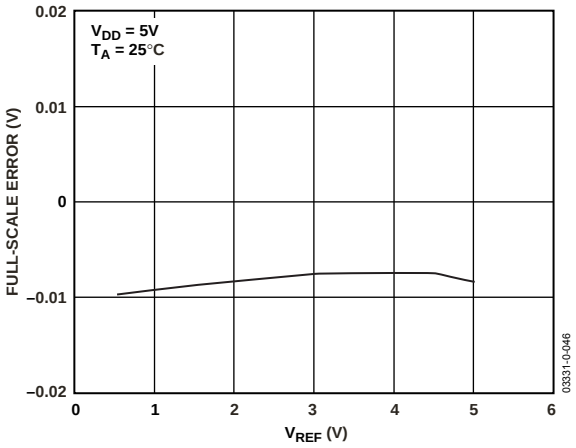


Figure 35. Full-Scale Error vs. V_{REF}

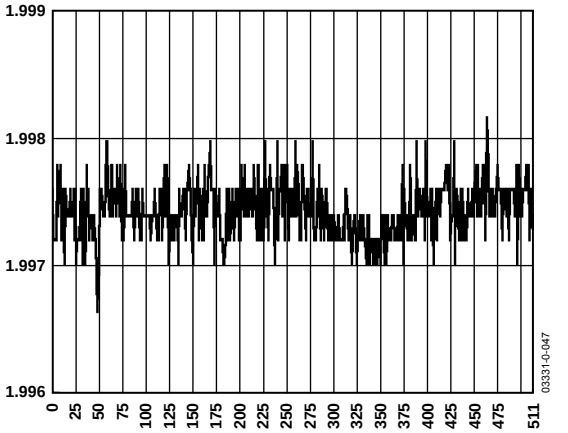


Figure 36. DAC-to-DAC Crosstalk

FUNCTIONAL DESCRIPTION

The AD5346/AD5347/AD5348 are octal resistor-string DACs fabricated by a CMOS process with resolutions of 8, 10, and 12 bits, respectively. They are written to using a parallel interface. They operate from single supplies of 2.5 V to 5.5 V, and the output buffer amplifiers offer rail-to-rail output swing. The gain of the buffer amplifiers can be set to 1 or 2 to give an output voltage range of 0 V to V_{REF} or 0 V to 2 × V_{REF}. The AD5346/AD5347/AD5348 have reference inputs that may be buffered to draw virtually no current from the reference source. The devices have a power-down feature that reduces current consumption to only 100 nA at 3 V.

DIGITAL-TO-ANALOG SECTION

The architecture of one DAC channel consists of a reference buffer and a resistor-string DAC followed by an output buffer amplifier. The voltage at the V_{REF} pin provides the reference voltage for the DAC. Figure 37 shows a block diagram of the DAC architecture. Because the input coding to the DAC is straight binary, the ideal output voltage is given by

$$V_{OUT} = V_{REF} \times \frac{D}{2^N} \times Gain$$

where:

D is the decimal equivalent of the binary code, which is loaded to the DAC register:

0 to 255 for AD5346 (8 bits)
0 to1023 for AD5347 (10 bits)
0 to 4095 for AD5348 (12 bits)

N is the DAC resolution.

Gain is the output amplifier gain (1 or 2).

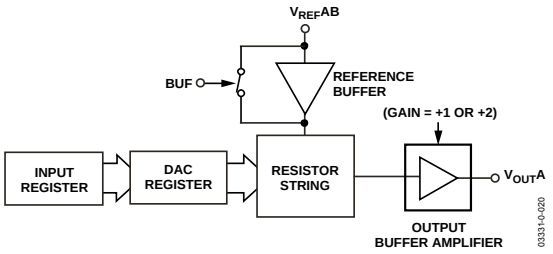


Figure 37. Single DAC Channel Architecture

RESISTOR STRING

The resistor string section is shown in Figure 38. It is simply a string of resistors, each of value R. The digital code loaded to the DAC register determines at what node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

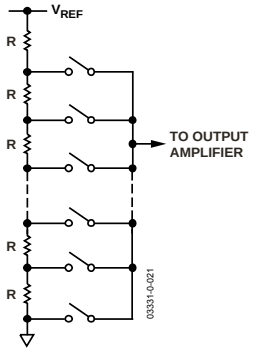


Figure 38. Resistor String

DAC REFERENCE INPUT

The DACs operate with an external reference. The AD5346/AD5347/AD5348 have a reference input for each pair of DACs. The reference inputs may be configured as buffered or unbuffered. This option is controlled by the BUF pin.

In buffered mode (BUF = 1), the current drawn from an external reference voltage is virtually zero because the impedance is at least 10 MΩ. The reference input range is 1 V to V_{DD}.

In unbuffered mode (BUF = 0), the user can have a reference voltage as low as 0.25 V and as high as V_{DD} because there is no restriction due to headroom and footroom of the reference amplifier. The impedance is still large at typically 90 kΩ for 0 V to V_{REF} mode and 45 kΩ for 0 V to 2 × V_{REF} mode.

If using an external buffered reference (such as REF192), there is no need to use the on-chip buffer.

OUTPUT AMPLIFIER

The output buffer amplifier is capable of generating output voltages to within 1 mV of either rail. Its actual range depends on V_{REF}, GAIN, the load on V_{OUT}, and offset error.

If a gain of +1 is selected (GAIN = 0), the output range is 0.001 V to V_{REF}.

If a gain of +2 is selected (GAIN = +1), the output range is 0.001 V to 2 × V_{REF}. However, because of clamping, the maximum output is limited to V_{DD} − 0.001 V.

The output amplifier is capable of driving a load of 2 kΩ to GND or V_{DD}, in parallel with 500 pF to GND or V_{DD}. The source and sink capabilities of the output amplifier can be seen in Figure 24.

The slew rate is 0.7 V/μs with a half-scale settling time to ±0.5 LSB (at 8 bits) of 6 s with the output unloaded. See Figure 29.

PARALLEL INTERFACE

The AD5346/AD5347/AD5348 load their data as a single 8-, 10-, or 12-bit word.

Double-Buffered Interface

The AD5346/AD5347/AD5348 DACs all have double-buffered interfaces consisting of an input register and a DAC register. DAC data, BUF, and GAIN inputs are written to the input register under control of the Chip Select ($\overline{CS}$) and Write ($\overline{WR}$) pins.

Access to the DAC register is controlled by the $\overline{LDAC}$ function. When $\overline{LDAC}$ is high, the DAC register is latched and the input register may change state without affecting the contents of the DAC register. However, when $\overline{LDAC}$ is brought low, the DAC register becomes transparent and the contents of the input register are transferred to it. The gain and buffer control signals are also double-buffered and are updated only when $\overline{LDAC}$ is taken low.

This is useful if the user requires simultaneous updating of all DACs and peripherals. The user can write to all input registers individually and then, by pulsing the $\overline{LDAC}$ input low, all outputs update simultaneously.

These parts contain an extra feature whereby the DAC register is not updated unless its input register has been updated since the last time that $\overline{LDAC}$ was brought low. Normally, when $\overline{LDAC}$ is brought low, the DAC registers are filled with the contents of the input registers. In the case of the AD5346/AD5347/AD5348, the part updates the DAC register only if the input register has been changed since the last time the DAC register was updated. This removes unnecessary crosstalk.

Clear Input ($\overline{CLR}$)

$\overline{CLR}$ is an active low, asynchronous clear that resets the input and DAC registers.

Chip Select Input ($\overline{CS}$)

$\overline{CS}$ is an active low input that selects the device.

Write Input ($\overline{WR}$)

$\overline{WR}$ is an active low input that controls writing of data to the device. Data is latched into the input register on the rising edge of $\overline{WR}$.

Read Input ($\overline{RD}$)

$\overline{RD}$ is an active low input that controls when data is read back from the internal DAC registers. On the falling edge of $\overline{RD}$, data is shifted onto the data bus. Under the conditions of a high capacitive load and high supplies, the user must ensure that the dynamic current remains at an acceptable level, therefore ensuring that the die temperature is within specification. The die temperature can be calculated as

$$T_{DIE} = T_{AMBIENT} + V_{DD}(I_{DD} + I_{DYNAMIC})\theta_{JA}$$

where:

$I_{DYNAMIC}$ = cvf (c = capacitance or the data bus, v = V_{DD}, and f = readback frequency)

Load DAC Input ($\overline{LDAC}$)

$\overline{LDAC}$ transfers data from the input register to the DAC register, and therefore updates the outputs. The $\overline{LDAC}$ function enables double-buffering of the DAC data, GAIN data, and BUF. There are two $\overline{LDAC}$ modes:

- In synchronous mode, the DAC register is updated after new data is read in on the rising edge of the $\overline{WR}$ input. $\overline{LDAC}$ can be tied permanently low or pulsed as shown in Figure 3.
- In asynchronous mode, the outputs are not updated at the same time that the input register is written to. When $\overline{LDAC}$ goes low, the DAC register is updated with the contents of the input register.

POWER-ON RESET

The AD5346/AD5347/AD5348 have a power-on reset function, so that they power up in a defined state. The power-on state is

- Normal operation
- Reference input buffered
- 0 V to V_{REF} output range
- Output voltage set to 0 V

Both input and DAC registers are filled with zeros and remain so until a valid write sequence is made to the device. This is particularly useful in applications where it is important to know the state of the DAC outputs while the device is powering up.

POWER-DOWN MODE

The AD5346/AD5347/AD5348 have low power consumption, dissipating typically 2.4 mW with a 3 V supply and 5 mW with a 5 V supply. Power consumption can be further reduced when the DACs are not in use by putting them into power-down mode, which is selected by taking the $\overline{PD}$ pin low.

When the $\overline{PD}$ pin is high, the DACs work normally with a typical power consumption of 1 mA at 5 V (0.8 mA at 3 V). In power-down mode, however, the supply current falls to 400 nA at 5 V (120 nA at 3 V) when the DACs are powered down. Not only does the supply current drop, but the output stage is also internally switched from the output of the amplifier, making it open-circuit. This has the advantage that the outputs are three-state while the part is in power-down mode, and provides a defined input condition for whatever is connected to the outputs of the DAC amplifiers. The output stage is illustrated in Figure 39.

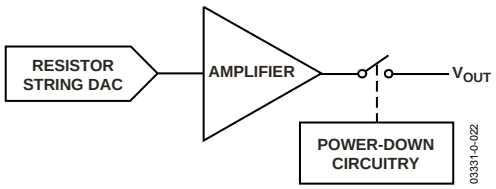


Figure 39. Output Stage During Power-Down

The bias generator, the output amplifier, the resistor string, and all other associated linear circuitry are all shut down when the power-down mode is activated. However, the contents of the registers are unaffected when in power-down. The time to exit power-down is typically 2.5 s for V_{DD} = 5 V and 5 µs when V_{DD} = 3 V. This is the time from a rising edge on the $\overline{PD}$ pin to when the output voltage deviates from its power-down voltage. See Figure 31.

SUGGESTED DATA BUS FORMATS

In many applications, the GAIN and BUF pins are hardwired. However, if more flexibility is required, they can be included in a data bus. This enables the user to software program GAIN, giving the option of doubling the resolution in the lower half of the DAC range. In a bused system, GAIN and BUF may be treated as data inputs because they are written to the device during a write operation and take effect when $\overline{LDAC}$ is taken low. This means that the reference buffers and the output amplifier gain of multiple DAC devices can be controlled using common GAIN and BUF lines. Note that GAIN and BUF are not read back during an $\overline{RD}$ operation.

The AD5347 and AD5348 data bus must be at least 10 and 12 bits wide, respectively, and are best suited to a 16-bit data bus system.

Examples of data formats for putting GAIN and BUF on a 16-bit data bus are shown in Figure 40. Note that any unused bits above the actual DAC data may be used for GAIN and BUF.

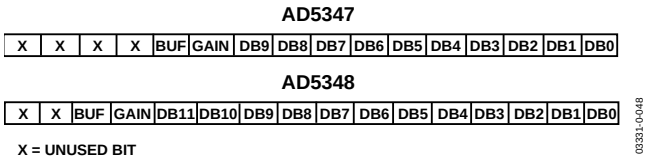


Figure 40. AD5347/AD5348 Data Format for Word Load with GAIN and BUF Data on 16-Bit Bus

Table 8. AD5346/AD5347/AD5348 Truth Table

$\overline{CLR}$	$\overline{LDAC}$	$\overline{CS}$	$\overline{WR}$	$\overline{RD}$	A2	A1	A0	Function
1	1	1	X	X	X	X	X	No data transfer
1	1	X	1	1	X	X	X	No data transfer
0	X	X	X	X	X	X	X	Clear all registers
1	1	0	0→1	1	0	0	0	Load DAC A input register
1	1	0	0→1	1	0	0	1	Load DAC B input register
1	1	0	0→1	1	0	1	0	Load DAC C input register
1	1	0	0→1	1	0	1	1	Load DAC D input register
1	1	0	0→1	1	1	0	0	Load DAC E input register
1	1	0	0→1	1	1	0	1	Load DAC F input register
1	1	0	0→1	1	1	1	0	Load DAC G input register
1	1	0	0→1	1	1	1	1	Load DAC H input register
1	X	0	1	1→0	0	0	0	Read Back DAC Register A
1	X	0	1	1→0	0	0	1	Read Back DAC Register B
1	X	0	1	1→0	0	1	0	Read Back DAC Register C
1	X	0	1	1→0	0	1	1	Read Back DAC Register D
1	X	0	1	1→0	1	0	0	Read Back DAC Register E
1	X	0	1	1→0	1	0	1	Read Back DAC Register F
1	X	0	1	1→0	1	1	0	Read Back DAC Register G
1	X	0	1	1→0	1	1	1	Read Back DAC Register H
1	0	X	X	1	X	X	X	Update DAC registers
X	X	0	0	0	X	X	X	Invalid operation

X = Don't Care

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUITS

The AD5346/AD5347/AD5348 can be used with a wide range of reference voltages, especially if the reference inputs are configured as unbuffered, in which case the devices offer full, one-quadrant multiplying capability over a reference range of 0.25 V to V_{DD}. More typically, these devices may be used with a fixed, precision reference voltage. Figure 41 shows a typical setup for the devices when using an external reference connected to the reference inputs. Suitable references for 5 V operation are the AD780, ADR381, and REF192 (2.5 V references). For 2.5 V operation, suitable external references are the AD589 and the AD1580 (1.2 V band gap references).

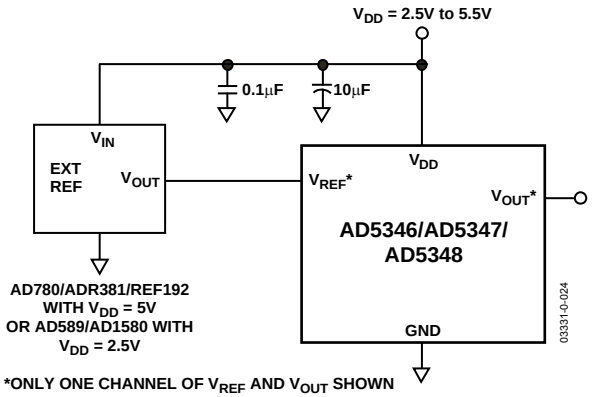


Figure 41. AD5346/AD5347/AD5348 Using an External Reference

BIPOLAR OPERATION USING THE AD5346/AD5347/AD5348

The AD5346/AD5347/AD5348 have been designed for single-supply operation, but a bipolar output range is also possible by using the circuit shown in Figure 42. This circuit has an output voltage range of ±5 V. Rail-to-rail operation at the amplifier output is achievable using an AD820, an AD8519, or an OP196 as the output amplifier.

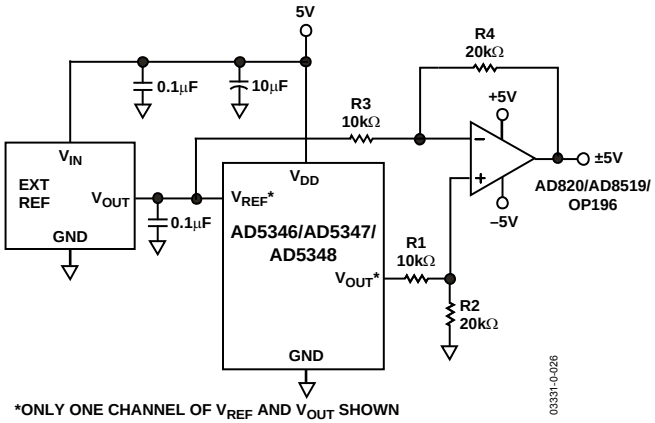


Figure 42. Bipolar Operation with the AD5346/AD5347/AD5348

The output voltage for any input code can be calculated as follows:

$$V_{OUT} = [(1 + R4/R3) \times (R2/(R1 + R2) \times (2 \times V_{REF} \times D/2^N)] - R4 \times V_{REF}/R3$$

where:
D is the decimal equivalent of the code loaded to the DAC.
N is the DAC resolution.
V_{REF} is the reference voltage input.

with:
$V_{REF} = 5$ V
$R1 = R3 = 10$ kΩ
$R2 = R4 = 20$ kΩ
$V_{DD} = 5$ V
GAIN = 2

$$V_{OUT} = (10 \times D/2^N) - 5$$

DECODING MULTIPLE AD5346/AD5347/AD5348s

The $\overline{CS}$ pin on these devices can be used in applications to decode a number of DACs. In this application, all DACs in the system receive the same data and $\overline{WR}$ pulses, but only the $\overline{CS}$ to one of the DACs will be active at any one time, so data will only be written to the DAC whose $\overline{CS}$ is low.

The 74HC139 is used as a 2-line to 4-line decoder to address any of the DACs in the system. To prevent timing errors from occurring, the enable input should be brought to its inactive state while the coded address inputs are changing state. Figure 43 shows a diagram of a typical setup for decoding multiple devices in a system. Once data has been written sequentially to all DACs in a system, all the DACs can be updated simultaneously using a common $\overline{LDAC}$ line. A common $\overline{CLR}$ line can also be used to reset all DAC outputs to 0 V.

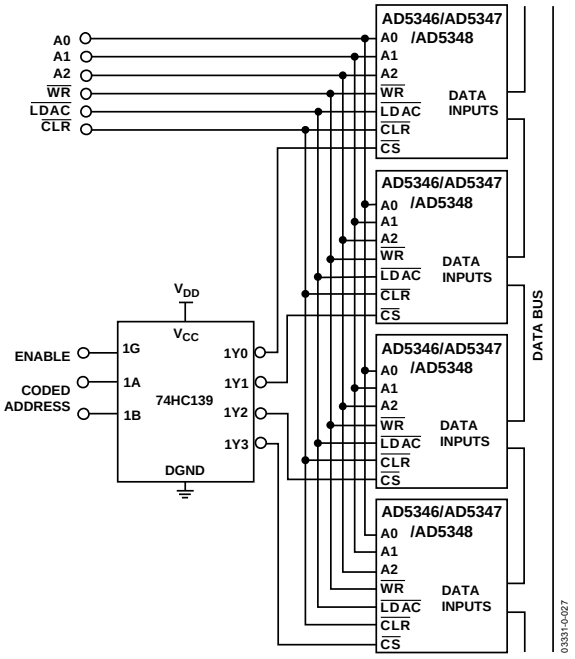


Figure 43. Decoding Multiple DAC Devices

AD5346/AD5347/AD5348 AS DIGITALLY PROGRAMMABLE WINDOW DETECTORS

A digitally programmable upper/lower limit detector using two of the DACs in the AD5346/AD5347/AD5348 is shown in Figure 44. Any pair of DACs in the device may be used, but for simplicity the description refers to DACs A and B.

The upper and lower limits for the test are loaded to DACs A and B which, in turn, set the limits on the CMP04. If a signal at the V_{IN} input is not within the programmed window, an LED indicates the fail condition.

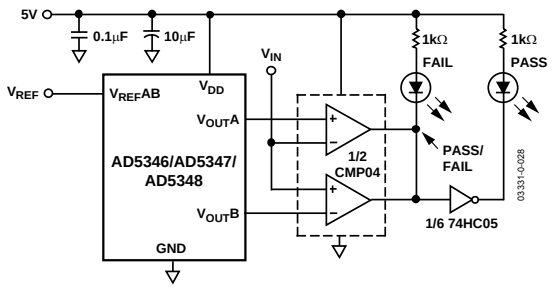


Figure 44. Programmable Window Detector

PROGRAMMABLE CURRENT SOURCE

Figure 45 shows the AD5346/AD5347/AD5348 used as the control element of a programmable current source. In this example, the full-scale current is set to 1 mA. The output voltage from the DAC is applied across the current setting resistor of 4.7 kΩ in series with the 470 Ω adjustment potentiometer, which gives an adjustment of about ±5%. Suitable transistors to place in the feedback loop of the amplifier include the BC107 and the 2N3904, which enable the current source to operate from a minimum V_{SOURCE} of 6 V. The operating range is determined by the operating characteristics of the transistor. Suitable amplifiers include the AD820 and the OP295, both having rail-to-rail operation on their outputs. The current for any digital input code and resistor value can be calculated as follows:

$$I = G \times V_{REF} \frac{D}{(2^N \times R)} mA$$

where:
G is the gain of the buffer amplifier (1 or 2).
D is the digital input code.
N is the DAC resolution (8, 10, or 12 bits).
R is the sum of the resistor plus adjustment potentiometer in kΩ.

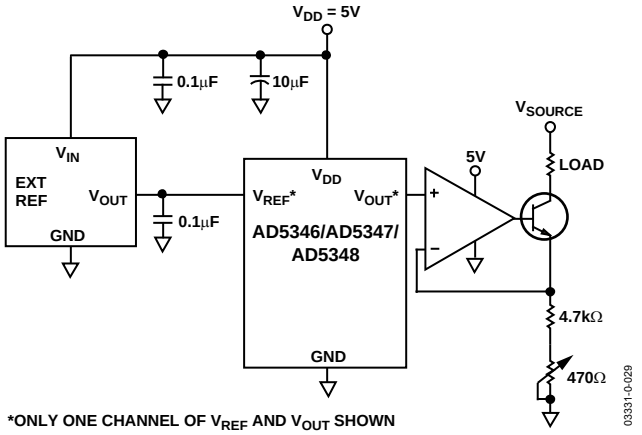


Figure 45. Programmable Current Source

COARSE AND FINE ADJUSTMENT USING THE AD5346/AD5347/AD5348

Two of the DACs in the AD5346/AD5347/AD5348 can be paired together to form a coarse and fine adjustment function, as shown in Figure 46. As with the window comparator previously described, the description refers to DACs A and B.

DAC A provides the coarse adjustment, while DAC B provides the fine adjustment. Varying the ratio of R1 and R2 changes the relative effect of the coarse and fine adjustments. With the resistor values shown, the output amplifier has unity gain for the DAC A output, so the output range is 0 V to (V_{REF} − 1 LSB). For DAC B, the amplifier has a gain of 7.6×10^{-3}, giving DAC B a range equal to 2 LSBs of DAC A.

The circuit is shown with a 2.5 V reference, but reference voltages up to V_{DD} may be used. The op amps indicated allow a rail-to-rail output swing.

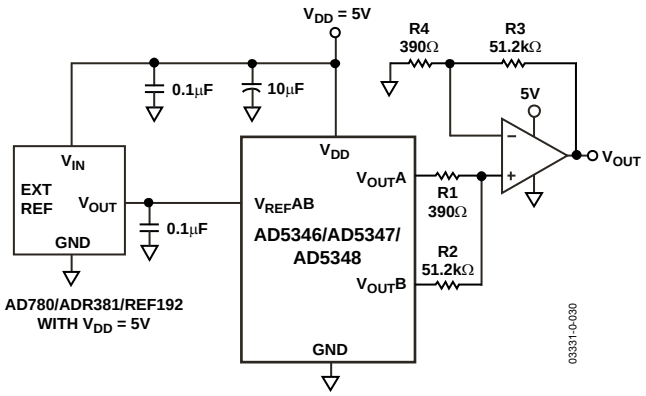


Figure 46. Coarse and Fine Adjustment

POWER SUPPLY BYPASSING AND GROUNDING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance.

The printed circuit board on which the AD5346/AD5347/AD5348 is mounted should be designed so that the analog and digital sections are separated and are confined to certain areas of the board. This facilitates the use of ground planes that can be separated easily. A minimum etch technique is generally best for ground planes because it gives the best shielding. Digital and analog ground planes should be joined in one place only. If the AD5346/AD5347/AD5348 is the only device requiring an AGND-to-DGND connection, then the ground planes should be connected at the AGND and DGND pins of the AD5346/AD5347/AD5348. If the AD5346/AD5347/AD5348 is in a system where multiple devices require AGND-to-DGND connections, the connection should be made at one point only, a star ground point that should be established as close as possible to the AD5346/AD5347/AD5348.

The AD5346/AD5347/AD5348 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on the supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the device should use the largest trace possible to provide low impedance paths and to reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board, and should never be run near the reference inputs. Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other to reduce the effects of feedthrough through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

OUTLINE DIMENSIONS

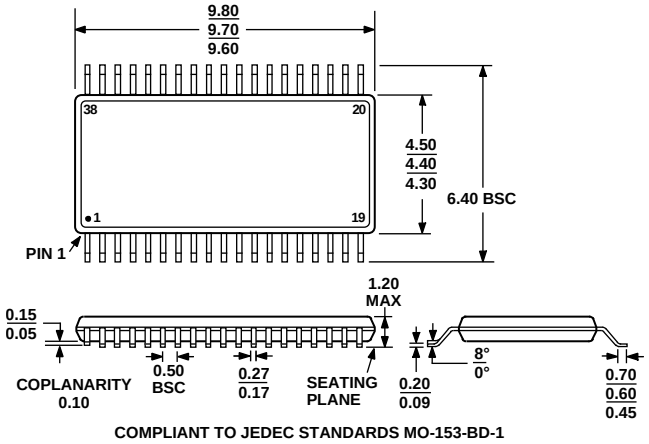


Figure 47. 38-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-38)
Dimensions shown in millimeters

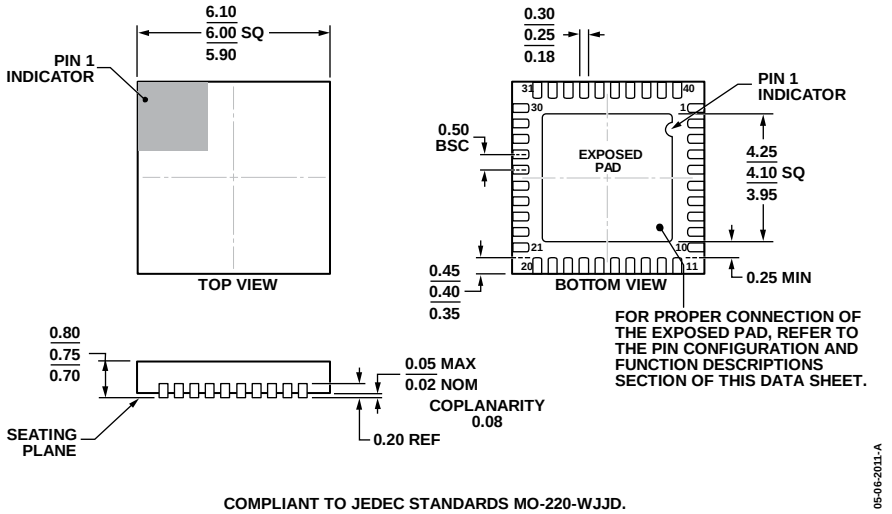


Figure 48. 40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]
6 mm × 6 mm, Very Very Thin Quad
(CP-40-9)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
AD5346BRU	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5346BRU-REEL7	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5346BRUZ	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5346BRUZ-REEL	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5346BRUZ-REEL7	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5346BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
AD5347BRU	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5347BRU-REEL7	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5347BRUZ	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5347BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9
AD5348BRU	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5348BRUZ	−40°C to +105°C	38-Lead Thin Shrink Small Outline Package [TSSOP]	RU-38
AD5348BCPZ	−40°C to +105°C	40-Lead Lead Frame Chip Scale Package [LFCSP_WQ]	CP-40-9

[1] Z = RoHS Compliant Part.

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