THE DATASHEET OF

AD5384BBCZ-5

40-Channel, 3 V/5 V, Single-Supply, Serial, 14-Bit *dense*DAC®

Data Sheet **AD5384**

FEATURES

- Guaranteed monotonic
- Relative accuracy (INL): ±4 LSB maximum
- On-chip 1.25 V/2.5 V, 10 ppm/°C reference
- Temperature range: −40°C to +85°C
- Rail-to-rail output amplifier
- Power-down
- Package type: 100-ball CSP_BGA
- User interfaces
  - Serial (SPI-/QSPI™-/MICROWIRE®-/DSP-compatible, featuring data readback)
  - I²C-compatible

INTEGRATED FUNCTIONS

- Channel monitor
- Simultaneous output update via $\overline{\text{LDAC}}$
- Clear function to user programmable code
- Amplifier boost mode to optimize slew rate
- User programmable offset and gain adjust
- Toggle mode enables square wave generation
- Thermal monitor

APPLICATIONS

- Variable optical attenuators (VOAs)
- Level settings (automatic test equipment [ATE])
- Optical micro-electromechanical systems (MEMS) control systems
- Instrumentation

FUNCTIONAL BLOCK DIAGRAM

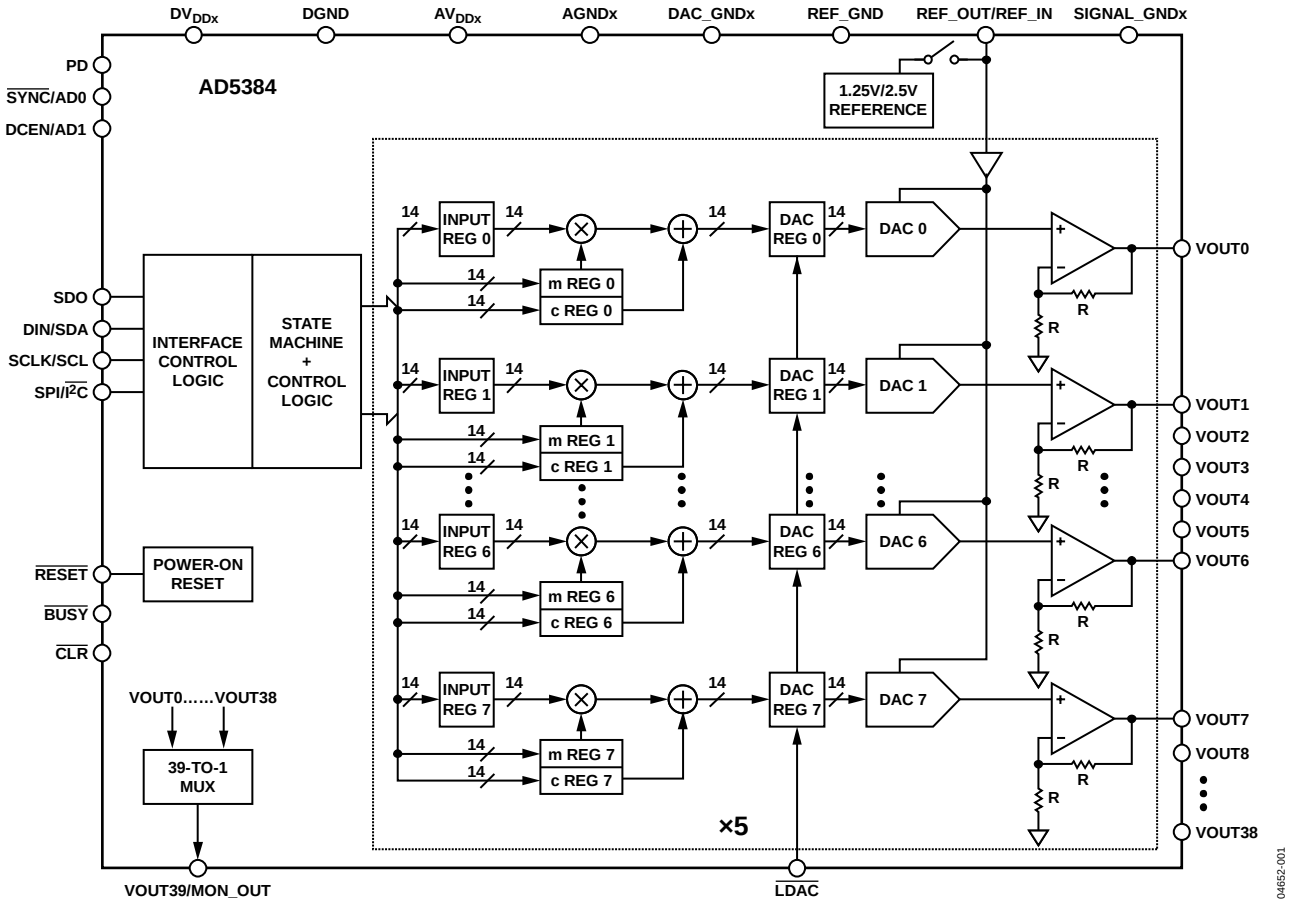

Figure 1.

Rev. C
Document Feedback

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1/14—Rev. A to Rev. B

Updated Format ... Universal
Changed DVDD to DV_{DDX}, AVDD to AV_{DDx}, AGND to $AGND_X$, VOUT to $VOUT_X$, REFIN TO REF_IN, REFOUT to REF_OUT, SCLK to SCLK/SCL, DAC GND to DAC_GND, SIGNAL GND to SIGNAL_GND, REFGND to REF_GND, $\overline{\text{SYNC}}$/AD 0 to $\overline{\text{SYNC}}$/AD0, DCEN/AD 1 to DCEN/AD1, DIN to DIN/SDA ... Throughout
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7/04—Revision 0: Initial Version

GENERAL DESCRIPTION

The AD5384 is a complete single-supply, 40-channel, 14-bit digital-to-analog converter (DAC) available in a 100-ball CSP_BGA package. All 40 channels have an on-chip output amplifier with rail-to-rail operation. The AD5384 includes an internal 1.25 V/2.5 V, 10 ppm/°C reference, an on-chip channel monitor function that multiplexes the analog outputs to a common MON_OUT pin for external monitoring, and an output amplifier boost mode that allows the amplifier slew rate to be optimized. The AD5384 contains a serial interface compatible with SPI, QSPI, MICROWIRE, and DSP interface standards with interface speeds in excess of 30 MHz and an I^2C-compatible interface supporting 400 kHz data transfer rate. An input register followed by a DAC register provides double buffering, allowing the DAC outputs to be updated independently or simultaneously, using the $\overline{\text{LDAC}}$ input. Each channel has a programmable gain and offset adjust register letting the user fully calibrate any DAC channel. Power consumption is typically 0.25 mA per channel with boost mode off.

SPECIFICATIONS

AV_{DDx} = 4.5 V to 5.5 V; DV_{DDx} = 2.7 V to 5.5 V, AGNDx = DGND = 0 V; external REF_IN = 2.5 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. The AD5384 is calibrated using an external 2.5 V reference. Temperature range −40°C to +85°C.

Table 1.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
ACCURACY					
Resolution		14		Bits	
Relative Accuracy[1] (INL)			±4	LSB	±1 LSB typical
Differential Nonlinearity (DNL)	−1		+2	LSB	Guaranteed monotonic by design over temperature
Zero-Scale Error			4	mV	
Offset Error			±4	mV	Measured at Code 32 in the linear region
Offset Error Temperature Coefficient		±5		µV/°C	
Gain Error			±0.05	% FSR	At 25°C
			±0.06	% FSR	T_{MIN} to T_{MAX}
Gain Temperature Coefficient[2]		2		ppm FSR/°C	
DC Crosstalk[2]			1	LSB	
REFERENCE INPUT/OUTPUT					
Reference Input[2]					
Reference Input Voltage		2.5		V	±1% for specified performance, AV_{DDx} = 2 × REF_IN + 50 mV
DC Input Impedance	1			MΩ	Typically 100 MΩ
Input Current			±1	µA	Typically ±30 nA
Reference Range	1		$V_{DD}/2$	V	
Reference Output[3]					Enabled via CR10 in the AD5384 control register (CR12) and selects the output voltage
Output Voltage	2.495		2.505	V	At ambient, CR12 = 1, optimized for 2.5 V operation
	1.22		1.28	V	CR12 = 0
Reference Temperature Coefficient[2]			±10	ppm	Temperature range: 25°C to 85°C
			±15	ppm	Temperature range: −40°C to +85°C
Output Impedance		800		Ω	
OUTPUT CHARACTERISTICS[2]					
Output Voltage Range[1]	0		AV_{DD}	V	
Short-Circuit Current			40	mA	
Load Current			±1	mA	
Capacitive Load Stability					
R_L = ∞			200	pF	
R_L = 5 kΩ			1000	pF	
DC Output Impedance			0.6	Ω	
MONITOR PIN					
Output Impedance		1		kΩ	
Three-State Leakage Current		100		nA	
LOGIC INPUTS (EXCEPT SDA, SCL)[2]					DV_{DDx} = 2.7 V to 5.5 V
Input High Voltage, V_{IH}	2			V	
Input Low Voltage, V_{IL}					
DV_{DDx} > 3.6 V			0.8	V	
DV_{DDx} ≤ 3.6 V			0.6	V	
Input Current			±10	µA	Total for all pins; $T_A = T_{MIN}$ to T_{MAX}
Pin Capacitance			10	pF	

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
LOGIC INPUTS (SDA, SCL ONLY)					
Input High Voltage, V_{IH}	0.7 × DV_{DDx}			V	SMBus-compatible at DV_{DDx} < 3.6 V
Input Low Voltage, V_{IL}			0.3 × DV_{DDx}	V	SMBus-compatible at DV_{DDx} < 3.6 V
Input Leakage Current, I_{IN}			±1	µA	
Input Hysteresis, V_{HYST}	0.05 × DV_{DDx}			V	
Input Capacitance, C_{IN}		8		pF	
Glitch Rejection			50	ns	Input filtering suppresses noise spikes of less than 50 ns
LOGIC OUTPUTS ($\overline{BUSY}$, SDO)[2]					
Output Low Voltage, V_{OL}			0.4	V max	DV_{DDx} = 5 V ± 10%, sinking 200 µA
			0.4	V max	DV_{DDx} = 2.7 V to 3.6 V, sinking 200 µA
Output High Voltage, V_{OH}	DV_{DDx} – 1			V min	DV_{DDx} = 5 V ± 10%, sourcing 200 µA
	DV_{DDx} – 0.5			V min	DV_{DDx} = 2.7 V to 3.6 V, sourcing 200 µA
High Impedance Leakage Current			±1	µA	SDO only
High Impedance Output Capacitance		5		pF	SDO only
LOGIC OUTPUT (SDA)[2]					
Output Low Voltage, V_{OL}			0.4	V	I_{SINK} = 3 mA
			0.6	V	I_{SINK} = 6 mA
Three-State Leakage Current			±1	µA	
Three-State Output Capacitance		8		pF	
POWER REQUIREMENTS					
AV_{DDx}	4.5		5.5	V	
DV_{DDx}	2.7		5.5	V	
Power Supply Sensitivity[2]					
ΔMidscale/ΔAV_{DDx}		−85		dB	
AI_{DD}			0.375	mA/channel	Outputs unloaded, boost off; 0.25 mA per channel typical
			0.475	mA/channel	Outputs unloaded, boost on; 0.325 mA per channel typical
DI_{DD}			1	mA	V_{IH} = DV_{DDx}, V_{IL} = DGND
AI_{DD} (Power-Down)			20	µA	Typically 100 nA
DI_{DD} (Power-Down)			20	µA	Typically 1 µA
Power Dissipation			80	mW	Outputs unloaded, boost off, AV_{DDx} = DV_{DDx} = 5 V

[1] Accuracy guaranteed from V_{OUT} = 10 mV to AV_{DD} – 50 mV.
[2] Guaranteed by characterization, not production tested.
[3] Default on the AD5384 is 2.5 V. Programmable to 1.25 V via CR12 in the AD5384 control register; operating the AD5384 with a 1.25 V reference leads to degraded accuracy specifications.

AC CHARACTERISTICS

AV_{DDx} = 4.5 V to 5.5 V; DV_{DDx} = 2.7 V to 5.5 V; $AGND_x$ = DGND = 0 V. Guaranteed by design and characterization, not production tested.

Table 2.

Parameter	Min	Typ	Max	Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE					
Output Voltage Settling Time					Boost mode off, CR11 = 0, 1/4 scale to 3/4 scale change settling to ±1 LSB
		3		µs	Boost mode off, CR11 = 0
			8	µs	Boost mode off, CR11 = 0
Slew Rate[1]		1.5		V/µs	Boost mode off, CR11 = 0
		2.5		V/µs	Boost mode on, CR11 = 1
Digital-to-Analog Glitch Energy		12		nV-sec	
Glitch Impulse Peak Amplitude		15		mV	
Channel-to-Channel Isolation		100		dB	See the Terminology section
DAC-to-DAC Crosstalk		1		nV-sec	See the Terminology section
Digital Crosstalk		0.8		nV-sec	
Digital Feedthrough		0.1		nV-sec	Effect of input bus activity on DAC output under test
Output Noise 0.1 Hz to 10 Hz		15		µV p-p	External reference, midscale loaded to DAC
		40		µV p-p	Internal reference, midscale loaded to DAC
Output Noise Spectral Density					
At 1 kHz		150		nV/√Hz	
At 10 kHz		100		nV/√Hz	

[1] Program the slew rate via the current boost control bit (CR11).

TIMING CHARACTERISTICS

Serial Interface

DV_{DDx} = 2.7 V to 5.5 V; AV_{DDx} = 4.5 V to 5.5 V; $AGND_x$ = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. The AD5384 must remain powered up when part of a multidevice system with a common I²C bus. Guaranteed by design and characterization, not production tested. All input signals are specified with $t_r = t_f$ = 5 ns (10% to 90% of DV_{DDx}) and are timed from a voltage level of 1.2 V. See Figure 2, Figure 3, Figure 4, and Figure 5.

Table 3.

Parameter	Min	Typ	Max	Unit	Description
t_1	33			ns	SCLK cycle time
t_2	13			ns	SCLK high time
t_3	13			ns	SCLK low time
t_4	13			ns	$\overline{SYNC}$ falling edge to SCLK falling edge setup time
t_5[1]	13			ns	24th SCLK falling edge to $\overline{SYNC}$ falling edge
t_6[1]	33			ns	Minimum $\overline{SYNC}$ low time
t_7	10			ns	Minimum $\overline{SYNC}$ high time
t_{7A}	140			ns	Minimum $\overline{SYNC}$ high time in readback mode
t_8	5			ns	Data setup time
t_9	4.5			ns	Data hold time
t_{10}[1]			36	ns	24th SCLK falling edge to $\overline{BUSY}$ falling edge
t_{11}			670	ns	$\overline{BUSY}$ pulse width low (single channel update)
t_{12}[1]	20			ns	24th SCLK falling edge to $\overline{LDAC}$ falling edge
t_{13}	20			ns	$\overline{LDAC}$ pulse width low
t_{14}	100		2000	ns	$\overline{BUSY}$ rising edge to DAC output response time
t_{15}	0			ns	$\overline{BUSY}$ rising edge to $\overline{LDAC}$ falling edge
t_{16}	100			ns	$\overline{LDAC}$ falling edge to DAC output response time
t_{17}		3		µs	DAC output settling time boost mode off
t_{18}	20			ns	$\overline{CLR}$ pulse width low
t_{19}			40	µs	$\overline{CLR}$ pulse activation time
t_{20}[2]			30	ns	SCLK rising edge to SDO valid
t_{21}[2]	5			ns	SCLK falling edge to $\overline{SYNC}$ rising edge
t_{22}[2]	8			ns	$\overline{SYNC}$ rising edge to SCLK rising edge
t_{23}	20			ns	$\overline{SYNC}$ rising edge to $\overline{LDAC}$ falling edge

[1] Standalone mode only.
[2] Daisy-chain mode only.

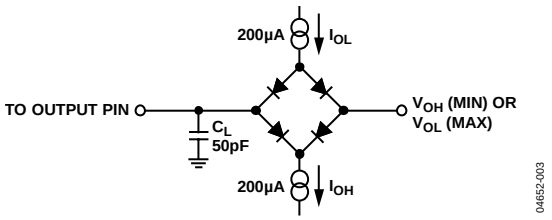

Figure 2. Load Circuit for Digital Output Timing

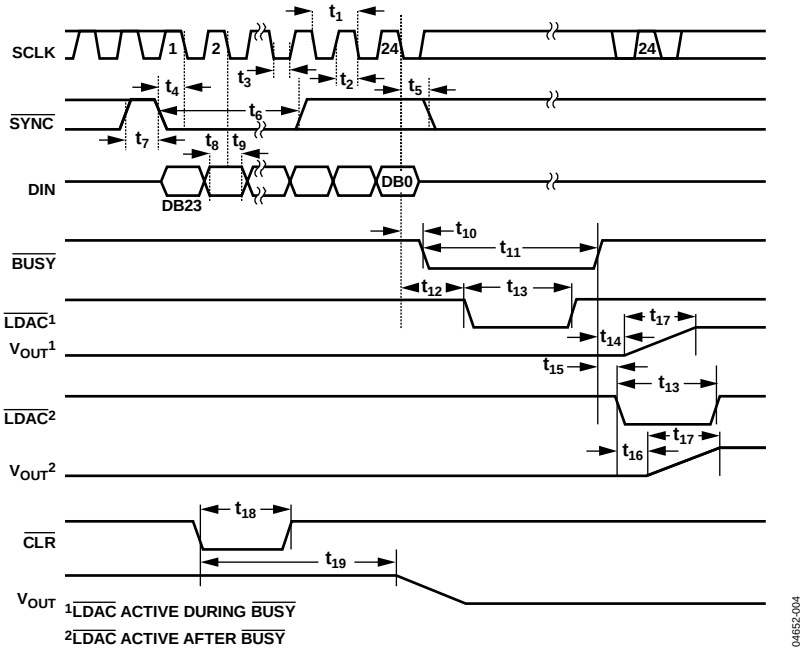

Figure 3. Serial Interface Timing Diagram (Standalone Mode)

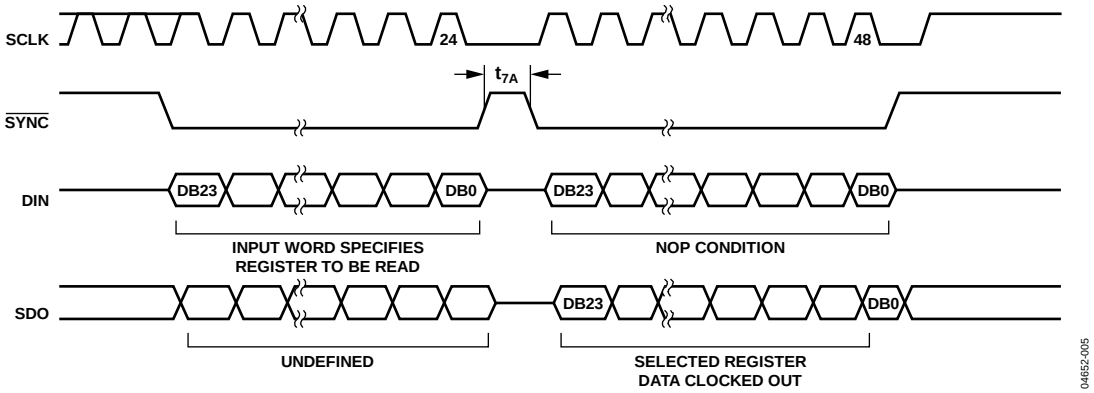

Figure 4. Serial Interface Timing Diagram (Data Readback Mode)

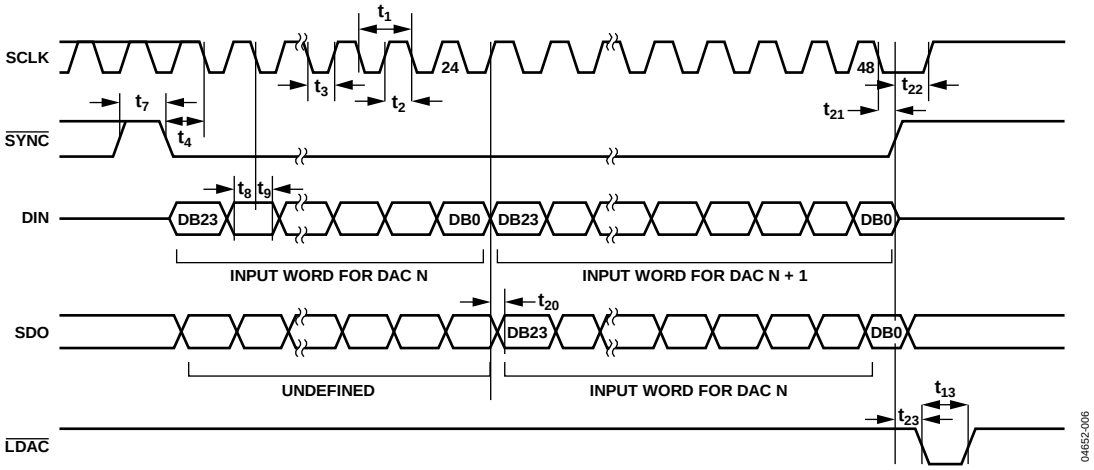

Figure 5. Serial Interface Timing Diagram (Daisy-Chain Mode)

I²C Serial Interface

DV_{DDx} = 2.7 V to 5.5 V; AV_{DDx} = 4.5 V to 5.5 V; $AGND_x$ = DGND = 0 V; all specifications T_{MIN} to T_{MAX}, unless otherwise noted. See Figure 6. Limit at T_{MIN}, T_{MAX}.

Table 4.

Parameter	Min	Typ	Max	Unit	Description
f_{SCL}			400	kHz	SCL clock frequency
t_1	2.5			µs	SCL cycle time
t_2	0.6			µs	SCL high time, t_{HIGH}
t_3	1.3			µs	SCL low time, t_{LOW}
t_4	0.6			µs	Start/repeated start condition hold time, $t_{HD, STA}$
t_5	100			ns	Data setup time, $t_{SU,DAT}$
t_6[1]			0.9	µs	Data hold time, $t_{HD,DAT}$
	0			µs	Data hold time, $t_{HD,DAT}$
t_7	0.6			µs	Setup time for repeated start, $t_{SU,STA}$
t_8	0.6			µs	Stop condition setup time, $t_{SU, STO}$
t_9	1.3			µs	Bus free time between a stop and a start condition, t_{BUF}
t_{10}			300	ns	Rise time of SCL and SDA when receiving, t_R
	0			ns	Rise time of SCL and SDA when receiving (CMOS-compatible), t_R
t_{11}			300	ns	Fall time of SDA when transmitting, t_F
	0			ns	Fall time of SDA when receiving (CMOS-compatible), t_F
			300	ns	Fall time of SCL and SDA when receiving, t_F
	$20 + 0.1C_b$[2]			ns	Fall time of SCL and SDA when transmitting, t_F
C_b			400	pF	Capacitive load for each bus line

[1] A master device must provide a hold time of at least 300 ns for the SDA signal (referred to the V_{IH} min of the SCL signal) in order to bridge the undefined region of the SCL falling edge.
[2] Cb is the total capacitance, in pF, of one bus line. t_R and t_F are measured between 0.3 DV_{DDx} and 0.7 DV_{DDx}.

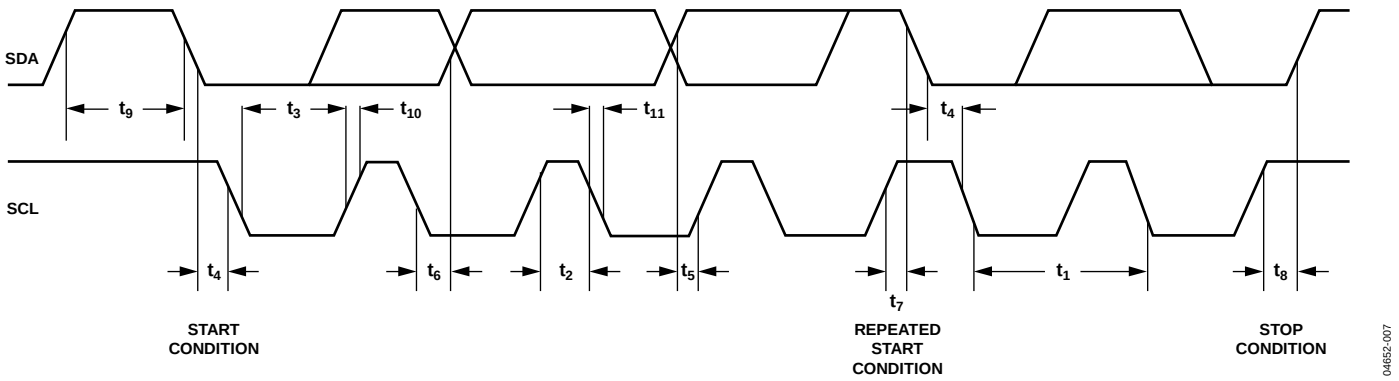

Figure 6. I²C-Compatible Serial Interface Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted. Transient currents of up to 100 mA do not cause silicon controlled rectifier (SCR) latch-up.

Table 5.

Parameter	Rating
AV_{DDx} to $AGND_x$	−0.3 V to +7 V
DV_{DDx} to DGND	−0.3 V to +7 V
Digital Inputs to DGND	−0.3 V to DV_{DDx} + 0.3 V
SDA/SCL to DGND	−0.3 V to + 7 V
Digital Outputs to DGND	−0.3 V to DV_{DDx} + 0.3 V
REF_IN/REF_OUT to $AGND_x$	−0.3 V to AV_{DDx} + 0.3 V
$AGND_x$ to DGND	−0.3 V to +0.3 V
VOUTx to $AGND_x$	−0.3 V to AV_{DDx} + 0.3 V
Analog Inputs to AGND	−0.3 V to AV_{DDx} + 0.3 V
Operating Temperature Range	
Commercial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	150°C
100-Ball CSP_BGA Package	
θ_{JA} Thermal Impedance	40°C/W
Reflow Soldering	
Peak Temperature	230°C
ESD	
Human Body Model (HBM)	6.5 kV
Field-Induced Charged Device Model (FICDM)	1.6 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

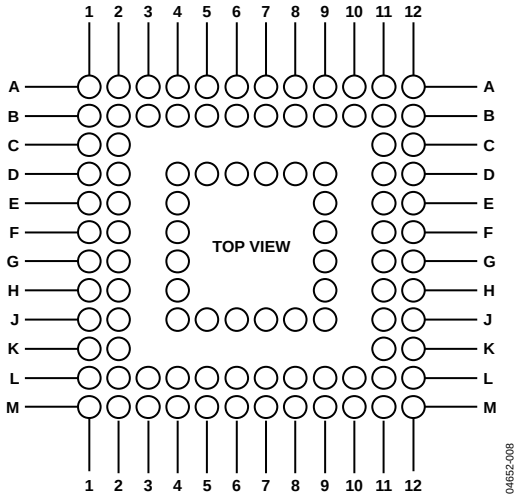

Figure 7. Pin Configuration

Table 6. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1, A12, B2, B11, C11, K11, L2, L11, M1, M12	NC	No Connect. Do not connect to these pins.
A2	VOUT24	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
A3	$\overline{CLR}$	Asynchronous Clear Input. The CLR input is falling edge sensitive. When $\overline{CLR}$ is activated, all channels are updated with the data in the $\overline{CLR}$ code register. $\overline{BUSY}$ is low for a duration of 35 µs while all channels are being updated with the $\overline{CLR}$ code.
A4	$\overline{SYNC}$/AD0	Multifunction Pin. In serial interface mode, the $\overline{SYNC}$ pin is the frame synchronization input signal for the serial clocks before the address register is updated. In I²C mode, AD0 acts as a hardware address pin used in conjunction with AD1 to determine the software address for the device on the I²C bus.
A5	SCLK/SCL	Multifunction Pin. In serial interface mode, data is clocked into the shift register on the falling edge of SCLK. SCLK operates at clock speeds up to 30 MHz. In I²C mode, the SCL pin clocks data into the device. The data transfer rate in I²C mode is compatible with both 100 kHz and 400 kHz operating modes.
A6, B6, D6	DV_{DD1} to DV_{DD3}	Logic Power Supply. Guaranteed operating range is 2.7 V to 5.5 V. Decouple these pins with 0.1 µF ceramic and 10 µF tantalum capacitors to DGND.
A7, B3, B7, D7	DGND	Ground for All Digital Circuitry.
A8	PD	Power-Down (Level Sensitive, Active High). Use PD to place the device in low power mode, where AI_{DD} reduces to 2 µA and DI_{DD} to 20 µA. In power-down mode, all internal analog circuitry is placed in low power mode, and the analog output is configured as a high impedance output or provides a 100 kΩ load to ground, depending on how the power-down mode is configured. The serial interface remains active during power-down.
A9	DCEN/AD1	Multifunction Pin. In SPI mode, the DCEN pin acts to enable the daisy-chain function. In I²C mode, the AD1 pin acts as a hardware address pin. Daisy-Chain Select Input (Level Sensitive, Active High). When DCEN is high, this pin is used in conjunction with the SPI/$\overline{I^2C}$ pin set high to enable the SPI serial interface in daisy-chain mode. In I²C mode, the AD1 pin acts as a hardware address pin used in conjunction with AD0 to determine the software address for this device on the I²C bus.

Pin No.	Mnemonic	Description
A10	$\overline{\text{LDAC}}$	Load DAC Logic Input (Active Low). If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is inactive (high), the contents of the input registers are transferred to the DAC registers, and the DAC outputs are updated. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is active and internal calculations are taking place, the $\overline{\text{LDAC}}$ event is stored, and the DAC registers are updated when $\overline{\text{BUSY}}$ goes inactive. However, any events on $\overline{\text{LDAC}}$ during power-on reset or at $\overline{\text{RESET}}$ are ignored.
A11	$\overline{\text{BUSY}}$	Digital CMOS Output. $\overline{\text{BUSY}}$ goes low during internal calculations of the data (×2) loaded to the DAC data register. During this time, the user can continue writing new data to the ×1, c, and m registers, but no further updates to the DAC registers and DAC outputs can take place. If $\overline{\text{LDAC}}$ is taken low while $\overline{\text{BUSY}}$ is low, this event is stored. $\overline{\text{BUSY}}$ also goes low during power-on reset, and when the $\overline{\text{BUSY}}$ pin is low. During this time, the interface is disabled, and any events on $\overline{\text{LDAC}}$ are ignored. A $\overline{\text{CLR}}$ operation also brings $\overline{\text{BUSY}}$ low.
B1	VOUT25	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
B4	DIN/SDA	In serial interface mode, DIN acts as the serial data input. Data must be valid on the falling edge of SCLK. In I^2C mode, this pin is the serial data pin (SDA) operating as an open-drain input/output.
B5	SDO	Serial Data Output in Serial Interface Mode. Three-state CMOS output. SDO can be used for daisy-chaining a number of devices together. Data is clocked out on SDO on the rising edge of SCLK, and is valid on the falling edge of SCLK.
B8	SPI/$\overline{\text{I}^2\text{C}}$	Serial Interface Mode Select. This is a multifunction pin. When this pin is high, SPI mode is selected. When this pin is low, $\overline{\text{I}^2\text{C}}$ is selected.
B9	$\overline{\text{RESET}}$	Asynchronous Digital Reset Input (Falling Edge Sensitive). The function of this pin is equivalent to that of the power-on reset generator. When this pin is taken low, the state machine initiates a reset sequence to digitally reset the ×1, m, c, and ×2 registers to their default power-on values. This sequence typically takes 270 µs. The falling edge of $\overline{\text{RESET}}$ initiates the $\overline{\text{RESET}}$ process, and $\overline{\text{BUSY}}$ goes low for the duration, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled, and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the device resumes normal operation, and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected.
B10	VOUT22	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
B12, C1	VOUT23, VOUT26	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
C2, D2	SIGNAL_GND4	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GNDx pins are connected together internally and must be connected to the AGND plane as close as possible to the AD5384.
C12, D1	VOUT21, VOUT27	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
D4, E4	DAC_GND4	Each Group of Eight Channels Contains a DAC_GNDx Pin. This is the ground reference point for the internal 14-bit DAC. Connect these pins to the AGND plane.
D5	AGND4	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. Connect all AGND pins externally to the AGND plane.
D8	AGND3	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. Connect all AGND pins externally to the AGND plane.
D9, E9	DAC_GND3	Each Group of Eight Channels Contains a DAC_GNDx Pin. This is the ground reference point for the internal 14-bit DAC. Connect these pins to the AGND plane.
D11	VOUT20	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
D12, E1	AV_{DD3}, AV_{DD4}	Analog Supply Pins. Each group of eight channels has a separate AV_{DDx} pin. Short these pins internally and decouple them with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range is 4.5 V to 5.5 V.
E2, F2	SIGNAL_GND1	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GNDx pins are connected together internally and must be connected to the AGND plane as close as possible to the AD5384.

Pin No.	Mnemonic	Description
E11, E12	VOUT17, VOUT19	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
F1	REF_GND	Ground Reference Point for the Internal Reference.
F4, G4	DAC_GND1	Each Group of Eight Channels Contains a DAC_GNDx Pin. This is the ground reference point for the internal 14-bit DAC. Connect these pins to the AGND plane.
F9, G9	SIGNAL_GND3	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GNDx pins are connected together internally and must be connected to the AGND plane as close as possible to the AD5384.
F11, F12, G1, G2, G11	VOUT16, VOUT18, VOUT28, VOUT29, VOUT15	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
G12	AV_{DD2}	Analog Supply Pin. Each group of eight channels has a separate AV_{DDx} pin. Short these pins internally and decouple them with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range is 4.5 V to 5.5 V.
H1	REF_OUT/ REF_IN	Common REF_OUT/REF_IN pin. The default for this pin is a reference input (REF_IN). When the internal reference is selected, this pin is the reference output (REF_OUT). If the application requires an external reference, apply it to this pin. The control register enables/disables the internal reference.
H2	VOUT31	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
H4, J4	DAC_GND5	Each Group of Eight Channels Contains a DAC_GNDx Pin. This is the ground reference point for the internal 14-bit DAC. Connect these pins to the AGND plane.
H9, J9	SIGNAL_GND2	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GNDx pins are connected together internally and must be connected to the AGND plane as close as possible to the AD5384.
H11, H12	VOUT13, VOUT14	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
J1	AV_{DD1}	Analog Supply Pin. Each group of eight channels has a separate AV_{DDx} pin. Short these pins internally and decouple them with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range is 4.5 V to 5.5 V.
J2	VOUT30	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
J5	AGND1	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. Connect all AGND pins externally to the AGND plane.
J6, J7	DAC_GND2	Each Group of Eight Channels Contains a DAC_GNDx Pin. This is the ground reference point for the internal 14-bit DAC. Connect these pins to the AGND plane.
J8	AGND2	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. Connect all AGND pins externally to the AGND plane.
J11, J12, K1, K2, K12, L1	VOUT12, VOUT11, VOUT0, VOUT1, VOUT10, VOUT2	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
L3, L4	SIGNAL_GND5	Analog Ground Reference Points for Each Group of Eight Output Channels. All SIGNAL_GNDx pins are connected together internally and must be connected to the AGND plane as close as possible to the AD5384.
L5	AGND5	Analog Ground Reference Point. Each group of eight channels contains an AGND pin. Connect all AGND pins externally to the AGND plane.

Pin No.	Mnemonic	Description
L6, L7, L8, L9, L10, L12, M2, M3, M4	VOUT6, VOUT32, VOUT34, VOUT36, VOUT38, VOUT9, VOUT3, VOUT4, VOUT5	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
M5	AV_{DD5}	Analog Supply Pin. Each group of eight channels has a separate AV_{DDx} pin. Short these pins internally and decouple them with a 0.1 µF ceramic capacitor and a 10 µF tantalum capacitor. Operating range is 4.5 V to 5.5 V.
M6, M7, M8, M9	VOUT7, VOUT33, VOUT35, VOUT37	Buffered Analog Outputs. Each analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. Each output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.
M10	VOUT39/ MON_OUT	This pin has a dual function. It acts as a buffered output for Channel 39 in default mode. However, when the monitor function is enabled, this pin acts as the output of a 39-to-1 channel multiplexer that can be programmed to multiplex one of Channel 0 to Channel 38 to the MON_OUT pin. The MON_OUT pin output impedance typically is 500 Ω, and it is intended to drive a high input impedance like that exhibited by the successive approximation register (SAR) analog-to-digital converter (ADC) inputs.
M11	VOUT8	Buffered Analog Output. The analog output is driven by a rail-to-rail output amplifier operating at a gain of 2. The output is capable of driving an output load of 5 kΩ to ground. Typical output impedance is 0.5 Ω.

TYPICAL PERFORMANCE CHARACTERISTICS

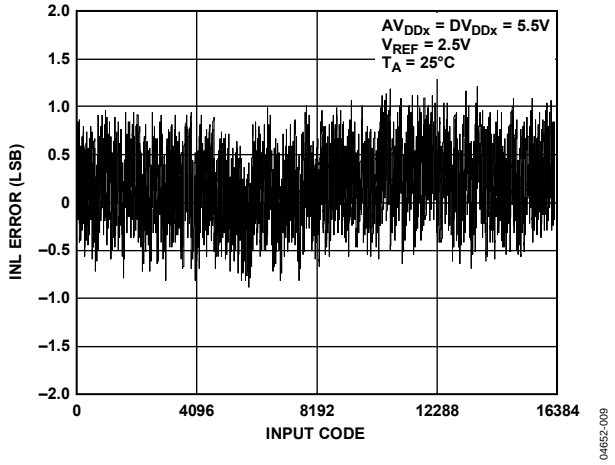

Figure 8. Typical INL Error Plot

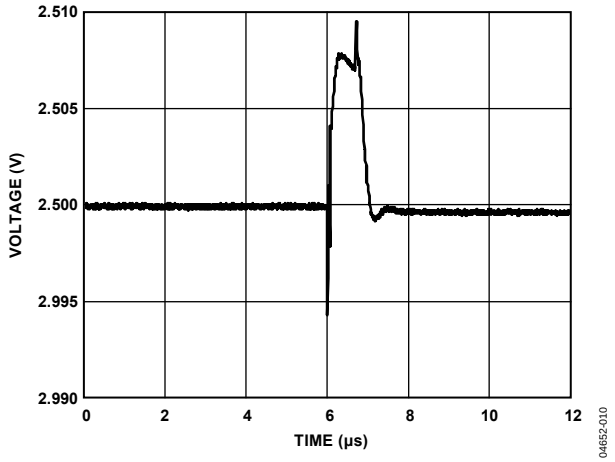

Figure 9. Glitch Impulse

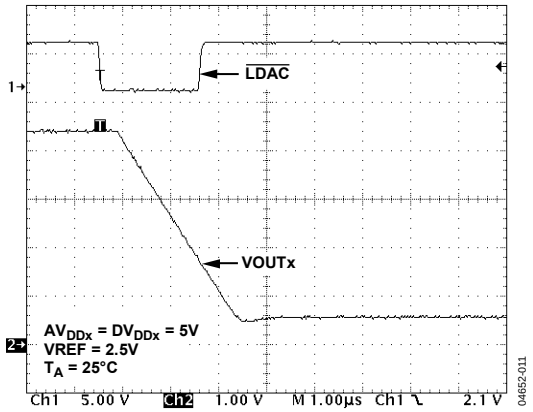

Figure 10. Slew Rate with Boost Off

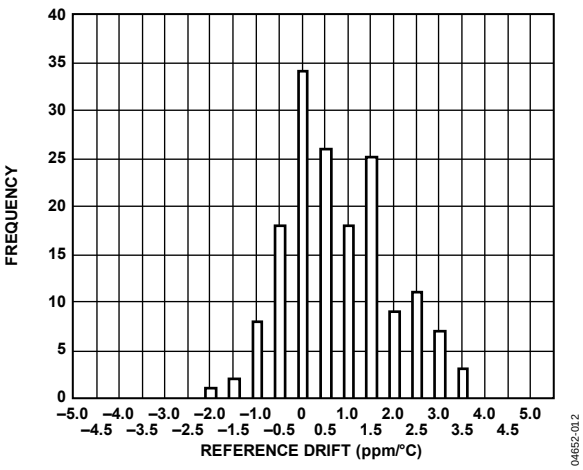

Figure 11. REF_OUT Temperature Coefficient

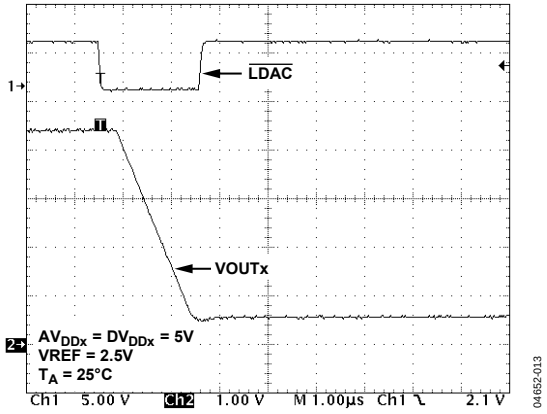

Figure 12. Slew Rate with Boost On

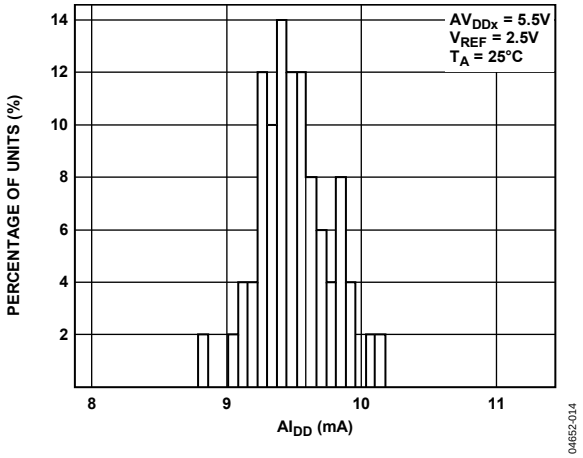

Figure 13. Histogram with Boost Off

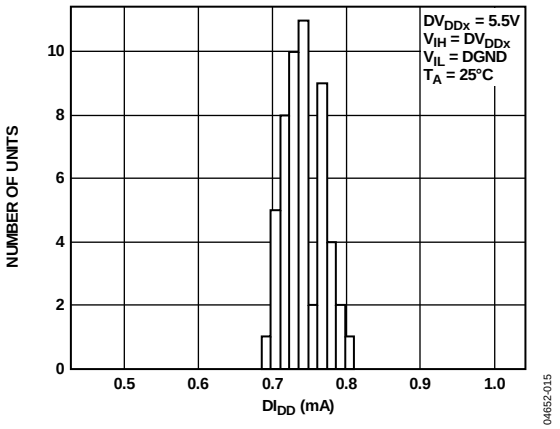

Figure 14. DI_{DD} Histogram

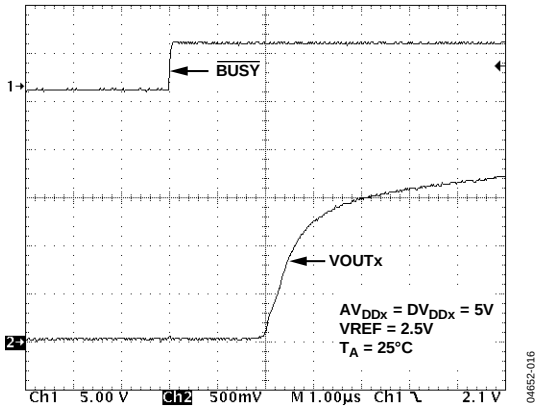

Figure 15. Exiting Soft Power-Down

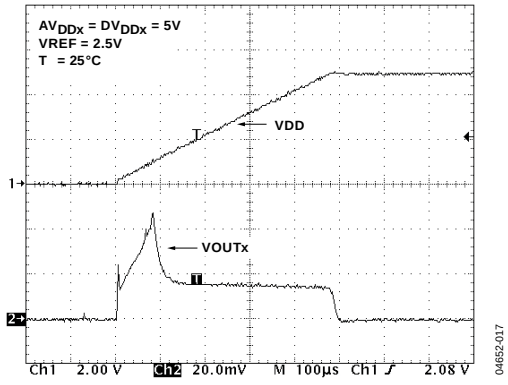

Figure 16. Power-Up Transient

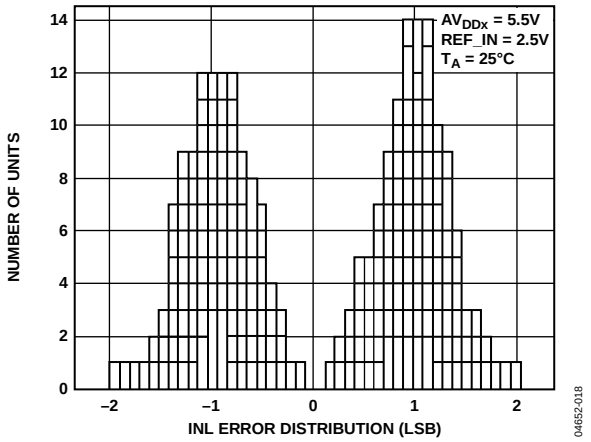

Figure 17. INL Distribution

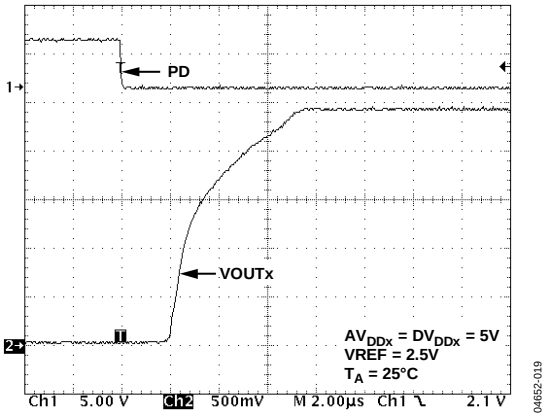

Figure 18. Exiting Hardware Power-Down

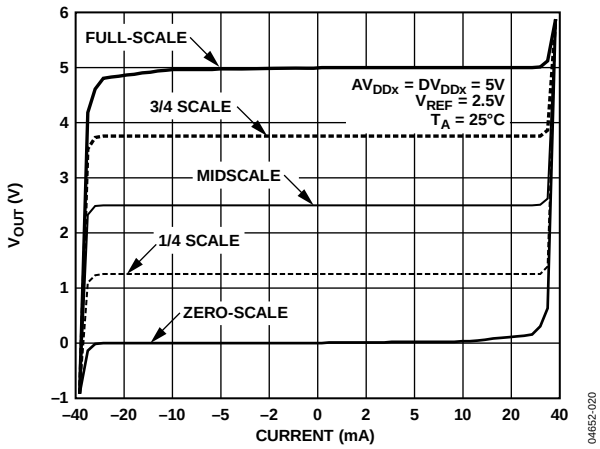

Figure 19. Output Amplifier Source and Sink Capability

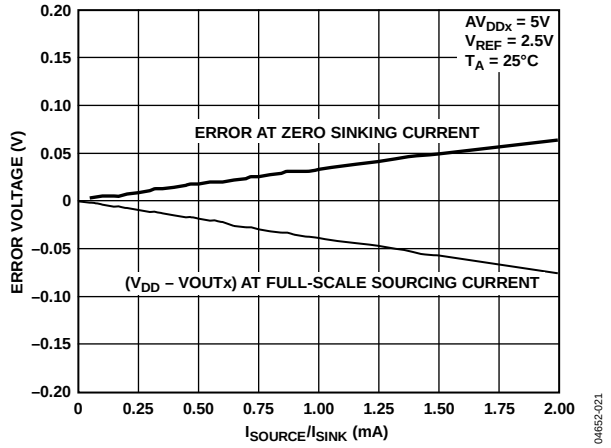

Figure 20. Headroom at Rail vs. I_{SOURCE}/I_{SINK}

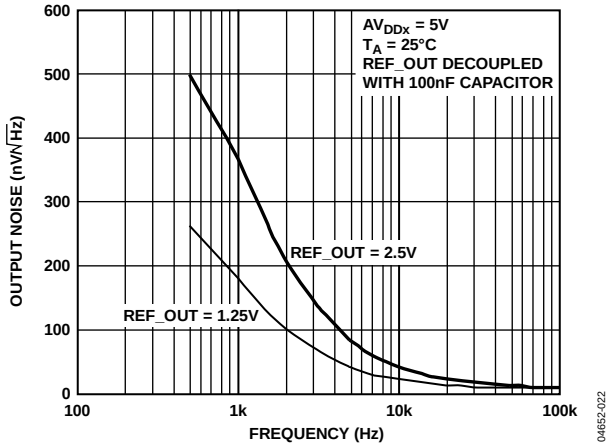

Figure 21. REF_OUT Noise Spectral Density

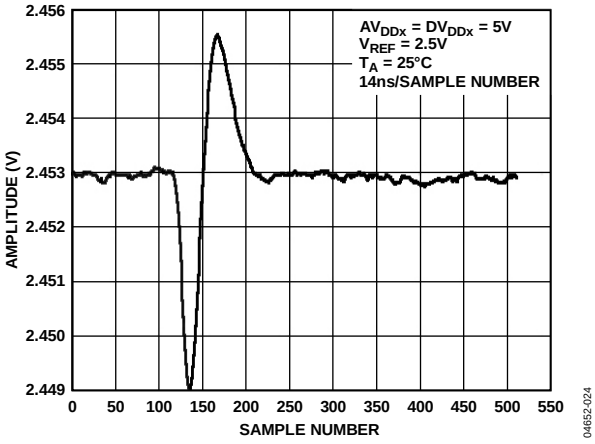

Figure 22. Adjacent Channel DAC to DAC Crosstalk

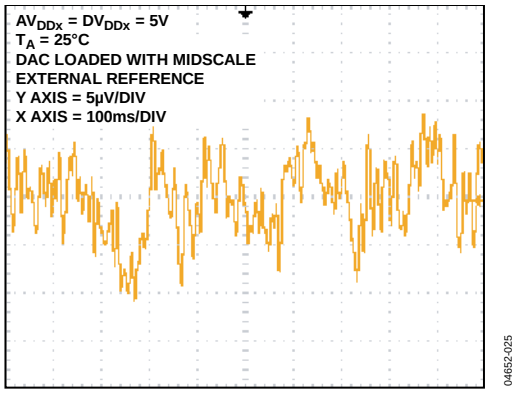

Figure 23. 0.1 Hz to 10 Hz Noise Plot

TERMINOLOGY

Relative Accuracy
Relative accuracy or endpoint linearity is a measure of the maximum deviation from a straight line passing through the endpoints of the DAC transfer function. It is measured after adjusting for zero-scale error and full-scale error, and is expressed in LSB.

Differential Nonlinearity
Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of 1 LSB maximum ensures monotonicity.

Zero-Scale Error
Zero-scale error is the error in the DAC output voltage when all 0s are loaded into the DAC register. Ideally, with all 0s loaded to the DAC and m = all 1s, $c = 2^{n-1}$.

$$V_{OUT\,(ZERO\text{-}SCALE)} = 0\ V$$

Zero-scale error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal), expressed in mV. It is mainly due to offsets in the output amplifier.

Offset Error
Offset error is a measure of the difference between V_{OUT} (actual) and V_{OUT} (ideal) in the linear region of the transfer function, expressed in mV. Offset error is measured on the AD5384-5 with Code 32 loaded into the DAC register.

Gain Error
Gain Error is specified in the linear region of the output range between V_{OUT} = 10 mV and $V_{OUT} = AV_{DDx} - 50$ mV. It is the deviation in slope of the DAC transfer characteristic from the ideal and is expressed in % FSR with the DAC output unloaded.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC at midscale, in response to a full-scale code (all 0s to all 1s, and vice versa) and output change of all other DACs. It is expressed in LSB.

DC Output Impedance
DC output impedance is the effective output source resistance. It is dominated by package lead resistance.

Output Voltage Settling Time
The output voltage settling time is the amount of time it takes for the output of a DAC to settle to a specified level for a ¼ to ¾ full-scale input change, and is measured from the $\overline{BUSY}$ rising edge.

Digital-to-Analog Glitch Energy
The digital-to-analog glitch energy is the amount of energy injected into the analog output at the major code transition. It is specified as the area of the glitch in nV-sec. It is measured by toggling the DAC register data between 0x1FFF and 0x2000.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse that appears at the output of one DAC due to both the digital change and the subsequent analog output change at another DAC. The victim channel is loaded with midscale. DAC-to-DAC crosstalk is specified in nV-sec.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one converter due to a change in the DAC register code of another converter. It is specified in nV-sec.

Digital Feedthrough
When the device is not selected, high frequency logic activity on the device digital inputs can be capacitively coupled both across and through the device to show up as noise on the VOUT pins. It can also be coupled along the supply and ground lines. This noise is digital feedthrough.

Output Noise Spectral Density
Output noise spectral density is a measure of internally generated random noise. Random noise is characterized as a spectral density (voltage per √Hertz). It is measured by loading all DACs to midscale and measuring noise at the output. It is measured in nV/√Hz in a 1 Hz bandwidth at 10 kHz.

FUNCTIONAL DESCRIPTION

DAC ARCHITECTURE—GENERAL

The AD5384 is a complete single-supply, 40-channel, voltage output DAC offering 14-bit resolution, available in a 100-ball CSP_BGA package. It features two serial interfaces, SPI and I²C. This family includes an internal 1.25 V/2.5 V, 10 ppm/°C that drives the buffered reference inputs. Alternatively, an external reference can drive these inputs. Reference selection is via a bit in the control register. Internal/external reference selection is via the CR10 bit in the control register, and the CR12 bit in the control register selects the reference magnitude if the internal reference is selected. All channels have an on-chip output amplifier with rail-to-rail output capable of driving 5 kΩ in parallel with a 200 pF load.

The architecture of a single DAC channel consists of a 14-bit resistor string DAC followed by an output buffer amplifier operating at a gain of 2. This resistor string architecture guarantees DAC monotonicity. The 14-bit binary digital code loaded to the DAC register determines at which node on the string the voltage is tapped off before being fed to the output amplifier.

Each channel on these devices contains independent offset and gain control registers allowing the user to digitally trim offset and gain. These registers let the user calibrate out errors in the complete signal chain, including the DAC, using the internal m and c registers that hold the correction factors. All channels are double buffered, allowing synchronous updating of all channels using the $\overline{\text{LDAC}}$ pin. Figure 24 shows a block diagram of a single channel on the AD5384. The following represents the digital input transfer function for each DAC:

$$x2 = [(m + 2)/ 2^n \times x1] + (c - 2^{n-1})$$

where:
x2 is the data-word loaded to the resistor-string DAC.
x1 is the 14-bit data-word written to the DAC input register.
m is the gain coefficient (default is 0x3FFE on the AD5384). The gain coefficient is written to the 13 most significant bits (DB13 to DB1) and the LSB (DB0) is 0.
n is the DAC resolution (*n* = 14 for AD5384).
c is the14-bit offset coefficient (default is 0x2000).

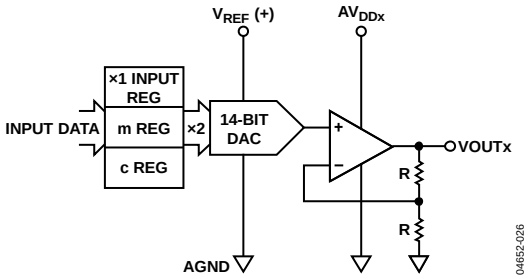

Figure 24. Single-Channel Architecture

The following represents the complete transfer function for these devices:

$$V_{OUT} = 2 \times V_{REF} \times x2/2^n$$

where:
x2 is the data-word loaded to the resistor string DAC.
V_{REF} is the internal reference voltage or the reference voltage externally applied to the DAC REF_OUT/REF_IN pin. For specified performance, an external reference voltage of 2.5 V is recommended.

DATA DECODING

The AD5384 contains a 14-bit data bus, DB13 to DB0. Depending on the value of REG1 and REG0 outlined in Table 7, this data is loaded into the addressed DAC input register(s), offset (c) register(s), or gain (m) register(s). Table 8, Table 9, and Table 10 outline the contents of the format data, offset (c), and gain (m) registers.

Table 7. Register Selection

REG1	REG0	Register Selected
1	1	Input data register (×1)
1	0	Offset register (c)
0	1	Gain register (m)
0	0	Special function registers (SFRs)

Table 8. DAC Data Format (REG1 = 1, REG0 = 1)

DB13 to DB0				DAC Output (V)
11	1111	1111	1111	$2 V_{REF} \times (16383/16384)$
11	1111	1111	1110	$2 V_{REF} \times (16382/16384)$
10	0000	0000	0001	$2 V_{REF} \times (8193/16384)$
10	0000	0000	0000	$2 V_{REF} \times (8192/16384)$
01	1111	1111	1111	$2 V_{REF} \times (8191/16384)$
00	0000	0000	0001	$2 V_{REF} \times (1/16384)$
00	0000	0000	0000	0

Table 9. Offset Data Format (REG1 = 1, REG0 = 0)

DB13 to DB0				Offset (LSB)
11	1111	1111	1111	+8191
11	1111	1111	1110	+8190
10	0000	0000	0001	+1
10	0000	0000	0000	0
01	1111	1111	1111	–1
00	0000	0000	0001	–8191
00	0000	0000	0000	–8192

Table 10. Gain Data Format (REG1 = 0, REG0 = 1)

DB13 to DB0				Gain Factor
11	1111	1111	1110	1
10	1111	1111	1110	0.75
01	1111	1111	1110	0.5
00	1111	1111	1110	0.25
00	0000	0000	0000	0

ON-CHIP SPECIAL FUNCTION REGISTERS (SFR)

The AD5384 contains a number of special function registers (SFRs), as outlined in Table 11. SFRs are addressed with REG1 = REG0 = 0 and are decoded using Address Bits A5 to A0.

Table 11. SFR Register Functions (REG1 = 0, REG0 = 0)

R/$\overline{W}$	A5	A4	A3	A2	A1	A0	Function
X	0	0	0	0	0	0	No operation (NOP)
0	0	0	0	0	0	1	Write CLR code
0	0	0	0	0	1	0	Soft CLR
0	0	0	1	0	0	0	Soft power-down
0	0	0	1	0	0	1	Soft power-up
0	0	0	1	1	0	0	Control register write
1	0	0	1	1	0	0	Control register read
0	0	0	1	0	1	0	Monitor channel
0	0	0	1	1	1	1	Software reset

SFR COMMANDS

NOP (No Operation)

REG1 = REG0 = 0, and A5 to A0 = 000000.

Performs no operation but is useful in serial readback mode to clock out data on D_{OUT} for diagnostic purposes. $\overline{BUSY}$ pulses low during an NOP operation.

Write CLR Code

REG1 = REG0 = 0, A5 to A0 = 000001, and DB13 to DB0 = contains the CLR data.

Bringing the $\overline{CLR}$ line low, or exercising the soft clear function, loads the contents of the DAC registers, with the data contained in the user configurable CLR register, and sets VOUT0 to VOUT39, accordingly. This is very useful for setting up a specific output voltage in a clear condition. It is also beneficial for calibration purposes; the user can load full scale or zero scale to the clear code register and then issue a hardware or software clear to load this code to all DACs, removing the need for individual writes to each DAC. Default at power-up is all 0s.

Soft CLR

REG1 = REG0 = 0, A5 to A0 = 000010, and DB13 to DB0 = don't care.

Executing this instruction performs the CLR, which is functionally the same as that provided by the external $\overline{CLR}$ pin. The DAC outputs are loaded with the data in the CLR code register. It takes 35 µs to execute fully the SOFT CLR, as indicated by the $\overline{BUSY}$ low time.

Soft Power-Down

REG1 = REG0 = 0, A5 to A0 = 001000, and DB13 to DB0 = don't care.

Executing this instruction performs a global power-down that puts all channels in low power mode, reducing the analog supply current to 2 µA maximum, and the digital current to 20 µA maximum. In power-down mode, the output amplifier can be configured as a high impedance output or can provide a 100 kΩ load to ground. The contents of all internal registers are retained in power-down mode. While in power-down mode, no registers can be written to.

Soft Power-Up

REG1 = REG0 = 0, A5 to A0 = 001001, and DB13 to DB0 = don't care.

This instruction powers up the output amplifiers and the internal reference. The time to exit power-down is 8 µs. The hardware power-down and software functions are internally combined in a digital OR function.

Software Reset

REG1 = REG0 = 0, A5 to A0 = 001111, and DB13 to DB0 = don't care.

This instruction implements a software reset. All internal registers reset to their default values, which correspond to m at full scale and c at zero. The contents of the DAC registers clear, setting all analog outputs to 0 V. The soft reset activation time is 135 µs. Only perform a soft reset when the AD5384 is not in power-down mode.

Table 12. Control Register Contents

MSB													LSB
CR13	CR12	CR11	CR10	CR9	CR8	CR7	CR6	CR5	CR4	CR3	CR2	CR1	CR0

Control Register Write/Read

REG1 = REG0 = 0, A5 to A0 = 001100, and R/$\overline{W}$ status determines if the operation is a write (R/$\overline{W}$ = 0) or a read (R/$\overline{W}$ = 1). The DB13 to DB0 bits contain the control register data.

Control Register Contents

CR13: power-down status. This bit configures the output amplifier state in power-down mode This bit is configured as follows:

- For CR13 = 1, the amplifier output is high impedance (default at power-up).
- For CR13 = 0, the amplifier output is 100 kΩ to ground.

CR12: REF select. This bit selects the operating internal reference for the AD5384. CR12 is programmed as follows:

- For CR12 = 1, the internal reference is 2.5 V, which is the recommended operating reference.
- For CR12 = 0, the internal reference is 1.25 V.

CR11: current boost control. This bit boosts the current in the output amplifier, thereby altering its slew rate. This bit is configured as follows:

- For CR11 = 1, boost mode is on, maximizing the bias current in the output amplifier, and optimizing its slew rate but increasing the power dissipation.
- For CR11 = 0, boost mode is off (default at power-up), reducing the bias current in the output amplifier and the overall power consumption.

CR10: internal/external reference. This bit determines if the DAC uses its internal reference or an externally applied reference. This bit is configured as follows:

- For CR10 = 1, the internal reference is enabled. The reference output depends on data loaded to CR12.
- For CR10 = 0, the external reference is selected (default at power-up).

CR9: channel monitor enable (see Channel Monitor Function). This bit is configured as follows:

- For CR9 = 1, the monitor is enabled which enables the channel monitor function. After a write to the monitor channel in the SFR register, the selected channel output routes to the MON_OUT pin. VOUT39 operates as the MON_OUT pin.
- For CR9 = 0, the monitor is disabled (default at power-up). When the monitor is disabled, the MON_OUT pin assumes its normal DAC output function.

CR8: thermal monitor function. This function monitors the AD5384 internal die temperature, when enabled. The thermal monitor powers down the output amplifiers when the temperature exceeds 130°C. This function protects the device when power dissipation is exceeded, if a number of output channels are simultaneously short circuited. If the die temperature drops below 130°C, a soft power-up reenables the output amplifiers. This bit is configured as follows:

- For CR8 = 1, the thermal monitor is enabled.
- For CR8 = 0, the thermal monitor is disabled (default at power-up).

CR7: don't care.

CR6 to CR2: toggle function enable. This function toggles the output between two codes loaded to the A and B register for each DAC. Control Register Bit CR6 to Control Register Bit CR2 enable individual groups of eight channels for operation in toggle mode. A Logic 1, written to any bit, enables a group of channels, and a Logic 0 disables a group. $\overline{LDAC}$ is used to toggle between the two registers. Table 13 shows the decoding for toggle mode operation. For example, CR6 controls group w, which contains Channel 32 to Channel 39, CR6 = 1 enables these channels.

CR1 and CR0: don't care.

Table 13. Toggle Function Enable

CR Bit	Group	Channels
CR6	4	32 to 39
CR5	3	24 to 31
CR4	2	16 to 23
CR3	1	8 to 15
CR2	0	0 to 7

Channel Monitor Function

REG1 = REG0 = 0, A5 to A0 = 001010, and DB13 to DB8 = contain data to address the monitored channel.

The AD5384 has a channel monitor function that consists of a multiplexer address via the interface, allows any channel output to be routed to the MON_OUT pin for monitoring, using an external ADC. In channel monitor mode, VOUT39 becomes the MON_OUT pin, to which all monitored pins are routed. Enable the channel monitor function in the control register before any channels are routed to the MON_OUT pin. On the AD5384, DB13 to DB8 contain the channel address for the monitored channel. Selecting Channel Address 63 three-states the MON_OUT pin.

Table 14. Channel Monitor Decoding

REG1	REG0	A5	A4	A3	A2	A1	A0	DB13	DB12	DB11	DB10	DB9	DB8	DB7 to DB0	MON_OUT
0	0	0	0	1	0	1	0	0	0	0	0	0	0	X	VOUT0
0	0	0	0	1	0	1	0	0	0	0	0	0	1	X	VOUT1
0	0	0	0	1	0	1	0	0	0	0	0	1	0	X	VOUT2
0	0	0	0	1	0	1	0	0	0	0	0	1	1	X	VOUT3
0	0	0	0	1	0	1	0	0	0	0	1	0	0	X	VOUT4
0	0	0	0	1	0	1	0	0	0	0	1	0	1	X	VOUT5
0	0	0	0	1	0	1	0	0	0	0	1	1	0	X	VOUT6
0	0	0	0	1	0	1	0	0	0	0	1	1	1	X	VOUT7
0	0	0	0	1	0	1	0	0	0	1	0	0	0	X	VOUT8
0	0	0	0	1	0	1	0	0	0	1	0	0	1	X	VOUT9
0	0	0	0	1	0	1	0	0	0	1	0	1	0	X	VOUT10
0	0	0	0	1	0	1	0	0	0	1	0	1	1	X	VOUT11
0	0	0	0	1	0	1	0	0	0	1	1	0	0	X	VOUT12
0	0	0	0	1	0	1	0	0	0	1	1	0	1	X	VOUT13
0	0	0	0	1	0	1	0	0	0	1	1	1	0	X	VOUT14
0	0	0	0	1	0	1	0	0	0	1	1	1	1	X	VOUT15
0	0	0	0	1	0	1	0	0	1	0	0	0	0	X	VOUT16
0	0	0	0	1	0	1	0	0	1	0	0	0	1	X	VOUT17
0	0	0	0	1	0	1	0	0	1	0	0	1	0	X	VOUT18
0	0	0	0	1	0	1	0	0	1	0	0	1	1	X	VOUT19
0	0	0	0	1	0	1	0	0	1	0	1	0	0	X	VOUT20
0	0	0	0	1	0	1	0	0	1	0	1	0	1	X	VOUT21
0	0	0	0	1	0	1	0	0	1	0	1	1	0	X	VOUT22
0	0	0	0	1	0	1	0	0	1	0	1	1	1	X	VOUT23
0	0	0	0	1	0	1	0	0	1	1	0	0	0	X	VOUT24
0	0	0	0	1	0	1	0	0	1	1	0	0	1	X	VOUT25
0	0	0	0	1	0	1	0	0	1	1	0	1	0	X	VOUT26
0	0	0	0	1	0	1	0	0	1	1	0	1	1	X	VOUT27
0	0	0	0	1	0	1	0	0	1	1	1	0	0	X	VOUT28
0	0	0	0	1	0	1	0	0	1	1	1	0	1	X	VOUT29
0	0	0	0	1	0	1	0	0	1	1	1	1	0	X	VOUT30
0	0	0	0	1	0	1	0	0	1	1	1	1	1	X	VOUT31
0	0	0	0	1	0	1	0	1	0	0	0	0	0	X	VOUT32
0	0	0	0	1	0	1	0	1	0	0	0	0	1	X	VOUT33
0	0	0	0	1	0	1	0	1	0	0	0	1	0	X	VOUT34
0	0	0	0	1	0	1	0	1	0	0	0	1	1	X	VOUT35
0	0	0	0	1	0	1	0	1	0	0	1	0	0	X	VOUT36
0	0	0	0	1	0	1	0	1	0	1	1	0	1	X	VOUT37
0	0	0	0	1	0	1	0	1	0	0	1	1	0	X	VOUT38
0	0	0	0	1	0	1	0	1	0	0	1	1	1	X	VOUT39
0	0	0	0	1	0	1	0	1	0	Values 0b1000 to 0b1110 are reserved				X	Undefined
0	0	0	0	1	0	1	0	1	1	1	1	1	1	X	Three-state

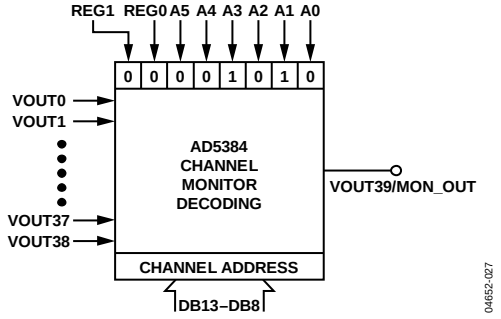

Figure 25. Channel Monitor Decoding

HARDWARE FUNCTIONS

RESET FUNCTION

Bringing the $\overline{\text{RESET}}$ line low resets the contents of the internal registers to their power-on reset state. $\overline{\text{RESET}}$ is a negative edge-sensitive input. The default corresponds to m at full scale and to c at zero. The contents of the DAC registers are cleared, setting VOUT0 to VOUT39 to 0 V. The hardware reset activation time takes 270 µs. The falling edge of $\overline{\text{RESET}}$ initiates the reset process; $\overline{\text{BUSY}}$ goes low during this process, returning high when $\overline{\text{RESET}}$ is complete. While $\overline{\text{BUSY}}$ is low, all interfaces are disabled, and all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{BUSY}}$ returns high, the device resumes normal operation, and the status of the $\overline{\text{RESET}}$ pin is ignored until the next falling edge is detected. Do not bring RESET low when the AD5384 is in power-down mode.

ASYNCHRONOUS CLEAR FUNCTION

Bringing the $\overline{\text{CLR}}$ line low loads the contents of the DAC registers with the data contained in the user-configurable CLR register, and sets VOUT0 to VOUT39 accordingly. Use this function in system calibration to load zero scale and full scale to all channels. The execution time for $\overline{\text{CLR}}$ is 35 µs.

$\overline{\text{BUSY}}$ AND $\overline{\text{LDAC}}$ FUNCTIONS

$\overline{\text{BUSY}}$ is a digital CMOS output that indicates the status of the AD5384. The value of x2, the internal data loaded to the DAC data register, is calculated each time the user writes new data to the corresponding x1, c, or m registers. During the calculation of x2, the $\overline{\text{BUSY}}$ output goes low. While $\overline{\text{BUSY}}$ is low, the user can continue writing new data to the x1, m, or c registers, but no DAC output updates can take place. The DAC outputs are updated by bringing the $\overline{\text{LDAC}}$ input low. If $\overline{\text{LDAC}}$ goes low while $\overline{\text{BUSY}}$ is active, the $\overline{\text{LDAC}}$ event is stored, and the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. The user can hold the $\overline{\text{LDAC}}$ input permanently low, in which case, the DAC outputs update immediately after $\overline{\text{BUSY}}$ goes high. $\overline{\text{BUSY}}$ also goes low during power-on reset and when a falling edge is detected on the $\overline{\text{RESET}}$ pin. During this time, all interfaces are disabled, and any events on $\overline{\text{LDAC}}$ are ignored. The AD5384 contains an extra feature, whereby a DAC register does not update unless its x2 register has been written to since the last time $\overline{\text{LDAC}}$ was brought low. Normally, when $\overline{\text{LDAC}}$ is brought low, the DAC registers fill with the contents of the x2 registers. However, the AD5384 updates the DAC register only if the x2 data has changed, thereby removing unnecessary digital crosstalk.

POWER-ON RESET

The AD5384 contains a power-on reset generator and state machine. The power-on reset generator resets all registers to a predefined state and configures the analog outputs as high impedance. The $\overline{\text{BUSY}}$ pin goes low during the power-on reset sequencing, preventing data writes to the device.

POWER-DOWN FEATURE

The AD5384 contains a global power-down feature that puts all channels into low power mode and reduces the analog power consumption to 2 µA maximum and digital power consumption to 20 µA maximum. In power-down mode, the output amplifier can be configured as a high impedance output, or it can provide a 100 kΩ load to ground. The contents of all internal registers remain in power-down mode. When exiting power-down mode, the settling time of the amplifier elapses before the outputs settle to their correct values.

POWER SUPPLY SEQUENCING

The power-on reset circuitry requires that the AV_{DDx} is applied before or within 10 ms of DV_{DDx}, which ensures that the registers are correctly loaded with their default values. If it is not possible for AV_{DDx} to be applied within 10 ms of DVDDx, a software or hardware reset is used to load the default register values.

INTERFACES

The AD5384 contains a serial interface that can be programmed as DSP-, SPI-, MICROWIRE-, or I²C-compatible. Select DSP, SPI, MICROWIRE, or I²C interface mode by using the SPI/$\overline{I^2C}$ pin . To minimize both the power consumption of the device and the on-chip digital noise, the active interface powers up fully only when the device is being written to on the falling edge of $\overline{SYNC}$.

DSP-, SPI-, MICROWIRE-COMPATIBLE SERIAL INTERFACE

The serial interface operates with a minimum of three wires in standalone mode or five wires in daisy-chain mode. Daisy-chaining allows many devices to be cascaded together to increase system channel count. Tie the SPI/$\overline{I^2C}$ (Ball B8) high to enable the DSP-, SPI-, or MICROWIRE-compatible serial interface. The following are the serial interface control pins:

- $\overline{SYNC}$/AD0, DIN/SDA, and SCLK/SCL are the standard 3-wire interface pins.
- DCEN/AD1 selects standalone mode or daisy-chain mode.
- SDO is the data out pin for daisy-chain mode.

Figure 3 and Figure 5 show the timing diagrams for a serial write to the AD5384 in standalone and in daisy-chain modes.

The 24-bit data-word format for the serial interface is shown in Table 15. The bit descriptions are as follows:

- When toggle mode is enabled, the $\overline{A}$/B bit selects whether the data write is to the A register or B register. When toggle mode is disabled, set $\overline{A}$/B to zero to select the A data register.
- R/$\overline{W}$ is the read or write control bit.
- A5 to A0 are used to address the input channels.
- REG1 and REG0 select the register to which data is written, as shown in Table 7.
- DB13 to DB0 contain the input data-word.
- X is a don't care condition.

Standalone Mode

Connect the DCEN (daisy-chain enable) pin low to enable standalone mode. The serial interface works with both a continuous and a noncontinuous serial clock. The first falling edge of $\overline{SYNC}$ starts the write cycle and resets a counter that counts the number of serial clocks to ensure that the correct number of bits are shifted into the serial shift register. Any further edges on $\overline{SYNC}$, except for a falling edge, are ignored until 24 bits are clocked in. Once 24 bits are shifted in, SCLK is ignored. For another serial transfer to take place, reset the counter by the falling edge of $\overline{SYNC}$.

Table 15. 40-Channel, DAC Serial Input Register Configuration

MSB																							LSB
$\overline{A}$/B	R/$\overline{W}$	A5	A4	A3	A2	A1	A0	REG1	REG0	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0

Daisy-Chain Mode

For systems that contain several devices, the SDO pin can be used to daisy-chain several devices together. This daisy-chain mode is useful in system diagnostics and in reducing the number of serial interface lines.

Connect the DCEN (daisy-chain enable) pin high, to enable daisy-chain mode. The first falling edge of $\overline{\text{SYNC}}$ starts the write cycle. The SCLK is applied continuously to the input shift register when $\overline{\text{SYNC}}$ is low. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the rising edge of SCLK and is valid on the falling edge. By connecting the SDO of the first device to the DIN input on the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24N, where N is the total number of AD5384 devices in the chain.

When the serial transfer to all devices is complete, $\overline{\text{SYNC}}$ goes high, latches the input data in each device in the daisy-chain, and prevents any further data from clocking into the input shift register.

If $\overline{\text{SYNC}}$ is taken high before 24 clocks are clocked into the device, it is considered a bad frame, and the data is discarded.

The serial clock is either a continuous or a gated clock. A continuous SCLK source is used only if $\overline{\text{SYNC}}$ is held low for the correct number of clock cycles. In gated clock mode, use a burst clock containing the exact number of clock cycles and take $\overline{\text{SYNC}}$ high after the final clock to latch the data.

Readback Mode

Readback mode is invoked by setting the R/$\overline{\text{W}}$ bit = 1 in the serial input register write. With R/$\overline{\text{W}}$ = 1, Bits A5 to A0, in association with Bit REG1 and Bit REG0, select the register to be read. The remaining data bits in the write sequence are don't cares. During the next SPI write, the data appearing on the SDO output contains the data from the previously addressed register. For a read of a single register, use the NOP command to clock out the data from the selected register on SDO. Figure 26 shows the readback sequence.

For example, to read back the m register of Channel 0 on the AD5384, the following sequence must be followed. First, write 0x404XXX to the AD5384 input register. This configures the AD5384 for read mode with the m register of Channel 0 selected. Note that Data Bit DB13 to Data Bit DB0 are don't cares. Follow this with a second write, an NOP condition, 0x000000. During this write, the data from the m register clocks out on the SDO line; data clocked out contains the data from the m register in Bit DB13 to Bit DB0, and the top 10 bits contain the address information as previously written. In readback mode, the $\overline{\text{SYNC}}$ signal frames the data. Data clocks out on the rising edge of SCLK and is valid on the falling edge of the SCLK signal. If the SCLK idles high between the write and read operations of a readback operation, the first bit of data clocks out on the falling edge of $\overline{\text{SYNC}}$.

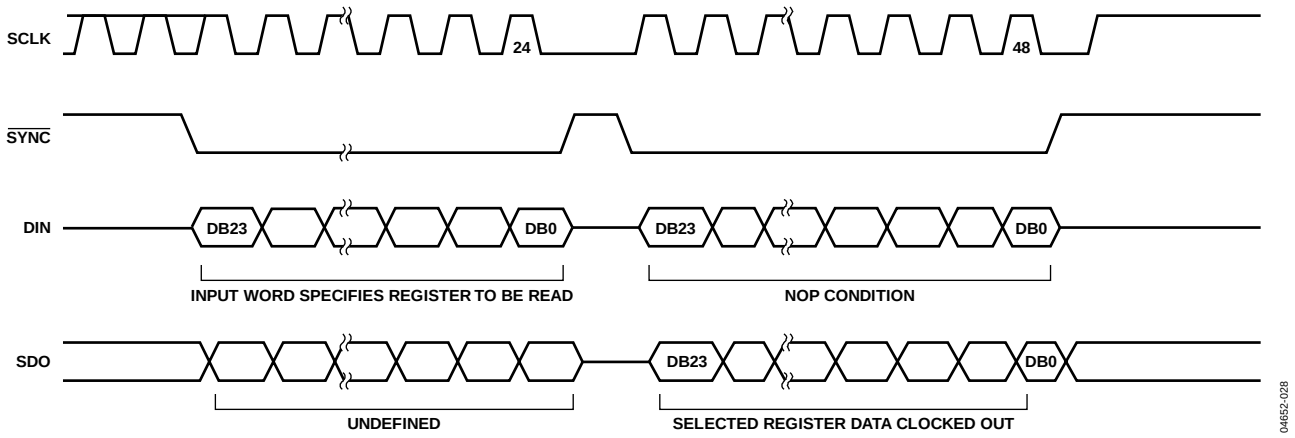

Figure 26. Serial Readback Operation

I²C SERIAL INTERFACE

The AD5384 features an I²C-compatible 2-wire interface consisting of a serial data line (SDA) and a serial clock line (SCL). SDA and SCL facilitate communication between the AD5384 and the master at rates up to 400 kHz. Figure 6 shows the 2-wire interface timing diagrams that incorporate three different modes of operation.

Select I²C mode by configuring the SPI/$\overline{\text{I²C}}$ pin to a Logic 0. The device is connected to this bus as a slave device, and no clock is generated by the AD5384. The AD5384 has a 7-bit slave address, 1010 1 (AD1)(AD0) The 5 MSBs are hard coded, and the two LSBs are determined by the state of the AD1 and AD0 pins. The ability to hardware-configure AD1 and AD0 allows four of these devices to be configured on the bus.

I²C Data Transfer

During each SCL clock cycle, one data bit transfers. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals that configure start and stop conditions. When the I²C bus is not busy, the external pull-up resistors pull both SDA and SCL high.

Start and Stop Conditions

A master device initiates communication by issuing a start condition. A start condition is a high to low transition on SDA with SCL high. A stop condition is a low to high transition on SDA while SCL is high. A start condition from the master signals the beginning of a transmission to the AD5384. The stop condition frees the bus. If a repeated start condition (Sr) generates instead of a stop condition, the bus remains active.

Repeated Start Conditions

A repeated start (Sr) condition can indicate a change of data direction on the bus. Use Sr when the bus master is writing to several I²C devices and wants to maintain control of the bus.

Acknowledge Bit (ACK)

The acknowledge bit (ACK) is the ninth bit attached to any 8-bit data-word. ACK is always generated by the receiving device. The AD5384 devices generate an ACK when receiving an address or data by pulling SDA low during the ninth clock period. Monitoring ACK allows detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault occurs. In the event of an unsuccessful data transfer, the bus master reattempts communication.

Slave Addresses

A bus master initiates communication with a slave device by issuing a start condition, followed by the 7-bit slave address. When idle, the AD5384 waits for a start condition followed by its slave address. The LSB of the address word is the read/write (R/$\overline{\text{W}}$) bit. The AD5384 devices are receive-only devices; when communicating with these, R/$\overline{\text{W}}$ = 0. After receiving the proper address 1010 1(AD1)(AD0), the AD5384 issues an ACK by pulling SDA low for one clock cycle.

The AD5384 has four different user programmable addresses determined by the AD1 and AD0 bits.

Write Operation

Data can be written to the AD5384 DACs in three modes: 4-byte mode, 3-byte mode, and 2-byte mode.

4-Byte Mode

When writing to the AD5384 DACs, the user must begin with an address byte (R/$\overline{\text{W}}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte; this addresses the specific channel in the DAC to be addressed and also is acknowledged by the DAC. Two bytes of data are then written to the DAC, as shown in Figure 27. A stop condition follows. This lets the user update a single channel within the AD5384 at any time, and requires four bytes of data to transfer from the master.

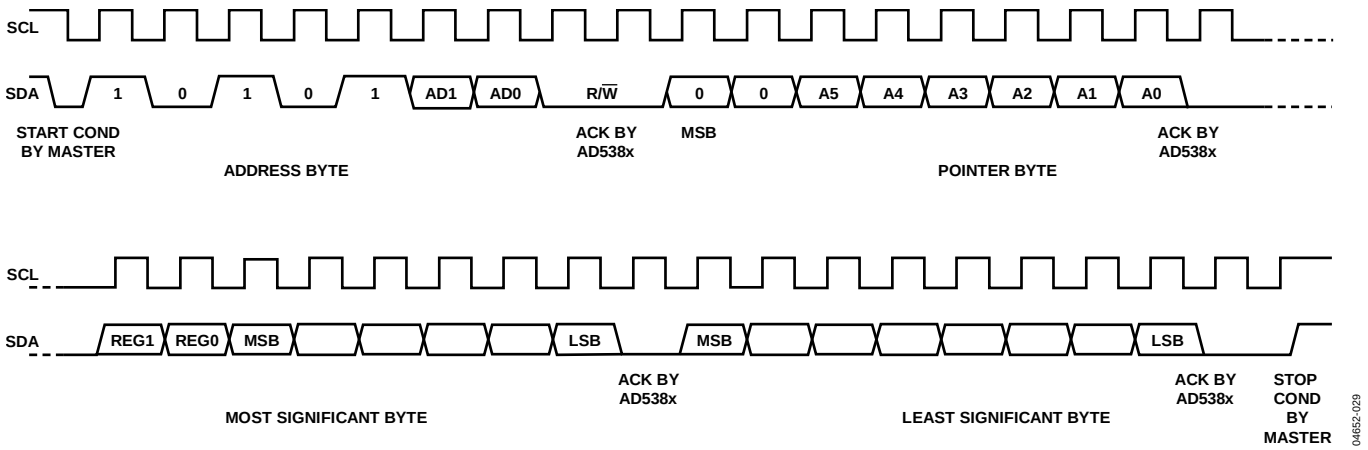

Figure 27. 4-Byte, I²C Write Operation

3-Byte Mode

In 3-byte mode, the user can update more than one channel in a write sequence without having to write the device address byte each time. The device address byte is required only once; subsequent channel updates require the pointer byte and the data bytes. In 3-byte mode, the use must begin with an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by the pointer byte. This addresses the specific channel in the DAC to be addressed and also is acknowledged by the DAC. This is then followed by the two data bytes, REG1 and REG0, which determine the register to be updated.

If a stop condition does not follow the data bytes, another channel can be updated by sending a new pointer byte, followed by the data bytes. This mode requires only three bytes to be sent to update any channel once the device is initially addressed, and it reduces the software overhead in updating the AD5384 channels. A stop condition at any time exits this mode. Figure 28 shows a typical configuration.

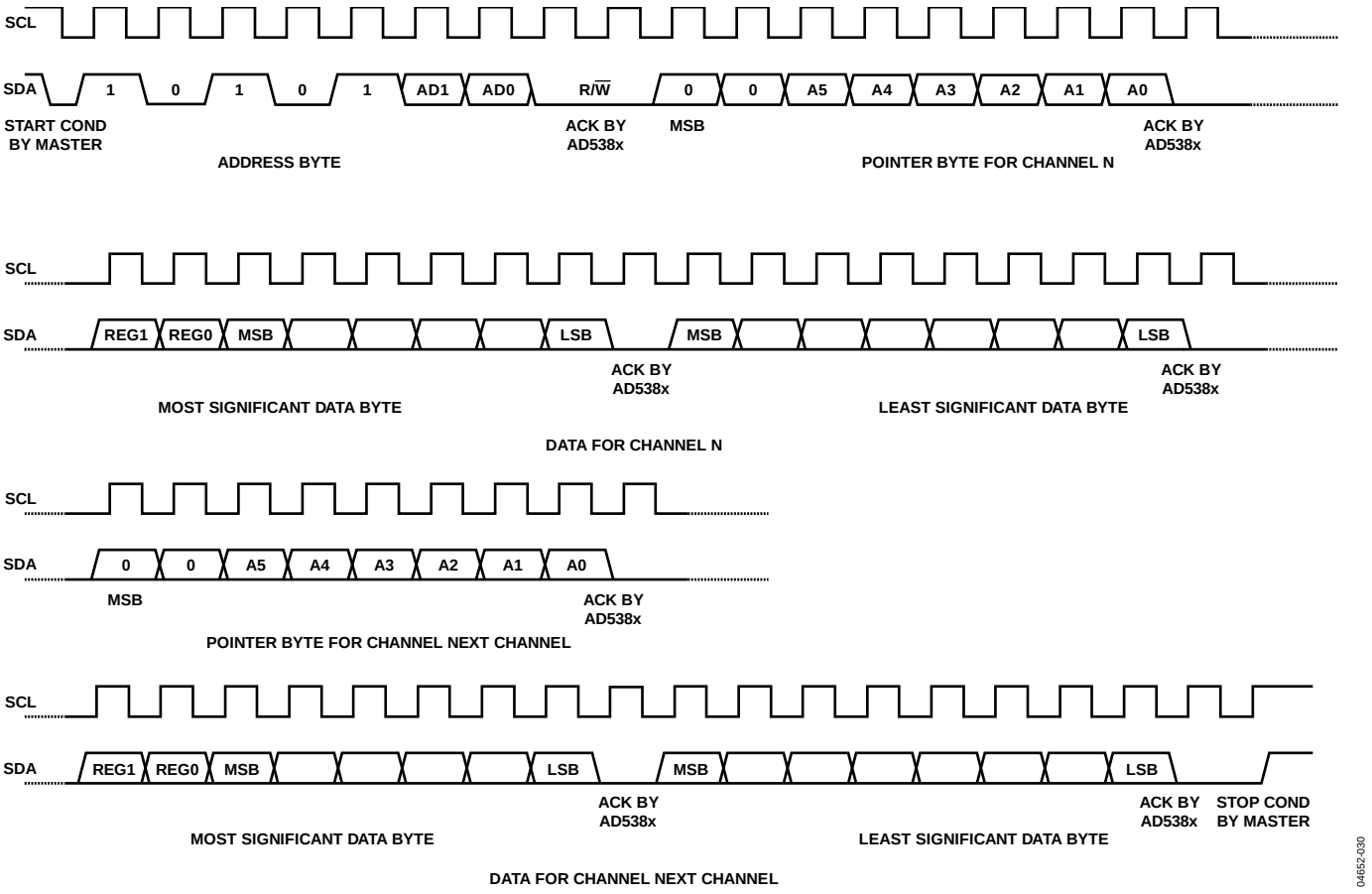

Figure 28. 3-Byte, I²C Write Operation

2-Byte Mode

Following initialization of 2-byte mode, the user can update channels sequentially. The device address byte is required only once, and the pointer byte is configured for auto-increment or burst mode.

The user must begin with an address byte (R/$\overline{W}$ = 0), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The address byte is followed by a specific pointer byte (0xFF) that initiates the burst mode of operation. The address pointer initializes to Channel 0, and upon receiving the two data bytes for the present address, automatically increments to the next address.

The REG0 and REG1 bits in the data byte determine which register updates. In this mode, following initialization, only two data bytes are required to update a channel. The channel address automatically increments from Address 0. This mode allows transmission of data to all channels in one block, and it reduces the software overhead in configuring all channels. A stop condition at any time exits this mode. Toggle mode is not supported in 2-byte mode. Figure 29 shows a typical configuration.

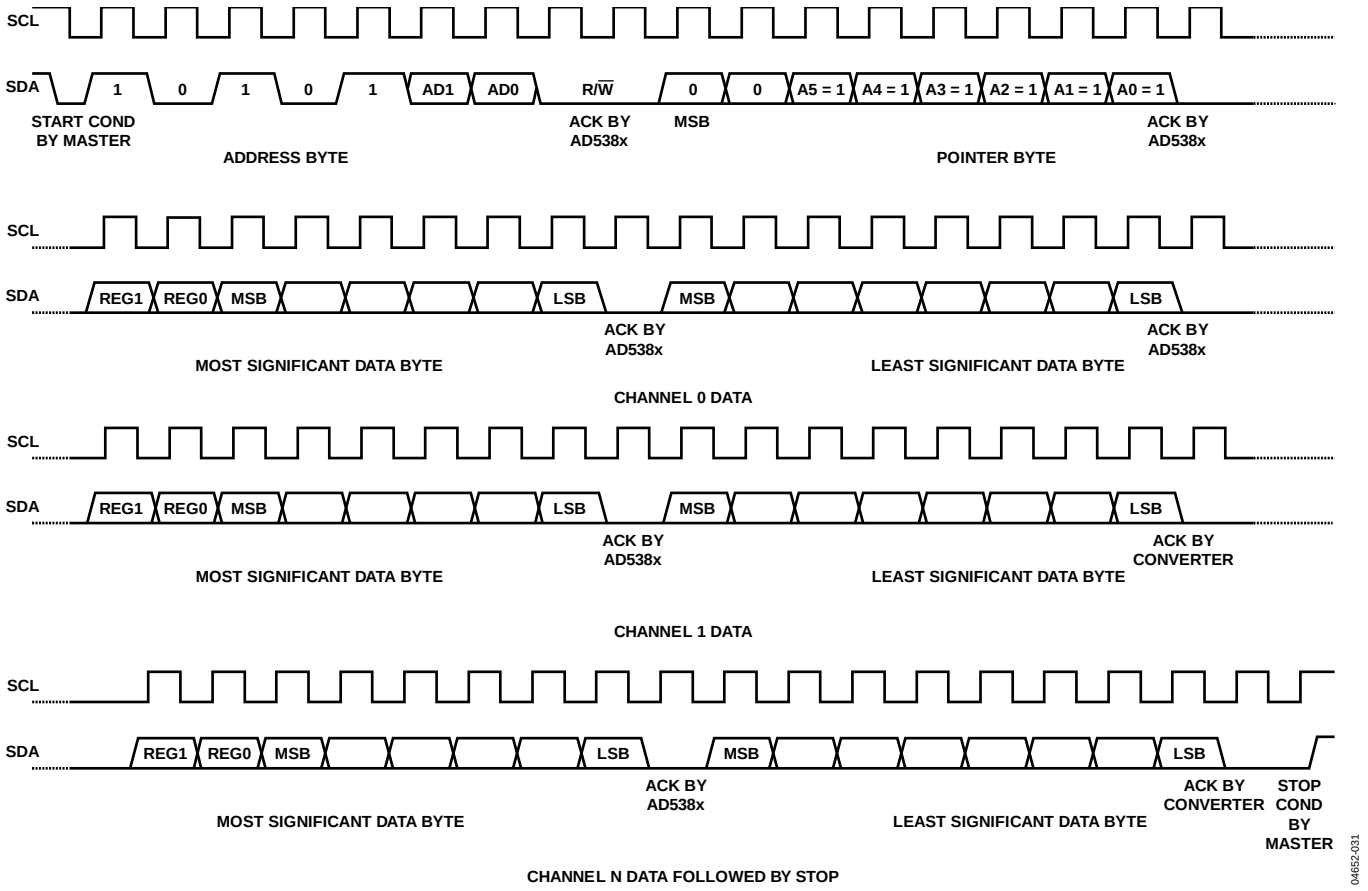

Figure 29. 2-Byte, I^2C Write Operation

APPLICATIONS INFORMATION

POWER SUPPLY DECOUPLING

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. Separate and confine the analog and digital sections to certain areas of the printed circuit board (PCB) of the AD5384. If the AD5384 is in a system where multiple devices require an AGND-to-DGND connection, make the connection at one point only, a star ground point established as near to the device as possible.

For supplies with multiple pins (AV_{DDx}, and AV_{CCx}), tie these pins together. Allow ample supply bypassing of 10 µF capacitators in parallel with 0.1 µF capacitors on each supply, located as near the package as possible and ideally right up against the AD5384 device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor has low effective series resistance (ESR) and effective series inductance (ESI), such as the common ceramic types that provide a low impedance path to ground at high frequencies, so that it can handle transient currents due to internal logic switching.

The power supply lines of the AD5384 use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Shield fast switching signals, such as clocks, with digital ground to avoid radiating noise elsewhere on the board, and do not run them near the reference inputs. A ground line routed between the D_{IN} and SCLK lines helps to reduce crosstalk between them (this is not required on a multilayer board because there is a separate ground plane; however, separating the lines helps). It is essential to minimize noise on the V_{IN} and REF_IN lines.

Avoid crossover of digital and analog signals. Run the traces on opposite sides of the board at right angles to each other. This reduces the effects of feedthrough through the board. A microstrip technique is by far the best; however, it is not always possible with a double-sided board. In this technique, the component side of the board is dedicated to the ground plane while signal traces are placed on the solder side.

POWER SUPPLY SEQUENCING

For proper operation, DV_{DD} must be applied first and AV_{DD} applied simultaneously or within 10 ms of DV_{DD}. This ensures that the power-on reset circuitry sets the registers to their default values and keeps the analog outputs at 0 V until a valid write operation takes place. When AV_{DD} cannot be applied within 10 ms of DV_{DD}, a hardware reset must be issued. This triggers the power-on reset circuitry and loads the default register values. For cases where the power supply applied first has the same or lower voltage than the second supply, a Schottkey diode can be used to supply power until the second power supply turns on. Table 18 lists power supply sequences and the recommended diode connection. Alternatively, a load switch such as the ADP196 can be used to delay the first power supply until the second power supply turns on. Figure 32 shows a typical configuration using the ADP196.

In this case, the AV_{DD} is applied first. This voltage does not appear at the AV_{DD} pin of the AD5384 until the DV_{DD} is applied and brings the EN pin high. The result is that the AV_{DD} and DV_{DD} are both applied to the AD5384 at the same time.

Table 16. Power Supply Sequencing

First Power Supply	Second Power Supply	Recommended Operation
AV_{DD} = 3 V	DV_{DD} ≥ 3 V	See Figure 30.
DV_{DD} = 3 V	AV_{DD} ≥ 3 V	See Figure 31.
AV_{DD} = DV_{DD}	DV_{DD} = AV_{DD}	See Figure 30; assumes separate analog and digital supplies.
DV_{DD} = AV_{DD}	AV_{DD} = DV_{DD}	See Figure 31; assumes separate analog and digital supplies.
AV_{DD} = 5 V	DV_{DD} = 3 V	See Figure 32.
DV_{DD} = 5 V	AV_{DD} = 3 V	Hardware reset or see Figure 33.

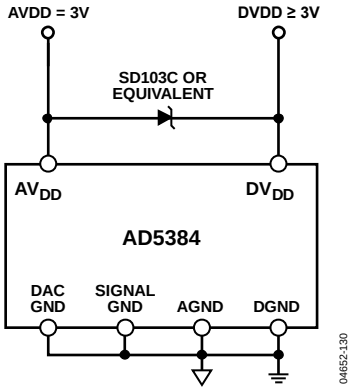

Figure 30. AV_{DD} first followed by DV_{DD}

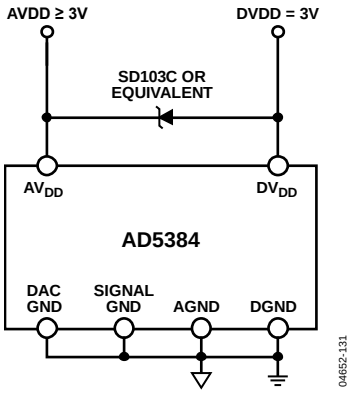

Figure 31. DV_{DD} first followed by AV_{DD}

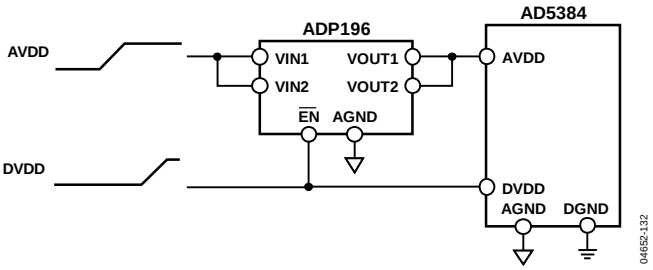

Figure 32. AV_{DD} Power Supply Controlled by a Load Switch

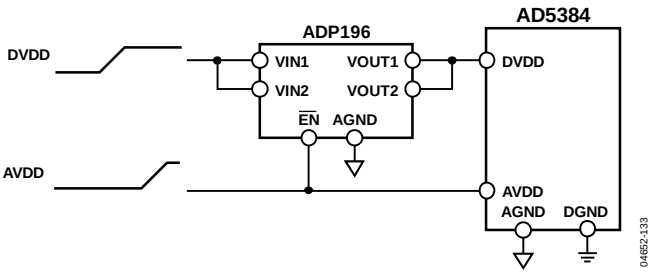

Figure 33. DV_{DD} Power Supply Controlled by a Load Switch

MONITOR FUNCTION

The AD5384 contains a channel monitor function that consists of a multiplexer addressed via the interface, allowing any channel output to be routed to this pin for monitoring, using an external ADC. In channel monitor mode, VOUT39 becomes the MON_OUT pin, to which all monitored signals are routed. Enable the channel monitor function in the control register before any channels are routed to the MON_OUT pin.

Table 14 shows the decoding information required to route any channel to MON_OUT. Selecting Channel Address 63 three-states the MON_OUT pin. Figure 34 shows a typical monitoring circuit implemented using a 12-bit SAR ADC in a 6-lead SOT package. The controller output port selects the channel to monitor, and the input port reads the converted data from the ADC.

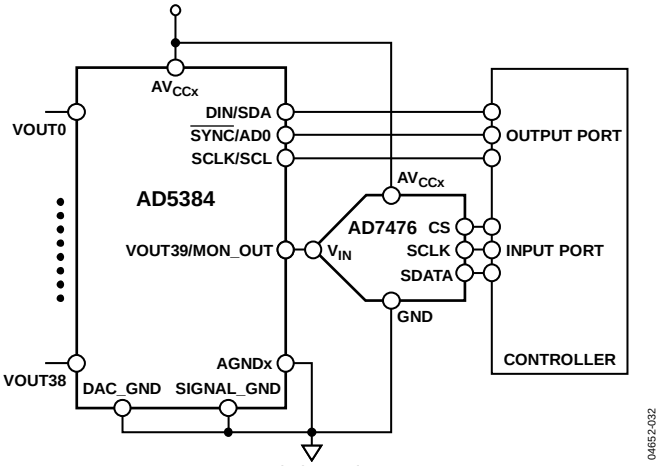

Figure 34. Typical Channel Monitoring Circuit

TOGGLE MODE FUNCTION

The toggle mode function allows an output signal to be generated using the $\overline{\text{LDAC}}$ control signal, which switches between two DAC data registers. This function is configured using the SFR control register as follows: A write with REG1 = REG0 = 0 and A5 to A0 = 001100 specifies a control register write. The toggle mode function is enabled in groups of eight channels using Bit CR6 to Bit CR2 in the control register (see Table 12). Figure 35 shows a block diagram of toggle mode implementation.

Each of the 40 DAC channels on the AD5384 contains an A and B data register. Note that the B registers load only when toggle mode is enabled. The sequence of events when configuring the AD5384 for toggle mode is

1. Enable toggle mode for the required channels via the control register.
2. Load data to A registers.
3. Load data to B registers.
4. Apply $\overline{\text{LDAC}}$.

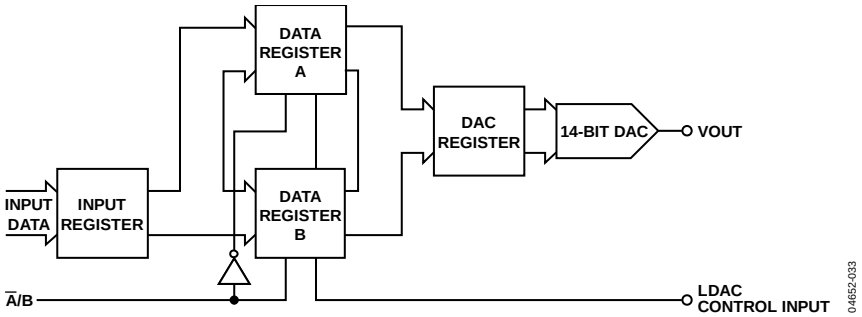

Figure 35. Toggle Mode Function

The $\overline{\text{LDAC}}$ is used to switch between the A and B registers in determining the analog output. The first $\overline{\text{LDAC}}$ configures the output to reflect the data in the A registers. This mode offers significant advantages if the user wants to generate a square wave at the output of all 40 channels, as can be required to drive a liquid crystal-based variable optical attenuator. In this case, the user writes to the control register, and enables the toggle function by setting CR6 to CR2 = 1, thus enabling the five groups of eight for toggle mode operation. The user must then load data to all 40 A and B registers. Toggling $\overline{\text{LDAC}}$ sets the output values to reflect the data in the A and B registers. The frequency of the $\overline{\text{LDAC}}$ determines the frequency of the square wave output.

Toggle mode is disabled via the control register. The first $\overline{\text{LDAC}}$ that follows the disabling of toggle mode, updates the outputs with the data contained in the A registers.

THERMAL MONITOR FUNCTION

The AD5384 contains a temperature shutdown function to protect the chip if multiple outputs are shorted. The short-circuit current of each output amplifier is typically 40 mA. Operating the AD5384 at 5 V leads to a power dissipation of 200 mW per shorted amplifier. With five channels shorted, this leads to an extra watt of power dissipation. For the 100-ball CSP_BGA, the θ_{JA} is typically 44°C/W.

Enable the thermal monitor via the CR8 bit in the control register. The output amplifiers on the AD5384 automatically power down if the die temperature exceeds approximately 130°C. After a thermal shutdown occurs, reenable the device by executing a soft power-up, if the temperature drops below 130°C, or by turning off the thermal monitor function via the control register.

AD5384 IN A MEMS-BASED OPTICAL SWITCH

In their feed-forward control paths, MEMS-based optical switches require high resolution DACs that offer high channel density with 14-bit monotonic behavior. The 40-channel, 14-bit AD5384 DAC satisfies these requirements. In the circuit in Figure 32, the 0 V to 5 V outputs of the AD5384 are amplified to achieve an output range of 0 V to 200 V, which is used to control actuators that determine the position of MEMS mirrors in an optical switch. The exact position of each mirror is measured using sensors. The sensor outputs are multiplexed into a high resolution ADC in determining the mirror position. The control loop is closed and driven by an ADSP-21065L, a 32-bit SHARC® DSP with an SPI-compatible SPORT interface. The ADSP-21065L writes data to the DAC, controls the multiplexer, and reads data from the ADC via the serial interface.

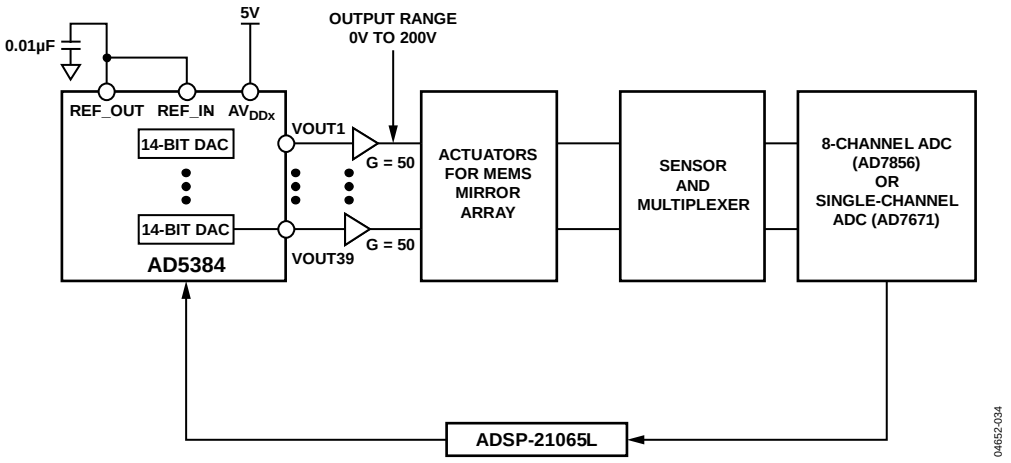

Figure 36. MEMS-Based Optical Switch

OPTICAL ATTENUATORS

Based on its high channel count, high resolution, monotonic behavior, and high level of integration, the AD5384 is ideally targeted at optical attenuation applications used in dynamic gain equalizers, variable optical attenuators (VOAs), and optical add-drop multiplexers (OADMs). In these applications, each wavelength is individually extracted using an arrayed wave guide; its power is monitored using a photodiode, transimpedance amplifier, and an ADC in a closed-loop control system.

The AD5384 controls the optical attenuator for each wavelength, ensuring that the power is equalized in all wavelengths before being multiplexed onto the fiber. Equalizing the power prevents information loss and saturation from occurring at amplification stages further along the fiber.

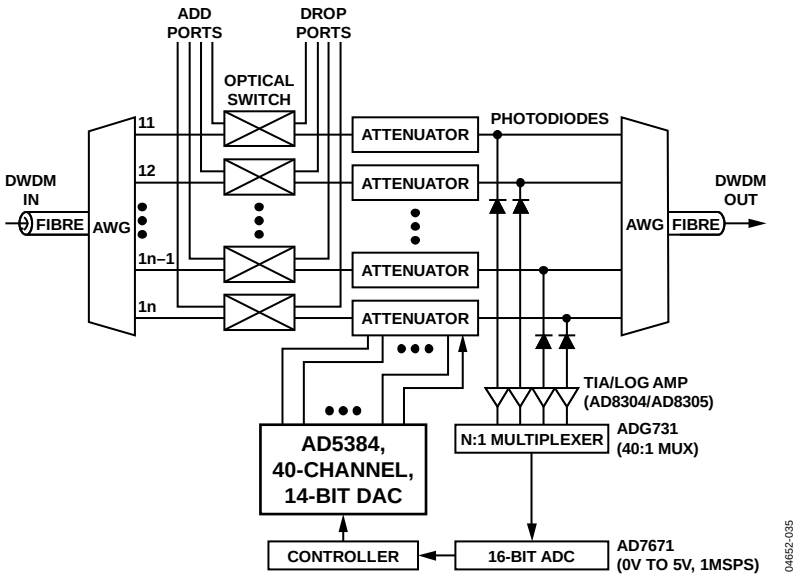

Figure 37. OADM Using the AD5384 as Part of an Optical Attenuator

OUTLINE DIMENSIONS

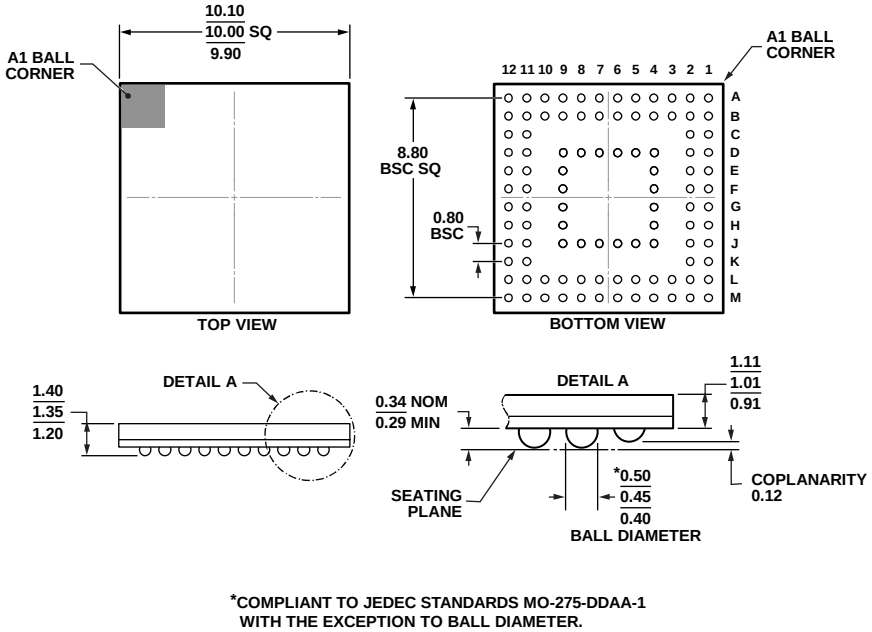

Figure 38. 100-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-100-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Resolution	Temperature Range	Output Channels	Linearity Error (LSB)	Package Description	Package Option
AD5384BBCZ-5	14 Bits	–40°C to +85°C	40	±4	100-Ball CSP_BGA	BC-100-2
AD5384BBCZ-5REEL7	14 Bits	–40°C to +85°C	40	±4	100-Ball CSP_BGA	BC-100-2

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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