THE DATASHEET OF

AD5629RACPZ-3-RL7

Octal, 12-/16-Bit, I²C, *dense*DACs with 5 ppm/°C On-Chip Reference

Data Sheet

AD5629R/AD5669R

FEATURES

- Low power octal DACs
  - AD5629R: 12 bits
  - AD5669R: 16 bits
- 2.6 mm × 2.6 mm 16-ball WLCSP
- 4 mm × 4 mm 16-lead LFCSP and 16-lead TSSOP
- On-chip 1.25 V/2.5 V, 5 ppm/°C reference
- Power down to 400 nA at 5 V, 200 nA at 3 V
- 2.7 V to 5.5 V power supply
- Guaranteed monotonic by design
- Power-on reset to zero scale or midscale
- 3 power-down functions
- Hardware $\overline{\text{LDAC}}$ and $\overline{\text{CLR}}$ functions
- I²C-compatible serial interface supports standard (100 kHz) and fast (400 kHz) modes

APPLICATIONS

- Process control
- Data acquisition systems
- Portable battery-powered instruments
- Digital gain and offset adjustment
- Programmable voltage and current sources

FUNCTIONAL BLOCK DIAGRAM

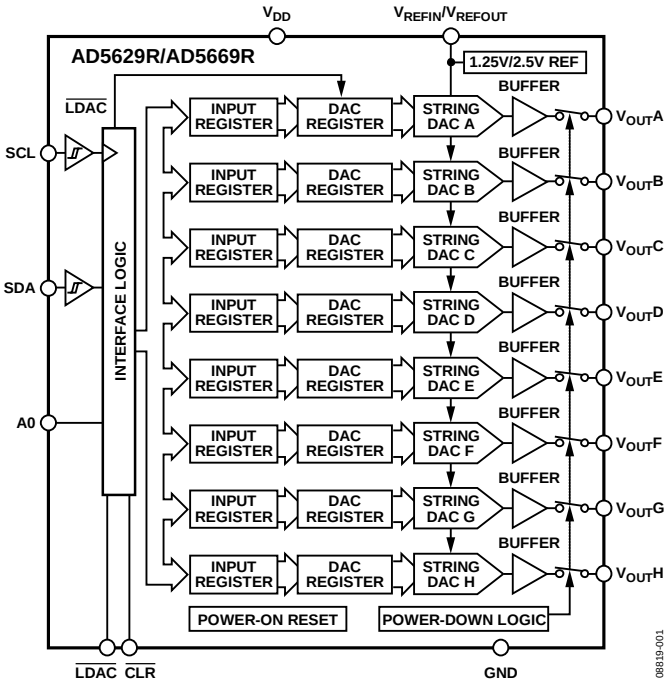

Figure 1.

GENERAL DESCRIPTION

The AD5629R/AD5669R devices are low power, octal, 12-/16-bit, buffered voltage-output DACs. All devices are guaranteed monotonic by design.

The AD5629R/AD5669R have an on-chip reference with an internal gain of 2. The AD5629R-1/AD5669R-1 have a 1.25 V, 5 ppm/°C reference, giving a full-scale output range of 2.5 V. The AD5629R-2/AD5629R-3 and the AD5669R-2/AD5669R-3 have a 2.5 V 5 ppm/°C reference, giving a full-scale output range of 5 V depending on the option selected. Devices with 1.25 V reference selected operate from a single 2.7 V to 5.5 V supply. Devices with 2.5 V reference selected operate from 4.5 V to 5.5 V. The on-chip reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a software write.

The parts incorporate a power-on reset circuit to ensure that the DAC output powers up to 0 V (AD5629R-1/AD5629R-2, AD5669R-1/AD5669R-2) or midscale (AD5629R-3/AD5669R-3) and remains powered up at this level until a valid write takes place. The part contains a power-down feature that reduces the current consumption of the device to 400 nA at 5 V and provides software-selectable output loads while in power-down mode for any or all DAC channels.

PRODUCT HIGHLIGHTS

1. Octal, 12-/16-bit DACs.
2. On-chip 1.25 V/2.5 V, 5 ppm/°C reference.
3. Available in 16-lead LFCSP and TSSOP, and 16-ball WLCSP.
4. Power-on reset to 0 V or midscale.
5. Power-down capability. When powered down, the DAC typically consumes 200 nA at 3 V and 400 nA at 5 V.

Rev. F
Document Feedback

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10/2010—Revision 0: Initial Version

SPECIFICATIONS

V_{DD} = 4.5 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
STATIC PERFORMANCE[2]								
AD5629R								
Resolution	12			12			Bits	
Relative Accuracy		±0.5	±4		±0.5	±1	LSB	See Figure 7
Differential Nonlinearity			±0.25			±0.25	LSB	Guaranteed monotonic by design (see Figure 9)
AD5669R								
Resolution	16			16			Bits	
Relative Accuracy		±8	±32		±8	±16	LSB	See Figure 6
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 8)
Zero-Code Error		6	19		6	19	mV	All 0s loaded to DAC register (see Figure 19)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 20)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±6	±19		±6	±19	mV	
DC Power Supply Rejection Ratio		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 5 V
Power-Up Time		4			4		µs	Coming out of power-down mode, V_{DD} = 5 V
REFERENCE INPUTS								
Reference Current		40	50		40	50	µA	V_{REFIN} = V_{DD} = 5.5 V (per DAC channel)
Reference Input Range	0		V_{DD}	0		V_{DD}	V	
Reference Input Impedance		14.6			14.6		kΩ	
REFERENCE OUTPUT (1.25 V)								
Output Voltage	1.247		1.253	1.247		1.253	µA	T_A = 25°C
Reference Input Range		±15			±5	±15	ppm/°C	LFCSP, TSSOP
					±15			WLCSP
Output Impedance		7.5			7.5		kΩ	
REFERENCE OUTPUT (2.5 V)								
Output Voltage	2.495		2.505	2.495		2.505	µA	T_A = 25°C
Reference Input Range		±15			±5	±10	ppm/°C	
Output Impedance		7.5			7.5		kΩ	

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Test Conditions/Comments
LOGIC INPUTS[3]								
Input Current			±3			±3	μA	All digital inputs
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 5 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 5 V
Pin Capacitance		3			3		pF	
POWER REQUIREMENTS								
V_{DD}	4.5		5.5	4.5		5.5	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 4.5 V to 5.5 V		1.3	1.8		1.3	1.8	mA	Internal reference off
		2	2.5		2	2.5	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 4.5 V to 5.5 V		0.4	1		0.4	1	μA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of the AD5629R (Code 32 to Code 4064) and the AD5669R (Code 512 to 65,024). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All eight DACs powered down.

V_{DD} = 2.7 V to 3.6 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, V_{REFIN} = V_{DD}. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	A Grade[1] Min	A Grade[1] Typ	A Grade[1] Max	B Grade[1] Min	B Grade[1] Typ	B Grade[1] Max	Unit	Conditions/Comments
STATIC PERFORMANCE[2]								
AD5629R								
Resolution	12			12			Bits	
Relative Accuracy		±0.5	±4		±0.5	±1	LSB	See Figure 7
Differential Nonlinearity			±0.25			±0.25	LSB	Guaranteed monotonic by design (see Figure 9)
AD5669R								
Resolution	16			16			Bits	
Relative Accuracy		±8	±32		±8	±16	LSB	See Figure 6
Differential Nonlinearity			±1			±1	LSB	Guaranteed monotonic by design (see Figure 8)
Zero-Code Error		6	19		6	19	mV	All 0s loaded to DAC register (see Figure 19)
Zero-Code Error Drift		±2			±2		µV/°C	
Full-Scale Error		−0.2	−1		−0.2	−1	% FSR	All 1s loaded to DAC register (see Figure 20)
Gain Error			±1			±1	% FSR	
Gain Temperature Coefficient		±2.5			±2.5		ppm	Of FSR/°C
Offset Error		±6	±19		±6	±19	mV	
DC Power Supply Rejection Ratio		−80			−80		dB	V_{DD} ± 10%
DC Crosstalk (External Reference)		10			10		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		5			5		µV/mA	Due to load current change
		10			10		µV	Due to powering down (per channel)
DC Crosstalk (Internal Reference)		25			25		µV	Due to full-scale output change, R_L = 2 kΩ to GND or V_{DD}
		10			10		µV/mA	Due to load current change
OUTPUT CHARACTERISTICS[3]								
Output Voltage Range	0		V_{DD}	0		V_{DD}	V	
Capacitive Load Stability		2			2		nF	R_L = ∞
		10			10		nF	R_L = 2 kΩ
DC Output Impedance		0.5			0.5		Ω	
Short-Circuit Current		30			30		mA	V_{DD} = 3 V
Power-Up Time		4			4		µs	Coming out of power-down mode, V_{DD} = 3 V
REFERENCE INPUTS								
Reference Current		40	50		40	50	µA	V_{REFIN} = V_{DD} = 3.6 V (per DAC channel)
Reference Input Range	0		V_{DD}	0		V_{DD}		
Reference Input Impedance		14.6			14.6		kΩ	
REFERENCE OUTPUT								
Output Voltage								
AD5629R/AD5669R	1.247		1.253	1.247		1.253	V	T_A = 25°C
Reference Tempco[3]		±15			±5	±15	ppm/°C	LFCSP, TSSOP
					±15			WLCSP
Reference Output Impedance		7.5			7.5		kΩ	
LOGIC INPUTS[3]								
Input Current			±3			±3	µA	All digital inputs
Input Low Voltage, V_{INL}			0.8			0.8	V	V_{DD} = 3 V
Input High Voltage, V_{INH}	2			2			V	V_{DD} = 3 V
Pin Capacitance		3			3		pF	

Parameter	A Grade[1] Min	Typ	Max	B Grade[1] Min	Typ	Max	Unit	Conditions/Comments
POWER REQUIREMENTS								
V_{DD}	2.7		3.6	2.7		3.6	V	All digital inputs at 0 or V_{DD}, DAC active, excludes load current
I_{DD} (Normal Mode)[4]								$V_{IH} = V_{DD}$ and V_{IL} = GND
V_{DD} = 2.7 V to 3.6 V		1.0	1.5		1.0	1.5	mA	Internal reference off
		1.8	2.25		1.7	2.25	mA	Internal reference on
I_{DD} (All Power-Down Modes)[5]								
V_{DD} = 2.7 V to 3.6 V		0.2	1		0.2	1	µA	$V_{IH} = V_{DD}$ and V_{IL} = GND

[1] Temperature range is −40°C to +105°C, typical at 25°C.
[2] Linearity calculated using a reduced code range of the AD5629R (Code 32 to Code 4064) and the AD5669R (Code 512 to 65,024). Output unloaded.
[3] Guaranteed by design and characterization; not production tested.
[4] Interface inactive. All DACs active. DAC outputs unloaded.
[5] All eight DACs powered down.

AC CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V, R_L = 2 kΩ to GND, C_L = 200 pF to GND, $V_{REFIN} = V_{DD}$. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 3.

Parameter[1, 2]	Min	Typ	Max	Unit	Conditions/Comments[3]
Output Voltage Settling Time		2.5	7	µs	¼ to ¾ scale settling to ±2 LSB
Slew Rate		1.2		V/µs	
Digital-to-Analog Glitch Impulse		4		nV-s	1 LSB change around major carry (see Figure 35)
		19		nV-s	From Code 59904 to Code 59903
Digital Feedthrough		0.1		nV-s	
Reference Feedthrough		−90		dB	V_{REFIN} = 2 V ± 0.1 V p-p, frequency = 10 Hz to 20 MHz
Digital Crosstalk		0.2		nV-s	
Analog Crosstalk		0.4		nV-s	
DAC-to-DAC Crosstalk		0.8		nV-s	
Multiplying Bandwidth		320		kHz	V_{REFIN} = 2 V ± 0.2 V p-p
Total Harmonic Distortion		−80		dB	V_{REFIN} = 2 V ± 0.1 V p-p, frequency = 10 kHz
Output Noise Spectral Density		120		nV/√Hz	DAC code = 0x8400, 1 kHz
		100		nV/√Hz	DAC code = 0x8400, 10 kHz

[1] Guaranteed by design and characterization; not production tested.
[2] See the Terminology section.
[3] Temperature range is −40°C to +105°C, typical at 25°C.

I²C TIMING CHARACTERISTICS

V_{DD} = 2.7 V to 5.5 V; all specifications T_{MIN} to T_{MAX}, f_{SCL} = 400 kHz, unless otherwise noted.

Table 4.

Parameter	Conditions	Min	Max	Unit	Description
f_{SCL}[1]	Standard mode		100	kHz	Serial clock frequency
	Fast mode		400	kHz	
t_1	Standard mode	4		µs	t_{HIGH}, SCL high time
	Fast mode	0.6		µs	
t_2	Standard mode	4.7		µs	t_{LOW}, SCL low time
	Fast mode	1.3		µs	
t_3	Standard mode	250		ns	$t_{SU;DAT}$, data setup time
	Fast mode	100		ns	
t_4	Standard mode	0	3.45	µs	$t_{HD;DAT}$, data hold time
	Fast mode	0	0.9	µs	
t_5	Standard mode	4.7		µs	$t_{SU;STA}$, setup time for a repeated start condition
	Fast mode	0.6		µs	
t_6	Standard mode	4		µs	$t_{HD;STA}$, hold time (repeated) start condition
	Fast mode	0.6		µs	
t_7	Standard mode	4.7		µs	t_{BUF}, bus-free time between a stop and a start condition
	Fast mode	1.3		µs	
t_8	Standard mode	4		µs	$t_{SU;STO}$, setup time for a stop condition
	Fast mode	0.6		µs	
t_9	Standard mode		1000	ns	t_{RDA}, rise time of SDA signal
	Fast mode		300	ns	
t_{10}	Standard mode		300	ns	t_{FDA}, fall time of SDA signal
	Fast mode		300	ns	
t_{11}	Standard mode		1000	ns	t_{RCL}, rise time of SCL signal
	Fast mode		300	ns	
t_{11A}	Standard mode		1000	ns	t_{RCL1}, rise time of SCL signal after a repeated start condition and after an acknowledge bit
	Fast mode		300	ns	
t_{12}	Standard mode		300	ns	t_{FCL}, fall time of SCL signal
	Fast mode		300	ns	
t_{13}	Standard mode	10		ns	$\overline{\text{LDAC}}$ pulse width low
	Fast mode	10		ns	
t_{14}	Standard mode	300		ns	Falling edge of ninth SCL clock pulse of last byte of a valid write to the $\overline{\text{LDAC}}$ falling edge
	Fast mode	300		ns	
t_{15}	Standard mode	20		ns	$\overline{\text{CLR}}$ pulse width low
	Fast mode	20		ns	
t_{SP}[2]	Fast mode	0	50	ns	Pulse width of spike suppressed

[1] The SDA and SCL timing is measured with the input filters enabled. Switching off the input filters improves the transfer rate but has a negative effect on the EMC behavior of the part.
[2] Input filtering on the SCL and SDA inputs suppresses noise spikes that are less than 50 ns for fast mode or less than 10 ns for high speed mode.

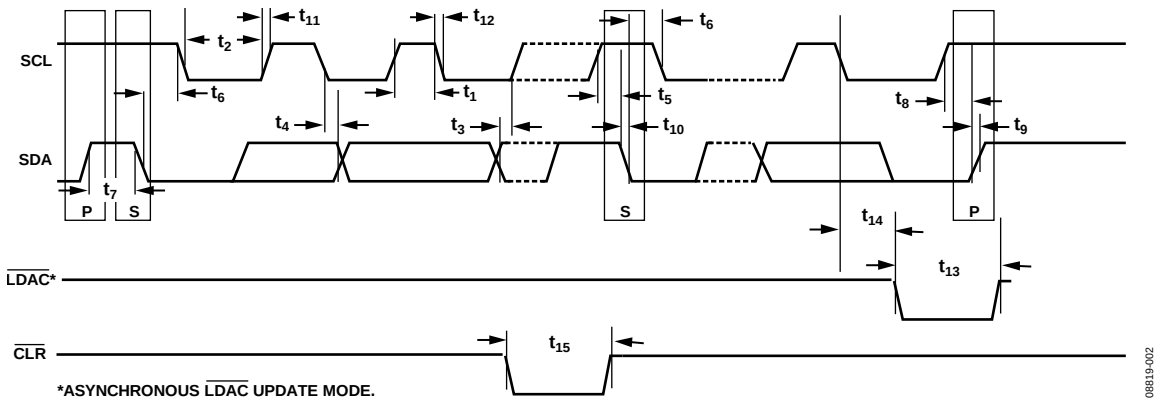


Figure 2. Serial Write Operation

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 5.

Parameter	Rating
V_{DD} to GND	−0.3 V to +7 V
Digital Input Voltage to GND	−0.3 V to V_{DD} + 0.3 V
V_{OUT} to GND	−0.3 V to V_{DD} + 0.3 V
V_{REFIN}/V_{REFOUT} to GND	−0.3 V to V_{DD} + 0.3 V
Operating Temperature Range	
Industrial	−40°C to +105°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature ($T_{J\ MAX}$)	+150°C
Power Dissipation	$(T_{J\ MAX} - T_A)/\theta_{JA}$
Thermal Impedance, θ_{JA}	
16-Lead TSSOP (4-Layer Board)	112.6°C/W
16-Lead LFCSP (4-Layer Board)	30.4°C/W
Reflow Soldering Peak Temperature	
Pb Free	260°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

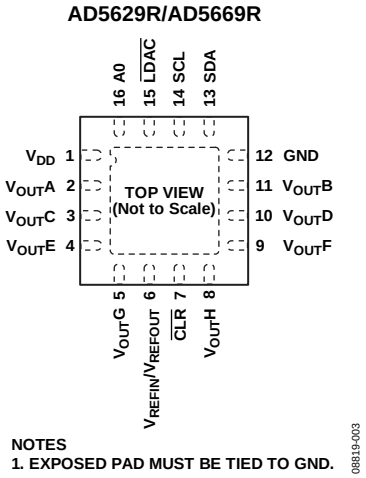


Figure 3. 16-Lead LFCSP (CP-16-17)

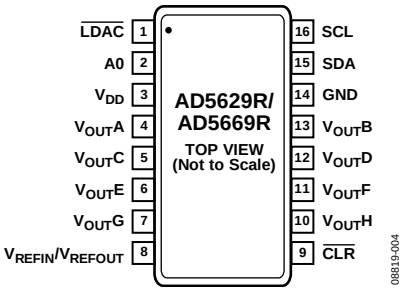


Figure 4. 16-Lead TSSOP (RU-16)

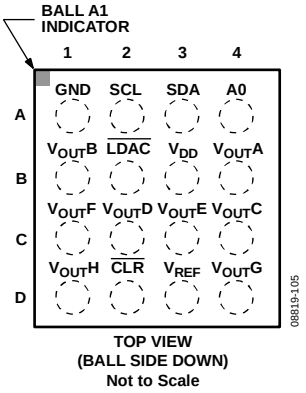


Figure 5. 16-Ball WLCSP

Table 6. Pin Function Descriptions

Pin No.				
LFCSP	**TSSOP**	**WLCSP**	**Mnemonic**	**Description**
15	1	B2	$\overline{\text{LDAC}}$	Pulsing this pin low allows any or all DAC registers to be updated if the input registers have new data. This allows all DAC outputs to simultaneously update. Alternatively, this pin can be tied permanently low.
16	2	A4	A0	Address Input. Sets the least significant bit of the 7-bit slave address.
1	3	B3	V_{DD}	Power Supply Input. These parts can be operated from 2.7 V to 5.5 V. Decouple the supply with a 10 µF capacitor in parallel with a 0.1 µF capacitor to GND.
2	4	B4	$V_{OUT}A$	Analog Output Voltage from DAC A. The output amplifier has rail-to-rail operation.
3	5	C4	$V_{OUT}C$	Analog Output Voltage from DAC C. The output amplifier has rail-to-rail operation.
4	6	C3	$V_{OUT}E$	Analog Output Voltage from DAC E. The output amplifier has rail-to-rail operation.
5	7	D4	$V_{OUT}G$	Analog Output Voltage from DAC G. The output amplifier has rail-to-rail operation.
6	8	D3	V_{REFIN}/V_{REFOUT}	The AD5629R/AD5669R have a common pin for reference input and reference output. When using the internal reference, this is the reference output pin. When using an external reference, this is the reference input pin. The default for this pin is as a reference input.
7	9	D2	$\overline{\text{CLR}}$	Asynchronous Clear Input. The $\overline{\text{CLR}}$ input is falling edge sensitive. When $\overline{\text{CLR}}$ is low, all $\overline{\text{LDAC}}$ pulses are ignored. When $\overline{\text{CLR}}$ is activated, the input register and the DAC register are updated with the data contained in the $\overline{\text{CLR}}$ code register—zero scale, midscale, or full scale. The default setting clears the output to 0 V.
8	10	D1	$V_{OUT}H$	Analog Output Voltage from DAC H. The output amplifier has rail-to-rail operation.
9	11	C1	$V_{OUT}F$	Analog Output Voltage from DAC F. The output amplifier has rail-to-rail operation.
10	12	C2	$V_{OUT}D$	Analog Output Voltage from DAC D. The output amplifier has rail-to-rail operation.
11	13	B1	$V_{OUT}B$	Analog Output Voltage from DAC B. The output amplifier has rail-to-rail operation.
12	14	A1	GND	Ground Reference Point for All Circuitry on the Parts.
13	15	A3	SDA	Serial Data Input. This is used in conjunction with the SCL line to clock data into or out of the 32-bit input shift register. It is a bidirectional, open-drain data line that should be pulled to the supply with an external pull-up resistor.
14	16	A2	SCL	Serial Clock Line. This is used in conjunction with the SDA line to clock data into or out of the 32-bit input shift register.
17	N/A	N/A	Exposed Pad (EPAD)	The exposed pad must be tied to GND.

TYPICAL PERFORMANCE CHARACTERISTICS

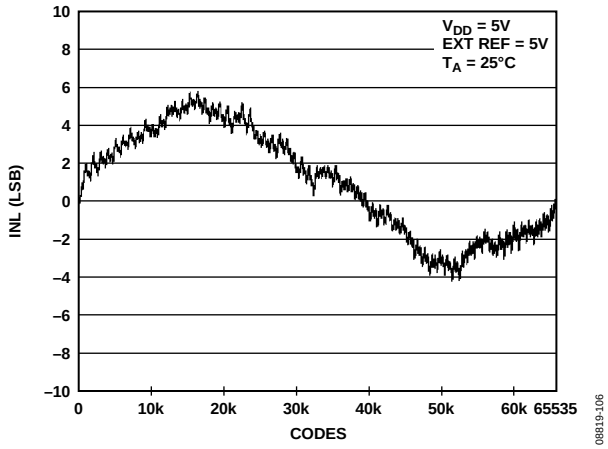


Figure 6. INL AD5669R—External Reference

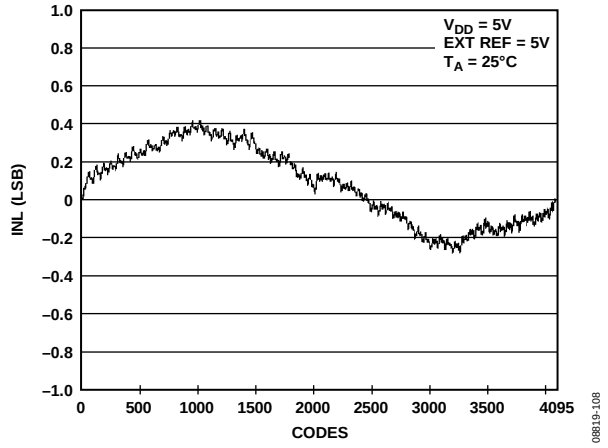


Figure 7. INL AD5629R—External Reference

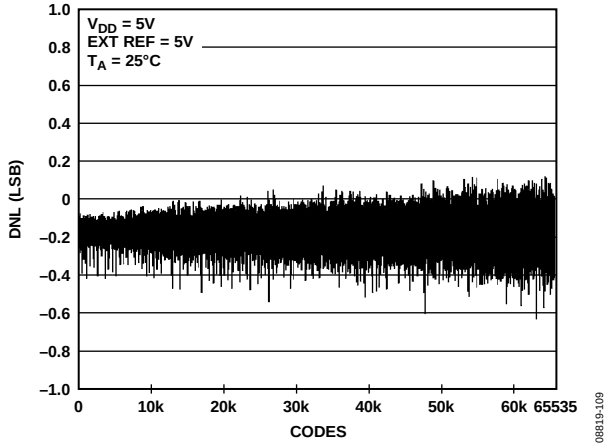


Figure 8. DNL AD5669R—External Reference

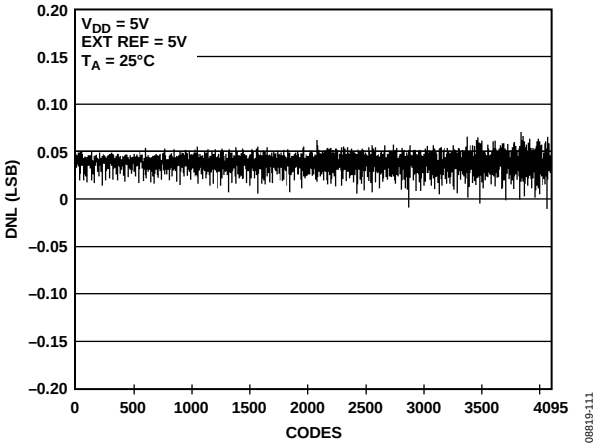


Figure 9. DNL AD5629R—External Reference

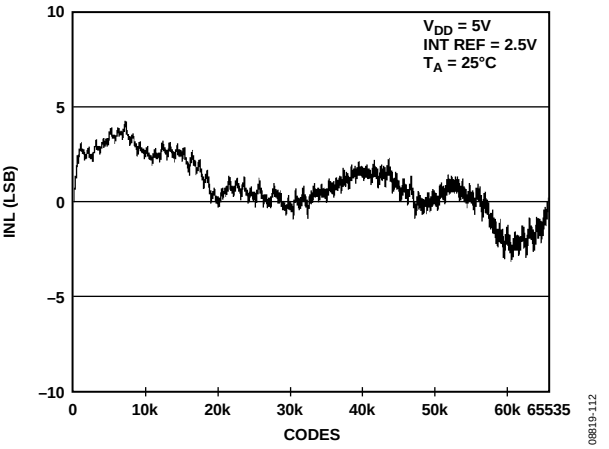


Figure 10. INL AD5669R-2—Internal Reference

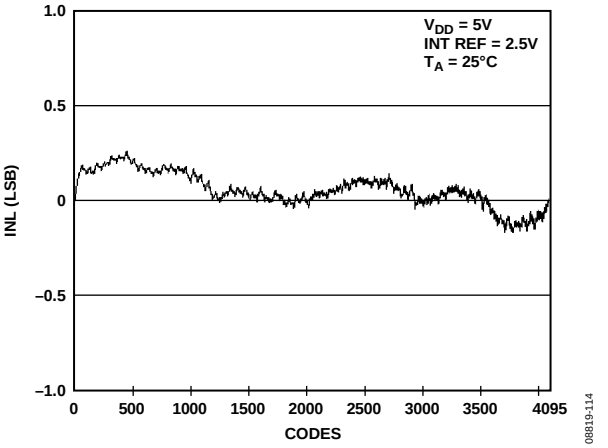


Figure 11. INL AD5629R-2—Internal Reference

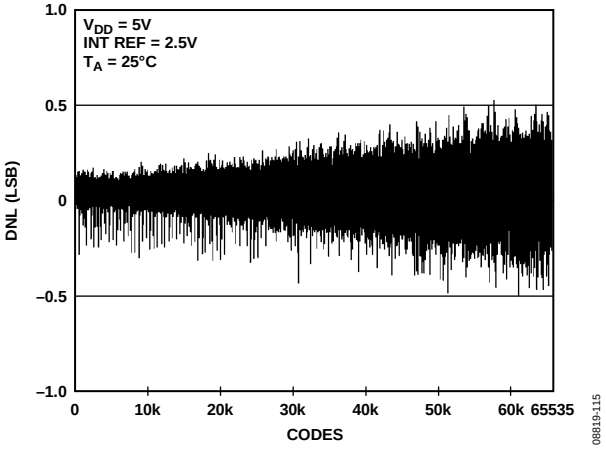


Figure 12. DNL AD5669R-2—Internal Reference

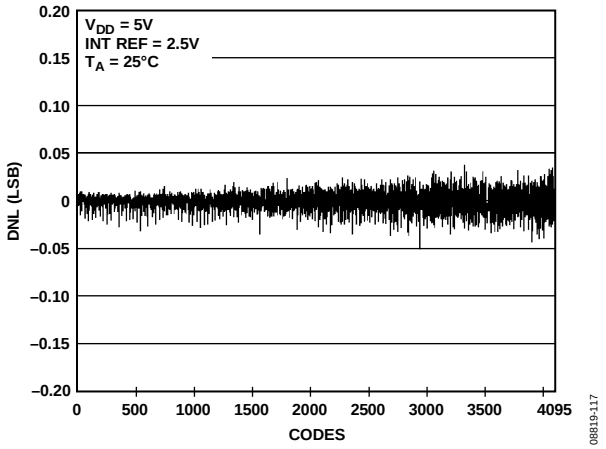


Figure 13. DNL AD5629R-2—Internal Reference

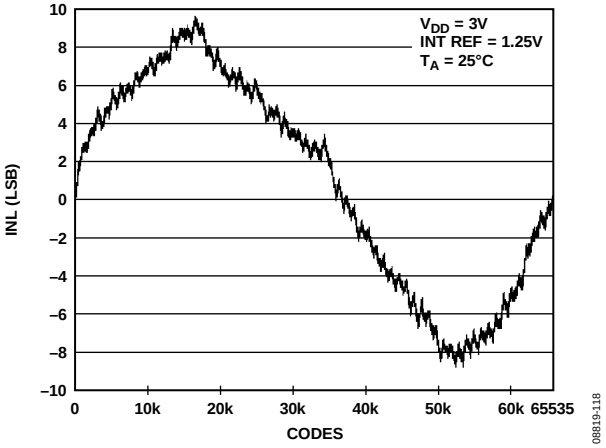


Figure 14. INL AD5669R-1—Internal Reference

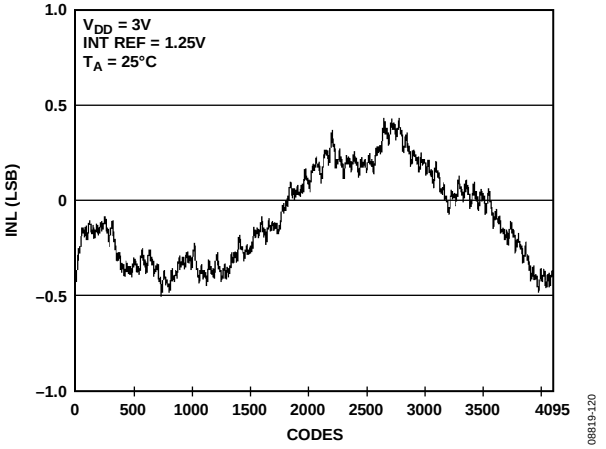


Figure 15. INL AD5629R-1—Internal Reference

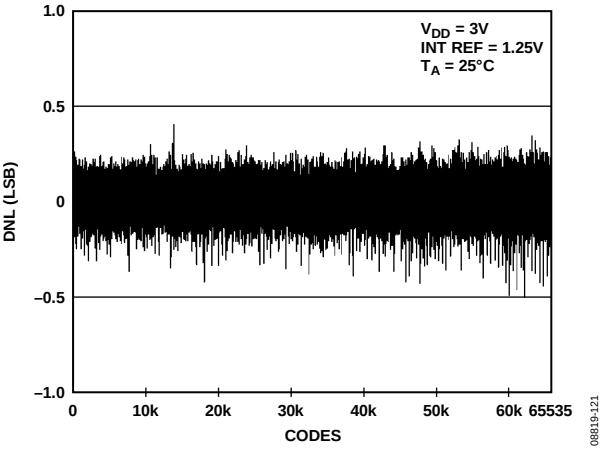


Figure 16. DNL AD5669R-1—Internal Reference

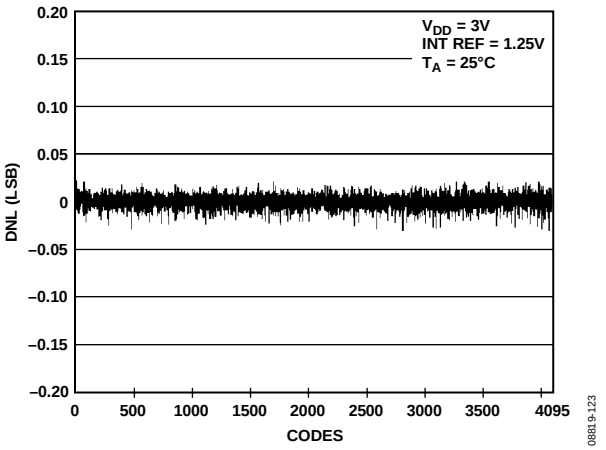


Figure 17. DNL AD5629R-1—Internal Reference

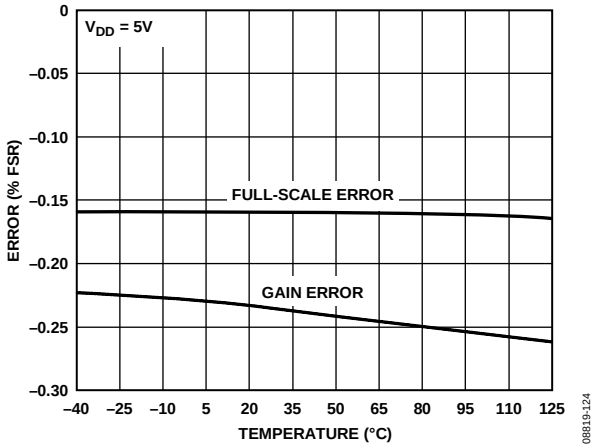


Figure 18. Gain Error and Full-Scale Error vs. Temperature

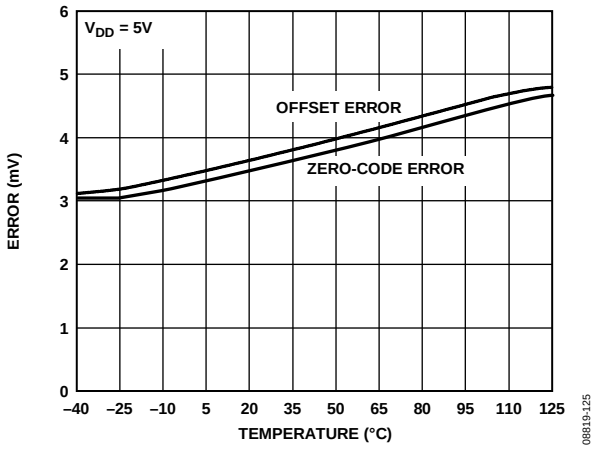


Figure 19. Zero-Code Error and Offset Error vs. Temperature

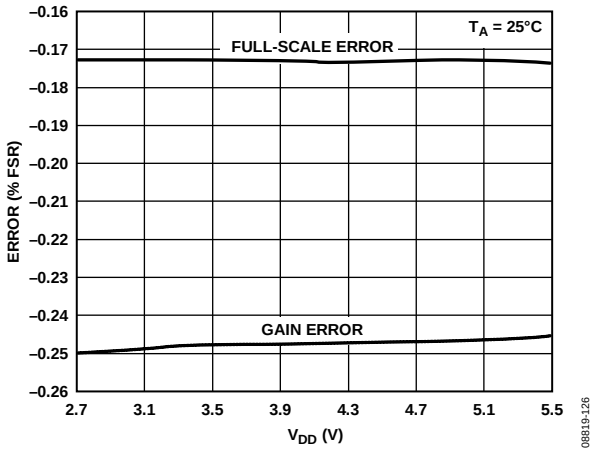


Figure 20. Gain Error and Full-Scale Error vs. Supply Voltage

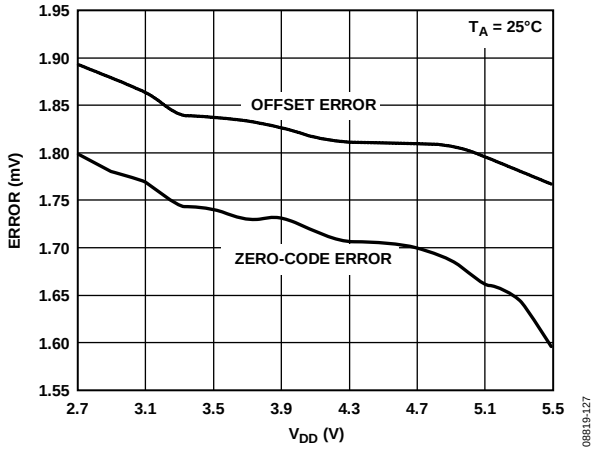


Figure 21. Zero-Code Error and Offset Error vs. Supply Voltage

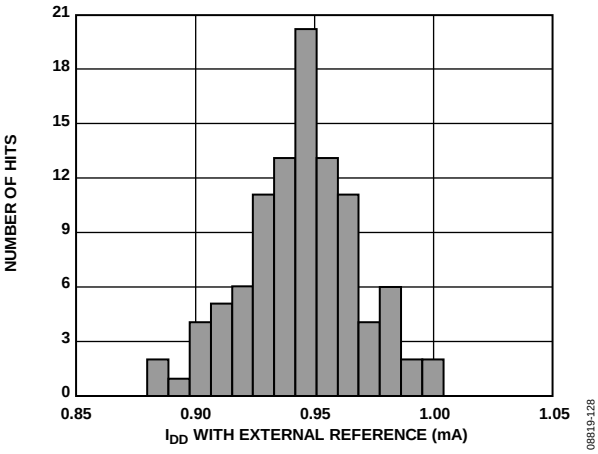


Figure 22. IDD Histogram with External Reference

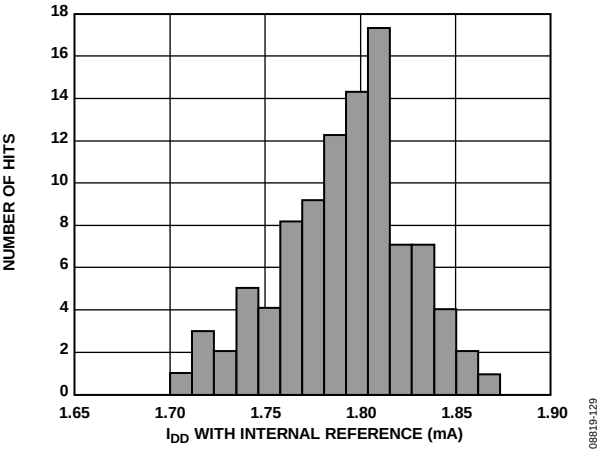


Figure 23. IDD Histogram with Internal Reference

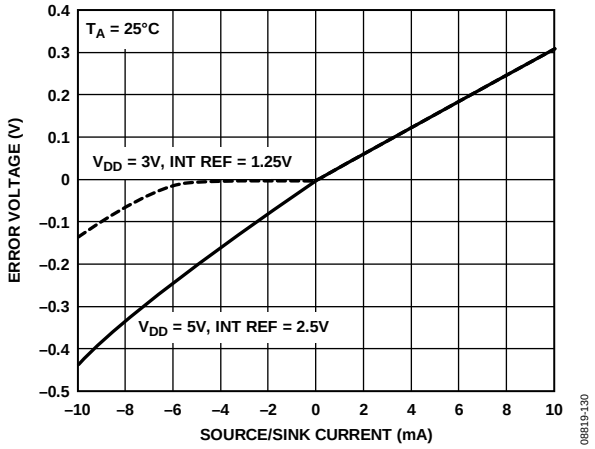


Figure 24. Headroom at Rails vs. Source and Sink

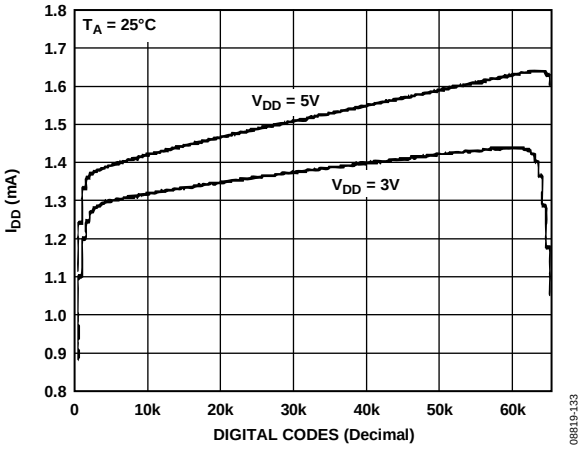


Figure 27. Supply Current vs. Code

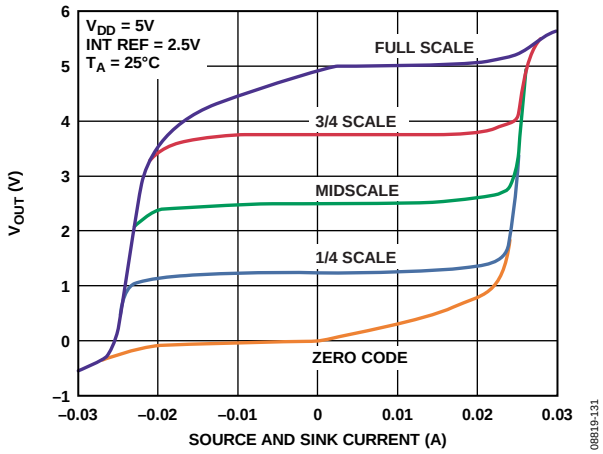


Figure 25. AD5669R-2 Source and Sink Capability

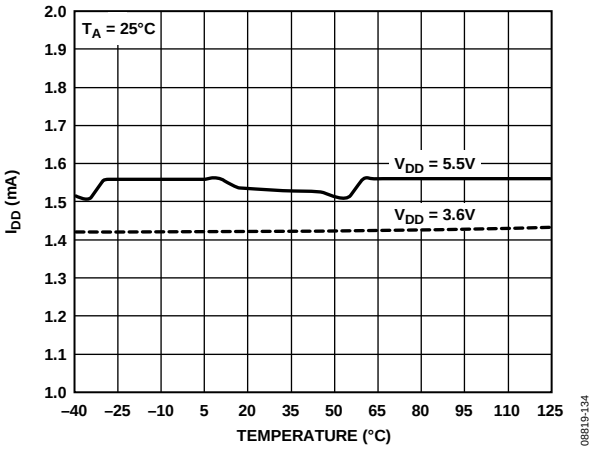


Figure 28. Supply Current vs. Temperature

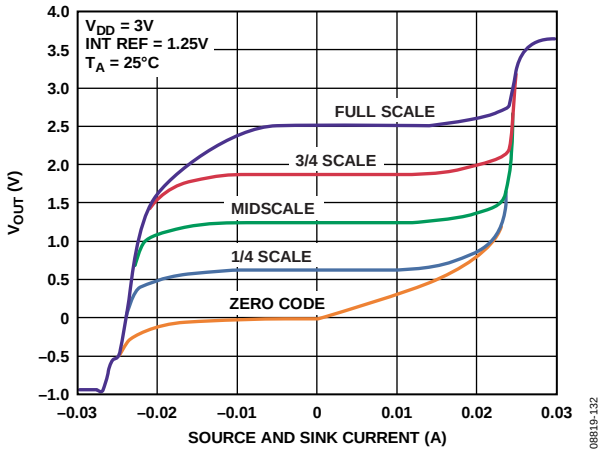


Figure 26. AD5669R-1 Source and Sink Capability

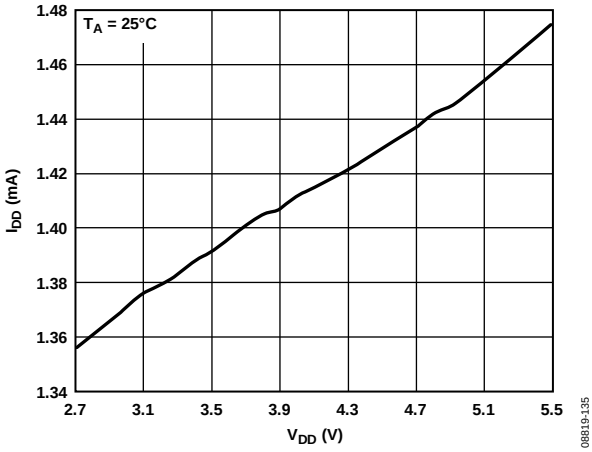


Figure 29. Supply Current vs. Supply Voltage

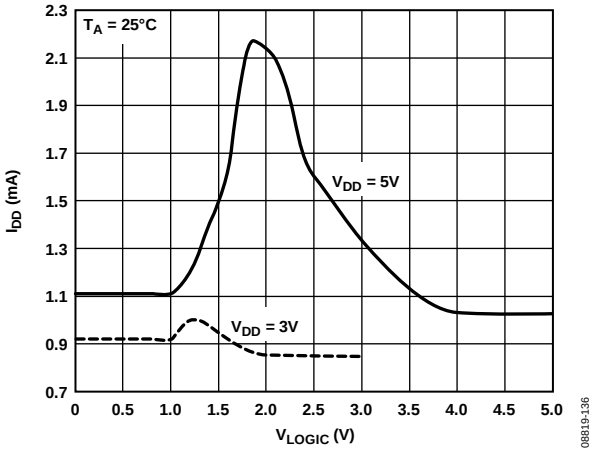


Figure 30. Supply Current vs. Logic Input Voltage

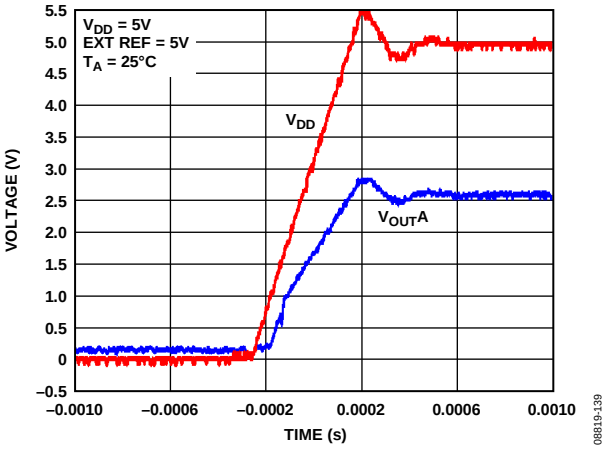


Figure 33. Power-On Reset to Midscale

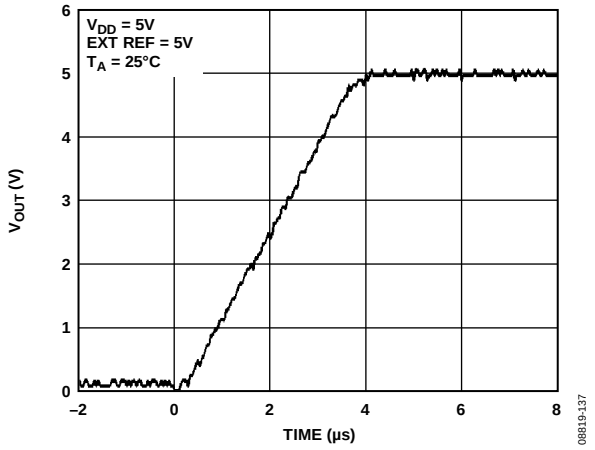


Figure 31. Full-Scale Settling Time, 5 V

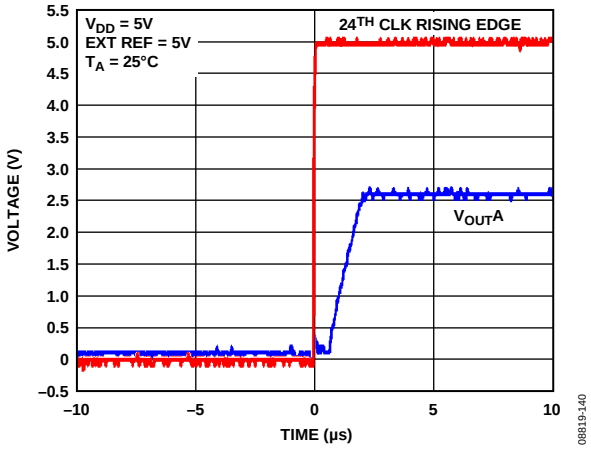


Figure 34. Exiting Power-Down to Midscale

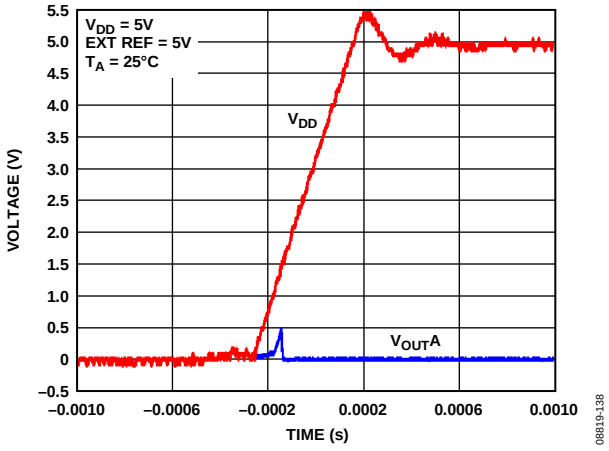


Figure 32. Power-On Reset to 0 V

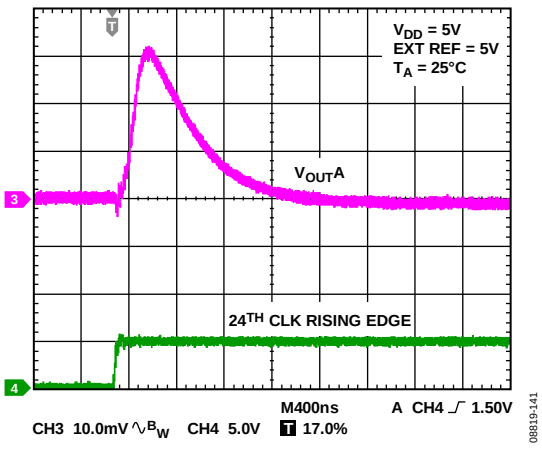


Figure 35. Digital-to-Analog Glitch Impulse (Negative)

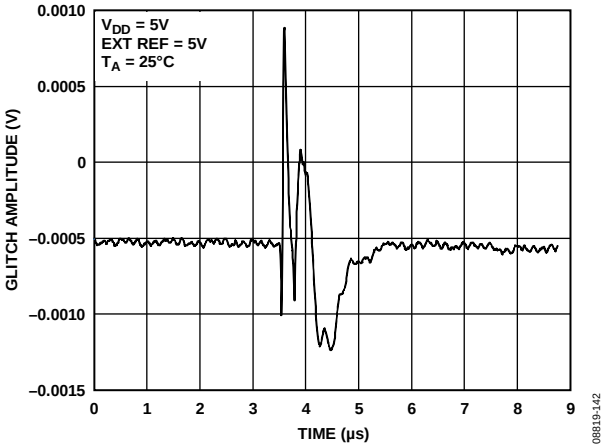


Figure 36. Analog Crosstalk

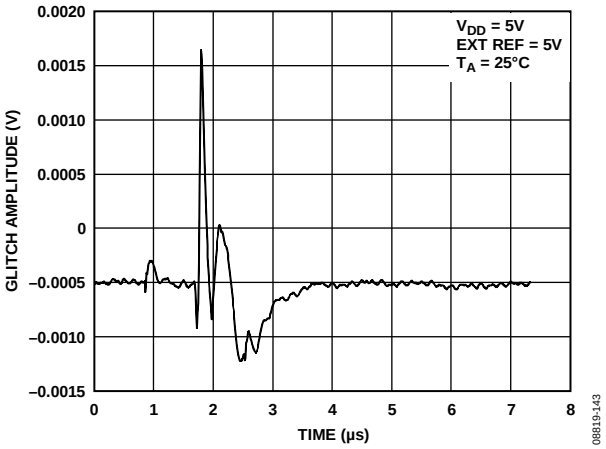


Figure 37. DAC-to-DAC Crosstalk

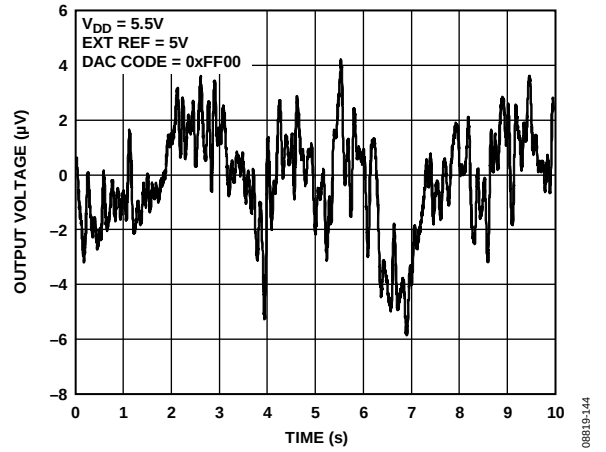


Figure 38. 0.1 Hz to 10 Hz Output Noise Plot, External Reference

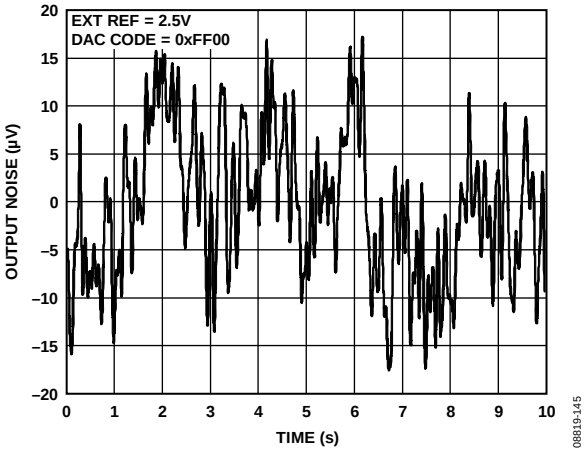


Figure 39. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

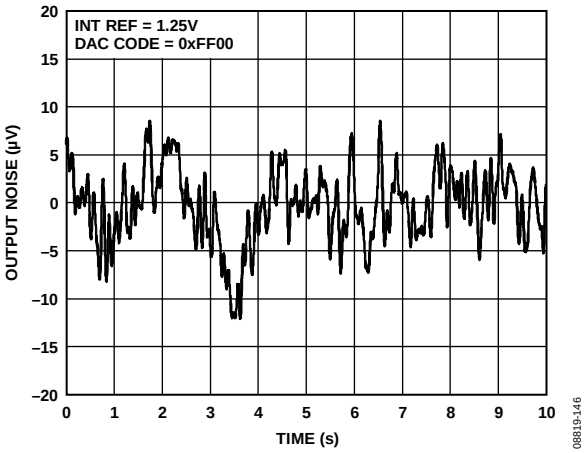


Figure 40. 0.1 Hz to 10 Hz Output Noise Plot, Internal Reference

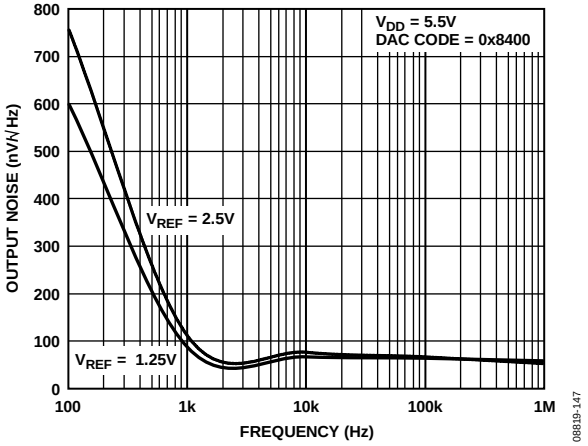


Figure 41. Noise Spectral Density, Internal Reference

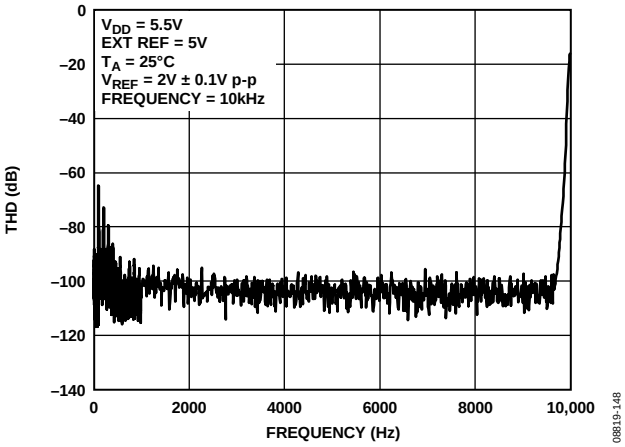


Figure 42. Total Harmonic Distortion

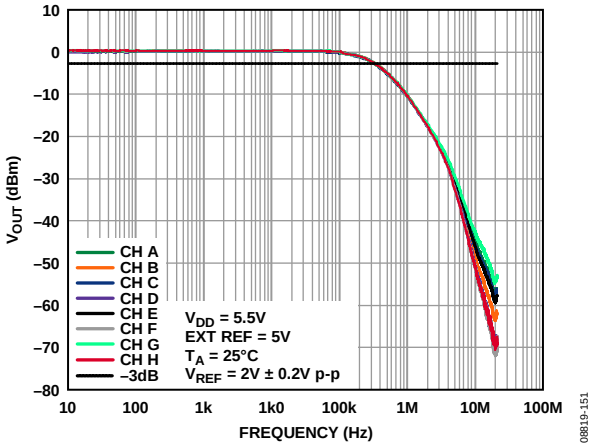


Figure 45. Multiplying Bandwidth

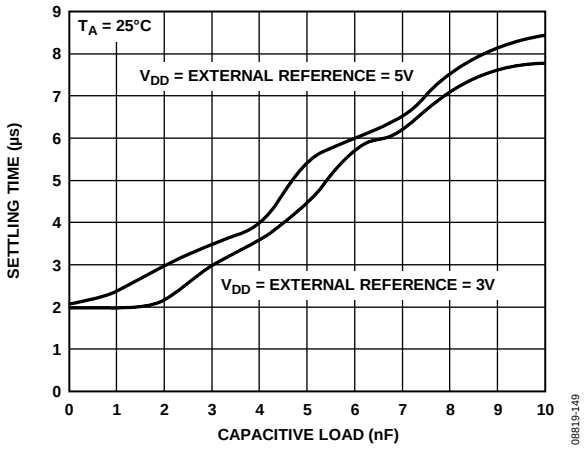


Figure 43. Settling Time vs. Capacitive Load

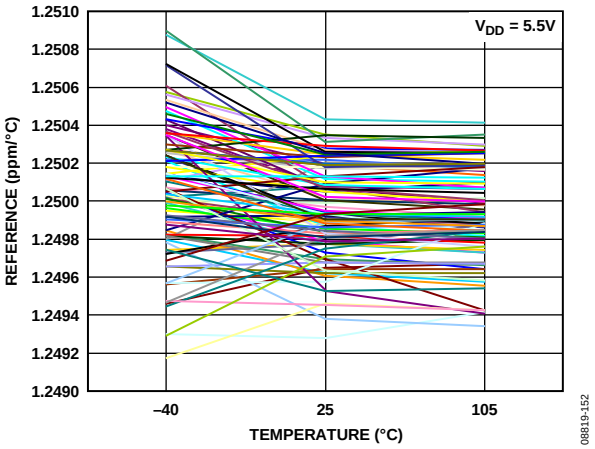


Figure 46. 1.25 V Reference Temperature Coefficient vs. Temperature

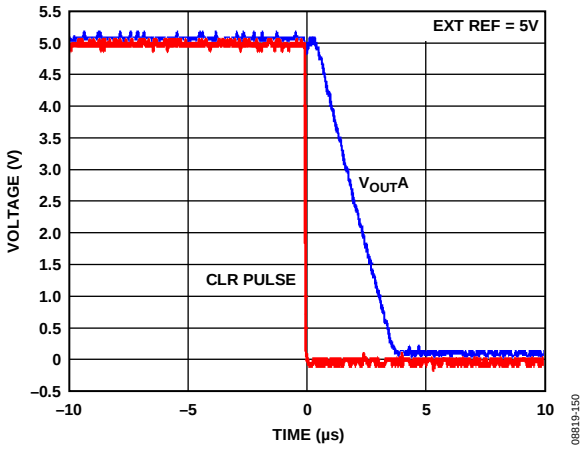


Figure 44. Hardware $\overline{CLR}$

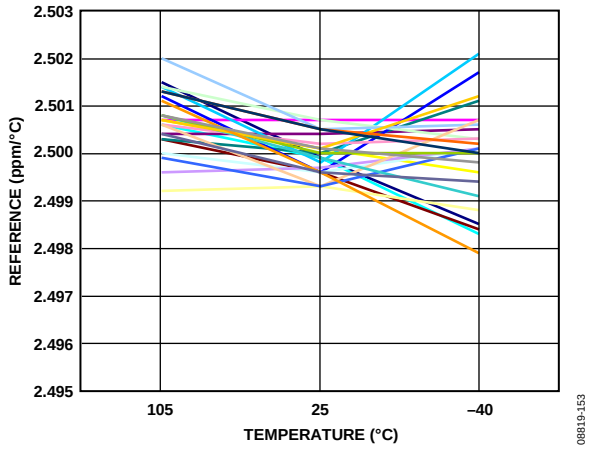


Figure 47. 2.5 V Reference Temperature Coefficient vs. Temperature

TERMINOLOGY

Relative Accuracy
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation in LSBs from a straight line passing through the endpoints of the DAC transfer function. Figure 6, Figure 7, Figure 10, Figure 11, Figure 14, and Figure 15 show plots of typical INL vs. code.

Differential Nonlinearity
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. Figure 8, Figure 9, Figure 12, Figure 13, Figure 16, and Figure 17 show plots of typical DNL vs. code.

Offset Error
Offset error is a measure of the difference between the actual V_{OUT} and the ideal V_{OUT}, expressed in millivolts in the linear region of the transfer function. Offset error is measured on the AD5669R between Code 512 and Code 65024 loaded into the DAC register. It can be negative or positive and is expressed in millivolts.

Zero-Code Error
Zero-code error is a measure of the output error when zero code (0x0000) is loaded into the DAC register. Ideally, the output should be 0 V. The zero-code error is always positive because the output of the DAC cannot go below 0 V. It is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in millivolts. Figure 19 shows a plot of typical zero-code error vs. temperature.

Gain Error
Gain error is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percentage of the full-scale range.

Zero-Code Error Drift
Zero-code error drift is a measure of the change in zero-code error with a change in temperature. It is expressed in µV/°C.

Gain Error Drift
Gain error drift is a measure of the change in gain error with changes in temperature. It is expressed in (ppm of full-scale range)/°C.

Full-Scale Error
Full-scale error is a measure of the output error when full-scale code (0xFFFF) is loaded into the DAC register. Ideally, the output should be V_{REF} − 1 LSB. Full-scale error is expressed as a percentage of the full-scale range. Figure 18 shows a plot of typical full-scale error vs. temperature.

Digital-to-Analog Glitch Impulse
Digital-to-analog glitch impulse is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nV-s and is measured when the digital input code is changed by 1 LSB at the major carry transition (0x7FFF to 0x8000). Figure 35 shows a typical digital-to-analog glitch impulse plot.

DC Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the supply voltage. PSRR is the ratio of the change in V_{OUT} to a change in V_{DD} for full-scale output of the DAC. V_{REF} is held at 2 V, and V_{DD} is varied ±10%. It is measured in decibels.

DC Crosstalk
DC crosstalk is the dc change in the output level of one DAC in response to a change in the output of another DAC. It is measured with a full-scale output change on one DAC (or soft power-down and power-up) while monitoring another DAC kept at midscale. It is expressed in microvolts.

DC crosstalk due to load current change is a measure of the impact that a change in load current on one DAC has on another DAC kept at midscale. It is expressed in microvolts per milliamp.

Digital Feedthrough
Digital feedthrough is a measure of the impulse injected into the analog output of a DAC from the digital input pins of the device, but is measured when the DAC is not being written to. It is specified in nV-s and measured with a full-scale change on the digital input pins, that is, from all 0s to all 1s or vice versa.

Digital Crosstalk
Digital crosstalk is the glitch impulse transferred to the output of one DAC at midscale in response to a full-scale code change (all 0s to all 1s or vice versa) in the input register of another DAC. It is measured in standalone mode and is expressed in nV-s.

Analog Crosstalk
Analog crosstalk is the glitch impulse transferred to the output of one DAC due to a change in the output of another DAC. It is measured by loading one of the input registers with a full-scale code change (all 0s to all 1s or vice versa) while keeping $\overline{\text{LDAC}}$ high and then pulsing $\overline{\text{LDAC}}$ low and monitoring the output of the DAC whose digital code has not changed. The area of the glitch is expressed in nV-s.

DAC-to-DAC Crosstalk
DAC-to-DAC crosstalk is the glitch impulse transferred to the output of one DAC due to a digital code change and subsequent output change of another DAC. This includes both digital and analog crosstalk. It is measured by loading one of the DACs with a full-scale code change (all 0s to all 1s or vice versa) with $\overline{\text{LDAC}}$ low and monitoring the output of another DAC. The energy of the glitch is expressed in nV-s.

Multiplying Bandwidth
The amplifiers within the DAC have a finite bandwidth. The multiplying bandwidth is a measure of this. A sine wave on the reference (with full-scale code loaded to the DAC) appears on the output. The multiplying bandwidth is the frequency at which the output amplitude falls to 3 dB below the input.

Total Harmonic Distortion (THD)
Total harmonic distortion is the difference between an ideal sine wave and its attenuated version using the DAC. The sine wave is used as the reference for the DAC, and the THD is a measure of the harmonics present on the DAC output. It is measured in decibels.

THEORY OF OPERATION

DIGITAL-TO-ANALOG CONVERTER (DAC) SECTION

The AD5629R/AD5669R are fabricated on a CMOS process. The architecture consists of a string of DACs followed by an output buffer amplifier. Each part includes an internal 1.25 V/2.5 V, 5 ppm/°C reference with an internal gain of 2. Figure 48 and Figure 49 show block diagrams of the DAC architecture.

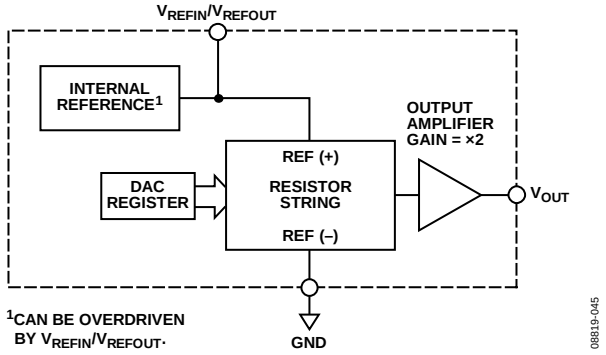


Figure 48. DAC Architecture for Internal Reference Configuration

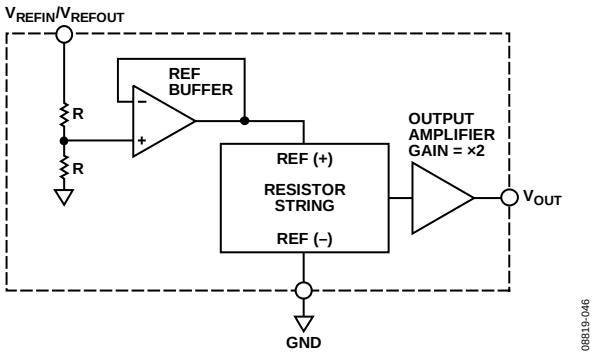


Figure 49. DAC Architecture for External Reference Configuration

Because the input coding to the DAC is straight binary, the ideal output voltage when using an external reference is given by

$$V_{OUT} = V_{REFIN} \times \left(\frac{D}{2^N} \right)$$

The ideal output voltage when using the internal reference is given by

$$V_{OUT} = 2 \times V_{REFOUT} \times \left(\frac{D}{2^N} \right)$$

where:
D = decimal equivalent of the binary code that is loaded to the DAC register as follows:
0 to 4095 for AD5629R (12 bits).
0 to 65,535 for AD5669R (16 bits).
N = the DAC resolution.

RESISTOR STRING

The resistor string section is shown in Figure 50. It is simply a string of resistors, each of value R. The code loaded into the DAC register determines at which node on the string the voltage is tapped off to be fed into the output amplifier. The voltage is tapped off by closing one of the switches connecting the string to the amplifier. Because it is a string of resistors, it is guaranteed monotonic.

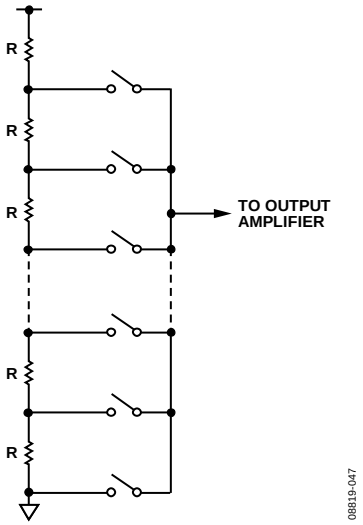


Figure 50. Resistor String

INTERNAL REFERENCE

The AD5629R/AD5669R have an on-chip reference with an internal gain of 2. The AD5629R-1/AD5669R-1 have a 1.25 V, 5 ppm/°C reference, giving a full-scale output of 2.5 V or the AD5629R-2/AD5629R-3/AD5669R-2/AD5669R-3 have a 2.5 V, 5 ppm/°C reference, working between a supply from 4.5 V to 5.5 V giving a full-scale output of 5 V. The on-board reference is off at power-up, allowing the use of an external reference. The internal reference is enabled via a write to the control register (see Table 8).

The internal reference associated with each part is available at the V_{REFOUT} pin. A buffer is required if the reference output is used to drive external loads. When using the internal reference, it is recommended that a 100 nF capacitor be placed between the reference output and GND for reference stability.

Individual channel power-down is not supported while using the internal reference.

OUTPUT AMPLIFIER

The output buffer amplifier can generate rail-to-rail voltages on its output, which gives an output range of 0 V to V_{DD}. The amplifier is capable of driving a load of 2 kΩ in parallel with 1000 pF to GND. The source and sink capabilities of the output amplifier can be seen in Figure 25 and Figure 26. The slew rate is 1.5 V/µs with a ¼ to ¾ scale settling time of 10 µs.

SERIAL INTERFACE

The AD5629R/AD5669R have 2-wire I²C-compatible serial interfaces (refer to *The I²C-Bus Specification*, Version 2.1, January 2000, available from Philips Semiconductor). The AD5629R/AD5669R can be connected to an I²C bus as a slave device under the control of a master device. See Figure 2 for a timing diagram of a typical write sequence.

The AD5629R/AD5669R support standard (100 kHz) and fast (400 kHz) modes. High speed operation is only available on selected models. See the Ordering Guide for a full list of models. Support is not provided for 10-bit addressing and general call addressing.

The AD5629R/AD5669R each have a 7-bit slave address. The parts have a slave address whose five MSBs are 10101, and the two LSBs are set by the state of the A0 address pin, which determines the state of the A0 and A1 address bits.

The facility to make hardwired changes to the A0 pin allows the user to incorporate up to three of these devices on one bus, as outlined in Table 7.

Table 7. ADDR Pin Settings

A0 Pin Connection	A1	A0
V_{DD}	0	0
NC	1	0
GND	1	1

The 2-wire serial bus protocol operates as follows:

1. The master initiates data transfer by establishing a start condition when a high-to-low transition on the SDA line occurs while SCL is high. The following byte is the address byte, which consists of the 7-bit slave address. The slave address corresponding to the transmitted address responds by pulling SDA low during the ninth clock pulse (this is termed the acknowledge bit). At this stage, all other devices on the bus remain idle while the selected device waits for data to be written to or read from its shift register.
2. Data is transmitted over the serial bus in sequences of nine clock pulses (eight data bits followed by an acknowledge bit). The transitions on the SDA line must occur during the low period of SCL and remain stable during the high period of SCL.
3. When all data bits have been read or written, a stop condition is established. In write mode, the master pulls the SDA line high during the 10th clock pulse to establish a stop condition. If a stop condition is generated between the 7th and 8th clock pulse of the I²C address frame, a power cycle is required to recover the part. In read mode, the master issues a no acknowledge for the ninth clock pulse (that is, the SDA line remains high). The master brings the SDA line low before the 10th clock pulse and then high during the 10th clock pulse to establish a stop condition.

WRITE OPERATION

When writing to the AD5629R/AD5669R, the user must begin with a start command followed by an address byte ($R/\overline{W} = 0$), after which the DAC acknowledges that it is prepared to receive data by pulling SDA low. The AD5629R/AD5669R require two bytes of data for the DAC and a command byte that controls various DAC functions. Three bytes of data must, therefore, be written to the DAC, the command byte followed by the most significant data byte and the least significant data byte, as shown in Figure 51. After these data bytes are acknowledged by the AD5629R/AD5669R, a stop condition follows.

READ OPERATION

When reading data back from the AD5629R/AD5669R, the user begins with a start command followed by an address byte ($R/\overline{W} = 1$), after which the DAC acknowledges that it is prepared to transmit data by pulling SDA low. Three bytes of data are then read from the DAC, the first two of which are both acknowledged by the master as shown in Figure 52. A stop condition follows.

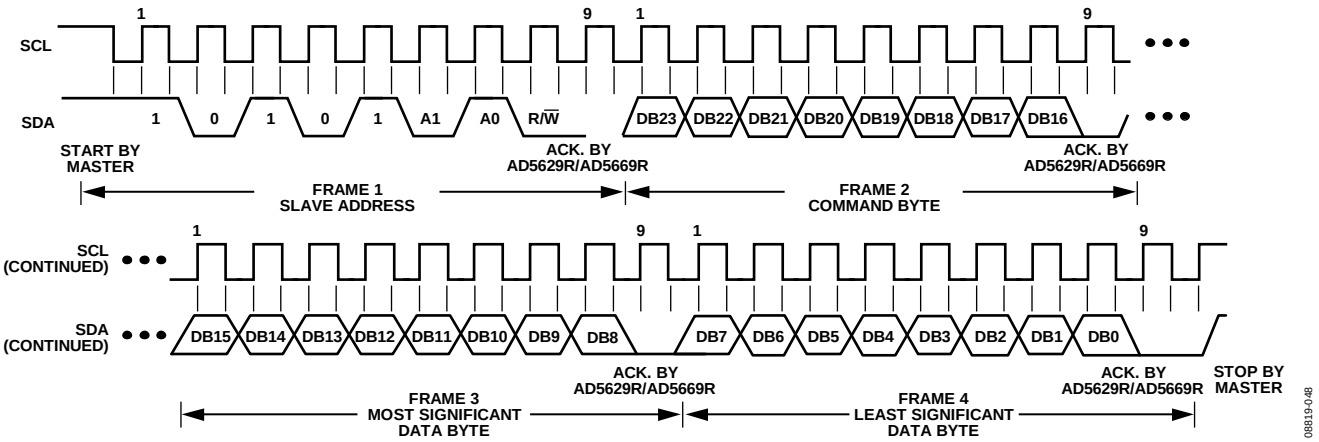


Figure 51. I²C Write Operation

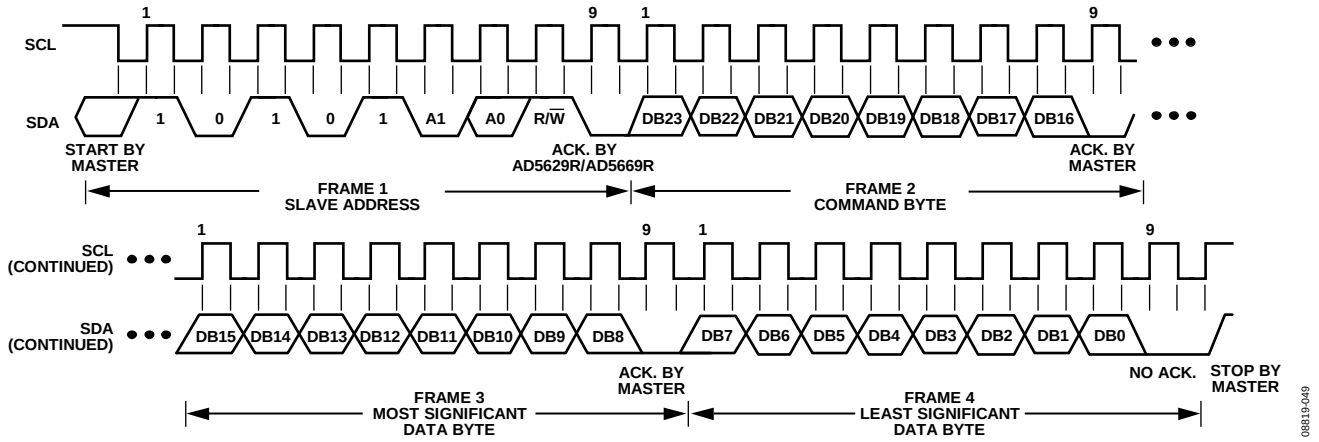


Figure 52. I²C Read Operation

Table 8. Command Definitions

Command				
C3	**C2**	**C1**	**C0**	**Description**
0	0	0	0	Write to Input Register n
0	0	0	1	Update DAC Register n
0	0	1	0	Write to Input Register n; update all (software $\overline{\text{LDAC}}$)
0	0	1	1	Write to and update DAC Channel n
0	1	0	0	Power down/power up DAC
0	1	0	1	Load clear code register
0	1	1	0	Load $\overline{\text{LDAC}}$ register
0	1	1	1	Reset (power-on reset)
1	0	0	0	Set up internal REF register
1	0	0	1	Enable multiple byte mode
1	0	1	0	Reserved
–	–	–	–	Reserved
1	1	1	1	Reserved

Table 9. Address Commands

Address (n)				
A3	**A2**	**A1**	**A0**	**Selected DAC Channel**
0	0	0	0	DAC A
0	0	0	1	DAC B
0	0	1	0	DAC C
0	0	1	1	DAC D
0	1	0	0	DAC E
0	1	0	1	DAC F
0	1	1	0	DAC G
0	1	1	1	DAC H
1	1	1	1	All DACs

INPUT SHIFT REGISTER

The input shift register is 24 bits wide. Data is loaded into the device as a 24-bit word under the control of a serial clock input, SCL. The input register contents for this operation is shown in Figure 53 and Figure 54. The eight MSBs make up the command byte. DB23 to DB20 are the command bits, C3, C2, C1, and C0, that control the mode of operation of the device (see Table 9 for details). The last four bits of the first byte are the address bits, A3, A2, A1, and A0, (see Table 9 for details). The rest of the bits are the 16-/12-bit data-word.

The AD5669R data-word comprises the 16-bit input code (see Figure 53) while the AD5629R data word is comprised of 12-bits followed by four don't cares (see Figure 54).

MULTIPLE BYTE OPERATION

Multiple byte operation is supported on the AD5629R/AD5669R. Command 1001 is reserved for multiple byte operation (see Table 8) A 2-byte operation is useful for applications that require fast DAC updating and do not need to change the command byte. The S bit (DB22) in the command register can be set to 1 for the 2-byte mode of operation. For standard 3-byte and 4-byte operation, the S bit (DB22) in the command byte should be set to 0.

INTERNAL REFERENCE REGISTER

The internal reference is available on all versions. The on-board reference is off at power-up by default. The on-board reference can be turned off or on by a user-programmable internal REF register by setting Bit DB0 high or low (see Table 10). DB1 selects the internal reference value. Command 1000 is reserved for setting the internal REF register (see Table 8). Table 11 shows how the state of the bits in the input shift register corresponds to the mode of operation of the device.

POWER-ON RESET

The AD5629R/AD5669R contain a power-on reset circuit that controls the output voltage during power-up. The AD5629R/AD5669R DAC output powers up to 0 V and the AD5669R-3 DAC output powers up to midscale. The output remains powered up at this level until a valid write sequence is made to the DAC. This is useful in applications where it is important to know the state of the output of the DAC while it is in the process of powering up. There is also a software executable reset function that resets the DAC to the power-on reset code. Command 0111 is reserved for this reset function (see Table 8). Any events on $\overline{\text{LDAC}}$ or $\overline{\text{CLR}}$ during power-on reset are ignored.

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
C3	C2	C1	C0	A3	A2	A1	A0	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
COMMAND				DAC ADDRESS				DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

08819-050

Figure 53. AD5669R Input Register Contents

DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15	DB14	DB13	DB12	DB11	DB10	DB9	DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
C3	C2	C1	C0	A3	A2	A1	A0	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	X	X	X	X
COMMAND				DAC ADDRESS				DAC DATA								DAC DATA							
COMMAND BYTE								DATA HIGH BYTE								DATA LOW BYTE							

08819-052

Figure 54. AD5629R Input Register Contents

POWER-DOWN MODES

The AD5629R/AD5669R contain four separate modes of operation. Command 0100 is reserved for the power-down function (see Table 8). These modes are software-programmable by setting two bits, Bit DB9 and Bit DB8, in the control register.

Table 12 shows how the state of the bits corresponds to the mode of operation of the device. Any or all DACs (DAC H to DAC A) can be powered down to the selected mode by setting the corresponding eight bits (DB7 to DB0) to 1. See Table 13 for the contents of the input shift register during power-down/power-up operation.

When both bits are set to 0, the part works normally with its normal power consumption of 1.3 mA at 5 V. However, for the three power-down modes, the supply current falls to 0.4 µA at 5 V (0.2 µA at 3 V). Not only does the supply current fall, but the output stage is also internally switched from the output of the amplifier to a resistor network of known values. This has the advantage that the output impedance of the part is known while the part is in power-down mode. There are three different options. The output is connected internally to GND through either a 1 kΩ or a 100 kΩ resistor, or it is left open-circuited (three-state). The output stage is illustrated in Figure 55.

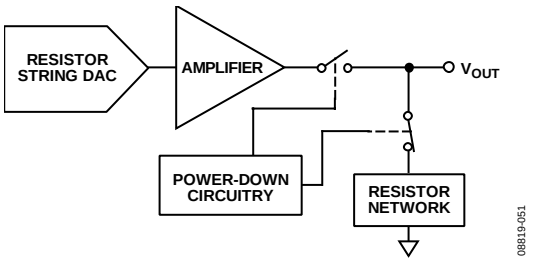


Figure 55. Output Stage During Power-Down

The bias generator of the selected DAC(s), output amplifier, resistor string, and other associated linear circuitry is shut down when the power-down mode is activated. The internal reference is powered down only when all channels are powered down. However, the contents of the DAC register are unaffected when in power-down. The time to exit power-down is typically 4 µs for V_{DD} = 5 V and for V_{DD} = 3 V.

Any combination of DACs can be powered up by setting PD1 and PD0 to 0 (normal operation). The output powers up to the value in the input register ($\overline{LDAC}$ low) or to the value in the DAC register before powering down ($\overline{LDAC}$ high).

CLEAR CODE REGISTER

The AD5629R/AD5669R have a hardware $\overline{CLR}$ pin that is an asynchronous clear input. The $\overline{CLR}$ input is falling edge sensitive. Bringing the $\overline{CLR}$ line low clears the contents of the input register and the DAC registers to the data contained in the user-configurable $\overline{CLR}$ register and sets the analog outputs accordingly. This function can be used in system calibration to load zero scale, midscale, or full scale to all channels together. These clear code values are user-programmable by setting two bits, Bit DB1 and Bit DB0, in the $\overline{CLR}$ control register (see Table 15). The default setting clears the outputs to 0 V. Command 0101 is reserved for loading the clear code register (see Table 8).

The part exits clear code mode at the end of the next valid write to the part. If $\overline{CLR}$ is activated during a write sequence, the write is aborted.

The $\overline{CLR}$ pulse activation time (the falling edge of $\overline{CLR}$ to when the output starts to change) is typically 280 ns. However, if outside the DAC linear region, it typically takes 520 ns after executing $\overline{CLR}$ for the output to start changing (see Figure 44).

See Table 14 for the contents of the input shift register during the loading clear code register operation.

Table 10. Internal Reference Register

Internal REF Register (DB0)	Action
0	Reference off (default)
1	Reference on

Table 11. 32-Bit Input Shift Register Contents for Reference Set-Up Command

MSB									LSB
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB1	DB0
1	0	0	0	X	X	X	X	X	1/0
Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Internal REF on/off

Table 12. Power-Down Modes of Operation

DB9	DB8	Operating Mode
0	0	Normal operation
		Power-down modes
0	1	1 kΩ to GND
1	0	100 kΩ to GND
1	1	Three-state

Table 13. 32-Bit Input Shift Register Contents for Power-Down/Power-Up Function

MSB									LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19 to DB16**	**DB15 to DB10**	**DB9**	**DB8**	**DB7 to DB1**	**DB0**
0	1	0	0	X	X	PD1	PD0	DAC H to DAC B	DAC A
Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares	Don't cares	Power-down mode		Power-down/power-up channel selection—set bit to 1 to select	

Table 14. 32-Bit Input Shift Register Contents for Clear Code Function

MSB										LSB
DB23	**DB22**	**DB21**	**DB20**	**DB19**	**DB18**	**DB17**	**DB16**	**DB15 to DB2**	**DB1**	**DB0**
0	1	0	1	X	X	X	X	X	CR1	CR0
Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Clear code register	

Table 15. Clear Code Register

Clear Code Register		
DB1	**DB0**	
CR1	**CR0**	**Clears to Code**
0	0	0x0000
0	1	0x8000
1	0	0xFFFF
1	1	No operation

$\overline{\text{LDAC}}$ FUNCTION

The outputs of all DACs can be updated simultaneously using the hardware $\overline{\text{LDAC}}$ pin.

Synchronous $\overline{\text{LDAC}}$

The DAC registers are updated after new data is read in. $\overline{\text{LDAC}}$ can be permanently low or pulsed as in Figure 2.

Asynchronous $\overline{\text{LDAC}}$

The outputs are not updated at the same time that the input registers are written to. When $\overline{\text{LDAC}}$ goes low, the DAC registers are updated with the contents of the input register.

Alternatively, the outputs of all DACs can be updated simultaneously using the software $\overline{\text{LDAC}}$ function by writing to Input Register n and updating all DAC registers. Command 0011 is reserved for this software $\overline{\text{LDAC}}$ function.

An $\overline{\text{LDAC}}$ register gives the user extra flexibility and control over the hardware $\overline{\text{LDAC}}$ pin. Setting the $\overline{\text{LDAC}}$ bit register to 0 for a DAC channel means that this channel's update is controlled by the $\overline{\text{LDAC}}$ pin. If this bit is set to 1, this channel updates synchronously; that is, the DAC register is updated after new data is read, regardless of the state of the $\overline{\text{LDAC}}$ pin. It effectively sees the $\overline{\text{LDAC}}$ pin as being tied low. See Table 16 for the $\overline{\text{LDAC}}$ register mode of operation.

This flexibility is useful in applications where the user wants to simultaneously update select channels while the rest of the channels are synchronously updating. Writing to the DAC using command 0110 loads the 8-bit $\overline{\text{LDAC}}$ register (DB7 to DB0). The default for each channel is 0, that is, the $\overline{\text{LDAC}}$ pin works normally. Setting the bits to 1 means the DAC channel is updated regardless of the state of the $\overline{\text{LDAC}}$ pin. See Table 17 for the contents of the input shift register during the load $\overline{\text{LDAC}}$ register mode of operation.

POWER SUPPLY BYPASSING AND GROUNDING

When accuracy is important in a circuit, it is helpful to carefully consider the power supply and ground return layout on the board. The printed circuit board containing the AD5629R/AD5669R should have separate analog and digital sections. If the AD5629R/AD5669R are in a system where other devices require an AGND-to-DGND connection, the connection should be made at one point only. This ground point should be as close as possible to the AD5629R/AD5669R.

The power supply to the AD5629R/AD5669R should be bypassed with 10 µF and 0.1 µF capacitors. The capacitors should be as physically close as possible to the device, with the 0.1 µF capacitor ideally right up against the device. The 10 µF capacitors are the tantalum bead type. It is important that the 0.1 µF capacitor have low effective series resistance (ESR) and low effective series inductance (ESI), such as is typical of common ceramic types of capacitors. This 0.1 µF capacitor provides a low impedance path to ground for high frequencies caused by transient currents due to internal logic switching.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals if possible. When traces cross on opposite sides of the board, ensure that they run at right angles to each other to reduce feedthrough effects through the board. The best board layout technique is the microstrip technique, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

Table 16. $\overline{\text{LDAC}}$ Register

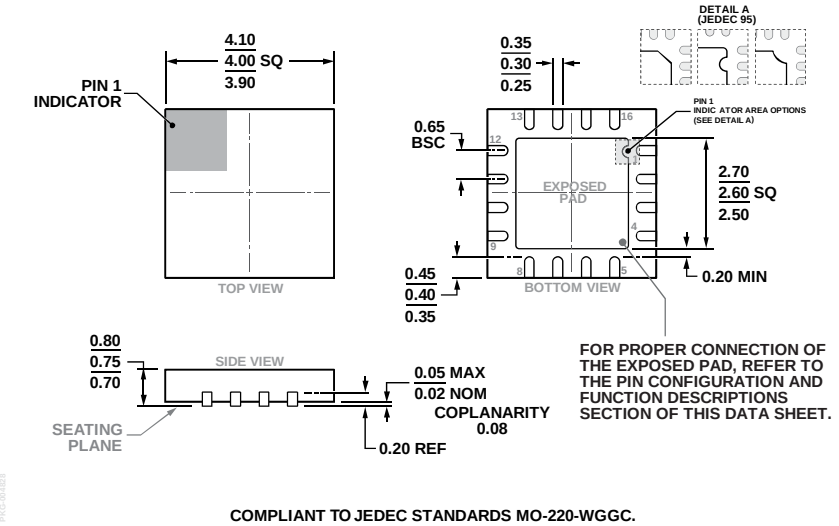
Load DAC Register		
$\overline{\text{LDAC}}$ Bits (DB7 to DB0)	**$\overline{\text{LDAC}}$ Pin**	**$\overline{\text{LDAC}}$ Operation**
0	1/0	Determined by $\overline{\text{LDAC}}$ pin.
1	X—don't care	DAC channels update, overriding the $\overline{\text{LDAC}}$ pin. DAC channels see $\overline{\text{LDAC}}$ as 0.

Table 17. 32-Bit Input Shift Register Contents for $\overline{\text{LDAC}}$ Register Function

MSB **LSB**

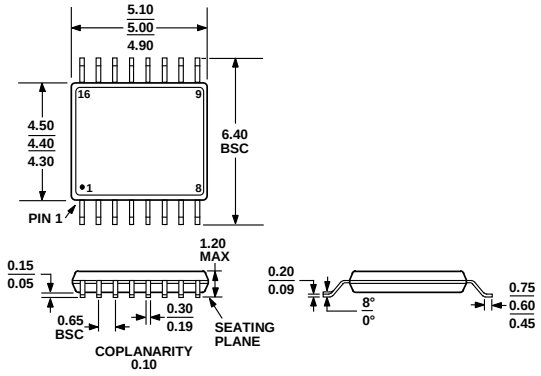
DB23	DB22	DB21	DB20	DB19	DB18	DB17	DB16	DB15 to DB8	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	1	0	X	X	X	X	X	DAC H	DAC G	DAC F	DAC E	DAC D	DAC C	DAC B	DAC A
Command bits (C3 to C0)				Address bits (A3 to A0)—don't cares				Don't cares	Setting $\overline{\text{LDAC}}$ bit to 1 overrides $\overline{\text{LDAC}}$ pin							

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 56. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body, 0.75 mm Package Height
(CP-16-17)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 57. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters

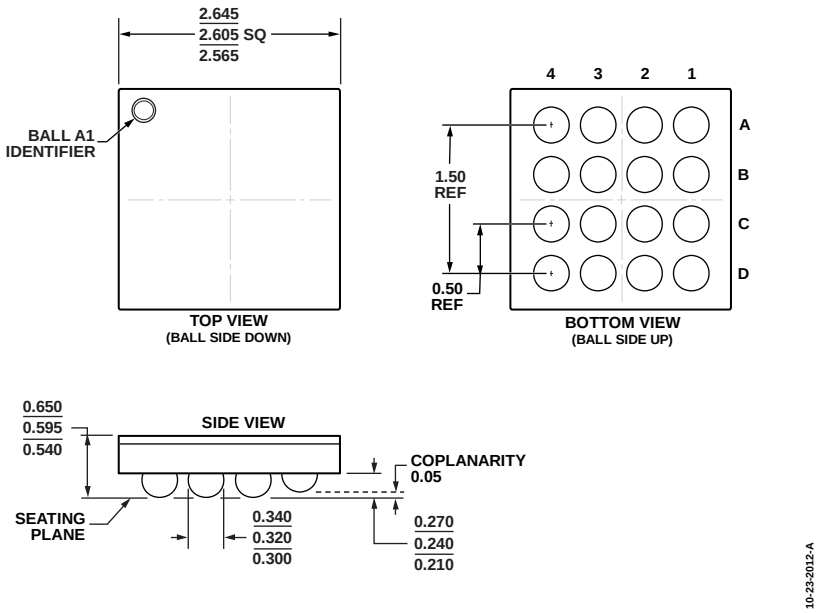


Figure 58. 16-Ball Wafer Level Chip Scale Package [WLCSP]
(CB-16-16)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Power-On Reset to Code	Accuracy	Internal Reference
AD5629RARUZ-1	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±4 LSB INL	1.25 V
AD5629RARUZ-1-RL7	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±4 LSB INL	1.25 V
AD5629RBRUZ-2	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	2.5 V
AD5629RBRUZ-2-RL7	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±1 LSB INL	2.5 V
AD5629RACPZ-2-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±4 LSB INL	2.5 V
AD5629RACPZ-3-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Midscale	±4 LSB INL	2.5 V
AD5629RBCPZ-1-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±1 LSB INL	1.25 V
AD5629RBCPZ-2-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±1 LSB INL	2.5 V
AD5629RBCBZ-1-RL7	−40°C to +105°C	16-Lead WLCSP	CB-16-16	Zero	±1 LSB INL	1.25 V
AD5669RARUZ-1	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±32 LSB INL	1.25 V
AD5669RARUZ-1-RL7	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±32 LSB INL	1.25 V
AD5669RBRUZ-2	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±16 LSB INL	2.5 V
AD5669RBRUZ-2-RL7	−40°C to +105°C	16-Lead TSSOP	RU-16	Zero	±16 LSB INL	2.5 V
AD5669RACPZ-2-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±32 LSB INL	2.5 V
AD5669RACPZ-3-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Midscale	±32 LSB INL	2.5 V
AD5669RBCPZ-1-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	1.25 V
AD5669RBCPZ-2-RL7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	2.5 V
AD5669RBCPZ-1500R7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	1.25 V
AD5669RBCPZ-2500R7	−40°C to +105°C	16-Lead LFCSP	CP-16-17	Zero	±16 LSB INL	2.5 V
AD5669RBCBZ-1-RL7	−40°C to +105°C	16-Lead WLCSP	CB-16-16	Zero	±16 LSB INL	1.25 V
AD5669RBCBZ-1-R5	−40°C to +105°C	16-Lead WLCSP	CB-16-16	Zero	±16 LSB INL	1.25 V
EVAL-AD5629RSDZ		Evaluation Board				
EVAL-AD5669RSDZ		Evaluation Board				

[1] Z = RoHS Compliant Part.

I²C refers to a communications protocol originally developed by Philips Semiconductors (now NXP Semiconductors).

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