THE DATASHEET OF

AD8235ACBZ-P7

40 µA Micropower Instrumentation Amplifier in WLCSP Package

Data Sheet

AD8235

FEATURES

- **Low power**
  - **40 µA maximum supply current**
  - **6 nA shutdown current**
- **Low input currents**
  - **50 pA input bias current**
  - **25 pA input offset current**
- **High Common Mode Rejection Ratio (CMRR)**
  - **110 dB CMRR , G = 100**
- **Space saving**
  - **WLCSP package**
- **Zero input crossover distortion**
- **Versatile**
  - **Rail-to-rail input and output**
  - **Shutdown**
  - **Gain set with single resistor (G = 5 to 200)**
- **AD8236: µSOIC package version of AD8235**

APPLICATIONS

- **Medical instrumentation**
- **Low-side current sense**
- **Portable electronics**

GENERAL DESCRIPTION

The AD8235 is the smallest and lowest power instrumentation amplifier in the industry. It is available in a 1.5 mm × 2.2 mm wafer level chip scale package (WLCSP). The AD8235 draws a maximum quiescent current of 40 µA. In addition, it draws a maximum 500 nA of current during shutdown mode, making it an excellent instrumentation amplifier for battery powered, portable applications.

The AD8235 can operate on supply voltages as low as 1.8 V. The input stage allows for wide rail-to-rail input voltage range without the crossover distortion, common in other designs. The rail-to-rail output enables easy interfacing to ADCs.

The AD8235 is an excellent choice for signal conditioning. Its low input bias current of 50 pA and high CMRR of 110 dB (G = 100) offer tremendous value for its size and low power.

It is specified over the extended industrial temperature range of −40°C to 125°C.

CONNECTION DIAGRAM

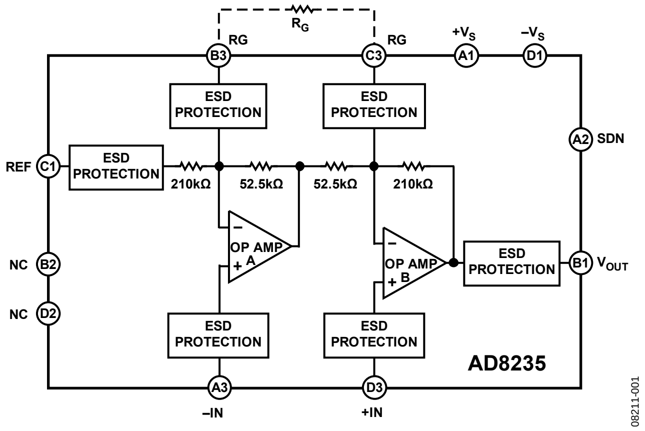

Figure 1.

PIN CONFIGURATION

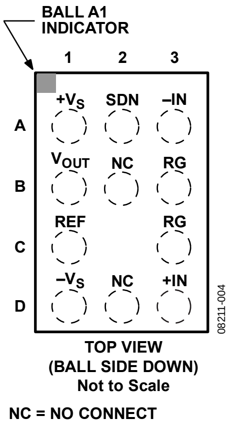

Figure 2. 11-Ball WLCSP (CB-11-1)

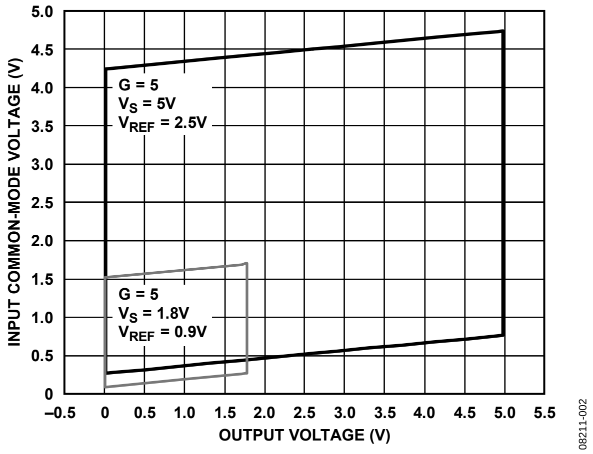

Figure 3. Wide Common-Mode Voltage Range vs. Output Voltage

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REVISION HISTORY

9/2016—Rev. 0 to Rev. A

Updated Outline Dimensions ... 20

8/2009—Revision 0: Initial Version

SPECIFICATIONS

$+V_S$ = 5 V, $-V_S$ = 0 V (GND), V_{REF} = 2.5 V, T_A = 25°C, G = 5, R_{LOAD} = 100 kΩ to GND, SDN pin tied to $+V_S$, unless otherwise noted.

Table 1.

Parameter	Test Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	V_S = ±2.5 V, V_{REF} = 0 V				
CMRR DC	V_{CM} = −1.8 V to +1.8 V				
G = 5		90	94		dB
G = 10		90	100		dB
G = 100		100	110		dB
G = 200		100	110		dB
NOISE					
Voltage Noise Spectral Density, RTI	f = 1 kHz, G = 5		76		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 5			4		µV p-p
G = 200			4		µV p-p
Current Noise			15		fA/√Hz
VOLTAGE OFFSET					
Input Offset, V_{OS}				2.5	mV
Average Temperature Coefficient (TC)	−40°C to +125°C		0.7		µV/°C
Offset RTI vs. Supply (PSR)	V_S = 1.8 V to 5 V				
G = 5		100	120		dB
G = 10		110	126		dB
G = 100		110	130		dB
G = 200		110	130		dB
INPUT CURRENT					
Input Bias Current			1	50	pA
Overtemperature	−40°C to +85°C			100	pA
	−40°C to +125°C			600	pA
Input Offset Current			0.5	25	pA
Overtemperature	−40°C to +85°C			50	pA
	−40°C to +125°C			130	pA
DYNAMIC RESPONSE					
Small Signal Bandwidth, −3 dB					
G = 5			23		kHz
G = 10			9		kHz
G = 100			0.8		kHz
G = 200			0.4		kHz
Settling Time 0.01%	V_{OUT} = 4 V step				
G = 5			444		µs
G = 10			456		µs
G = 100			992		µs
G = 200			1816		µs
Slew Rate					
G = 5 to 100			9		mV/µs

Parameter	Test Conditions	Min	Typ	Max	Unit
GAIN					
Gain Range	G = 5 + 420 kΩ/R_G	5		200[1]	V/V
Gain Error	V_S = ±2.5 V, V_{REF} = 0 V, V_{OUT} = −2 V to +2 V				
G = 5			0.005	0.05	%
G = 10			0.03	0.2	%
G = 100			0.06	0.2	%
G = 200			0.15	0.3	%
Nonlinearity	R_L = 10 kΩ or 100 kΩ				
G = 5			2	10	ppm
G = 10			1.2	10	ppm
G = 100			0.5	10	ppm
G = 200			0.5	10	ppm
Gain vs. Temperature	−40°C to +125°C				
G = 5			0.35	1.5	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Differential Impedance			440||1.6		GΩ||pF
Common-Mode Impedance			110||6.2		GΩ||pF
Input Voltage Range	−40°C to +125°C	0		$+V_S$	V
OUTPUT					
Output Voltage High, V_{OH}	R_L = 100 kΩ	4.98	4.99		V
	−40°C to +125°C	4.98			V
	R_L = 10 kΩ	4.9	4.95		V
	−40°C to +125°C	4.9			V
Output Voltage Low, V_{OL}	R_L = 100 kΩ		2	5	mV
	−40°C to +125°C			5	mV
	R_L = 10 kΩ		10	25	mV
	−40°C to +125°C			30	mV
Short-Circuit Limit, I_{SC}			±55		mA
REFERENCE INPUT					
R_{IN}	−IN, +IN = 0 V		210		kΩ
I_{IN}			20		nA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1		V/V
SHUTDOWN OPERATION					
Shutdown current			6	500	nA
	−40°C to +125°C			1.5	µA
SDN PIN INPUT VOLTAGE RANGE					
V_{OH}	−40°C to +125°C	$+V_S - 0.5$		$+V_S$	V
V_{OL}	−40°C to +125°C	$-V_S$		$-V_S + 0.5$	V
POWER SUPPLY					
Operating Range		1.8		5.5	V
Quiescent Current			30	40	µA
Overtemperature	−40°C to +125°C			50	µA
TEMPERATURE RANGE					
For Specified Performance		−40		+125	°C

[1] Although the specifications of the AD8235 list only low to midrange gains, gains can be set beyond 200.

$+V_S = 1.8$ V, $-V_S = 0$ V (GND), $V_{REF} = 0.9$ V, $T_A = 25°C$, G = 5, $R_{LOAD} = 100$ kΩ to GND, SDN pin tied to $+V_S$, unless otherwise noted.

Table 2.

Parameter	Test Conditions	Min	Typ	Max	Unit
COMMON-MODE REJECTION RATIO (CMRR)	$V_S = \pm0.9$ V, $V_{REF} = 0$ V				
CMRR DC	$V_{CM} = -0.6$ V to +0.6 V				
G = 5		90	94		dB
G = 10		90	100		dB
G = 100		100	110		dB
G = 200		100	110		dB
NOISE					
Voltage Noise Spectral Density, RTI	f = 1 kHz, G = 5		76		nV/√Hz
RTI, 0.1 Hz to 10 Hz					
G = 5			4		μV p-p
G = 200			4		μV p-p
Current Noise			15		fA/√Hz
VOLTAGE OFFSET					
Input Offset, V_{OS}				2.5	mV
Average Temperature Coefficient (TC)	−40°C to +125°C		0.7		μV/°C
Offset RTI vs. Supply (PSR)	$V_S = 1.8$ V to 5 V				
G = 5		100	120		dB
G = 10		110	126		dB
G = 100		110	130		dB
G = 200		110	130		dB
INPUT CURRENT					
Input Bias Current			1	50	pA
Overtemperature	−40°C to +85°C			100	pA
	−40°C to +125°C			600	pA
Input Offset Current			0.5	25	pA
Overtemperature	−40°C to +85°C			50	pA
	−40°C to +125°C			130	pA
DYNAMIC RESPONSE					
Small Signal Bandwidth, −3 dB					
G = 5			23		kHz
G = 10			9		kHz
G = 100			0.8		kHz
G = 200			0.4		kHz
Settling Time 0.01%	$V_{OUT} = 1.4$ V step				
G = 5			143		μs
G = 10			178		μs
G = 100			1000		μs
G = 200			1864		μs
Slew Rate					
G = 5 to 100			11		mV/μs

Parameter	Test Conditions	Min	Typ	Max	Unit
GAIN					
Gain Range	G = 5 + 420 kΩ/R_G	5		200[1]	V/V
Gain Error	V_S = ±0.9 V, V_{REF} = 0 V, V_{OUT} = −0.6 V to +0.6 V				
G = 5			0.005	0.05	%
G = 10			0.03	0.2	%
G = 100			0.06	0.2	%
G = 200			0.15	0.3	%
Nonlinearity	R_L = 10 kΩ or 100 kΩ				
G = 5			1	10	ppm
G = 10			1	10	ppm
G = 100			0.5	10	ppm
G = 200			0.4	10	ppm
Gain vs. Temperature	−40°C to +125°C				
G = 5			0.35	1.5	ppm/°C
G > 10				−50	ppm/°C
INPUT					
Differential Impedance			440‖1.6		GΩ‖pF
Common-Mode Impedance			110‖6.2		GΩ‖pF
Input Voltage Range	−40°C to +125°C	0		$+V_S$	V
OUTPUT					
Output Voltage High, V_{OH}	R_L = 100 kΩ	1.78	1.79		V
	−40°C to +125°C	1.78			V
	R_L = 10 kΩ	1.65	1.75		V
	−40°C to +125°C	1.65			V
Output Voltage Low, V_{OL}	R_L = 100 kΩ		2	5	mV
	−40°C to +125°C			5	mV
	R_L = 10 kΩ		12	25	mV
	−40°C to +125°C			25	mV
Short-Circuit Limit, I_{SC}			±6		mA
REFERENCE INPUT					
R_{IN}	−IN, +IN = 0 V		210		kΩ
I_{IN}			20		nA
Voltage Range		$-V_S$		$+V_S$	V
Gain to Output			1		V/V
SHUTDOWN OPERATION					
Shutdown Current			6	500	nA
	−40°C to +125°C			1.5	µA
SDN PIN INPUT VOLTAGE RANGE					
V_{OH}	−40°C to +125°C	$+V_S - 0.5$		$+V_S$	V
V_{OL}	−40°C to +125°C	$-V_S$		$-V_S + 0.5$	V
TEMPERATURE RANGE					
For Specified Performance		−40		+125	°C

[1] Although the specifications of the AD8235 list only low to midrange gains, gains can be set beyond 200.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Output Short-Circuit Current	55 mA
Input Voltage (Common Mode)	$\pm V_S$
Differential Input Voltage	$\pm V_S$
Storage Temperature Range	−65°C to +125°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature	125°C
ESD	
Human Body Model	1.5 kV
Charge Device Model	0.5 kV
Machine Model	200 V

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board, unless otherwise specified.

Table 4. Thermal Resistance

Package Type	PCB	Power (W)	θ_{JA} (°C/W)
11-Ball WLCSP CB-11-1	1S0P[1]	0.25	139.1
		1.25	130
	2S2P[2]	0.25	69.5
		1.25	68.3

[1] Simulated thermal numbers per JESD51-9:
1-layer PCB (1S0P), low effective thermal conductivity test board.

[2] 4-layer PCB (2S2P), high effective thermal conductivity test board.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

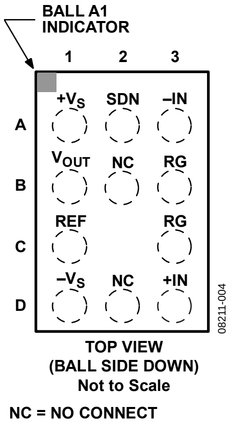

Figure 4. Pin Configuration (Top View Looking Through Package)

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
A1	$+V_S$	Positive Power Supply Terminal.
B1	V_{OUT}	Output Terminal.
C1	REF	Reference Voltage Terminal. Drive this terminal with a low impedance voltage source to level-shift the output.
D1	$-V_S$	Negative Power Supply Terminal.
A2	SDN	Shutdown Pin. Tie to $-V_S$ for shutdown. Tie to $+V_S$ for normal operation.
B2, D2	NC	No Connect. Leave both pins floating. Should not connect to any potential.
A3	−IN	Negative Input Terminal (True Differential Input).
B3, C3	RG	Gain Setting Terminals. Place resistor across the R_G pins.
D3	+IN	Positive Input Terminal (True Differential Input).

TYPICAL PERFORMANCE CHARACTERISTICS

G = 5, +V_S = 5 V, V_{REF} = 2.5 V, R_L = 100 kΩ tied to GND, T_A = 25°C, SDN pin connected to +V_S, unless otherwise noted

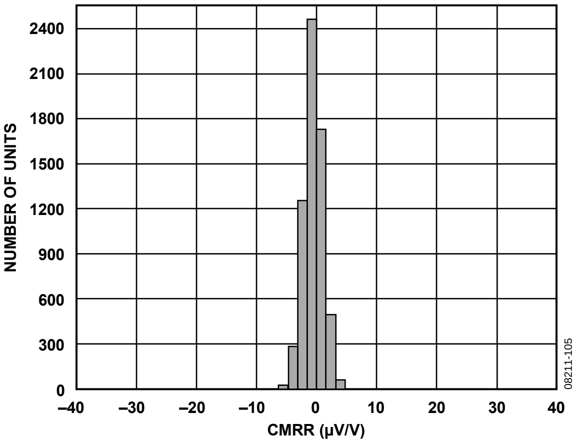

Figure 5. CMRR Distribution

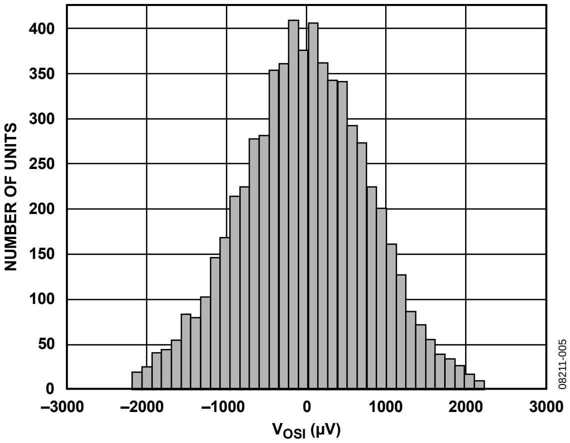

Figure 6. Typical Distribution of Input Offset Voltage

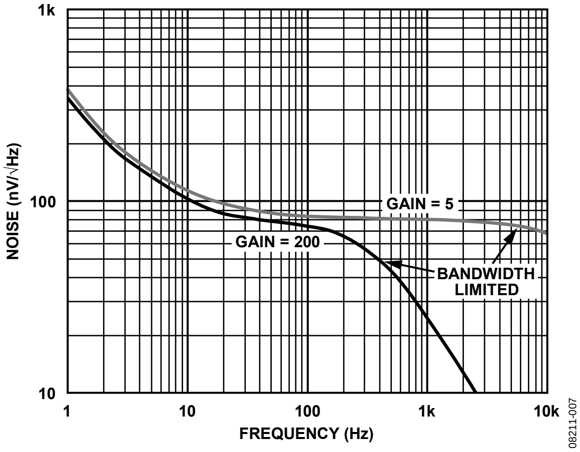

Figure 7. Voltage Noise Spectral Density vs. Frequency

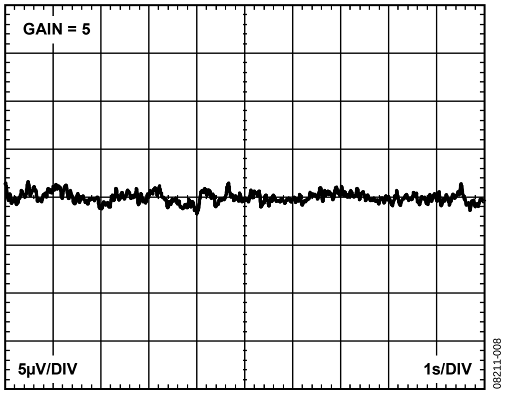

Figure 8. 0.1 Hz to 10 Hz RTI Voltage Noise

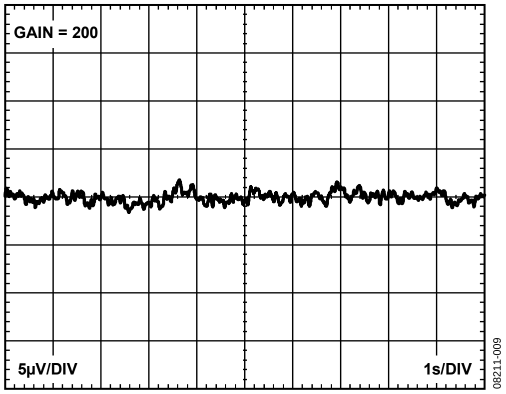

Figure 9. 0.1 Hz to 10 Hz RTI Voltage Noise

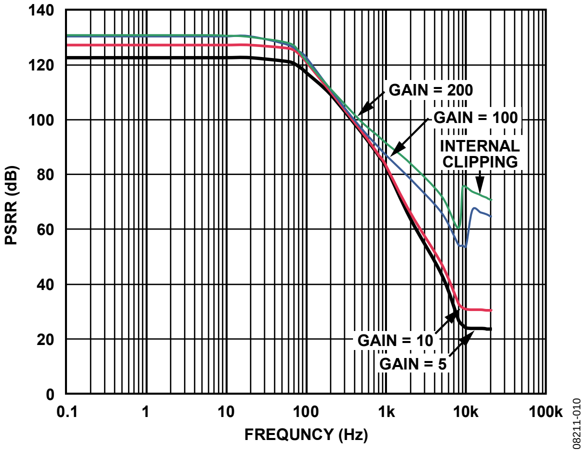

Figure 10. Positive PSRR vs. Frequency, RTI, V_S = ±0.9 V, ±2.5 V, V_{REF} = 0 V

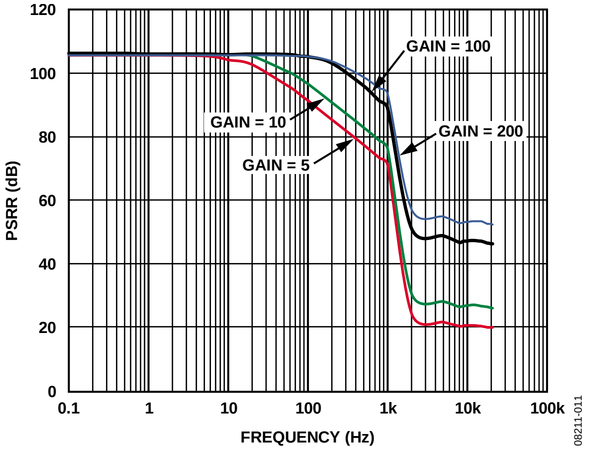

Figure 11. Negative PSRR vs. Frequency, RTI, V_S = ±0.9 V, ±2.5 V, V_{REF} = 0 V

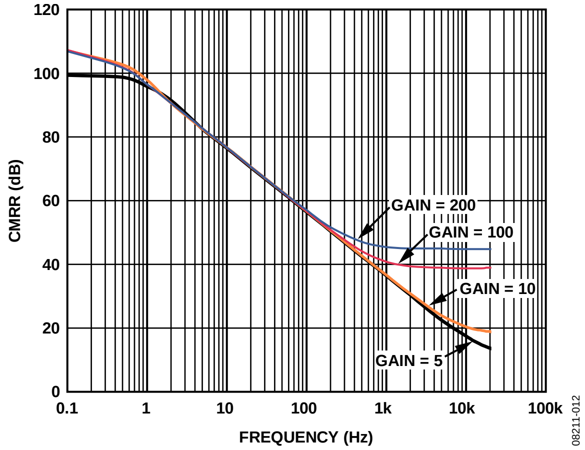

Figure 12. CMRR vs. Frequency, RTI

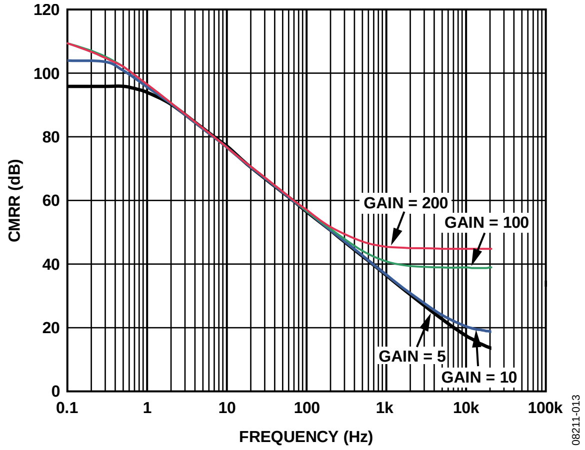

Figure 13. CMRR vs. Frequency, 1 kΩ Source Imbalance, RTI

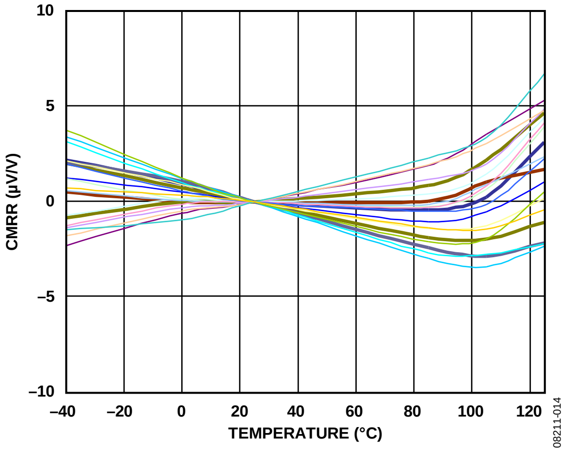

Figure 14. Change in CMRR vs. Temperature, G = 5, Normalized at 25°C

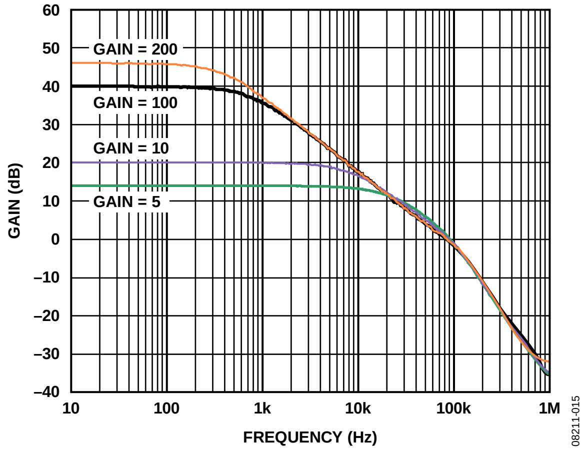

Figure 15. Gain vs. Frequency, V_S = 1.8 V, 5 V

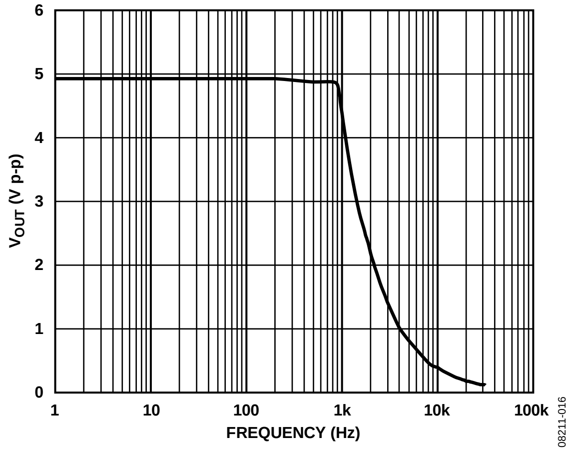

Figure 16. Maximum Output Voltage vs. Frequency

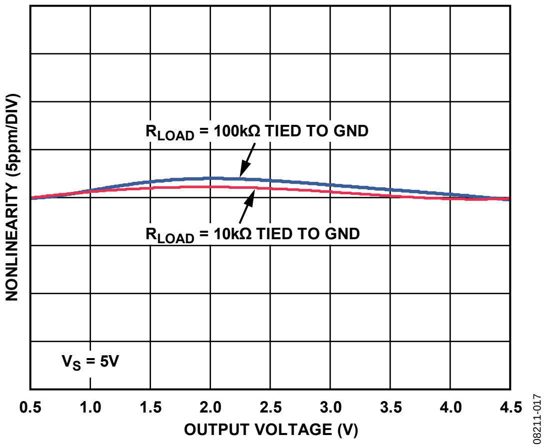

Figure 17. Gain Nonlinearity, G = 5

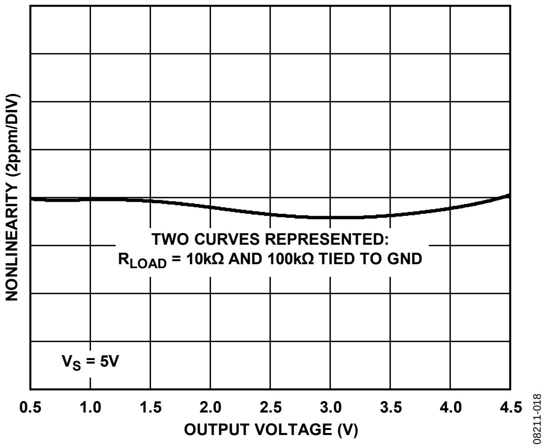

Figure 18. Gain Nonlinearity, G = 10

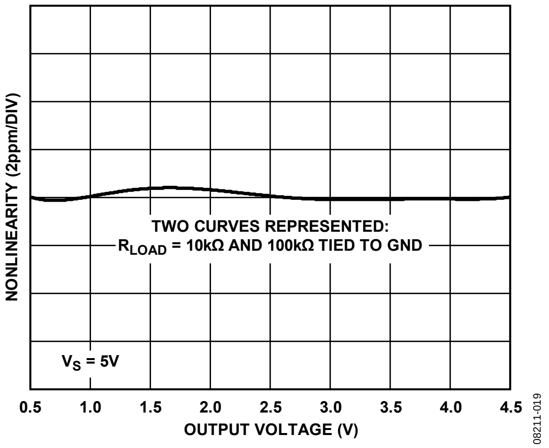

Figure 19. Gain Nonlinearity, G = 200

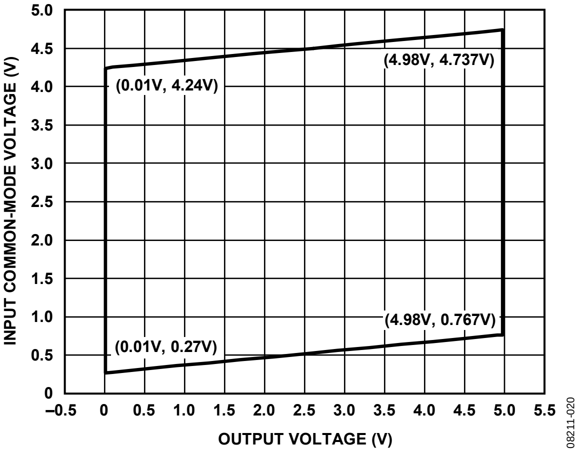

Figure 20. Input Common-Mode Voltage Range vs. Output Voltage, G = 5, V_S = 5 V, V_{REF} = 2.5 V

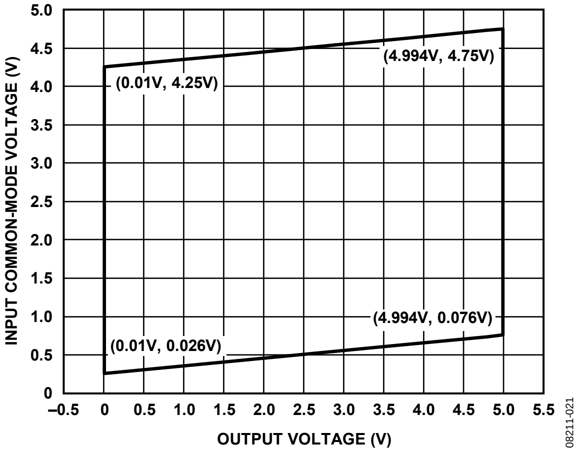

Figure 21. Input Common-Mode Voltage Range vs. Output Voltage, G = 200, V_S = 5 V, V_{REF} = 2.5 V

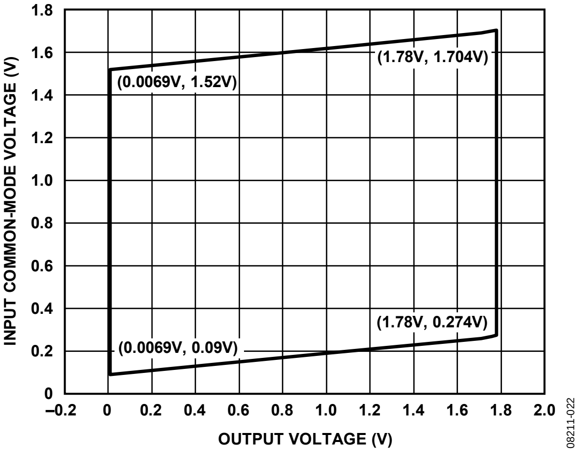

Figure 22. Input Common-Mode Voltage Range vs. Output Voltage, G = 5, V_S = 1.8 V, V_{REF} = 0.9 V

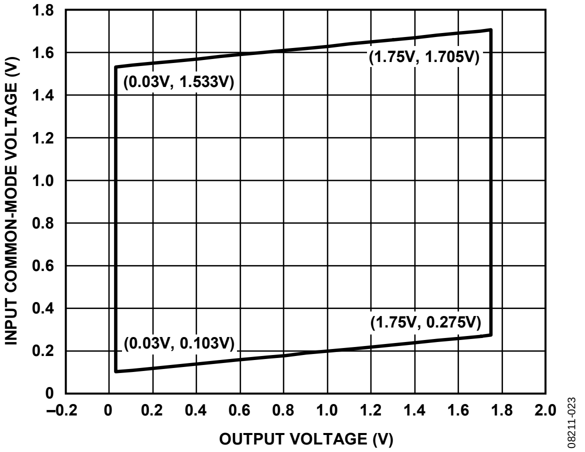

Figure 23. Input Common-Mode Voltage Range vs. Output Voltage, $G = 200$, $V_S = 1.8$ V, $V_{REF} = 0.9$ V

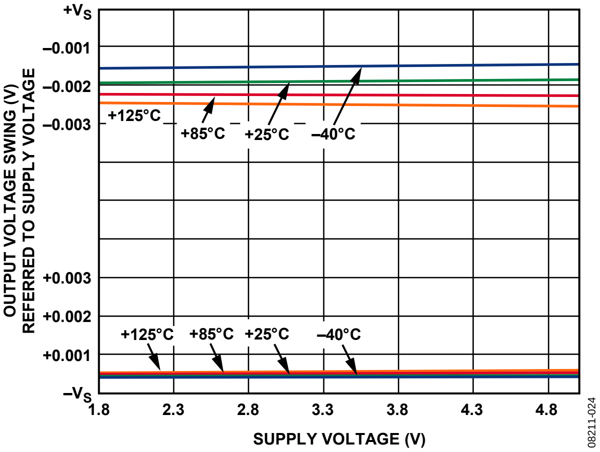

Figure 24. Output Voltage Swing vs. Supply Voltage, $V_S = \pm 0.9$ V, ±2.5 V, $V_{REF} = 0$ V, $R_{LOAD} = 100$ kΩ Tied to $-V_S$

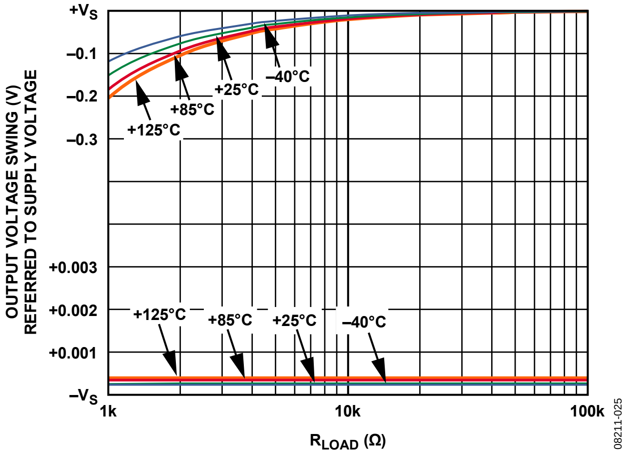

Figure 25. Output Voltage Swing vs. Load Resistance, $V_S = \pm 0.9$ V, ±2.5 V, $V_{REF} = 0$ V, $R_{LOAD} = 100$ kΩ Tied to $-V_S$

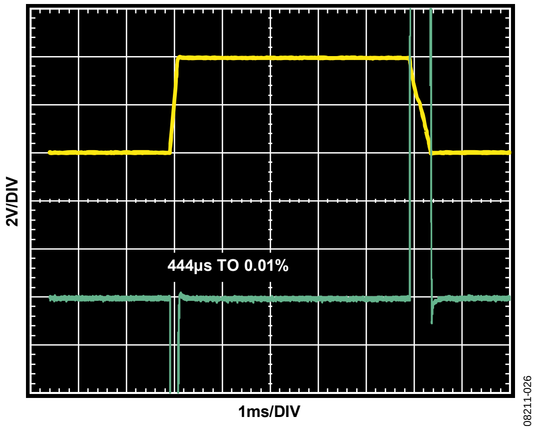

Figure 26. Large Signal Pulse Response and Settling Time, $V_S = \pm 2.5$ V, $V_{REF} = 0$ V, $R_{LOAD} = 10$ kΩ to V_{REF}

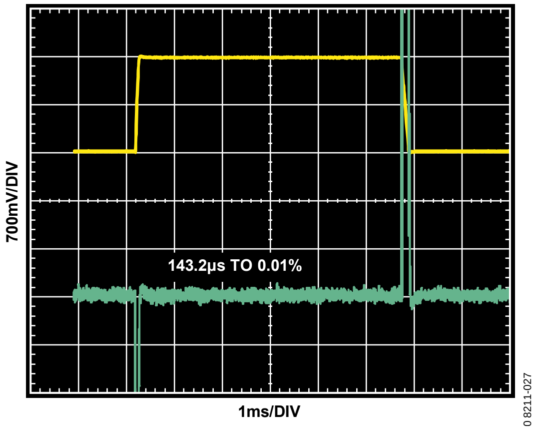

Figure 27. Large Signal Pulse Response and Settling Time, $V_S = \pm 0.9$ V, $V_{REF} = 0$ V, $R_{LOAD} = 10$ kΩ to V_{REF}

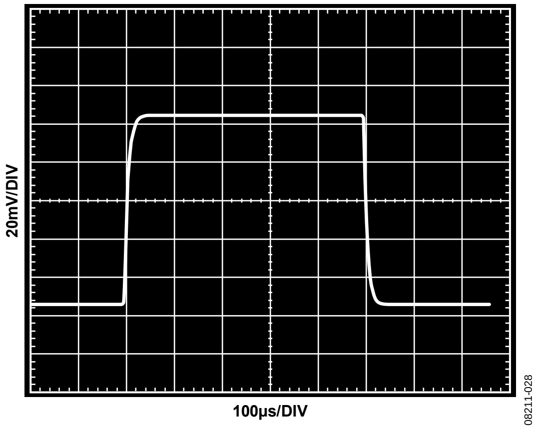

Figure 28. Small Signal Pulse Response, $G = 5$, $V_S = \pm 2.5$ V, $V_{REF} = 0$ V, $R_{LOAD} = 100$ kΩ to V_{REF}, $C_L = 100$ pF

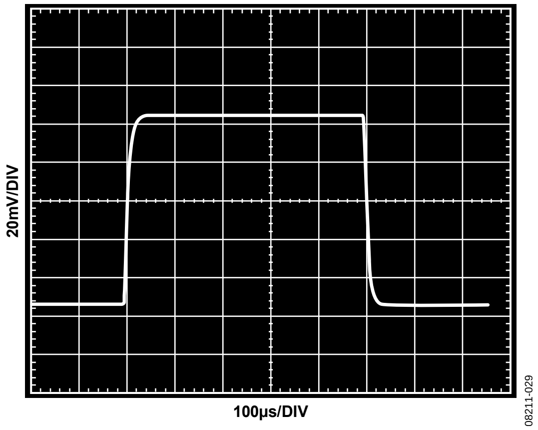

Figure 29. Small Signal Pulse Response, G = 5, C_L = 100 pF, V_S = ±0.9 V, V_{REF} = 0 V, R_{LOAD} = 100 kΩ to V_{REF}

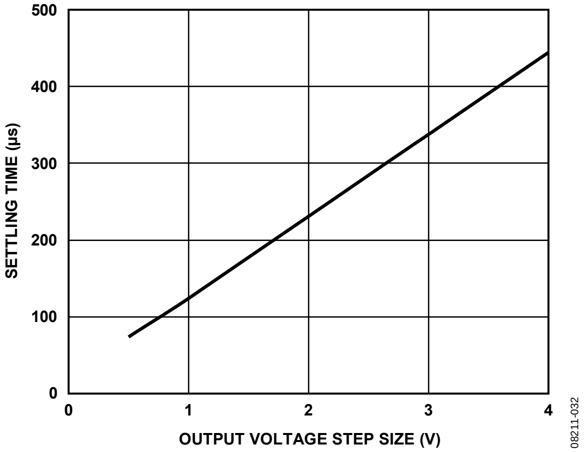

Figure 32. Settling Time vs. Output Voltage Step Size, V_S = ±2.5 V, V_{REF} = 0 V, R_{LOAD} = 10 kΩ Tied to V_{REF}

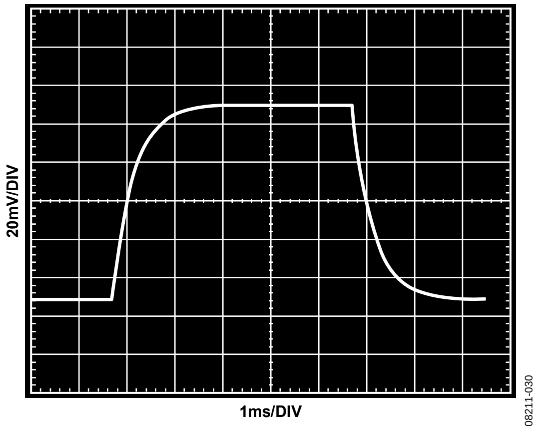

Figure 30. Small Signal Pulse Response, G = 200, C_L = 100 pF, V_S = 2.5 V, V_{REF} = 0 V, R_{LOAD} = 100 kΩ to V_{REF}

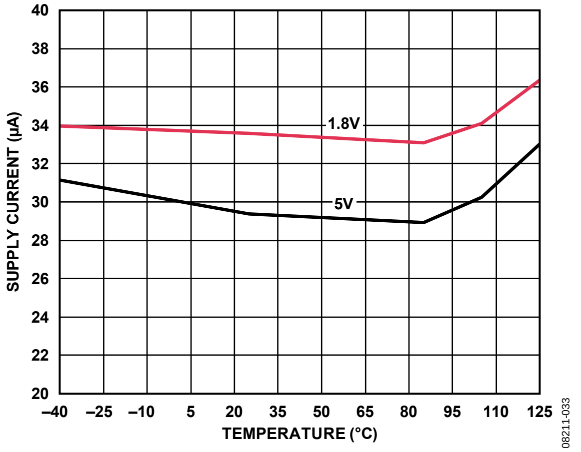

Figure 33. Total Supply Current vs. Temperature

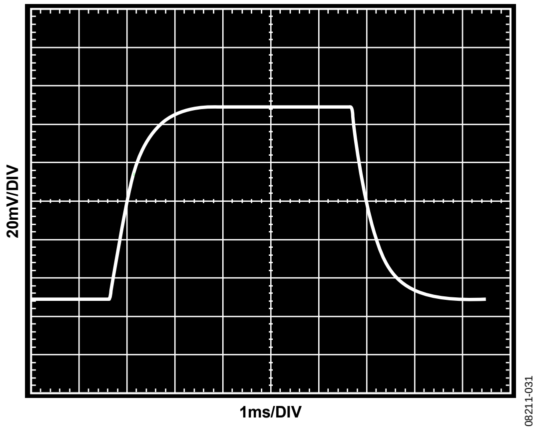

Figure 31. Small Signal Pulse Response, G = 200, C_L = 100 pF, V_S = 0.9 V, V_{REF} = 0 V, R_{LOAD} = 100 kΩ to V_{REF}

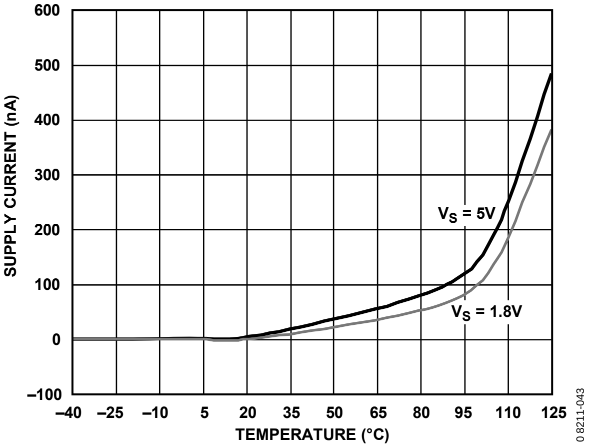

Figure 34. Total Supply Current During Shutdown vs. Temperature

THEORY OF OPERATION

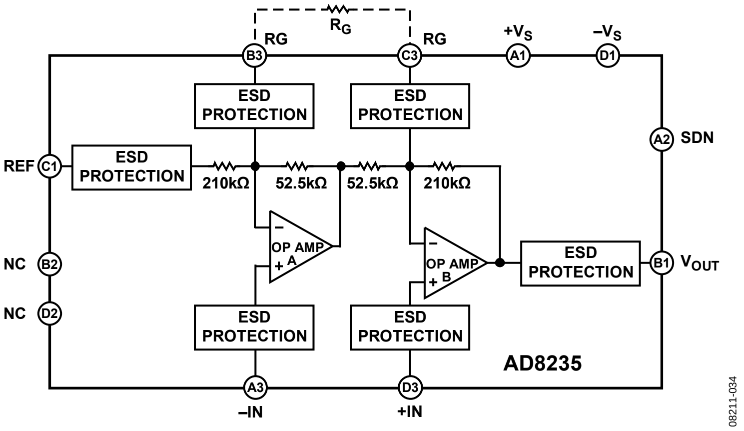

Figure 35. Simplified Schematic

The AD8235 is a monolithic, two-op amp instrumentation amplifier. It is designed for low power, portable applications where size and low quiescent current are paramount. The AD8235 is offered in a WLCSP package, minimizing layout area. Additional features that make this part optimal for portable applications include a rail-to-rail input and output stage that offers more dynamic range when operating on low voltage batteries. Unlike traditional rail-to-rail input amplifiers that use a complementary differential pair stage and suffer from nonlinearity, the AD8235 uses a novel architecture to internally boost the supply rail, allowing the amplifier to operate rail-to-rail yet still deliver a low 0.5 ppm of nonlinearity. In addition, the two-op amp instrumentation amplifier architecture offers a wide operational common-mode voltage range. Additional information is provided in the Common-Mode Input Voltage Range section. Precision, laser-trimmed resistors provide the AD8235 with a high CMRR of 90 dB (minimum) at G = 5 and gain accuracy of 0.05% (maximum).

BASIC OPERATION

The AD8235 amplifies the difference between its positive input (+IN) and its negative input (−IN). The REF pin allows the user to level-shift the output signal. This is convenient when interfacing to a filter or analog-to-digital converter (ADC). The basic setup is shown in Figure 36. Figure 39 shows an example configuration for operating the AD8235 with dual supplies. The equation for the AD8235 is as follows:

$$V_{OUT} = G \times (VINP - VINM) + VREF$$

If no gain setting resistor is installed, the default gain, G, is 5. The Gain Selection section describes how to program the gain, G.

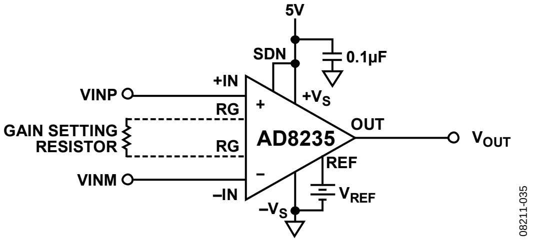

Figure 36. Basic Setup

GAIN SELECTION

Placing a resistor across the R_G terminals sets the gain of the AD8235. The gain may be derived by referring to Table 6 or by using the following equation:

$$R_G = \frac{420\ \text{k}\Omega}{G - 5}$$

Table 6. Gains Achieved Using 1% Resistors

1% Standard Table Value of R_G (kΩ)	Calculated Gain
422	6.0
210	7.0
140	8.0
105	9.0
84.5	10.0
28	20.0
9.31	50.1
4.42	100.0
2.15	200.3

The AD8235 defaults to G = 5 when no gain resistor is used. Gain accuracy is determined by the absolute tolerance of R_G. The TC of the external gain resistor increases the gain drift of the instrumentation amplifier. Gain error and gain drift are at a minimum when the gain resistor is not used.

SHUTDOWN FEATURE

The AD8235 includes a shutdown pin (SDN) that further enhances the flexibility and ease of use in portable applications where power consumption is critical. A logic level signal can be applied to this pin to switch to shutdown mode, even when the supply is still on.

When connecting the SDN pin to $+V_S$ or applying a voltage within $+V_S - 0.5$ V, the AD8235 operates in its normal condition and, therefore, draws approximately 40 µA of supply current. When connecting the SDN pin to $-V_S$, or any voltage within $-V_S + 0.5$ V, the AD8235 operates in shutdown mode and, therefore, draws less than 500 nA of supply current, offering considerable power savings.

In cases where the AD8235 is operating in shutdown mode, if a voltage potential exists at the REF pin, and there is a load to $-V_S$ at the output of the part, some additional current draw is noticeable. In this mode, a path from the REF pin to $-V_S$ exists, leading to some additional current draw from the reference. Typically, this current is negligible because the output of the AD8235 is driving a high impedance node, such as the input of an ADC.

LAYOUT RECOMMENDATIONS

The critical board design parameters, as it pertains to a WLCSP package, are pad opening, pad type, pad finish, and board thickness.

Pad Opening

Based on the IPC (Institute for Printed Circuits) standard, the pad opening equals the UBM (Under Bump Metallurgy) opening. The typical pad openings for the AD8235 shown in Figure 37 are:

- 250 µm (0.5 mm pitch WLCSP)

The solder mask opening is 100 µm plus the pad opening (or 350 µm in the case of the AD8235). The trace width should be less than two-thirds of the pad opening. Increasing the trace width can cause reduction in the stand-off height of the solder bump. Therefore, maintaining the proper trace width ratio is important to ensure the reliability of the solder connections.

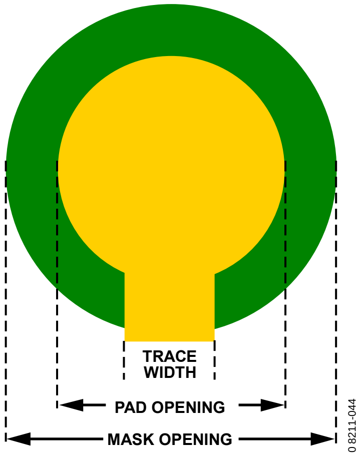

Figure 37. Pad Opening

Pad Type

For the actual board fabrication, the following types of pads/land patterns are used for surface mount assembly:

- Nonsolder mask defined (NSMD). The metal pad on the PCB (to which the I/O is attached) is smaller than the solder mask opening.
- Solder mask defined (SMD). The solder mask opening is smaller than the metal pad.

Because the copper etching process has tighter control than the solder mask opening process, NSMD is preferred over SMD. The solder mask opening on NSMD pads is larger than the copper pads, allowing the solder to attach to the sides of the copper pad and improving the reliability of the solder joints.

Pad Finish

The finish layer on the metal pads has a significant effect on assembly yield and reliability. The typical metal pad finishes used are organic surface preservative (OSP) and electroless nickel immersion gold (ENIG). The thickness of the OSP finish on a metal pad is 0.2 µm to 0.5 µm. This finish evaporates during the reflow soldering process and interfacial reactions occur between the solder and metal pad. The ENIG finish consists of 5 µm of electroless nickel and 0.02 µm to 0.05 µm of gold. During reflow soldering, the gold layer dissolves rapidly, followed by reaction between the nickel and solder. It is extremely important to keep the thickness of gold below 0.05 µm to prevent the formation of brittle intermetallic compounds.

Board Thickness

Typical board thicknesses used in the industry range from 0.4 mm to 1.6 mm and are most applicable for the AD8235. The thickness selected depends on the required robustness of the populated system assembly. The thinner board results in smaller shear stress range, creep shear strain range, and creep strain energy density range in the solder joints under the thermal loading. Therefore, the thinner build-up board leads to longer thermal fatigue life of solder joints [John H. Lau and S.W. Ricky Lee][1]

Grounding

The output voltage of the AD8235 is developed with respect to the potential on the reference terminal, REF. To ensure the most accurate output, the trace from the REF pin should either be connected to the AD8235 local ground (see Figure 39) or connected to a voltage that is referenced to the AD8235 local ground (Figure 36).

REFERENCE TERMINAL

The reference terminal, REF, is at one end of a 210 kΩ resistor (see Figure 35). The output of the instrumentation amplifier is referenced to the voltage on the REF terminal; this is useful when the output signal needs to be offset to voltages other than common. For example, a voltage source can be tied to the REF pin to level-shift the output so that the AD8235 can interface with an ADC. The allowable reference voltage range is a function of the gain, common-mode input, and supply voltages. The REF pin should not exceed either $+V_S$ or $-V_S$ by more than 0.5 V.

For best performance, especially in cases where the output is not measured with respect to the REF terminal, source impedance to the REF terminal should be kept low because parasitic resistance can adversely affect CMRR and gain accuracy. Figure 38 demonstrates how an op amp is configured to provide a low source impedance to the REF terminal when a midscale reference voltage is desired.

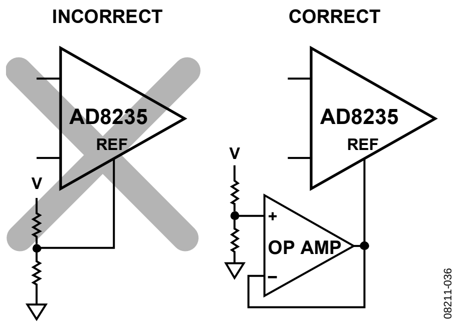

Figure 38. Driving the REF Pin

POWER SUPPLY REGULATION AND BYPASSING

The AD8235 has high power supply rejection ration (PSRR). However, for optimal performance, a stable dc voltage should be used to power the instrumentation amplifier. Noise on the supply pins can adversely affect performance. As in all linear circuits, bypass capacitors must be used to decouple the amplifier.

A 0.1 µF capacitor should be placed close to each supply pin. A 10 µF tantalum capacitor can be used farther away from the part (see Figure 39). In most cases, it can be shared by other precision integrated circuits.

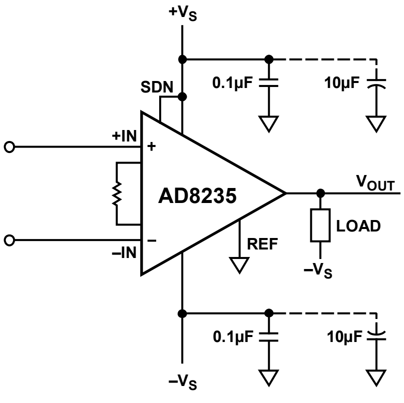

Figure 39. Supply Decoupling, REF, and Output Referred to Ground

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[1] John H. Lau and S.W. Ricky Lee, "Effects of Build-Up Printed Circuit Board Thickness on the Solder Joint Reliability of a Wafer Level Chip Scale Package (WLCSP)," IEEE Transactions on Components and Packaging Technologies, Vol.25, No.1, March 2002, pages 3-14.

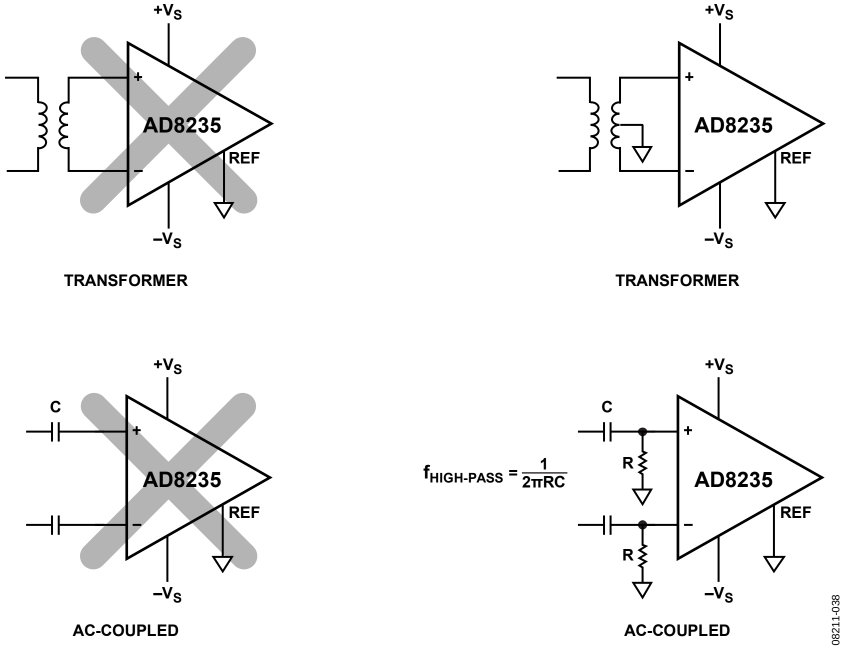

Figure 40. Creating an I_{BIAS} Path

INPUT BIAS CURRENT RETURN PATH

The AD8235 input bias current is extremely small at less than 50 pA. Nonetheless, the input bias current must have a return path to common. When the source, such as a transformer, cannot provide a return current path, one should be created (see Figure 40).

INPUT PROTECTION

All terminals of the AD8235 are protected against ESD. In addition, the input structure allows for dc overload conditions a diode drop above the positive supply and a diode drop below the negative supply. Voltages beyond a diode drop of the supplies cause the ESD diodes to conduct and enable current to flow through the diode. Therefore, an external resistor should be used in series with each of the inputs to limit current for voltages above $+V_S$. In either scenario, the AD8235 safely handles a continuous 6 mA current at room temperature.

For applications where the AD8235 encounters extreme overload voltages, as in cardiac defibrillators, external series resistors and low leakage diode clamps, such as BAV199Ls, FJH1100s, or SP720s, should be used.

RF INTERFERENCE

RF rectification is often a problem in applications where there are large RF signals. The problem appears as a small dc offset voltage. The AD8235, by its nature, has a 3.1 pF gate capacitance, C_G, at each input. Matched series resistors form a natural low-pass filter that reduces rectification at high frequency (see Figure 41). The relationship between external, matched series resistors and the internal gate capacitance is expressed as

$$FilterFreq_{DIFF} = \frac{1}{2\pi RC_G}$$

$$FilterFreq_{CM} = \frac{1}{2\pi RC_G}$$

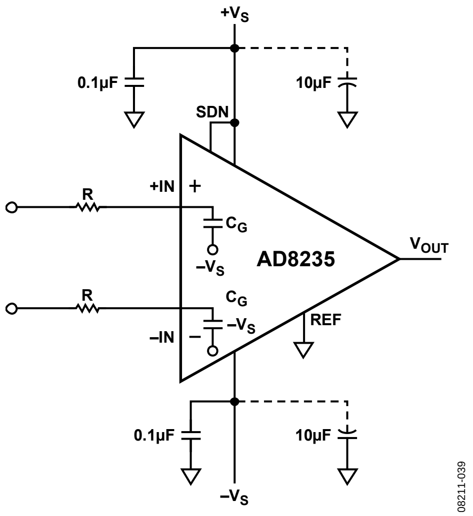

Figure 41. RFI Filtering Without External Capacitors

To eliminate high frequency common-mode signals while using smaller source resistors, a low-pass RC network can be placed at the input of the instrumentation amplifier (see Figure 42). The filter limits the input signal bandwidth according to the following relationship:

$$FilterFreq_{DIFF} = \frac{1}{2\pi R(2C_D + C_C + C_G)}$$

$$FilterFreq_{CM} = \frac{1}{2\pi R(C_C + C_G)}$$

Mismatched C_C capacitors result in mismatched low-pass filters. The imbalance causes the AD8235 to treat what is a common-mode signal as a differential signal. To reduce the effect of mismatched external C_C capacitors, select a value of C_D greater than 10× C_C. This sets the differential filter frequency lower than the common-mode frequency.

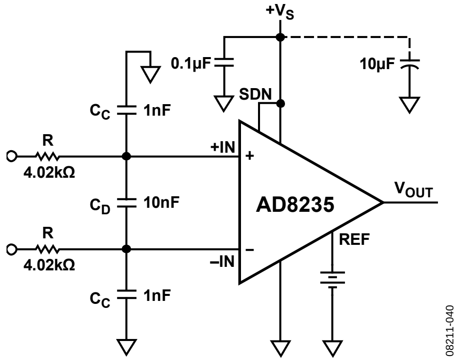

Figure 42. RFI Suppression

COMMON-MODE INPUT VOLTAGE RANGE

The common-mode input voltage range is a function of the input voltages, reference voltage, supplies, and the output of Internal Op Amp A. Figure 35 shows the internal nodes of the AD8235. Figure 20 to Figure 23 show the common-mode voltage ranges for typical supply voltages and gains.

If the supply voltages and reference voltage are not represented in Figure 20 to Figure 23, the following methodology can be used to calculate the acceptable common-mode voltage range:

1. Adhere to the input, output, and reference voltage ranges shown in Table 1 and Table 2.
2. Calculate the output of Internal Op Amp A. The following equation calculates this output:

   $$A = \frac{5}{4}\left(V_{CM} - \frac{V_{DIFF}}{2}\right) - \frac{52.5\ k\Omega}{R_G} V_{DIFF} - \frac{V_{REF}}{4}$$

   where:
   V_{DIFF} is defined as the difference in input voltages,
   V_{DIFF} = VINP − VINM.
   V_{CM} is defined as the common-mode voltage,
   V_{CM} = (VINP + VINM)/2.
   If no gain setting resistor, R_G, is installed, set R_G to infinity.
3. Keep A within 10 mV of either supply rail. This is valid over the −40°C to +125°C temperature range.

   $$-V_S + 10\text{ mV} < A < +V_S - 10\text{ mV}$$

APPLICATIONS INFORMATION

AC-COUPLED INSTRUMENTATION AMPLIFIER

An integrator can be tied to the AD8235 in feedback to create a high-pass filter, as shown in Figure 43. This circuit can be used to reject dc voltages and offsets. At low frequencies, the impedance of the capacitor, C, is high. Therefore, the gain of the integrator is high. DC voltage at the output of the AD8235 is inverted and gained by the integrator. The inverted signal is injected back into the REF pin, nulling the output. In contrast, at high frequencies, the integrator has low gain because the impedance of C is low. Voltage changes at high frequencies are inverted but at a low gain. The signal is injected into the REF pins, but it is not enough to null the output. At very high frequencies, the capacitor appears as a short. The op amp is at unity gain. High frequency signals are, therefore, allowed to pass.

When a signal exceeds $f_{HIGH\text{-}PASS}$, the AD8235 outputs the high-pass filtered input signal.

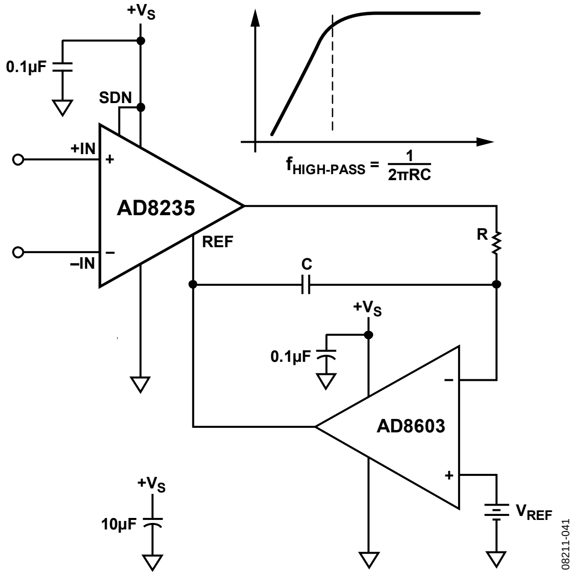

Figure 43. AC-Coupled Circuit

LOW POWER HEART RATE MONITOR

The low power and small size of the AD8235 make it an excellent choice for heart rate monitors. As shown in Figure 44, the AD8235 measures the biopotential signals from the body. It rejects common-mode signals and serves as the primary gain stage set at G = 5. The 4.7 µF capacitor and the 100 kΩ resistor set the −3 dB cutoff of the high-pass filter that follows the instrumentation amplifier. It rejects any differential dc offsets that may develop from the half-cell overpotential of the electrode.

A secondary gain stage, set at G = 403, amplifies the ECG signal, which is then sent into a second-order, low-pass, Bessel filter with −3 dB cutoff at 48 Hz. The 324 Ω resistor and 1 µF capacitor serve as an antialiasing filter. The 1 µF capacitor also serves as a charge reservoir for the ADC switched capacitor input stage.

This circuit was designed and tested using the AD8609, low power, quad op amp. The fourth op amp is configured as a Schmitt trigger to indicate if the right arm or left arm electrodes fall off the body. Used in conjunction with the 953 kΩ resistors at the inputs of the AD8235, the resistors pull the inputs apart when the electrodes fall off the body. The Schmitt trigger sends an active low signal to indicate a leads off condition.

The reference electrode (right leg) is set tied to ground. Likewise, the shield of the electrode cable is also tied to ground. Some portable heart rate monitors do not have a third electrode. In such cases, the negative input of the AD8235 can be tied to GND.

Note that this circuit is shown, solely, to demonstrate the capability of the AD8235. Additional effort must be made to ensure compliance with medical safety guidelines.

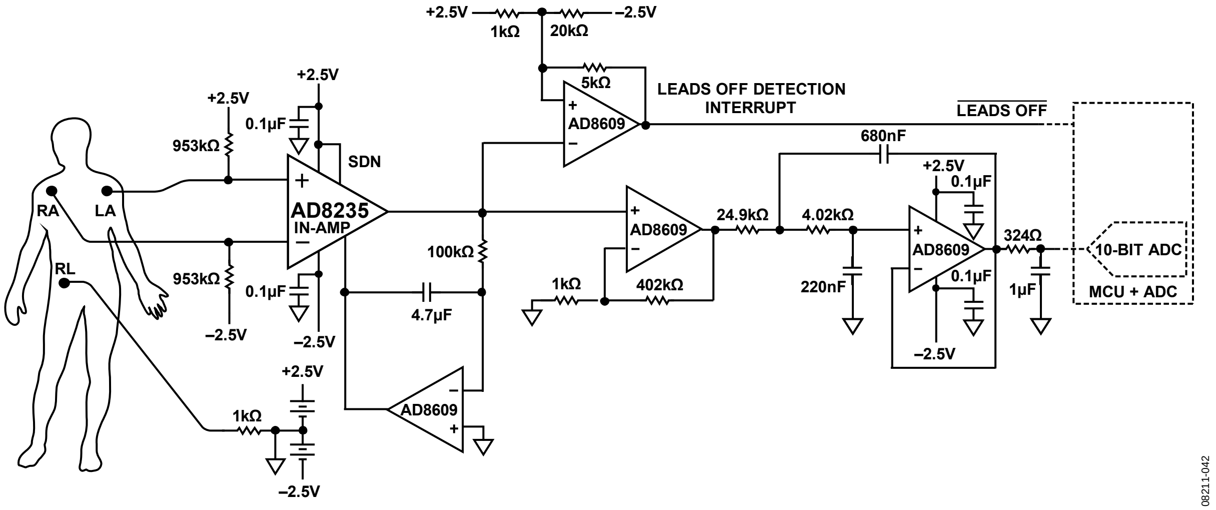

Figure 44. Example Low Power Heart Rate Monitor Schematic

OUTLINE DIMENSIONS

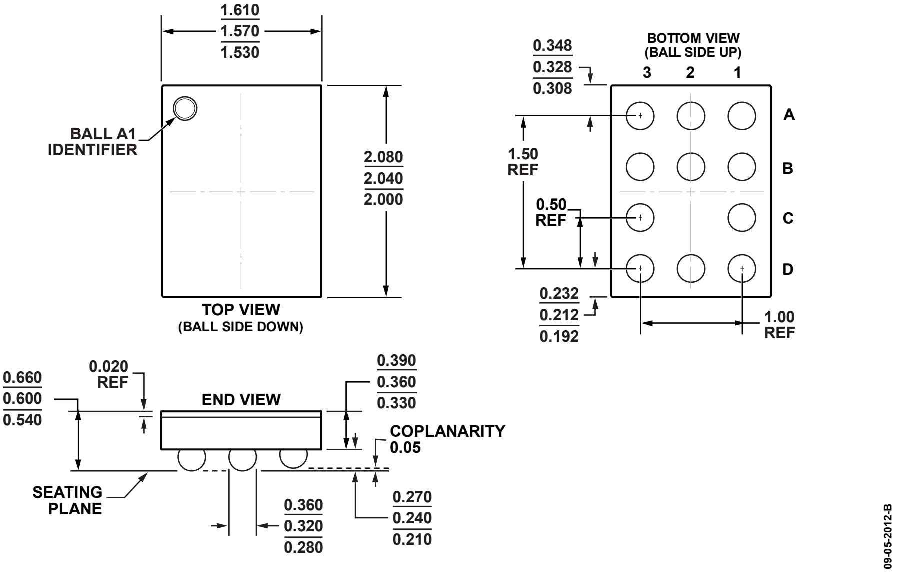

Figure 45. 11-Ball, Backside-Coated, Wafer Level Chip Scale Package [WLCSP] (CB-11-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option	Branding
AD8235ACBZ-P7	−40°C to + 125°C	11-Ball WLCSP	CB-11-1	H20

[1] Z = RoHS Compliant Part.