THE DATASHEET OF

ADG3246BRUZ-REEL7

2.5 V/3.3 V, 10-Bit, 2-Port Level Translating, Bus Switch

ADG3246

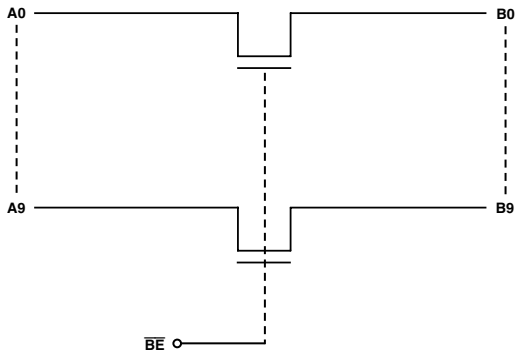
FEATURES

225 ps Propagation Delay through the Switch
4.5 Ω Switch Connection between Ports
Data Rate 1.244 Gbps
2.5 V/3.3 V Supply Operation
Selectable Level Shifting/Translation
Small Signal Bandwidth 610 MHz
Level Translation
  3.3 V to 2.5 V
  3.3 V to 1.8 V
  2.5 V to 1.8 V
24-Lead LFCSP Package

APPLICATIONS

3.3 V to 1.8 V Voltage Translation
3.3 V to 2.5 V Voltage Translation
2.5 V to 1.8 V Voltage Translation
Bus Switching
Bus Isolation
Hot Swap
Hot Plug
Analog Signal Switching

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADG3246 is a 2.5 V or 3.3 V, 10-bit, 2-port digital switch. It is designed on Analog Devices' low voltage CMOS process, which provides low power dissipation yet gives high switching speed and very low on resistance, allowing inputs to be connected to outputs without additional propagation delay or generating additional ground bounce noise.

The switches are enabled by means of the bus enable ($\overline{BE}$) input signal. These digital switches allow bidirectional signals to be switched when ON. In the OFF condition, signal levels up to the supplies are blocked.

This device is ideal for applications requiring level translation. When operated from a 3.3 V supply, level translation from 3.3 V inputs to 2.5 V outputs occurs. Similarly, if the device is operated from a 2.5 V supply and 2.5 V inputs are applied, the device will translate the outputs to 1.8 V. In addition to this, the ADG3246 has a level translating select pin ($\overline{SEL}$). When $\overline{SEL}$ is low, V_{CC} is reduced internally, allowing for level translation between 3.3 V inputs and 1.8 V outputs. This makes the device suited to applications requiring level translation between different supplies, such as converter to DSP/microcontroller interfacing.

PRODUCT HIGHLIGHTS

1. 3.3 V or 2.5 V supply operation
2. Extremely low propagation delay through switch
3. 4.5 Ω switches connect inputs to outputs
4. Level/voltage translation
5. 24-lead 4 mm × 4 mm LFCSP package

REV. A

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ADG3246–SPECIFICATIONS[1] (V_{CC} = 2.3 V to 3.6 V, GND = 0 V, all specifications T_{MIN} to T_{MAX}, unless otherwise noted.)

Parameter	Symbol	Conditions	B Version Min	B Version Typ[2]	B Version Max	Unit
DC ELECTRICAL CHARACTERISTICS						
Input High Voltage	V_{INH}	V_{CC} = 2.7 V to 3.6 V	2.0			V
	V_{INH}	V_{CC} = 2.3 V to 2.7 V	1.7			V
Input Low Voltage	V_{INL}	V_{CC} = 2.7 V to 3.6 V			0.8	V
	V_{INL}	V_{CC} = 2.3 V to 2.7 V			0.7	V
Input Leakage Current	I_I			±0.01	±1	µA
OFF State Leakage Current	I_{OZ}	0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
ON State Leakage Current		0 ≤ A, B ≤ V_{CC}		±0.01	±1	µA
Maximum Pass Voltage	V_P	V_A/V_B = V_{CC} = $\overline{SEL}$ = 3.3 V, I_O = –5 µA	2.0	2.5	2.9	V
		V_A/V_B = V_{CC} = $\overline{SEL}$ = 2.5 V, I_O = –5 µA	1.5	1.8	2.1	V
		V_A/V_B = V_{CC} = 3.3 V, $\overline{SEL}$ = 0 V, I_O = –5 µA	1.5	1.8	2.1	V
CAPACITANCE[3]						
A Port Off Capacitance	C_A OFF	f = 1 MHz		5		pF
B Port Off Capacitance	C_B OFF	f = 1 MHz		5		pF
A, B Port On Capacitance	C_A, C_B ON	f = 1 MHz		10		pF
Control Input Capacitance	C_{IN}	f = 1 MHz		6		pF
SWITCHING CHARACTERISTICS[3]						
Propagation Delay A to B or B to A, t_{PD}[4]	t_{PHL}, t_{PLH}	C_L = 50 pF, V_{CC} = $\overline{SEL}$ = 3 V			0.225	ns
Propagation Delay Matching[5]					22.5	ps
Bus Enable Time $\overline{BE}$ to A or B[6]	t_{PZH}, t_{PZL}	V_{CC} = 3.0 V to 3.6 V; $\overline{SEL}$ = V_{CC}	1	3.2	4.8	ns
Bus Disable Time $\overline{BE}$ to A or B[6]	t_{PHZ}, t_{PLZ}	V_{CC} = 3.0 V to 3.6 V; $\overline{SEL}$ = V_{CC}	1	3.2	4.8	ns
Bus Enable Time $\overline{BE}$ to A or B[6]	t_{PZH}, t_{PZL}	V_{CC} = 3.0 V to 3.6 V; $\overline{SEL}$ = 0 V	0.5	2.2	3.3	ns
Bus Disable Time $\overline{BE}$ to A or B[6]	t_{PHZ}, t_{PLZ}	V_{CC} = 3.0 V tp 3.6 V; $\overline{SEL}$ = 0 V	0.5	1.7	2.9	ns
Bus Enable Time $\overline{BE}$ to A or B[6]	t_{PZH}, t_{PZL}	V_{CC} = 2.3 V to 2.7 V; $\overline{SEL}$ = V_{CC}	0.5	2.2	3	ns
Bus Disable Time $\overline{BE}$ to A or B[6]	t_{PHZ}, t_{PLZ}	V_{CC} = 2.3 V to 2.7 V; $\overline{SEL}$ = V_{CC}	0.5	1.75	2.6	ns
Maximum Data Rate		V_{CC} = $\overline{SEL}$ = 3.3 V; V_A/V_B = 2 V		1.244		Gbps
Channel Jitter		V_{CC} = $\overline{SEL}$ = 3.3 V; V_A/V_B = 2 V		50		ps p-p
Operating Frequency—Bus Enable	$f_{\overline{BE}}$				10	MHz
DIGITAL SWITCH						
On Resistance	R_{ON}	V_{CC} = 3 V, $\overline{SEL}$ = V_{CC}, V_A = 0 V, I_{BA} = 8 mA		4.5	8	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = V_{CC}, V_A = 1.7 V, I_{BA} = 8 mA		15	28	Ω
		V_{CC} = 2.3 V, $\overline{SEL}$ = V_{CC}, V_A = 0 V, I_{BA} = 8 mA		5	9	Ω
		V_{CC} = 2.3 V, $\overline{SEL}$ = V_{CC}, V_A = 1 V, I_{BA} = 8 mA		11	18	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 0 V, I_{BA} = 8 mA		5	8	Ω
		V_{CC} = 3 V, $\overline{SEL}$ = 0 V, V_A = 1 V, I_{BA} = 8 mA		14		Ω
On Resistance Matching	ΔR_{ON}	V_{CC} = 3 V, $\overline{SEL}$ = V_{CC}, V_A = 0 V, I_{BA} = 8 mA		0.45		Ω
		V_{CC} = 3 V, $\overline{SEL}$ = V_{CC}, V_A = 1 V, I_{BA} = 8 mA		0.65		Ω
POWER REQUIREMENTS						
V_{CC}			2.3		3.6	V
Quiescent Power Supply Current	I_{CC}	Digital Inputs = 0 V or V_{CC}; $\overline{SEL}$ = V_{CC}		0.001	1	µA
	I_{CC}	Digital Inputs = 0 V or V_{CC}; $\overline{SEL}$ = 0 V		0.65	1.2	mA
Increase in I_{CC} per Input[7]	ΔI_{CC}	V_{CC} = 3.6 V, $\overline{BE}$ = 3.0 V; $\overline{SEL}$ = V_{CC}			130	µA

NOTES

[1]Temperature range is as follows: B Version: –40°C to +85°C.

[2]Typical values are at 25°C, unless otherwise stated.

[3]Guaranteed by design, not subject to production test.

[4]The digital switch contributes no propagation delay other than the RC delay of the typical R_{ON} of the switch and the load capacitance when driven by an ideal voltage source. Since the time constant is much smaller than the rise/fall times of typical driving signals, it adds very little propagation delay to the system. Propagation delay of the digital switch when used in a system is determined by the driving circuit on the driving side of the switch and its interaction with the load on the driven side.

[5]Propagation delay matching between channels is calculated from the on resistance matching and load capacitance of 50 pF.

[6]See Timing Measurement Information section.

[7]This current applies to the control pin ($\overline{BE}$) only. The A and B ports contribute no significant ac or dc currents as they transition.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS*

(T_A = 25°C, unless otherwise noted.)

V_{CC} to GND . . . . . –0.5 V to +4.6 V
Digital Inputs to GND . . . . . –0.5 V to +4.6 V
DC Input Voltage . . . . . –0.5 V to +4.6 V
DC Output Current . . . . . 25 mA per channel
Operating Temperature Range
Industrial (B Version) . . . . . –40°C to +85°C
Storage Temperature Range . . . . . –65°C to +150°C
Junction Temperature . . . . . 150°C
LFCSP Package
θ_{JA} Thermal Impedance . . . . . 35°C/W
Lead Temperature, Soldering (10 seconds) . . . . . 300°C
IR Reflow, Peak Temperature (<20 seconds) . . . . . 235°C

*Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG3246BCPZ	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10
ADG3246BCPZ-REEL7	–40°C to +85°C	24-Lead Lead Frame Chip Scale Package [LFCSP]	CP-24-10

[1] Z = RoHS Compliant Part.

Table I. Pin Description

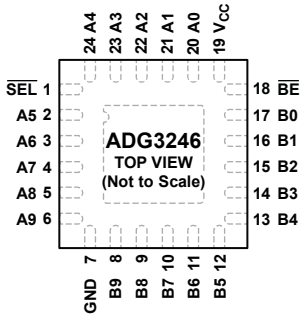
Mnemonic	Description
$\overline{BE}$	Bus Enable (Active Low)
$\overline{SEL}$	Level Translation Select
Ax	Port A, Inputs or Outputs
Bx	Port B, Inputs or Outputs
EPAD	Exposed Pad. It is recommended that the exposed pad be thermally connected to a copper plane for enhanced thermal performance. The pad should be grounded as well.

Table II. Truth Table

$\overline{BE}$	$\overline{SEL}$*	Function
L	L	A = B, 3.3 V to 1.8 V Level Shifting
L	H	A = B, 3.3 V to 2.5 V/2.5 V to 1.8 V Level Shifting
H	X	Disconnect

*$\overline{SEL}$ = 0 only when V_{DD} = 3.3 V ± 10%

PIN CONFIGURATION
24-Lead LFCSP



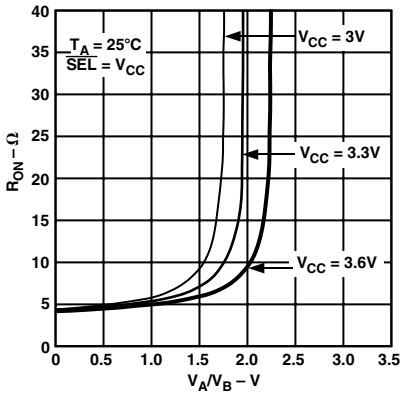
NOTES
1. IT IS RECOMMENDED THAT THE EXPOSED PAD BE THERMALLY CONNECTED TO A COPPER PLANE FOR ENHANCED THERMAL PERFORMANCE. THE PAD SHOULD BE GROUNDED AS WELL.

CAUTION

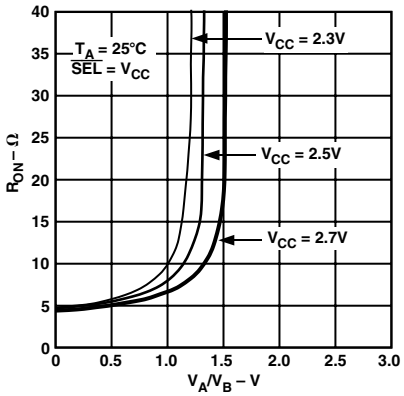
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG3246 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

TERMINOLOGY

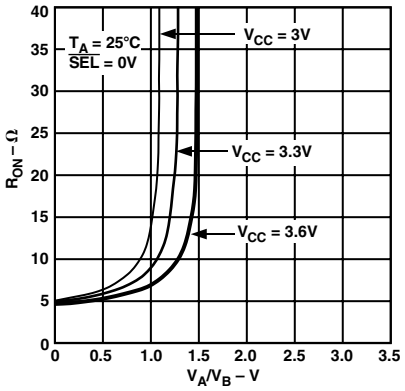
V_{CC}	Positive Power Supply Voltage.
GND	Ground (0 V) Reference.
V_{INH}	Minimum Input Voltage for Logic 1.
V_{INL}	Maximum Input Voltage for Logic 0.
I_I	Input Leakage Current at the Control Inputs.
I_{OZ}	OFF State Leakage Current. It is the maximum leakage current at the switch pin in the OFF state.
I_{OL}	ON State Leakage Current. It is the maximum leakage current at the switch pin in the ON state.
V_P	Maximum Pass Voltage. The maximum pass voltage relates to the clipped output voltage of an NMOS device when the switch input voltage is equal to the supply voltage.
R_{ON}	Ohmic Resistance Offered by a Switch in the ON State. It is measured at a given voltage by forcing a specified amount of current through the switch.
ΔR_{ON}	On Resistance Match between Any Two Channels, i.e., R_{ON} Max – R_{ON} Min.
C_X OFF	OFF Switch Capacitance.
C_X ON	ON Switch Capacitance.
C_{IN}	Control Input Capacitance. This consists of $\overline{BE}$ and $\overline{SEL}$.
I_{CC}	Quiescent Power Supply Current. It is measured when all control inputs are at a logic HIGH or LOW level and the switches are OFF.
ΔI_{CC}	Extra power supply current component for the $\overline{BE}$ control input when the input is not criven at the supplies.
t_{PLH}, t_{PHL}	Data Propagation Delay through the Switch in the ON State. Propagation delay is related to the RC time constant $R_{ON} \times C_L$, where C_L is the load capacitance.
t_{PZH}, t_{PZL}	Bus Enable Times. These are times taken to cross the V_T voltage at the switch output when the switch turns on in response to the control signal, $\overline{BE}$.
t_{PHZ}, t_{PLZ}	Bus Disable Times. This is the time taken to place the switch in the high impedance OFF state in response to the control signal. It is measured as the time taken for the output voltage to change by V_Δ from the original quiescent level, with reference to the logic level transition at the control input. (Refer to Figure 3 for enable and disable times.)
Max Data Rate	Maximum Rate at which Data Can Be Passed through the Switch.
Channel Jitter	Peak-to-Peak Value of the Sum of the Deterministic and Random Jitter of the Switch Channel.
$f_{\overline{BE}}$	Operating Frequency of Bus Enable. This is the maximum frequency at which bus enable ($\overline{BE}$) can be toggled.



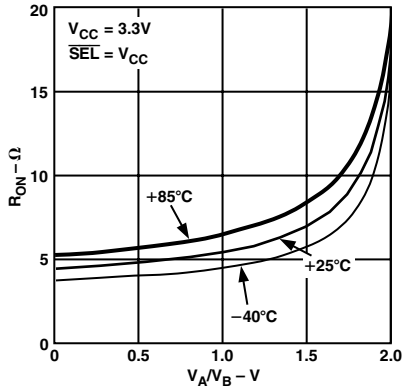
TPC 1. On Resistance vs. Input Voltage



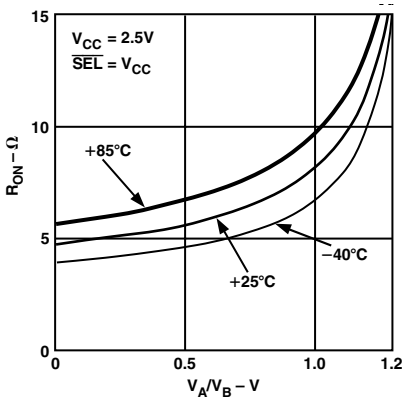
TPC 2. On Resistance vs. Input Voltage



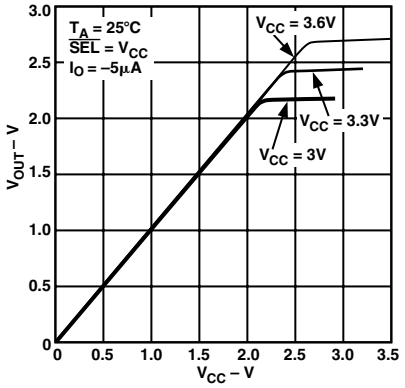
TPC 3. On Resistance vs. Input Voltage



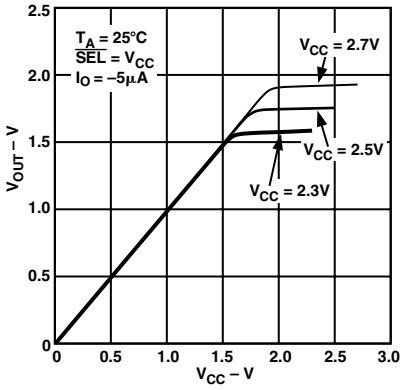
TPC 4. On Resistance vs. Input Voltage for Different Temperatures



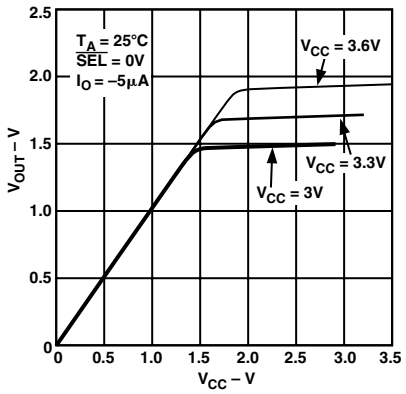
TPC 5. On Resistance vs. Input Voltage for Different Temperatures



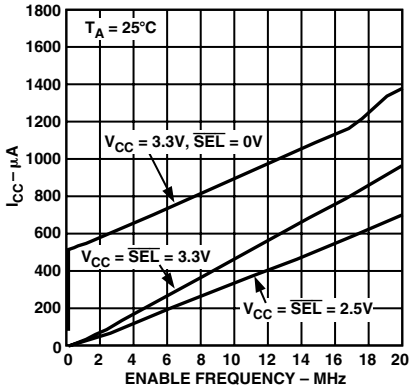
TPC 6. Pass Voltage vs. V_{CC}



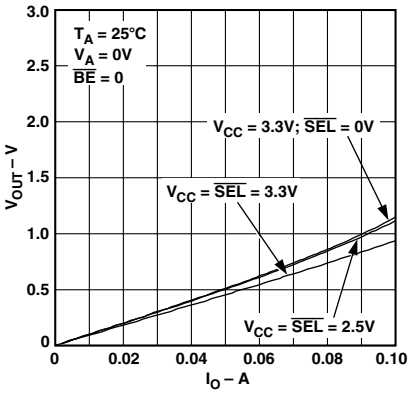
TPC 7. Pass Voltage vs. V_{CC}



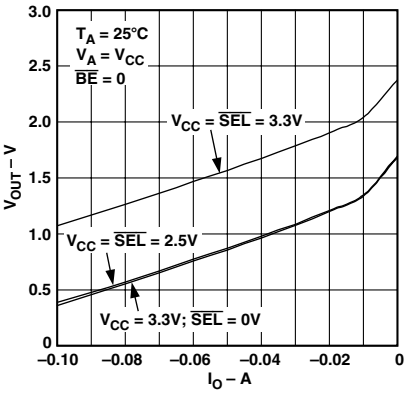
TPC 8. Pass Voltage vs. V_{CC}



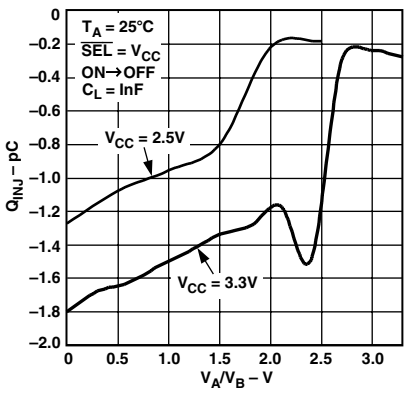
TPC 9. I_{CC} vs. Enable Frequency



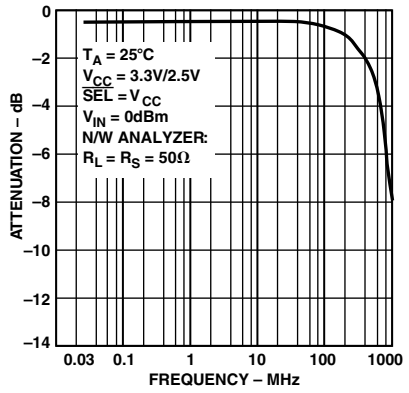
TPC 10. Output Low Characteristic



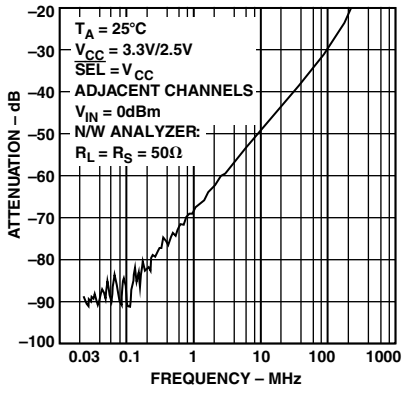
TPC 11. Output High Characteristic



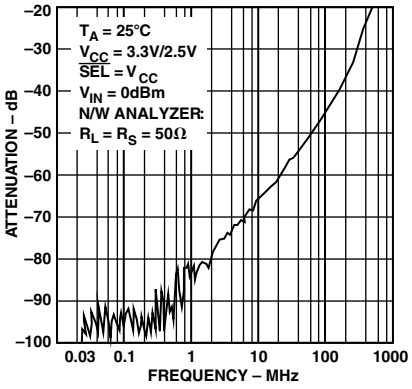
TPC 12. Charge Injection vs. Source Voltage



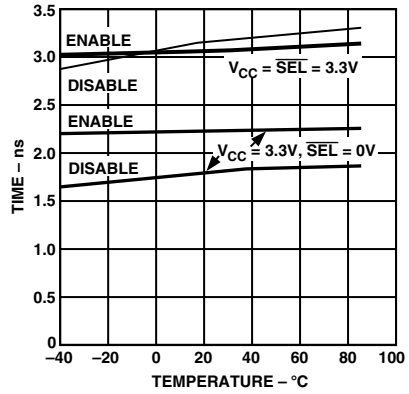
TPC 13. Bandwidth vs. Frequency



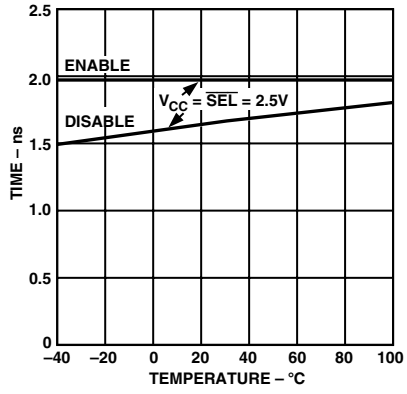
TPC 14. Crosstalk vs. Frequency



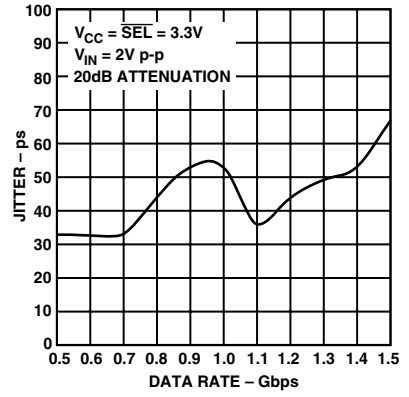
TPC 15. Off Isolation vs. Frequency



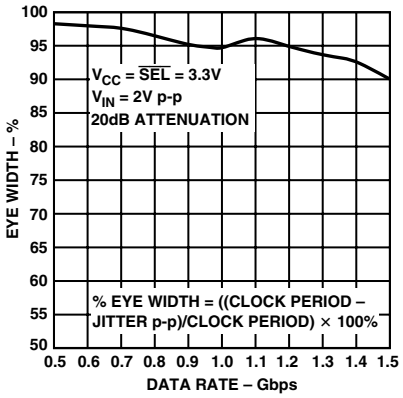
TPC 16. Enable/Disable Time vs. Temperature



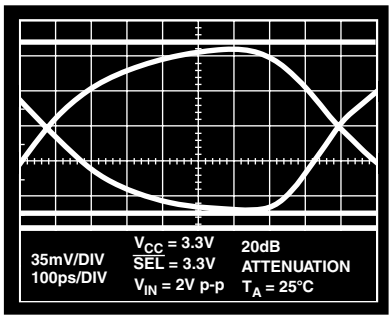
TPC 17. Enable/Disable Time vs. Temperature



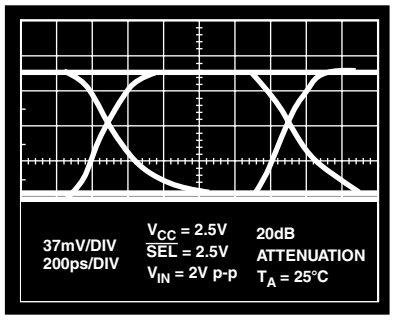
TPC 18. Jitter vs. Data Rate; PRBS 31



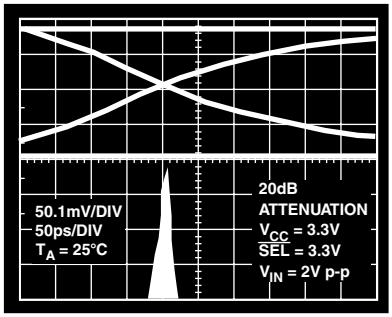
TPC 19. Eye Width vs. Data Rate; PRBS 31



TPC 20. Eye Pattern; 1.244 Gbps, V_{CC} = 3.3 V, PRBS 31



TPC 21. Eye Pattern; 1 Gbps, V_{CC} = 2.5 V, PRBS 31

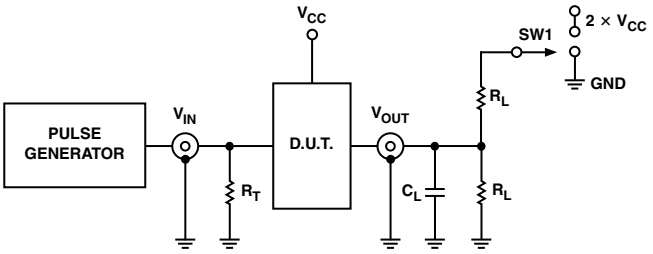


TPC 22. Jitter @ 1.244 Gbps, PRBS 31

TIMING MEASUREMENT INFORMATION

For the following load circuit and waveforms, the notation that is used is V_{IN} and V_{OUT} where

$$V_{IN} = V_A \text{ and } V_{OUT} = V_B \text{ or } V_{IN} = V_B \text{ and } V_{OUT} = V_A$$



NOTES
PULSE GENERATOR FOR ALL PULSES: $t_R \leq 2.5$ns, $t_F \leq 2.5$ns, FREQUENCY $\leq$ 10MHz.
C_L INCLUDES BOARD, STRAY, AND LOAD CAPACITANCES.
R_T IS THE TERMINATION RESISTOR, SHOULD BE EQUAL TO Z_{OUT} OF THE PULSE GENERATOR.

Figure 1. Load Circuit

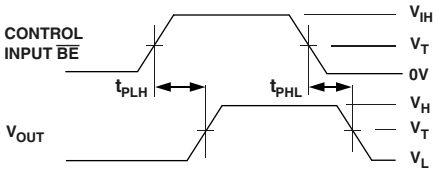


Figure 2. Propagation Delay

Test Conditions

Symbol	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 2.5 V ± 0.2 V ($\overline{SEL}$ = V_{CC})	V_{CC} = 3.3 V ± 0.3 V ($\overline{SEL}$ = 0 V)	Unit
R_L	500	500	500	Ω
V_Δ	300	150	150	mV
C_L	50	30	30	pF
V_T	1.5	0.9	0.9	V

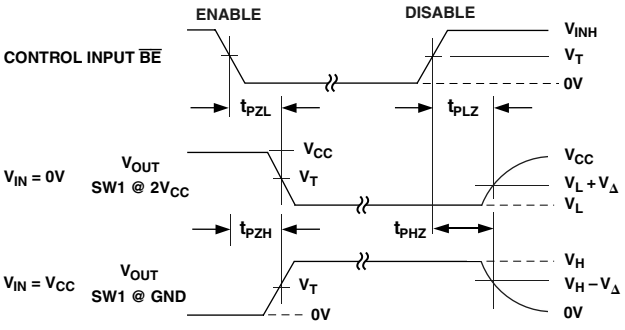


Figure 3. Enable and Disable Times

Table III. Switch Position

TEST	S1
t_{PLZ}, t_{PZL}	2 × V_{CC}
t_{PHZ}, t_{PZH}	GND

BUS SWITCH APPLICATIONS

Mixed Voltage Operation, Level Translation

Bus switches can be used to provide an ideal solution for interfacing between mixed voltage systems. The ADG3246 is suitable for applications where voltage translation from 3.3 V technology to a lower voltage technology is needed. This device can translate from 3.3 V to 1.8 V, from 2.5 V to 1.8 V, or from 3.3 V directly to 2.5 V.

Figure 4 shows a block diagram of a typical application in which a user needs to interface between a 3.3 V ADC and a 2.5 V microprocessor. The microprocessor may not have 3.3 V tolerant inputs, therefore placing the ADG3246 between the two devices allows the devices to communicate easily. The bus switch directly connects the two blocks, thus introducing minimal propagation delay, timing skew, or noise.

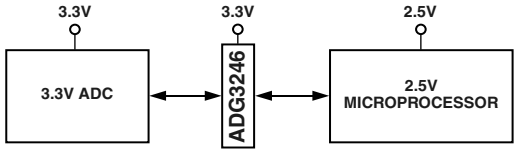


Figure 4. Level Translation between a 3.3 V ADC and a 2.5 V Microprocessor

3.3 V to 2.5 V Translation

When V_{CC} is 3.3 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to within a voltage threshold below the V_{CC} supply.

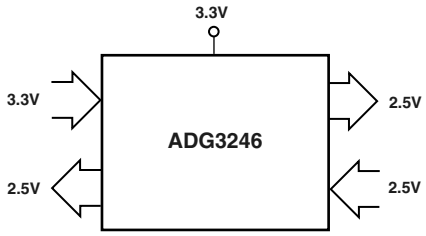


Figure 5. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output will be limited to 2.5 V, as shown in Figure 6.

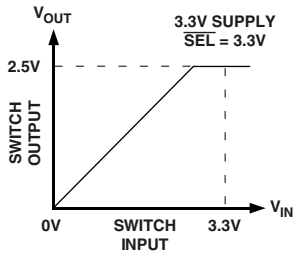


Figure 6. 3.3 V to 2.5 V Voltage Translation, $\overline{SEL}$ = V_{CC}

This device can be used for translation from 2.5 V to 3.3 V devices and also between two 3.3 V devices.

2.5 V to 1.8 V Translation

When V_{CC} is 2.5 V ($\overline{SEL}$ = V_{CC}) and the input signal range is 0 V to V_{CC}, the maximum output signal will, as before, be clamped to within a voltage threshold below the V_{CC} supply.

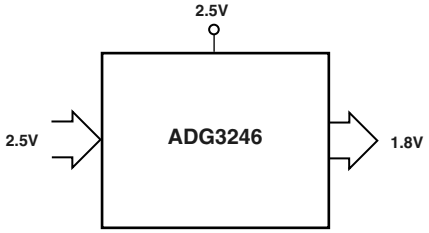


Figure 7. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

In this case, the output will be limited to approximately 1.8 V, as shown in Figure 7.

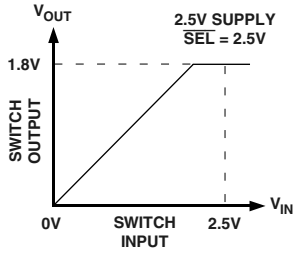


Figure 8. 2.5 V to 1.8 V Voltage Translation, $\overline{SEL}$ = V_{CC}

3.3 V to 1.8 V Translation

The ADG3246 offers the option of interfacing between a 3.3 V device and a 1.8 V device. This is possible through use of the $\overline{SEL}$ pin.

$\overline{SEL}$ pin: An active low control pin. $\overline{SEL}$ activates internal circuitry in the ADG3246 that allows voltage translation between 3.3 V devices and 1.8 V devices.

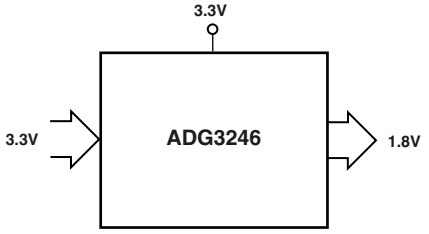


Figure 9. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

When V_{CC} is 3.3 V and the input signal range is 0 V to V_{CC}, the maximum output signal will be clamped to 1.8 V, as shown in Figure 9. To do this, the $\overline{SEL}$ pin must be tied to Logic 0. If $\overline{SEL}$ is unused, it should be tied directly to V_{CC}.

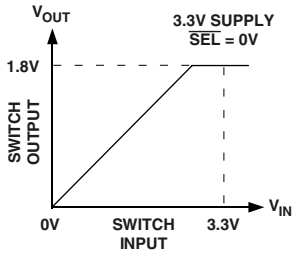


Figure 10. 3.3 V to 1.8 V Voltage Translation, $\overline{SEL}$ = 0 V

Bus Isolation

A common requirement of bus architectures is low capacitance loading of the bus. Such systems require bus bridge devices that extend the number of loads on the bus without exceeding the specifications. Because the ADG3246 is designed specifically for applications that do not need drive yet require simple logic functions, it solves this requirement. The device isolates access to the bus, thus minimizing capacitance loading.

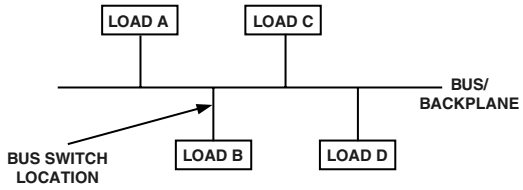


Figure 11. Location of Bus Switched in a Bus Isolation Application

Hot Plug and Hot Swap Isolation

The ADG3246 is suitable for hot swap and hot plug applications. The output signal of the ADG3246 is limited to a voltage that is below the V_{CC} supply, as shown in Figures 6, 8, and 10. Therefore the switch acts like a buffer to take the impact from hot insertion, protecting vital and expensive chipsets from damage.

In hot-plug applications, the system cannot be shutdown when new hardware is being added. To overcome this, a bus switch can be positioned on the backplane between the bus devices and the hot plug connectors. The bus switch is turned off during hot plug. Figure 12 shows a typical example of this type of application.

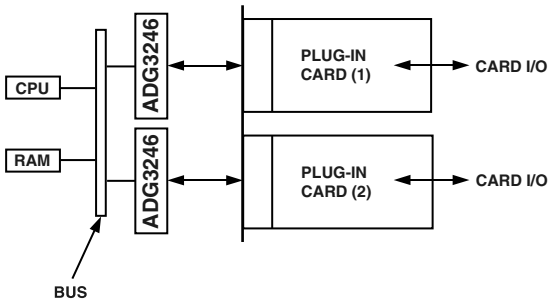


Figure 12. ADG3246 in a Hot Plug Application

There are many systems that require the ability to handle hot swapping, such as docking stations, PCI boards for servers, and line cards for telecommunications switches. If the bus can be isolated prior to insertion or removal, then there is more control over the hot swap event. This isolation can be achieved using a bus switch. The bus switches are positioned on the hot swap card between the connector and the devices. During hot swap, the ground pin of the hot swap card must connect to the ground pin of the back plane before any other signal or power pins.

Analog Switching

Bus switches can be used in many analog switching applications; for example, video graphics. Bus switches can have lower on resistance, smaller ON and OFF channel capacitance and thus improved frequency performance than their analog counterparts. The bus switch channel itself consisting solely of an NMOS switch limits the operating voltage (see TPC 1 for a typical plot), but in many cases, this does not present an issue.

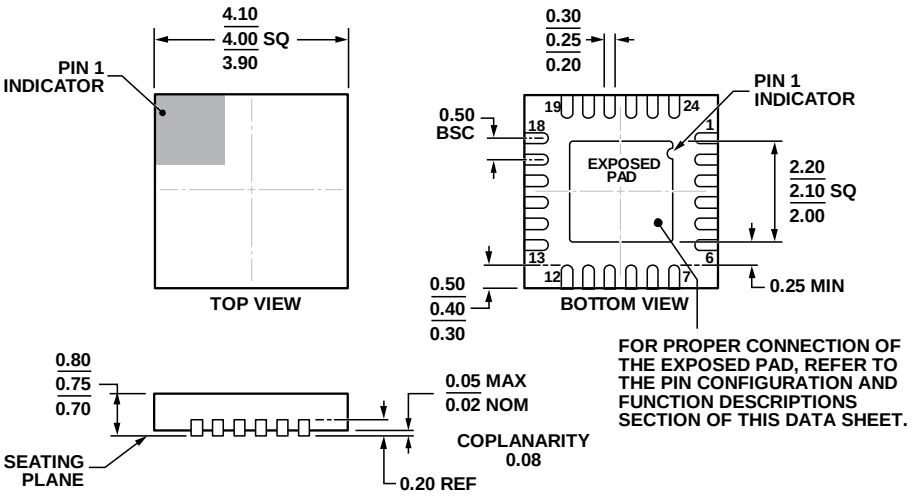
High Impedance During Power-Up/Power-Down

To ensure the high impedance state during power-up or power-down, $\overline{BE}$ should be tied to V_{CC} through a pull-up resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

PACKAGE AND PINOUT

The ADG3246 is packaged in a tiny 24-lead LFCSP package. The area of the LFCSP option is 16 mm^2. This makes the LFCSP option an excellent choice for space-constrained applications.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-220-WGGD-8.

Figure 13. 24-Lead Lead Frame Chip Scale Package [LFCSP]
4 x 4 mm Body and 0.75 mm Package Height
(CP-24-10)
Dimensions shown in millimeters

REVISION HISTORY

3/16—Rev. 0 to Rev. A

Deleted 24-Lead TSSOP Package..... Universal
Changes to Ordering Guide, Table 1, and LFCSP
Pin Configuration 3
Change to Mixed Voltage Operation, Level Translation Section.....9
Updated Outline Dimensions.....11

D03012-0-3/16(A)

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