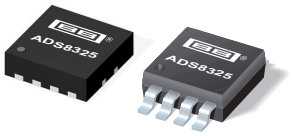
THE DATASHEET OF

ADS8325IDGKTG4

www.win-source.net 0086-755-83957316



SBAS226C – MARCH 2002 – REVISED AUGUST 2007

16-Bit, High-Speed, 2.7V to 5.5V *micro*Power Sampling ANALOG-TO-DIGITAL CONVERTER

FEATURES

- **16-Bits No Missing Codes**
- **Very Low Noise: 3LSB$_{PP}$**
- **Excellent Linearity: ±1.5LSB typ**
- ***micro*Power:**
  - **4.5mW at 100kHz**
  - **1mW at 10kHz**
- **MSOP-8 and SON-8 Packages (SON Package Size Same as 3x3 QFN)**
- **16-Bit Upgrade to the 12-Bit ADS7816 and ADS7822**
- **Pin-Compatible With the ADS7816, ADS7822, ADS7826, ADS7827, ADS7829, and ADS8320**
- **Serial (SPI™/SSI) Interfaces**

APPLICATIONS

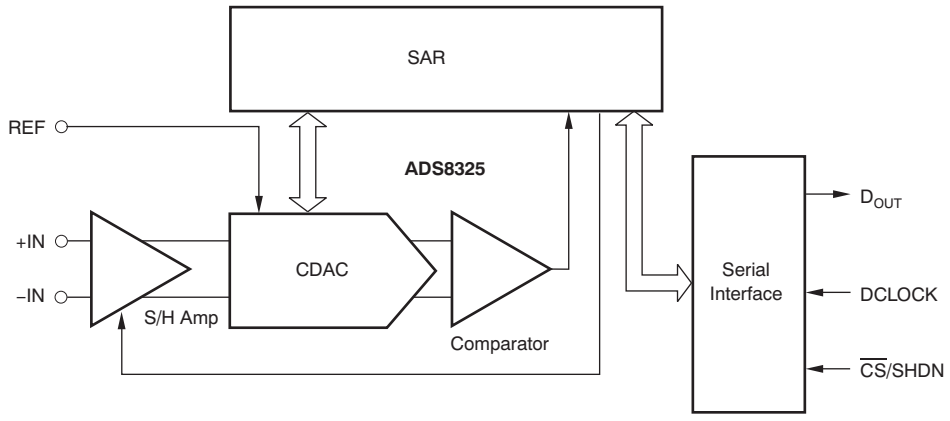
- **Battery-Operated Systems**
- **Remote Data Acquisition**
- **Isolated Data Acquisition**
- **Simultaneous Sampling, Multi-Channel Systems**
- **Industrial Controls**
- **Robotics**
- **Vibration Analysis**

DESCRIPTION

The ADS8325 is a 16-bit, sampling, Analog-to-Digital (A/D) converter specified for a supply voltage range from 2.7V to 5.5V. It requires very little power, even when operating at the full 100kHz data rate. At lower data rates, the high speed of the device enables it to spend most of its time in the power-down mode. For example, the average power dissipation is less than 1mW at a 10kHz data rate.

The ADS8325 offers excellent linearity and very low noise and distortion. It also features a synchronous serial (SPI/SSI compatible) interface and a differential input. The reference voltage can be set to any level within the range of 2.5V to V_{DD}.

Low power and small size make the ADS8325 ideal for portable and battery-operated systems. It is also a perfect fit for remote data acquisition modules, simultaneous multichannel systems, and isolated data acquisition. The ADS8325 is available in MSOP-8 and SON-8 packages. The SON package size is the same as a 3x3 QFN package.



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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	MAXIMUM INTEGRAL LINEARITY ERROR (LSB)	NO MISSING CODES ERROR (LSB)(2)	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
ADS8325I	±6	15	MSOP-8	DGK	–40°C to +85°C	B25	ADS8325IDGKT	Tape and Reel, 250
							ADS8325IDGKR	Tape and Reel, 2500
ADS8325IB	±4	16	MSOP-8	DGK	–40°C to +85°C	B25	ADS8325IBDGKT	Tape and Reel, 250
							ADS8325IBDGKR	Tape and Reel, 2500
ADS8325I	±6	15	SON-8	DRB	–40°C to +85°C	B25	ADS8325IDRBT	Tape and Reel, 250
							ADS8325IDRBR	Tape and Reel, 2500
ADS8325IB	±4	16	SON-8	DRB	–40°C to +85°C	B25	ADS8325IBDRBT	Tape and Reel, 250
							ADS8325IBDRBR	Tape and Reel, 2500

(1) For the most current specifications and package information, refer to our web site at www.ti.com.
(2) No Missing Codes Error specifies a 5V power supply and reference voltage.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range (unless otherwise noted)

		ADS8325	UNIT
	Supply voltage, DGND to V_{DD}	–0.3 to 6	V
	Analog input voltage(2)	–0.3 to V_{DD} + 0.3	V
	Reference input voltage(2)	–0.3 to V_{DD} + 0.3	V
	Digital input voltage(2)	–0.3 to V_{DD} + 0.3	V
	Input current to any pin except supply	–20 to 20	mA
	Power dissipation	See Dissipation Rating Table	
T_J	Operating virtual junction temperature range	–40 to +150	°C
T_A	Operating free-air temperature range	–40 to +85	°C
T_{STG}	Storage temperature range	–65 to +150	°C
	Lead temperature 1,6 mm (1/16 inch) from case for 10 sec	+260	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions of extended periods may affect device reliability.
(2) All voltage values are with respect to ground terminal.

PACKAGE DISSIPATION RATINGS

PACKAGE	$R_{\theta JC}$	$R_{\theta JA}$	DERATING FACTOR ABOVE T_A = +25°C	$T_A \le$ +25°C POWER RATING	T_A = +70°C POWER RATING	T_A = +85°C POWER RATING
DGK	39.1°C/W	206.3°C/W	4.847mW/°C	606mW	388mW	315mW
DRB	5°C/W	45.8°C/W	3.7mW/C	370mW	204mW	148mW

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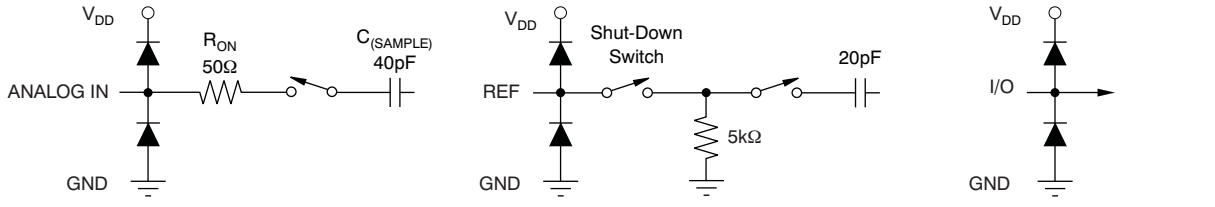
EQUIVALENT INPUT CIRCUIT



Diode Turn-On Voltage: 0.35V
Equivalent Analog Input Circuit

Equivalent Reference
Input Circuit

Equivalent Digital Input/Output Circuit

RECOMMENDED OPERATING CONDITIONS

Over operating free-air temperature range (unless otherwise noted)

			MIN	TYP	MAX	UNIT
	Supply voltage, GND to V_{DD}	Low-voltage levels	2.7		3.6	V
		5V logic levels	4.5	5.0	5.5	V
	Reference input voltage		2.5		V_{DD}	V
	Analog input voltage	–IN	–0.3	0	0.5	V
		+IN – (–IN)	0		V_{REF}	V
T_J	Operating junction temperature range		–40		+125	°C

ELECTRICAL CHARACTERISTICS: V_{DD} = +5 V

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = 5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8325I			ADS8325IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Full-scale range	FSR	+IN – (–IN)	0		V_{REF}	0		V_{REF}	V
Operating common-mode signal			–0.3		0.5	–0.3		0.5	V
Input resistance		–IN = GND		5			5		GΩ
Input capacitance		–IN = GND, during sampling		45			45		pF
Input leakage current		–IN = GND		±50			±50		nA
Differential input capacitance		+IN to –IN, during sampling		20			20		pF
Full-power bandwidth	FSBW	FS sinewave, SINAD = –3dB		20			20		kHz
DC ACCURACY									
Resolution			16			16			Bits
No missing code	NMC		15			16			Bits
Integral linearity error	INL			±3	±6		±1.5	±4	LSB
Offset error	V_{OS}			±0.75	±1.5		±0.5	±1	mV
Offset error drift	TCV_{OS}			±0.2			±0.2		ppm/°C
Gain error	G_{ERR}				±24			±12	LSB
Gain error drift	TCG_{ERR}			±3			±3		ppm/°C
Noise				20			20		μVRMS
Power-supply rejection		4.75V ≤ V_{DD} ≤ 5.25V		3			3		LSB
SAMPLING DYNAMICS									
Conversion time	t_{CONV}	24kHz < f_{CLK} ≤ 2.4MHz	6.667		666.7	6.667		666.7	μs
Acquisition time	t_{AQ}	f_{CLK} = 2.4MHz	1.875			1.875			μs
Throughput rate					100			100	kSPS
Clock frequency			0.024		2.4	0.024		2.4	MHz
AC ACCURACY									

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ELECTRICAL CHARACTERISTICS: V_{DD} = +5 V (continued)

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = 5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8325I			ADS8325IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Total harmonic distortion	THD	$5V_{PP}$ sinewave, at 1kHz		–100			–106		dB
Spurious-free dynamic range	SFDR	$5V_{PP}$ sinewave, at 1kHz		–100			–108		dB
Signal-to-noise ratio	SNR			–90			–91		dB
Signal-to-noise + distortion	SINAD	$5V_{PP}$ sinewave, at 1kHz		–90			–91		dB
Effective number of bits	ENOB			14.6			14.7		Bits
VOLTAGE REFERENCE INPUT									
Reference voltage			2.5		V_{DD} + 0.3	2.5		V_{DD} + 0.3	V
Reference input resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5		kΩ
		$\overline{CS}$ = V_{DD}		5			5		GΩ
Reference input capacitance				20			20		pF
Reference input current				1	1.5		1	1.5	mA
		$\overline{CS}$ = V_{DD}		0.1			0.1		μA
DIGITAL INPUTS(1)									
Logic family				CMOS			CMOS		
High-level input voltage	V_{IH}		0.7 × V_{DD}		V_{DD} + 0.3	0.7 × V_{DD}		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}		–0.3		0.3 × V_{DD}	–0.3		0.3 × V_{DD}	V
Input current	I_{IN}	V_I = V_{DD} or GND			±50			±50	nA
Input capacitance	C_I			5			5		pF
DIGITAL OUTPUTS(1)									
Logic family				CMOS			CMOS		
High-level output voltage	V_{OH}	V_{DD} = 4.5V, I_{OH} = –100μA	4.44			4.44			V
Low-level output voltage	V_{OL}	V_{DD} = 4.5V, I_{OL} = 100μA			0.5			0.5	V
High-impedance-state output current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND			±50			±50	nA
Output capacitance	C_O			5			5		pF
Load capacitance	C_L				30			30	pF
Data format				Straight Binary			Straight Binary		

(1) Applies for 5.0V nominal supply: V_{DD} (min) = 4.5V and V_{DD} (max) = 5.5V.

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ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = +2.5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8325I			ADS8325IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
ANALOG INPUT									
Full-scale range	FSR	+IN – (–IN)	0		V_{REF}	0		V_{REF}	V
Operating common-mode signal			–0.3		0.5	–0.3		0.5	V
Input resistance		–IN = GND		5			5		GΩ
Input capacitance		–IN = GND, during sampling		45			45		pF
Input leakage current		–IN = GND		±50			±50		nA
Differential input capacitance		+IN to –IN, during sampling		20			20		pF
Full-power bandwidth	FSBW	FS sinewave, SINAD = –3 dB		4			4		kHz
DC ACCURACY									
Resolution			16			16			Bits
No missing code	NMC		14			15			Bits
Integral linearity error	INL			±3	±6		±1.5	±4	LSB
Offset error	V_{OS}			±0.75	±1.5		±0.5	±1	mV
Offset error drift	TCV_{OS}			±3			±3		ppm/°C
Gain error	G_{ERR}			±33			±16		LSB
Gain error drift	TCG_{ERR}			±0.3			±0.3		ppm/°C
Noise				20			20		μVRMS
Power-supply rejection		2.7V ≤ V_{DD} ≤ 3.6V		7			7		LSB
SAMPLING DYNAMICS									
Conversion time	t_{CONV}	24kHz < f_{CLK} ≤ 2.4MHz	6.667		666.7	6.667		666.7	μs
Acquisition time	t_{AQ}	f_{CLK} = 2.4MHz	1.875			1.875			μs
Throughput rate					100			100	kSPS
Clock frequency			0.024		2.4	0.024		2.4	MHz
AC ACCURACY									
Total harmonic distortion	THD	2.5V_{PP} sinewave, at 1kHz		–94			–94		dB
Spurious-free dynamic range	SFDR	2.5V_{PP} sinewave, at 1kHz		–96			–96		dB
Signal-to-noise ratio	SNR			–85			–86		dB
Signal-to-noise + distortion	SINAD	2.5V_{PP} sinewave, at 1kHz		–85			–85.5		dB
Effective number of bits	ENOB			13.8			13.9		Bits
VOLTAGE REFERENCE INPUT									
Reference voltage			2.5		V_{DD} + 0.3	2.5		V_{DD} + 0.3	V
Reference input resistance		$\overline{CS}$ = GND, f_{SAMPLE} = 0Hz		5			5		kΩ
		$\overline{CS}$ = V_{DD}		5			5		GΩ
Reference input capacitance				20			20		pF
Reference input current				0.5	0.75		0.5	0.75	mA
		$\overline{CS}$ = V_{DD}		0.1			0.1		μA
DIGITAL INPUTS(1)									
Logic family				LVCMOS			LVCMOS		
High-level input voltage	V_{IH}	V_{DD} = 3.6V	2		V_{DD} + 0.3	2		V_{DD} + 0.3	V
Low-level input voltage	V_{IL}	V_{DD} = 2.7V	–0.3		0.8	–0.3		0.8	V
Input current	I_{IN}	V_I = V_{DD} or GND			±50			±50	nA
Input capacitance	C_I			5			5		pF

(1) Applies for 3.0V nominal supply: V_{DD} (min) = 2.7V and V_{DD} (max) = 3.6V.

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ELECTRICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = +2.5V, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8325I			ADS8325IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
DIGITAL OUTPUTS(2)									
Logic family				LVCMOS			LVCMOS		
High-level output voltage	V_{OH}	V_{DD} = 2.7V, I_{OH} = –100µA	V_{DD} – 0.2			V_{DD} – 0.2			V
Low-level output voltage	V_{OL}	V_{DD} = 2.7V, I_{OL} = 100µA			0.2			0.2	V
High-impedance-state output current	I_{OZ}	$\overline{CS}$ = V_{DD}, V_I = V_{DD} or GND			±50	±50		±50	nA
Output capacitance	C_O			5			5		pF
Load capacitance	C_L				30			30	pF
Data format				Straight Binary			Straight Binary		

(2) Applies for 3.0V nominal supply: V_{DD} (min) = 2.7V and V_{DD} (max) = 3.6V.

ELECTRICAL CHARACTERISTICS

Over recommended operating free-air temperature at –40°C to +85°C, V_{REF} = V_{DD}, –IN = GND, f_{SAMPLE} = 100kHz, and f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

PARAMETER		TEST CONDITIONS	ADS8325I			ADS8325IB			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
POWER-SUPPLY REQUIREMENTS									
Power supply	V_{DD}	Low-voltage levels	2.7		3.6	2.7		3.6	V
		5V logic levels	4.5		5.5	4.5		5.5	V
Operating supply current	I_{DD}	V_{DD} = 3V		0.75	1.5		0.75	1.5	mA
		V_{DD} = 5V		0.9	1.5		0.9	1.5	mA
Power-down supply current	(I_{DD}	V_{DD} = 3V		0.1			0.1		µA
		V_{DD} = 5V		0.2			0.2		µA
Power dissipation		V_{DD} = 3V		2.25	4.5		2.25	4.5	mW
		V_{DD} = 5V		4.5	7.5		4.5	7.5	mW
Power dissipation in power-down		V_{DD} = 3V, $\overline{CS}$ = V_{DD}		0.3			0.3		µW
		V_{DD} = 5V, $\overline{CS}$ = V_{DD}		0.6			0.6		µW

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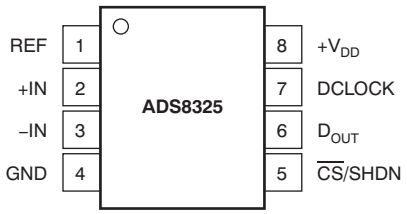
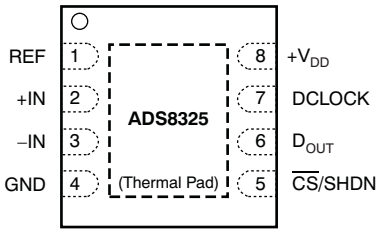
PIN CONFIGURATIONS

DGK PACKAGE
MSOP
(TOP VIEW)



DRB PACKAGE(1)
SON
(TOP VIEW)



(1) The thermal pad is internally connected to the substrate. This pad can be connected to the analog ground or left floating. Keep the thermal pad separate from the digital ground, if possible.

PIN ASSIGNMENTS

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
REF	1	AI	Reference Input
+IN	2	AI	Noninverting Input
–IN	3	AI	Inverting Analog Input
GND	4	P	Ground
$\overline{CS}$/SHDN	5	DI	Chip select when low; Shutdown mode when high.
D_{OUT}	6	DO	The serial output data word.
DCLOCK	7	DI	Data clock synchronizes the serial data transfer and determines conversion speed.
$+V_{DD}$	8	P	Power supply

(1) AI is Analog Input, DI is Digital Input, DO is Digital Output, and P is Power-Supply Connection.

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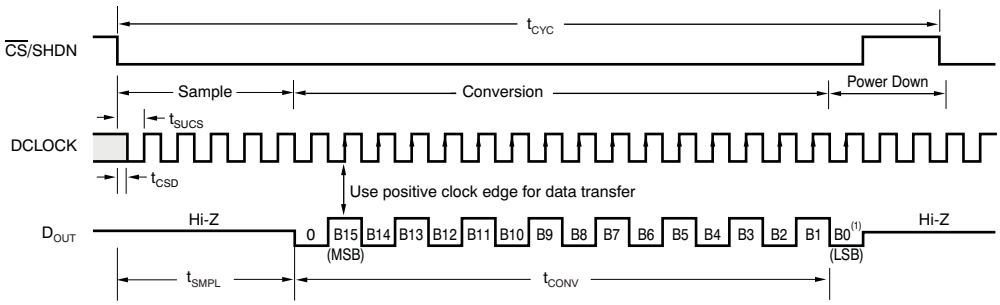
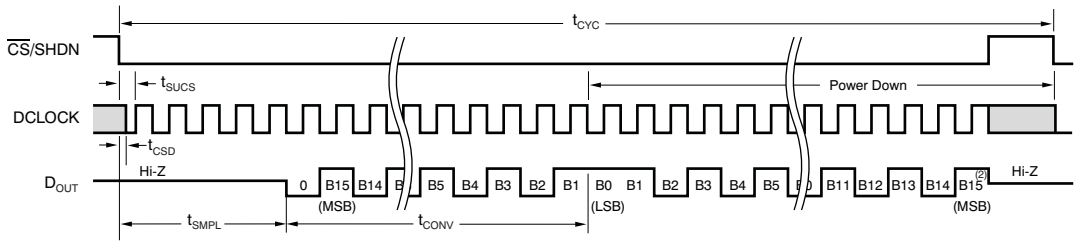
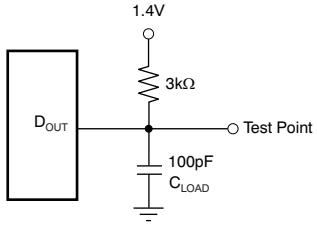
TIMING INFORMATION



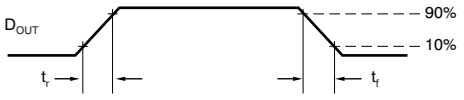
NOTE: (1) A minimum of 22 clock cycles are required for 16-bit conversion; 24 clock cycles are shown. If $\overline{CS}$ remains low at the end of conversion, a new data stream is shifted out with LSB-first data followed by zeroes indefinitely.



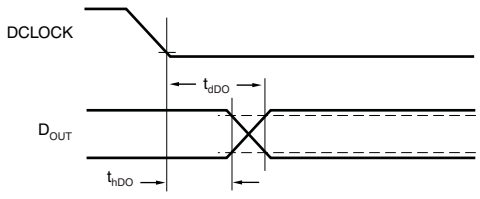
NOTE: (2) After completing the data transfer, if further clocks are applied with $\overline{CS}$ low, the A/D converter will output zeroes indefinitely.



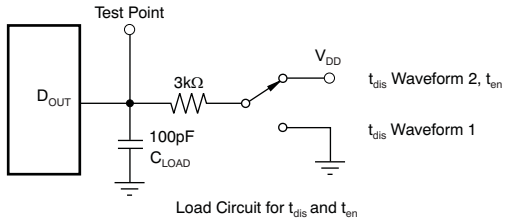
Load Circuit for t_{dDO}, t_r, and t_f



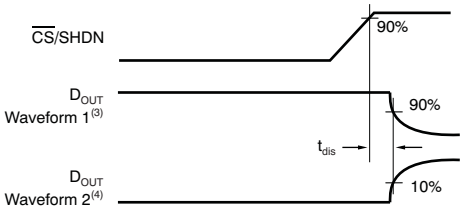
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



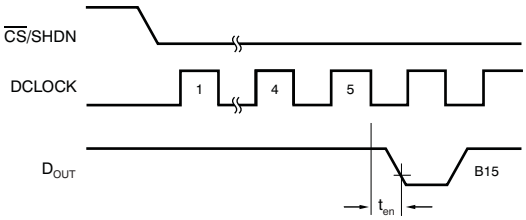
Voltage Waveforms for D_{OUT} Delay Times, t_{dDO}



Load Circuit for t_{dis} and t_{en}



Voltage Waveforms for t_{dis}



Voltage Waveforms for t_{en}

NOTES: (3) Waveform 1 is for an output with internal conditions such that the output is high unless disabled by the output control.
(4) Waveform 2 is for an output with internal conditions such that the output is low unless disabled by the output control.

Figure 1. Timing Diagrams and Test Circuits for the Paramters in Table 1

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TIMING INFORMATION (continued)

Table 1. Timing Characteristics

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
t_{SMPL}	Analog Input Sample Time	4.5		5.0	Clk Cycles
t_{CONV}	Conversion Time		16		Clk Cycles
t_{CYC}	Throughput Rate			100	kHz
t_{CSD}	$\overline{CS}$ Falling to DCLOCK LOW			0	ns
t_{SUCS}	$\overline{CS}$ Falling to DCLOCK Rising	20			ns
t_{HDO}	DCLOCK Falling to Current D_{OUT} Not Valid	5	15		ns
t_{DIS}	$\overline{CS}$ Rising to DOUT 3-State		70	100	ns
t_{EN}	DCLOCK Falling to D_{OUT} Enabled		20	50	ns
t_F	D_{OUT} Fall Time		5	25	ns
t_R	D_{OUT} Rise Time		7	25	ns

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TYPICAL CHARACTERISTICS: V_{DD} = +5V

At T_A = +25°C, V_{DD} = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

INTEGRAL LINEARITY ERROR vs CODE

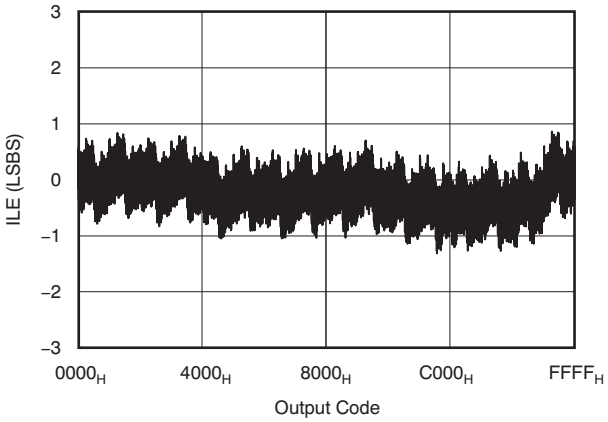

Figure 2.

DIFFERENTIAL LINEARITY ERROR vs CODE

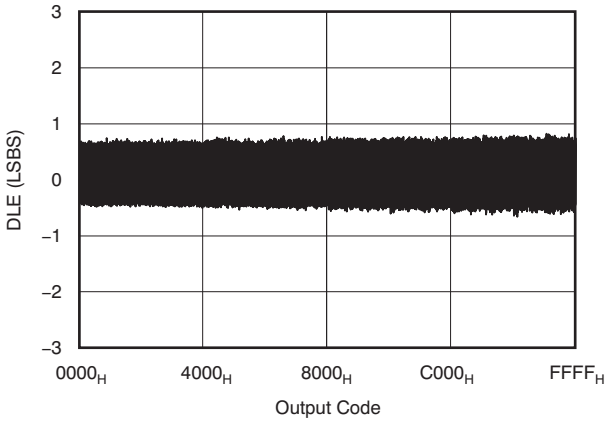

Figure 3.

FREQUENCY SPECTRUM (8192 Point FFT, f_{IN} = 1.0132kHz, –0.2 dB)

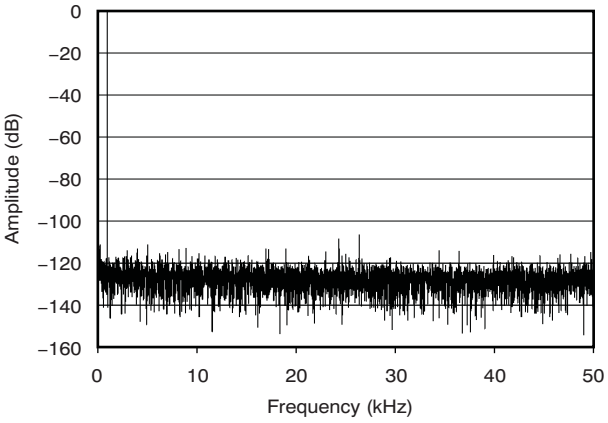

Figure 4.

FREQUENCY SPECTRUM (8192 Point FFT, f_{IN} = 10.0022kHz, –0.2 dB)

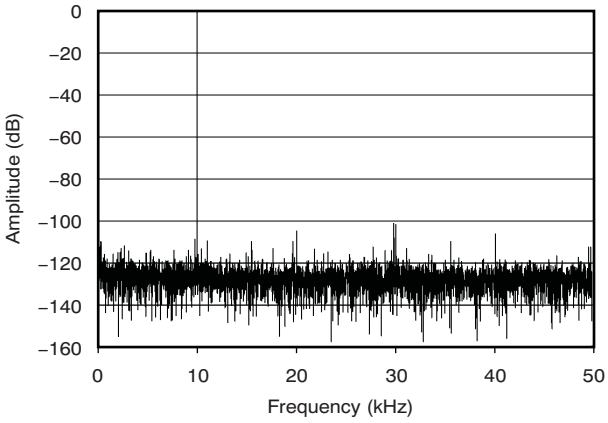

Figure 5.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

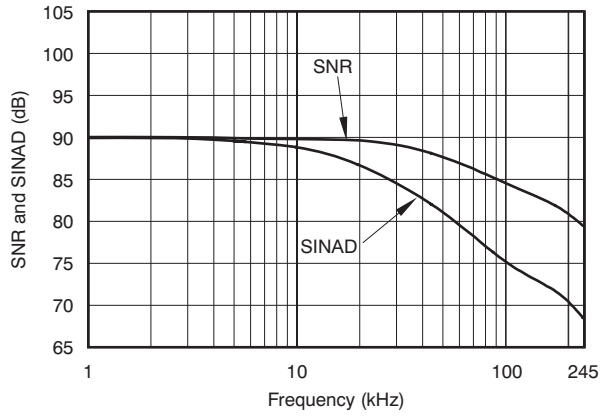

Figure 6.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

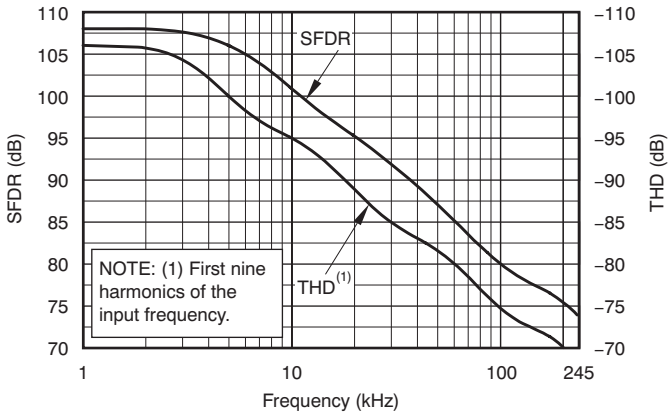

Figure 7.

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TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{DD} = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

SIGNAL-TO-NOISE + DISTORTION vs INPUT LEVEL

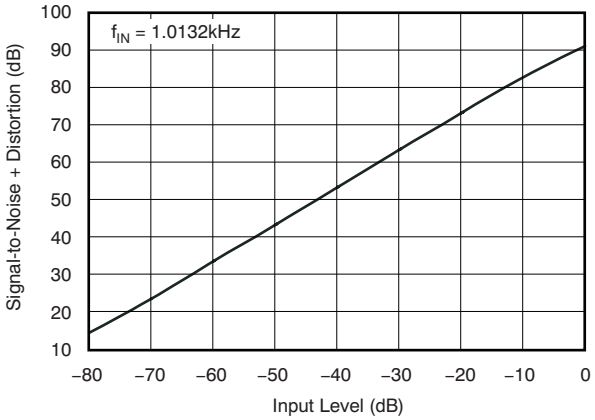

Figure 8.

PEAK-TO-PEAK NOISE FOR A DC INPUT vs REFERENCE VOLTAGE

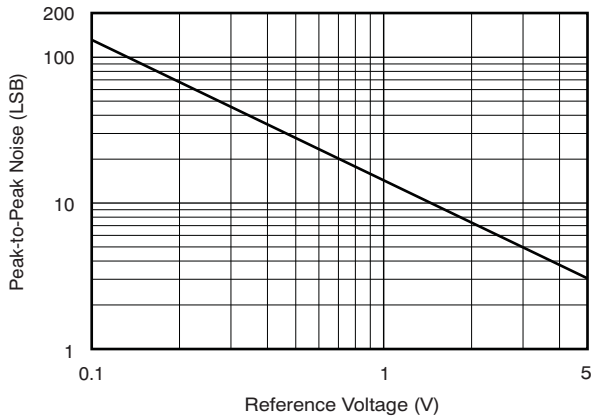

Figure 9.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

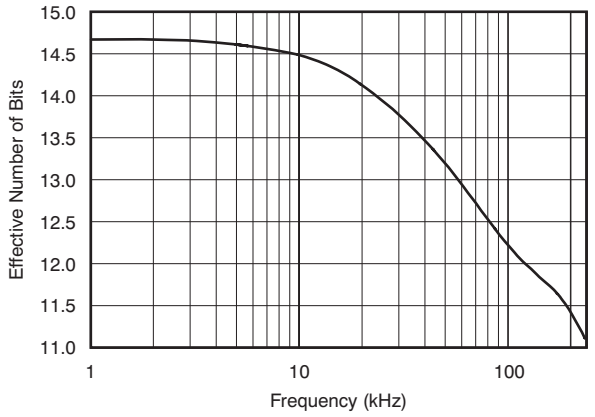

Figure 10.

CHANGE IN SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

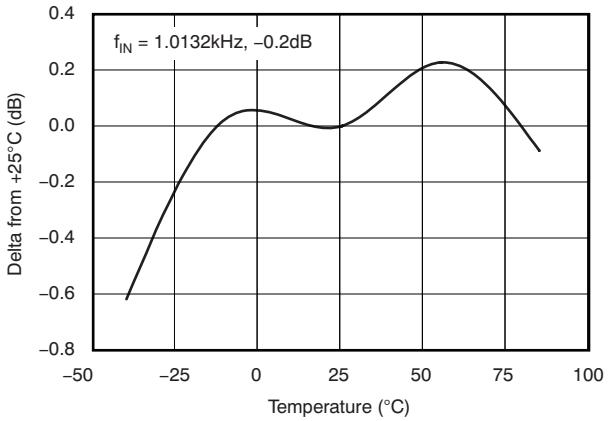

Figure 11.

CHANGE IN GAIN vs TEMPERATURE

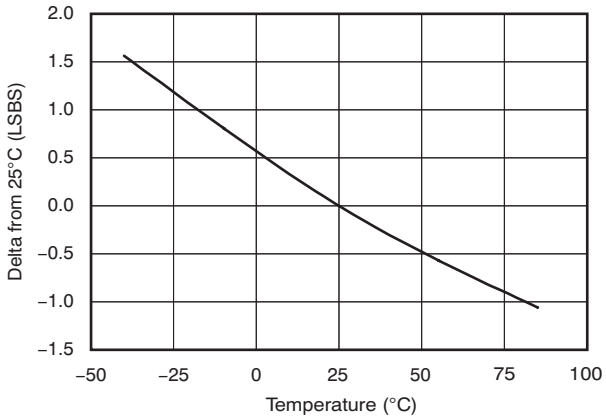

Figure 12.

CHANGE IN UPO vs TEMPERATURE

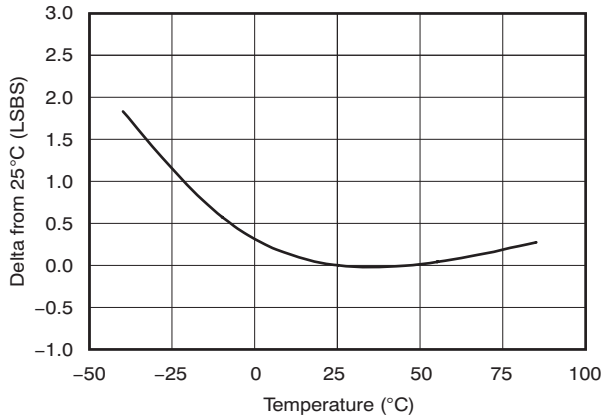

Figure 13.

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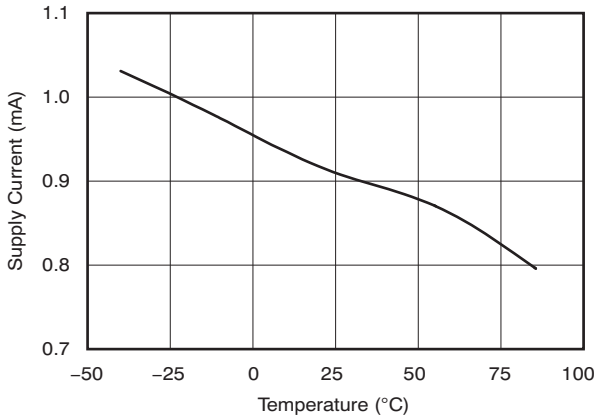
TYPICAL CHARACTERISTICS: V_{DD} = +5V (continued)

At T_A = +25°C, V_{DD} = +5V, V_{REF} = +5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

SUPPLY CURRENT vs TEMPERATURE



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TYPICAL CHARACTERISTICS: V_{DD} = +2.7V

At T_A = +25°C, V_{DD} = 2.7V, V_{REF} = 2.5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

INTEGRAL LINEARITY ERROR vs CODE

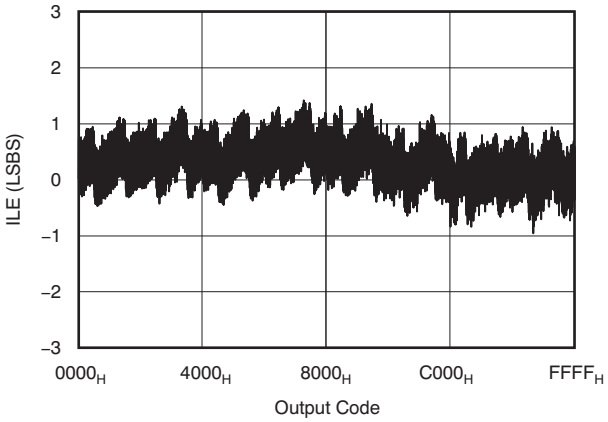

Figure 15.

DIFFERENTIAL LINEARITY ERROR vs CODE

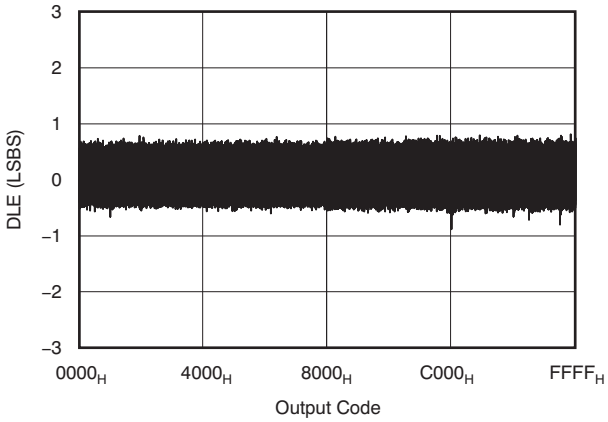

Figure 16.

FREQUENCY SPECTRUM (8192 Point FFT, f_{IN} = 1.0132kHz, –0.2 dB)

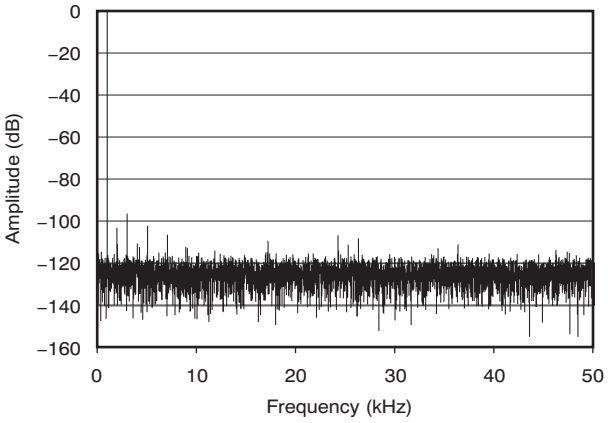

Figure 17.

FREQUENCY SPECTRUM (8192 Point FFT, f_{IN} = 10.0022kHz, –0.2 dB)

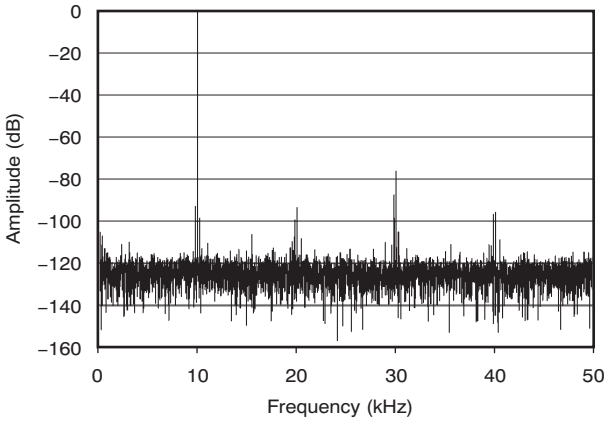

Figure 18.

SIGNAL-TO-NOISE RATIO AND SIGNAL-TO-NOISE + DISTORTION vs INPUT FREQUENCY

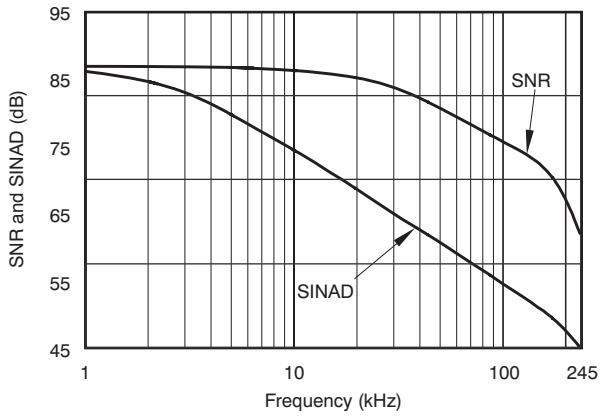

Figure 19.

SPURIOUS-FREE DYNAMIC RANGE AND TOTAL HARMONIC DISTORTION vs INPUT FREQUENCY

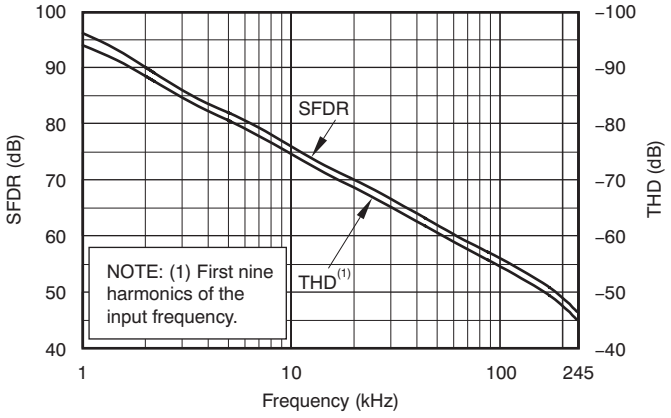

Figure 20.

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TYPICAL CHARACTERISTICS: V_{DD} = +2.7V (continued)

At T_A = +25°C, V_{DD} = 2.7V, V_{REF} = 2.5V, f_{SAMPLE} = 100kHz, f_{CLK} = 24 × f_{SAMPLE}, unless otherwise noted.

SIGNAL-TO-NOISE + DISTORTION vs INPUT LEVEL

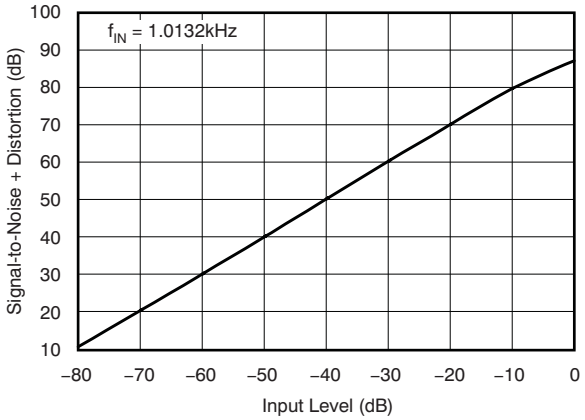


Figure 21.

EFFECTIVE NUMBER OF BITS vs INPUT FREQUENCY

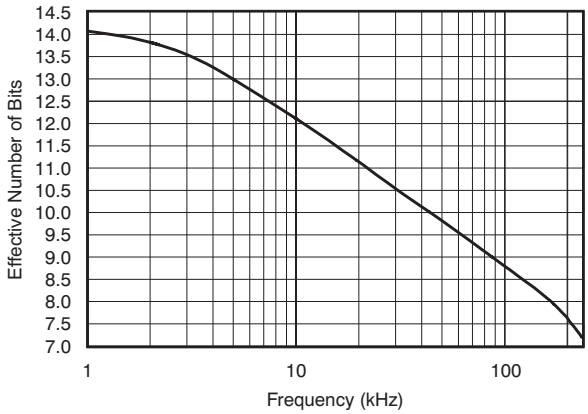


Figure 22.

CHANGE IN SIGNAL-TO-NOISE + DISTORTION vs TEMPERATURE

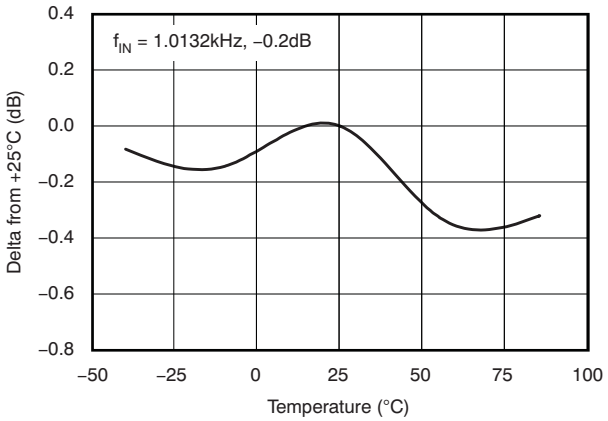


Figure 23.

CHANGE IN GAIN vs TEMPERATURE

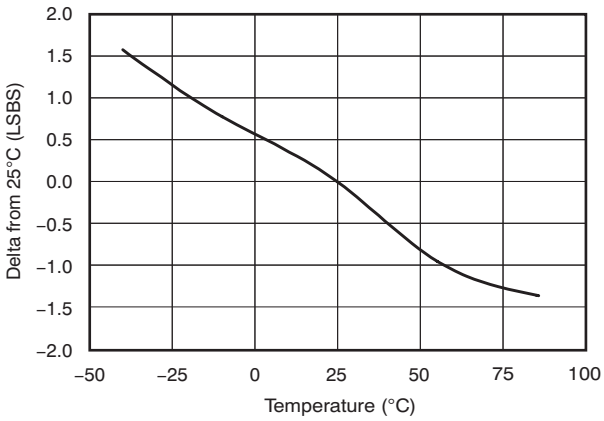
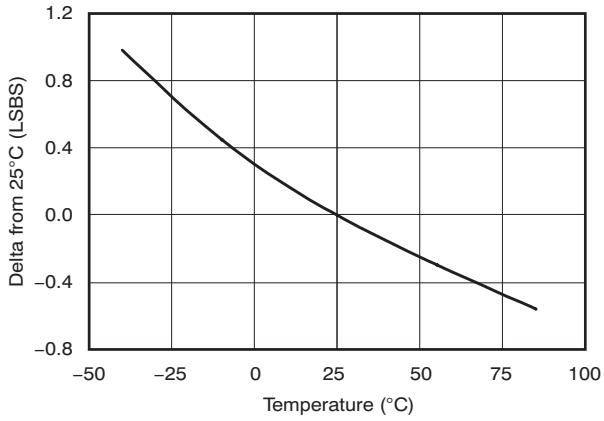
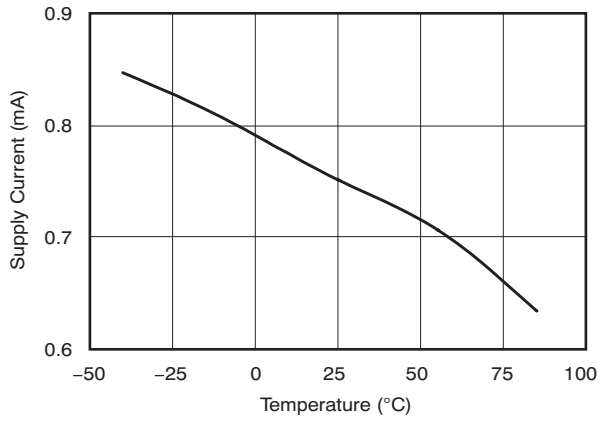


Figure 24.

CHANGE IN UPO vs TEMPERATURE



SUPPLY CURRENT vs TEMPERATURE



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THEORY OF OPERATION

The ADS8325 is a classic Successive Approximation Register (SAR) Analog-to-Digital (A/D) converter. The architecture is based on capacitive redistribution that inherently includes a sample-andhold function. The converter is fabricated on a 0.6µ CMOS process. The architecture and process allow the ADS8325 to acquire and convert an analog signal at up to 100,000 conversions per second while consuming less than 4.5mW from $+V_{DD}$.

The ADS8325 requires an external reference, an external clock, and a single power source (V_{DD}). The external reference can be any voltage between 2.5V and 5.5V. The value of the reference voltage directly sets the range of the analog input. The reference input current depends on the conversion rate of the ADS8325.

The external clock can vary between 24kHz (1kHz throughput) and 2.4MHz (100kHz throughput). The duty cycle of the clock is essentially unimportant as long as the minimum high and low times are at least 200ns (V_{DD} = 4.75V or greater). The minimum clock frequency is set by the leakage on the internal capacitors to the ADS8325.

The analog input is provided to two input pins: +IN and –IN. When a conversion is initiated, the differential input on these pins is sampled on the internal capacitor array. While a conversion is in progress, both inputs are disconnected from any internal function.

The digital result of the conversion is clocked out by the DCLOCK input and is provided serially, most significant bit first, on the D_{OUT} pin. The digital data that is provided on the D_{OUT} pin is for the conversion currently in progress—there is no pipeline delay. It is possible to continue to clock the ADS8325 after the conversion is complete and to obtain the serial data least significant bit first. See the *Timing Information* section for more information.

ANALOG INPUT

The analog input of ADS8325 is differential. The +IN and –IN input pins allow for a differential input signal. The amplitude of the input is the difference between the +IN and –IN input, or (+IN) – (–IN). Unlike some converters of this type, the –IN input is not resampled later in the conversion cycle. When the converter goes into the hold mode or conversion, the voltage difference between +IN and –IN is captured on the internal capacitor array.

The range of the –IN input is limited to –0.3V to +0.5V. Due to this, the differential input could be used to reject signals that are common to both inputs in the specified range. Thus, the –IN input is best used to sense a remote signal ground that may move slightly with respect to the local ground potential.

The general method for driving the analog input of the ADS8325 is shown in Figure 26 and Figure 27. The –IN input is held at the common-mode voltage. The +IN input swings from –IN (or common-mode voltage) to –IN + V_{REF} (or commonmode voltage + V_{REF}), and the peak-to-peak amplitude is $+V_{REF}$. The value of V_{REF} determines the range over which the common-mode voltage may vary (see Figure 28). Figure 29 and Figure 30 illustrate the typical change in gain and offset as a function of the common-mode voltage applied to the –IN pin.

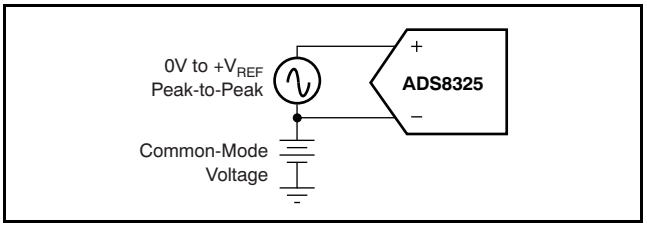
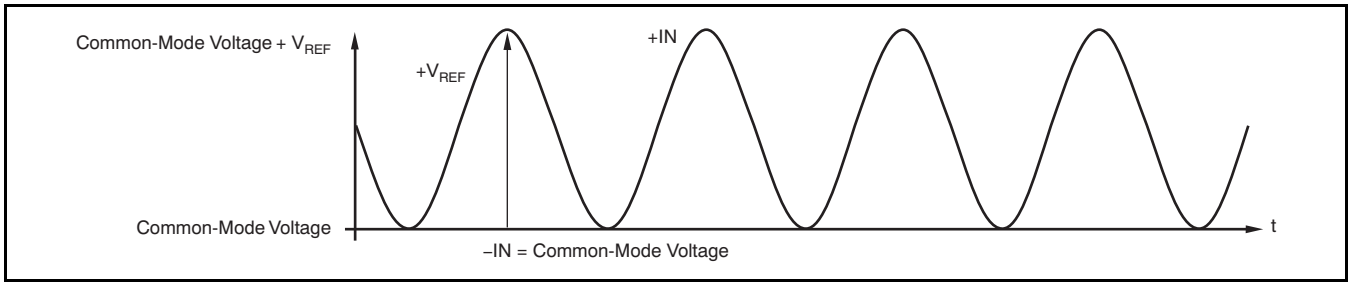


Figure 26. Methods of Driving the ADS8325



NOTE: The maximum differential voltage between +IN and –IN of the ADS8325 is V_{REF}. See Figure 28 for a further explanation of the common-mode voltage range for differential inputs.

Figure 27. Differential Input Mode of the ADS8325

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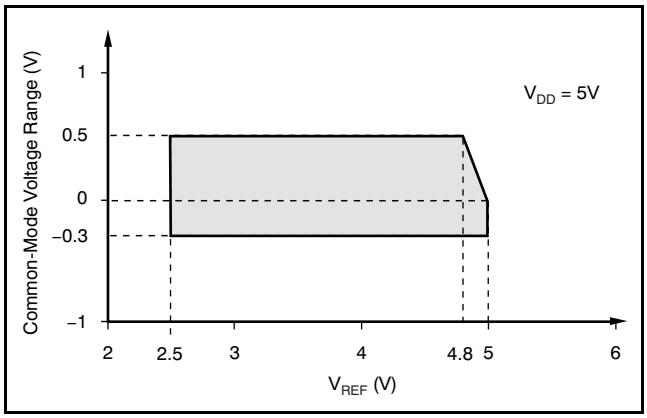

Figure 28. +IN Analog Input: Common-Mode Voltage Range vs V_{REF}

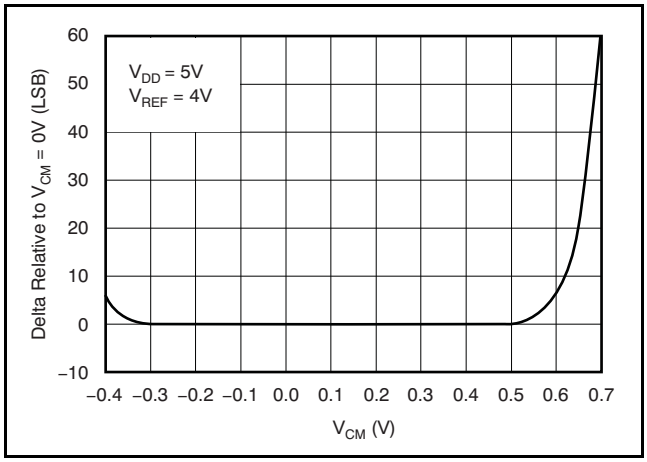

Figure 29. Change in Gain vs Common-Mode Voltage

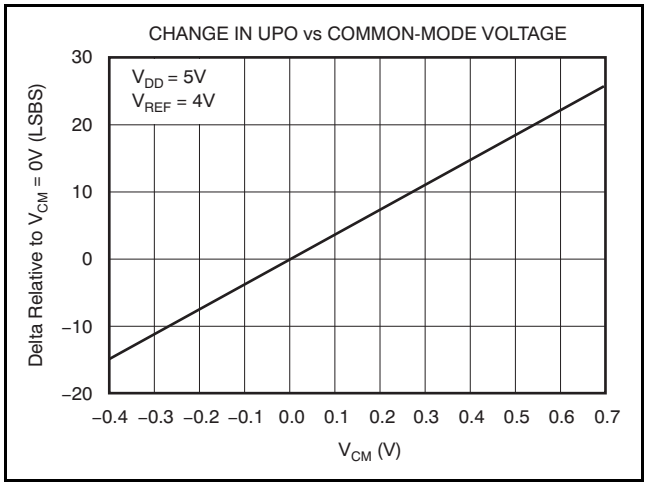

Figure 30. Change in Unipolar Offset vs Common-Mode Voltage

The input current required by the analog inputs depends on a number of factors: sample rate, input voltage, source impedance, and power-down mode. Essentially, the current into the ADS8325 charges the internal capacitor array during the sample period. After this capacitance has been fully charged, there is no further input current. The source of the analog input voltage must be able to charge the input capacitance (40pF) to a 16-bit settling level within 4.5 clock cycles (1.875µs). When the converter goes into the hold mode, or while it is in the power-down mode, the input impedance is greater than 1GΩ.

Care must be taken regarding the absolute analog input voltage. To maintain the linearity of the converter, the –IN input should not drop below GND – 0.3V or exceed GND + 0.5V. The +IN input should always remain within the range of GND – 0.3V to V_{DD} + 0.3V, or –IN to –IN + V_{REF}, whichever limit is reached first. Outside of these ranges, the converter's linearity may not meet specifications.

To minimize noise, low bandwidth input signals with lowpass filters should be used. In each case, care should be taken to ensure that the output impedance of the sources driving the +IN and –IN inputs are matched. Often, a small capacitor (20pF) between the positive and negative inputs helps to match their impedance. To obtain maximum performance from the ADS8325, the input circuit from Figure 31 is recommended.

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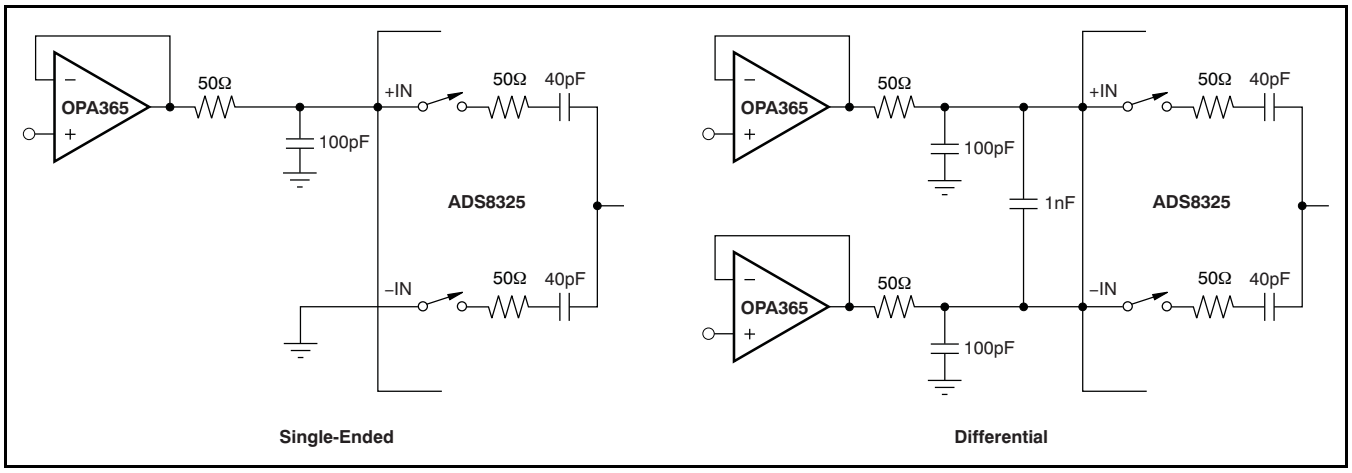

Figure 31. Single-Ended and Differential Methods of Interfacing the ADS8325

REFERENCE INPUT

The external reference sets the analog input range. The ADS8325 will operate with a reference in the range of 2.5V to V_{DD}. There are several important implications to this.

As the reference voltage is reduced, the analog voltage weight of each digital output code is reduced. This is often referred to as the Least Significant Bit (LSB) size and is equal to the reference voltage divided by 65,536. This means that any offset or gain error inherent in the A/D converter will appear to increase, in terms of LSB size, as the reference voltage is reduced. For a reference voltage of 2.5V, the value of LSB is 38.15μV, and for reference voltage of 5V, the LSB is 76.3μV.

The noise inherent in the converter will also appear to increase with lower LSB size. With a 5V reference, the internal noise of the converter typically contributes only 1.5LSBs peak-to-peak of potential error to the output code. When the external reference is 2.5V, the potential error contribution from the internal noise will be 2 times larger (3LSBs). The errors due to the internal noise are Gaussian in nature and can be reduced by averaging consecutive conversion results.

For more information regarding noise, consult Figure 9, *Peak-to-Peak Noise vs Reference Voltage*. Note that Figure 10, *Effective Number Of Bits vs Input Frequency*, is calculated based on the converter's signal-to-(noise + distortion) ratio with a 1kHz, 0dB input signal. SINAD is related to ENOB as follows:

$$SINAD = 6.02 \times ENOB + 1.76$$

As the difference between the power-supply voltage and reference voltage increases, the gain and offset performance of the converter will decrease. Figure 32 shows the typical change in gain and offset as a function of the difference between the power-supply voltage and reference voltage. For the combination of V_{DD} = 2.7V and V_{REF} = 2.5V, or V_{DD} = 5V and V_{REF} = 5V, offset and gain error will be minimal. The most dramatic difference in offset can be seen when V_{DD} = 5V and V_{REF} = 2.5V.

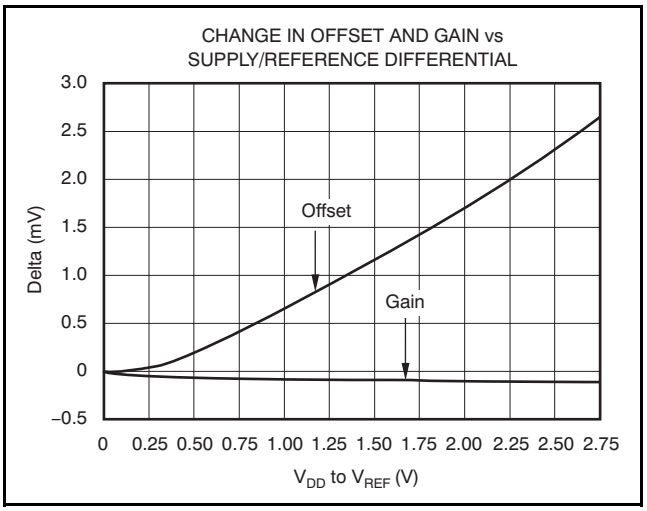

Figure 32. Change in Offset and Gain vs the Difference Between Power-Supply and Reference Voltage

With lower reference voltages, extra care should be taken to provide a clean layout including adequate bypassing, a clean power supply, a low-noise reference, and a low-noise input signal. Due to the lower LSB size, the converter will also be more sensitive to external sources of error, such as nearby digital signals and electromagnetic interference.

The equivalent input circuit for the reference voltage is presented in Figure 33. The 5kΩ resistor presents a constant load during the conversion process. At the same time, an equivalent capacitor of 20pF is switched. To obtain optimum performance from the ADS8325, special care must be taken in designing the interface circuit to the reference input pin. To ensure a stable reference voltage, a 47µF tantalum capacitor with low ESR should be connected as close as possible to the input pin. If a high output impedance reference source is used, an additional operational amplifier with a current limiting resistor must be placed in front of the capacitors.

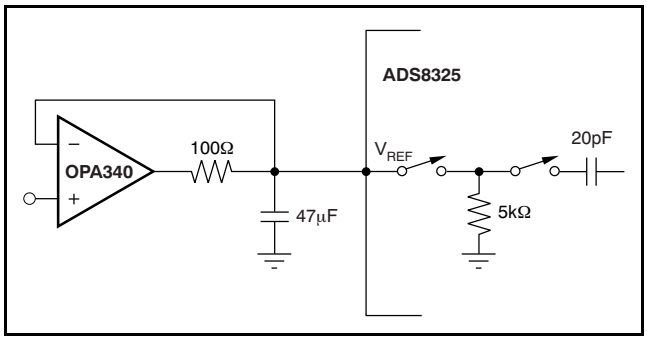

Figure 33. Input Reference Circuit and its Interface

When the ADS8325 is in power-down mode, the input resistance of the reference pin will have a value of 5GΩ. Since the input capacitors must be recharged before the next conversion starts, an operational amplifier with good dynamic characteristics must be used to buffer the reference input.

NOISE

The transition noise of the ADS8325 itself is extremely low (see Figure 34 and Figure 35); it is much lower than competing A/D converters. These histograms were generated by applying a low-noise DC input and initiating 5000 conversions. The digital output of the A/D converter will vary in output code due to the internal noise of the ADS8325. This is true for all 16-bit, SAR-type A/D converters. Using a histogram to plot the output codes, the distribution should appear bell-shaped with the peak of the bell curve representing the nominal code for the input value. The ±1σ, ±2σ, and ±3σ distributions will represent the 68.3%, 95.5%, and 99.7%, respectively, of all codes. The transition noise can be calculated by dividing the number of codes measured by 6 and this will yield the ±3σ distribution, or 99.7%, of all codes. Statistically, up to three codes could fall outside the distribution when executing 1000 conversions. The ADS8325, with < 3 output codes for the ±3σ distribution, will yield a < ±0.5LSBs of transition noise. Remember, to achieve this low-noise performance, the peak-to-peak noise of the input signal and reference must be < 50µV.

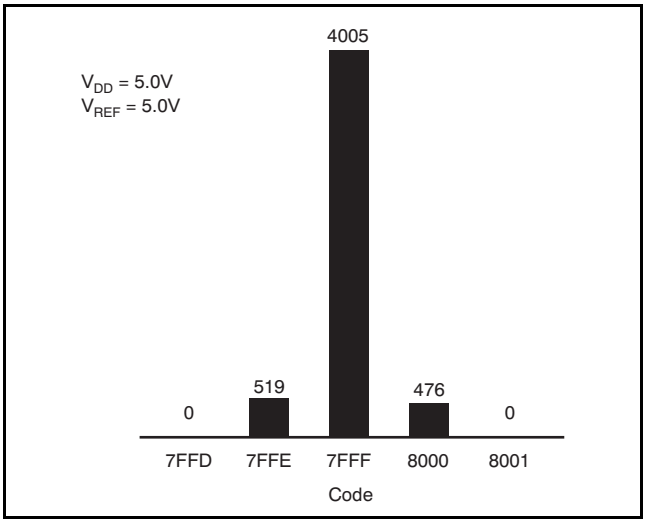

Figure 34. 5000 Conversion Histogram of a DC Input

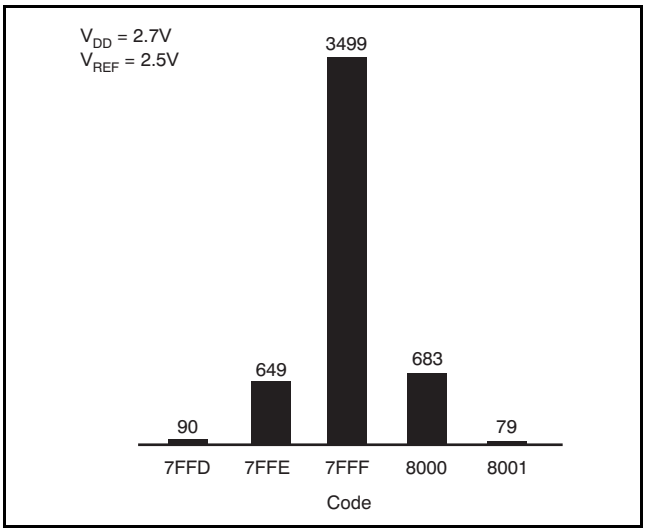

Figure 35. 5000 Conversion Histogram of a DC Input

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AVERAGING

The noise of the A/D converter can be compensated by averaging the digital codes. By averaging conversion results, transition noise will be reduced by a factor of $1/\sqrt{n}$, where n is the number of averages. For example, averaging four conversion results will reduce the transition noise from ±0.5LSB to ±0.25LSB. Averaging should only be used for input signals with frequencies near DC.

For AC signals, a digital filter can be used to low-pass filter and decimate the output codes. This works in a similar manner to averaging; for every decimation by 2, the signal-to-noise ratio will improve 3dB.

DIGITAL INTERFACE

SIGNAL LEVELS

The ADS8325 has a wide range of power-supply voltage. The A/D converter, as well as the digital interface circuit, is designed to accept and operate from 2.7V up to 5.5V. This voltage range will accommodate different logic levels.

When the ADS8325's power-supply voltage is in the range of 4.5V to 5.5V (5V logic level), the ADS8325 can be connected directly to another 5V CMOS integrated circuit.

Another possibility is that the ADS8325's power-supply voltage is in the range of 2.7V to 3.6V. The ADS8325 can be connected directly to another 3.3V LVCMOS integrated circuit.

SERIAL INTERFACE

The ADS8325 communicates with microprocessors and other digital systems via a synchronous 3-wire serial interface, as illustrated in the *Timing Information* section. The DCLOCK signal synchronizes the data transfer with each bit being transmitted on the falling edge of DCLOCK. Most receiving systems will capture the bitstream on the rising edge of DCLOCK. However, if the minimum hold time for D_{OUT} is acceptable, the system can use the falling edge of DCLOCK to capture each bit.

A falling $\overline{CS}$ signal initiates the conversion and data transfer. The first 4.5 to 5.0 clock periods of the conversion cycle are used to sample the input signal. After the fifth falling DCLOCK edge, D_{OUT} is enabled and will output a LOW value for one clock period. For the next 16 DCLOCK periods, D_{OUT} will output the conversion result, most significant bit first. After the least significant bit (B0) has been output, subsequent clocks will repeat the output data, but in a least significant bit first format.

After the most significant bit (B15) has been repeated, D_{OUT} will tri-state. Subsequent clocks will have no effect on the converter. A new conversion is initiated only when $\overline{CS}$ has been taken HIGH and returned LOW.

DATA FORMAT

The output data from the ADS8325 is in Straight Binary format (see Figure 36. This figure represents the ideal output code for a given input voltage and does not include the effects of offset, gain error, or noise.

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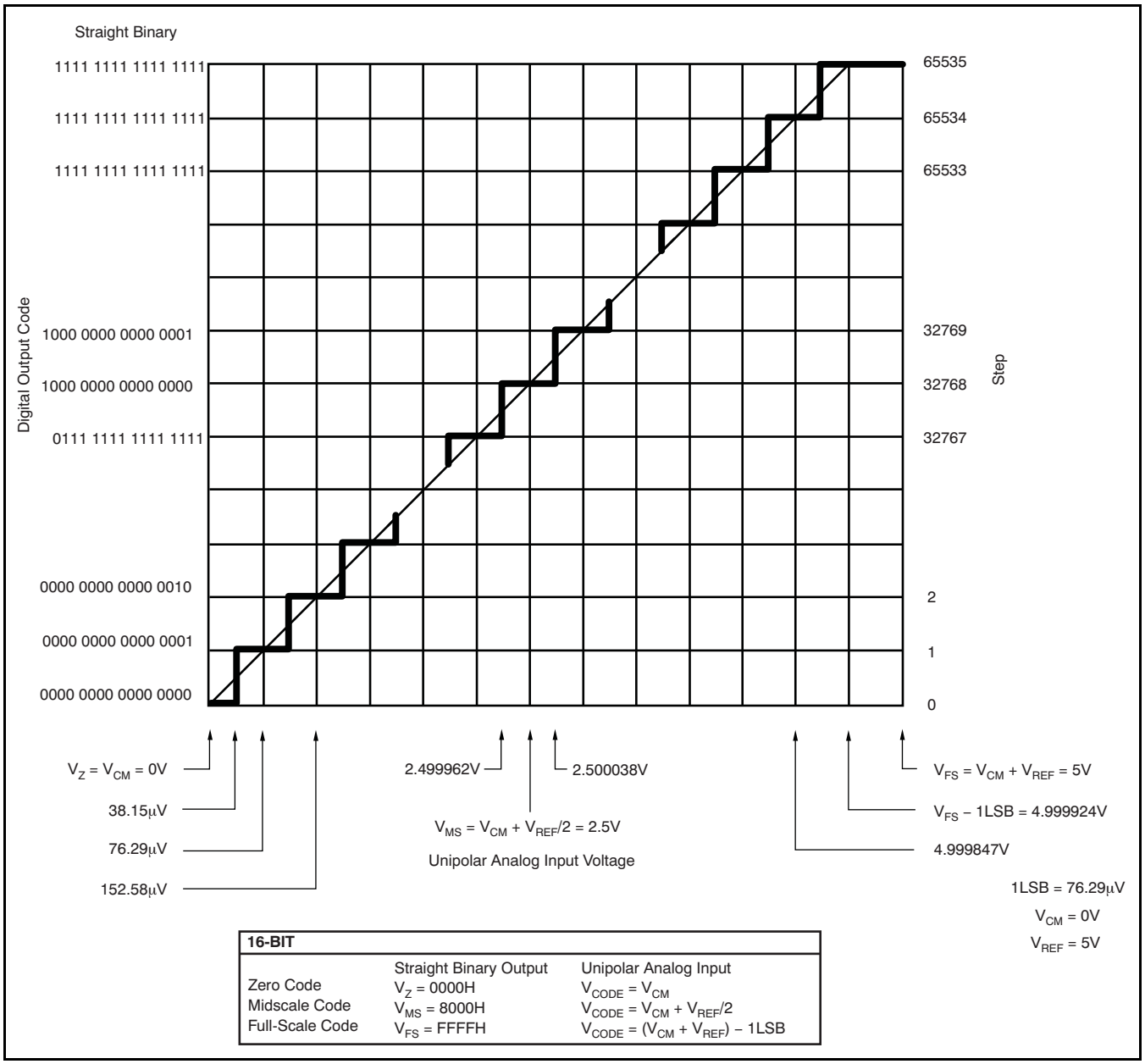

Figure 36. Ideal Conversion Characteristics (Condition: V_{CM} = 0V, V_{REF} = 5V)

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POWER DISSIPATION

The architecture of the converter, the semiconductor fabrication process, and a careful design, allow the ADS8325 to convert at up to a 100kHz rate while requiring very little power. However, for the absolute lowest power dissipation, there are several things to keep in mind.

The power dissipation of the ADS8325 scales directly with conversion rate. Therefore, the first step to achieving the lowest power dissipation is to find the lowest conversion rate that will satisfy the requirements of the system.

In addition, the ADS8325 is in power-down mode under two conditions: when the conversion is complete and whenever $\overline{CS}$ is HIGH (see the *Timing Information* section). Ideally, each conversion should occur as quickly as possible, preferably at a 2.4MHz clock rate. This way, the converter spends the longest possible time in the power-down mode. This is very important as the converter not only uses power on each DCLOCK transition (as is typical for digital CMOS components), but also uses some current for the analog circuitry, such as the comparator. The analog section dissipates power continuously until the power-down mode is entered.

See Figure 37 and Figure 38 for the current consumption of the ADS8325 versus sample rate. For these graphs, the converter is clocked at 2.4MHz regardless of the sample rate. $\overline{CS}$ is held HIGH during the remaining sample period.

There is an important distinction between the power-down mode that is entered after a conversion is complete and the full power-down mode that is enabled when $\overline{CS}$ is HIGH. $\overline{CS}$ LOW will shut down only the analog section. The digital section is completely shut down only when $\overline{CS}$ is HIGH. Thus, if $\overline{CS}$ is left LOW at the end of a conversion, and the converter is continually clocked, the power consumption will not be as low as when $\overline{CS}$ is HIGH.

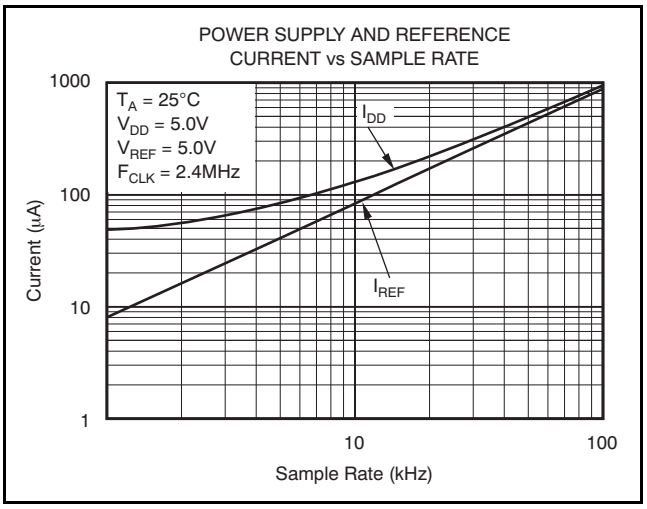

Figure 37. Power-Supply and Reference Current vs Sample Rate at V_{DD} = 5V

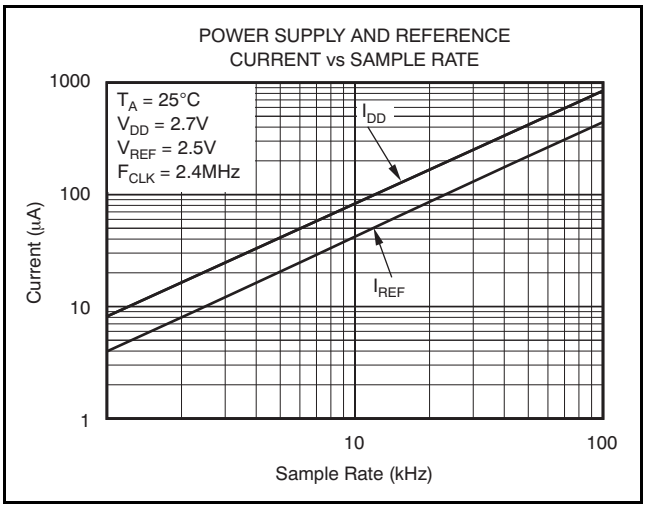

Figure 38. Power-Supply and Reference Current vs Sample Rate at V_{DD} = 2.7V

SHORT CYCLING

Another way to save power is to utilize the $\overline{CS}$ signal to short cycle the conversion. Due to the ADS8325 placing the latest data bit on the D_{OUT} line as it is generated, the converter can easily be short cycled. This term means that the conversion can be terminated at any time. For example, if only 14 bits of the conversion result are needed, then the conversion can be terminated (by pulling $\overline{CS}$ HIGH) after the 14th bit has been clocked out.

This technique can be used to lower the power dissipation (or to increase the conversion rate) in those applications where an analog signal is being monitored until some condition becomes true. For example, if the signal is outside a predetermined range, the full 16-bit conversion result may not be needed. If so, the conversion can be terminated after the first n bits, where n might be as low as 3 or 4. This results in lower power dissipation in both the converter and the rest of the system as they spend more time in power-down mode.

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LAYOUT

For optimum performance, care should be taken with the physical layout of the ADS8325 circuitry. This will be particularly true if the reference voltage is low and/or the conversion rate is high. At a 100kHz conversion rate, the ADS8325 makes a bit decision every 416ns. That is, for each subsequent bit decision, the digital output must be updated with the results of the last bit decision, the capacitor array appropriately switched and charged, and the input to the comparator settled to a 16-bit level all within one clock cycle.6

The basic SAR architecture is sensitive to spikes on the power supply, reference, and ground connections that occur just prior to latching the comparator output. Thus, during any single conversion for an n-bit SAR converter, there are n *windows* in which large external transient voltages can easily affect the conversion result. Such spikes might originate from switching power supplies, digital logic, and high-power devices, to name a few. This particular source of error can be very difficult to track down if the glitch is almost synchronous to the converter's DCLOCK signal as the phase difference between the two changes with time and temperature, causing sporadic misoperation.

With this in mind, power to the ADS8325 should be clean and well-bypassed. A 0.1µF ceramic bypass capacitor should be placed as close as possible to the ADS8325 package. In addition, a 1µF to 10µF capacitor and a 5Ω or 10Ω series resistor may be used to low-pass filter a noisy supply.

The reference should be similarly bypassed with a 47µF capacitor. Again, a series resistor and large capacitor can be used to low-pass filter the reference voltage. If the reference voltage originates from an op amp, make sure that the op amp can drive the bypass capacitor without oscillation (the series resistor can help in this case). Keep in mind that while the ADS8325 draws very little current from the reference on average, there are still instantaneous current demands placed on the external input and reference circuitry.

Texas Instruments' OPA627 op amp provides optimum performance for buffering both the signal and reference inputs. For low-cost, low-voltage, single-supply applications, the OPA2350 or OPA2340 dual op amps are recommended.

Also, keep in mind that the ADS8325 offers no inherent rejection of noise or voltage variation in regards to the reference input. This is of particular concern when the reference input is tied to the power supply. Any noise and ripple from the supply will appear directly in the digital results. While high-frequency noise can be filtered out as described in the previous paragraph, voltage variation due to the line frequency (50Hz or 60Hz) can be difficult to remove.

The GND pin on the ADS8325 should be placed on a clean ground point. In many cases, this will be the *analog* ground. Avoid connecting the GND pin too close to the grounding point for a microprocessor, microcontroller, or digital signal processor. If needed, run a ground trace directly from the converter to the power-supply connection point. The ideal layout will include an analog ground plane for the converter and associated analog circuitry.

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APPLICATION CIRCUITS

Figure 39 shows a basic data acquisition system. The ADS8325 input range is connected to 2.5V or 4.096V. The 5Ω resistor and 1µF to 10µF capacitor filters the microcontroller *noise* on the supply, as well as any high-frequency noise from the supply itself. The exact values should be picked such that the filter provides adequate rejection of noise. Operational amplifiers and voltage reference are connected to analog power supply, AV_{DD}.

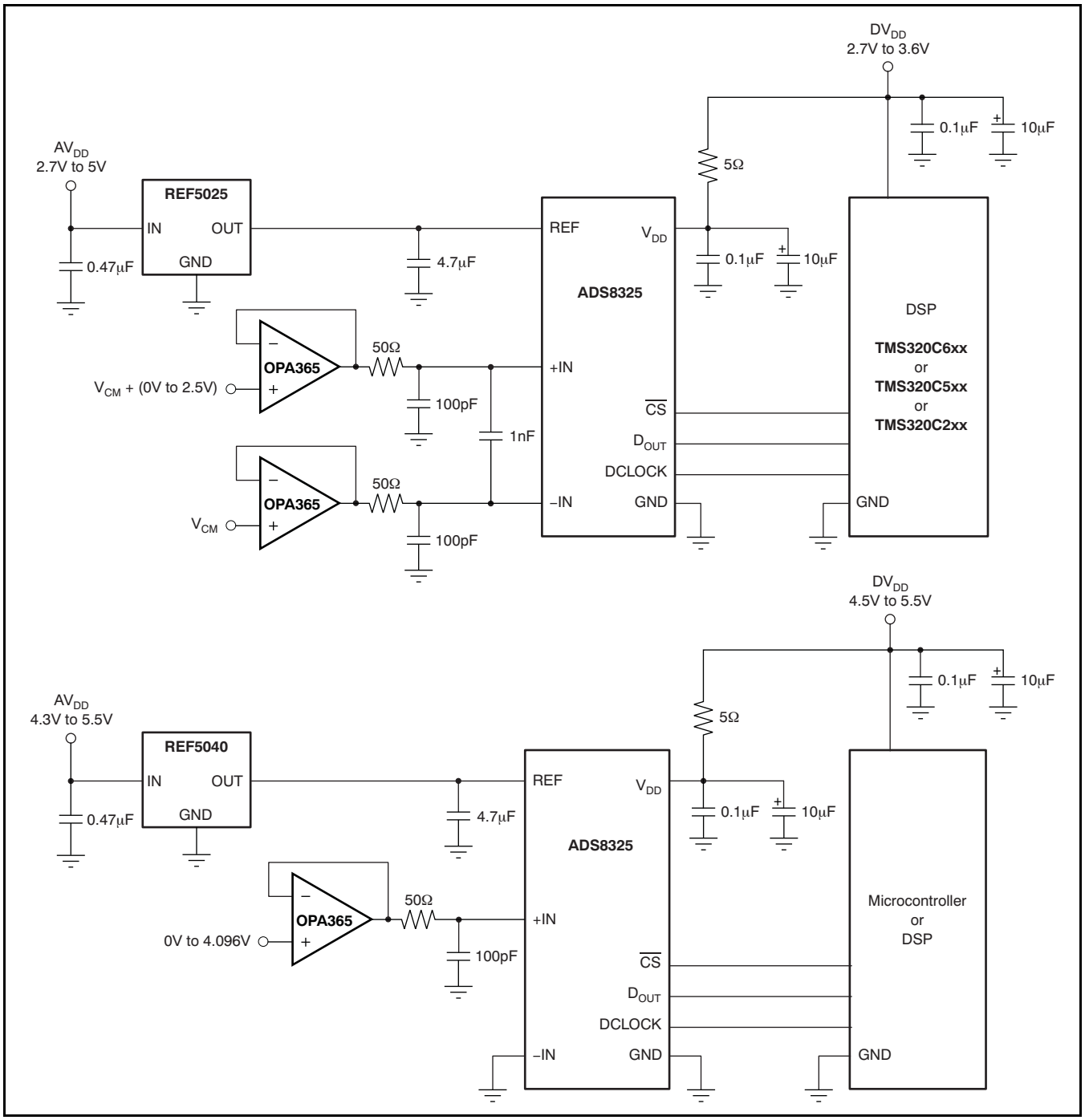

Figure 39. Two Examples of a Basic Data Acquisition System

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Revision History

Changes from Revision B (June 2007) to Revision C **Page**

- Changed note for DRB package. 7
- Changed second timing diagram from the top; moved Hi-Z to span the entire range of t_{SMPL} 8

Changes from Revision A (June 2003) to Revision B **Page**

- Changed format of document to current standard look 1
- Changed R_{ON} and $C_{(SAMPLE)}$ values in Equivalent Input Circuit 3
- Added missing value from Digital Inputs, Input Current, B Grade (typo) 3
- Added missing values from Sampling Dynamics, B Grade (typo) 5
- Changed DRB package pinout drawing to include thermal pad outline (not to scale) 7
- Changed timing diagram (added new diagram to existing figures) 8
- Added *Peak-to-Peak Noise For a DC Input vs Reference Voltage* plot 11
- Changed input capcitance from 20pF to 40pF (regarding the source of the analog input voltage) 16
- Changed Figure 31 17
- Changed Figure 33 capacitor from 47F to 47µF (typo) 18
- Changed V_{FS} from 7FFFH to FFFFH in Figure 36 20
- Changed Figure 39 23

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
ADS8325IBDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDGKRG4	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDRBR	ACTIVE	SON	DRB	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDRBRG4	ACTIVE	SON	DRB	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IBDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDGKR	ACTIVE	MSOP	DGK	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDGKT	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDGKTG4	ACTIVE	MSOP	DGK	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDRBR	ACTIVE	SON	DRB	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDRBRG4	ACTIVE	SON	DRB	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDRBT	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
ADS8325IDRBTG4	ACTIVE	SON	DRB	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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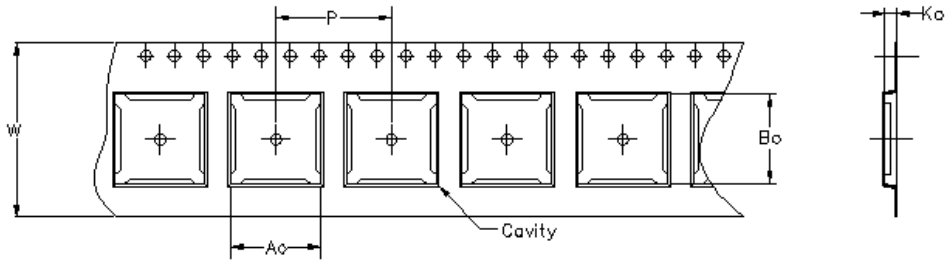
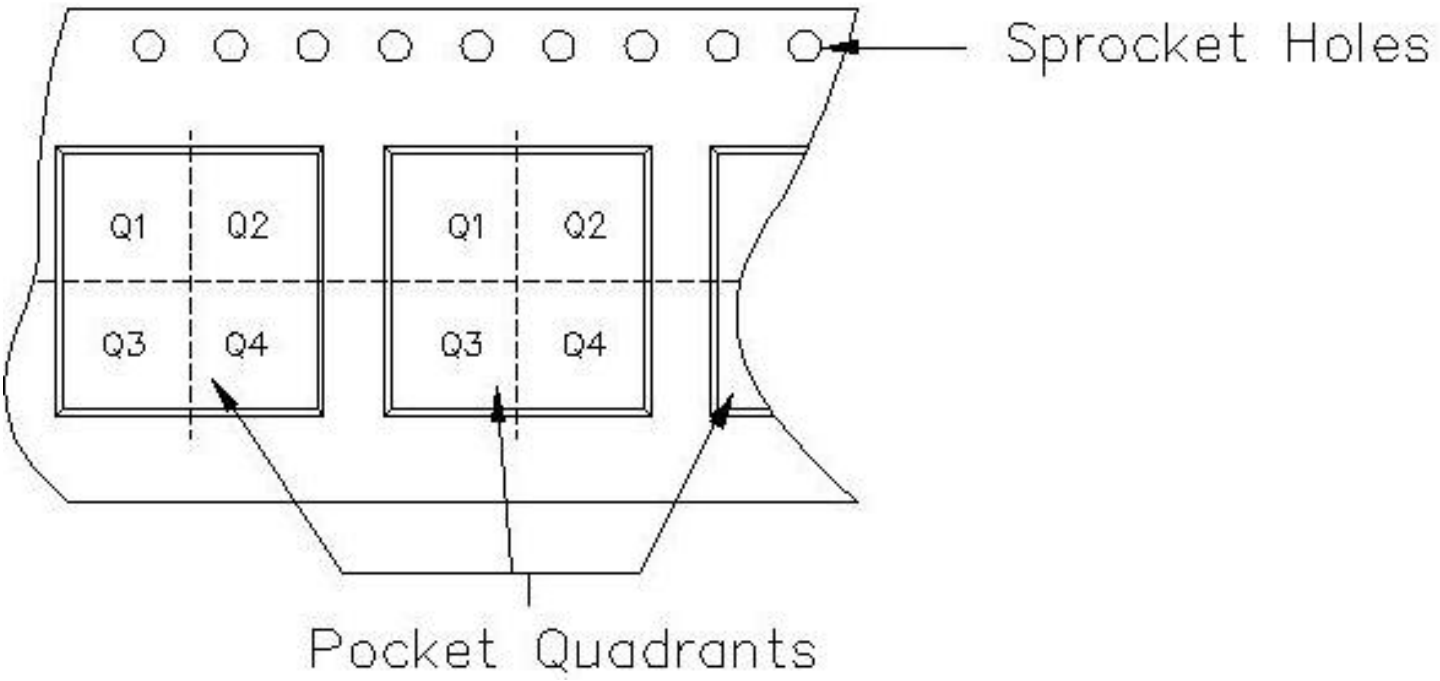


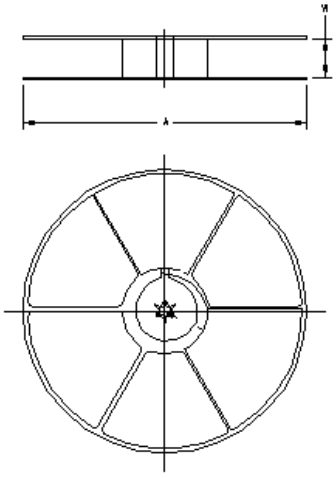
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao = Dimension designed to accommodate the component width.
Bo = Dimension designed to accommodate the component length.
Ko = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



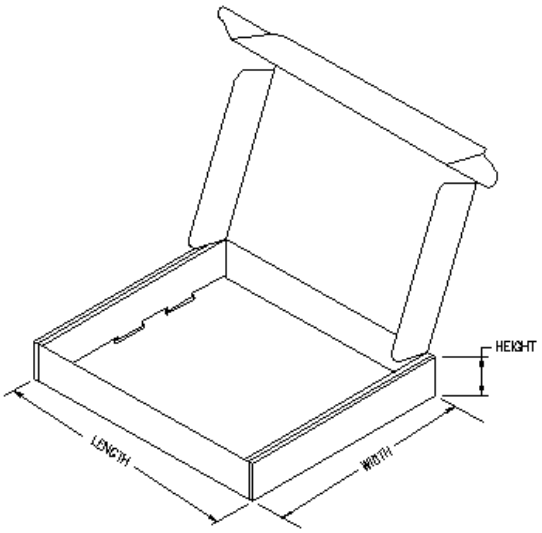
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8325IBDGKR	DGK	8	MLA	330	12	5.2	3.3	1.6	12	12	NONE
ADS8325IBDGKT	DGK	8	MLA	330	12	5.2	3.3	1.6	12	12	NONE
ADS8325IBDRBR	DRB	8	TUA	330	12	3.3	3.3	1.1	8	12	Q2
ADS8325IBDRBT	DRB	8	TUA	330	12	3.3	3.3	1.1	8	12	Q2
ADS8325IDGKR	DGK	8	MLA	330	12	5.2	3.3	1.6	12	12	NONE
ADS8325IDGKT	DGK	8	MLA	330	12	5.2	3.3	1.6	12	12	NONE
ADS8325IDRBR	DRB	8	TUA	330	12	3.3	3.3	1.1	8	12	Q2
ADS8325IDRBT	DRB	8	TUA	330	12	3.3	3.3	1.1	8	12	Q2

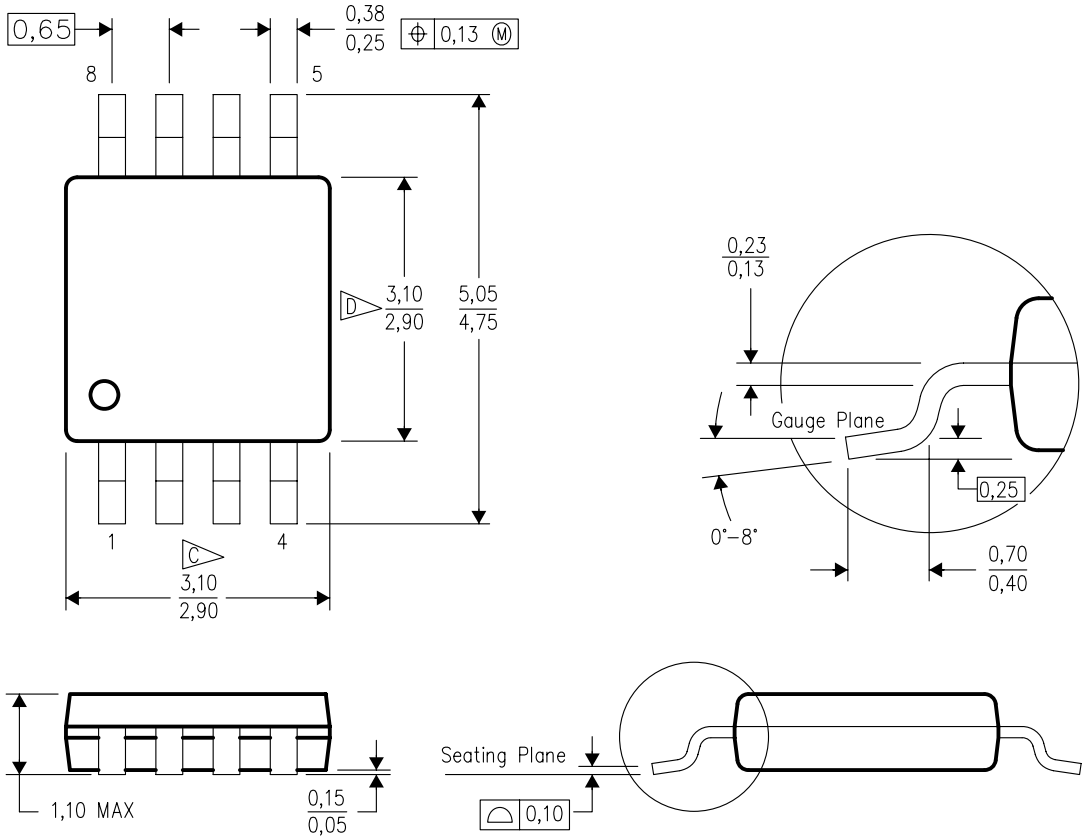


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
ADS8325IBDGKR	DGK	8	MLA	390.0	348.0	63.0
ADS8325IBDGKT	DGK	8	MLA	390.0	348.0	63.0
ADS8325IBDRBR	DRB	8	TUA	0.0	0.0	0.0
ADS8325IBDRBT	DRB	8	TUA	0.0	0.0	0.0
ADS8325IDGKR	DGK	8	MLA	390.0	348.0	63.0
ADS8325IDGKT	DGK	8	MLA	390.0	348.0	63.0
ADS8325IDRBR	DRB	8	TUA	0.0	0.0	0.0
ADS8325IDRBT	DRB	8	TUA	0.0	0.0	0.0


HEIGHT
LENGTH
WIDTH

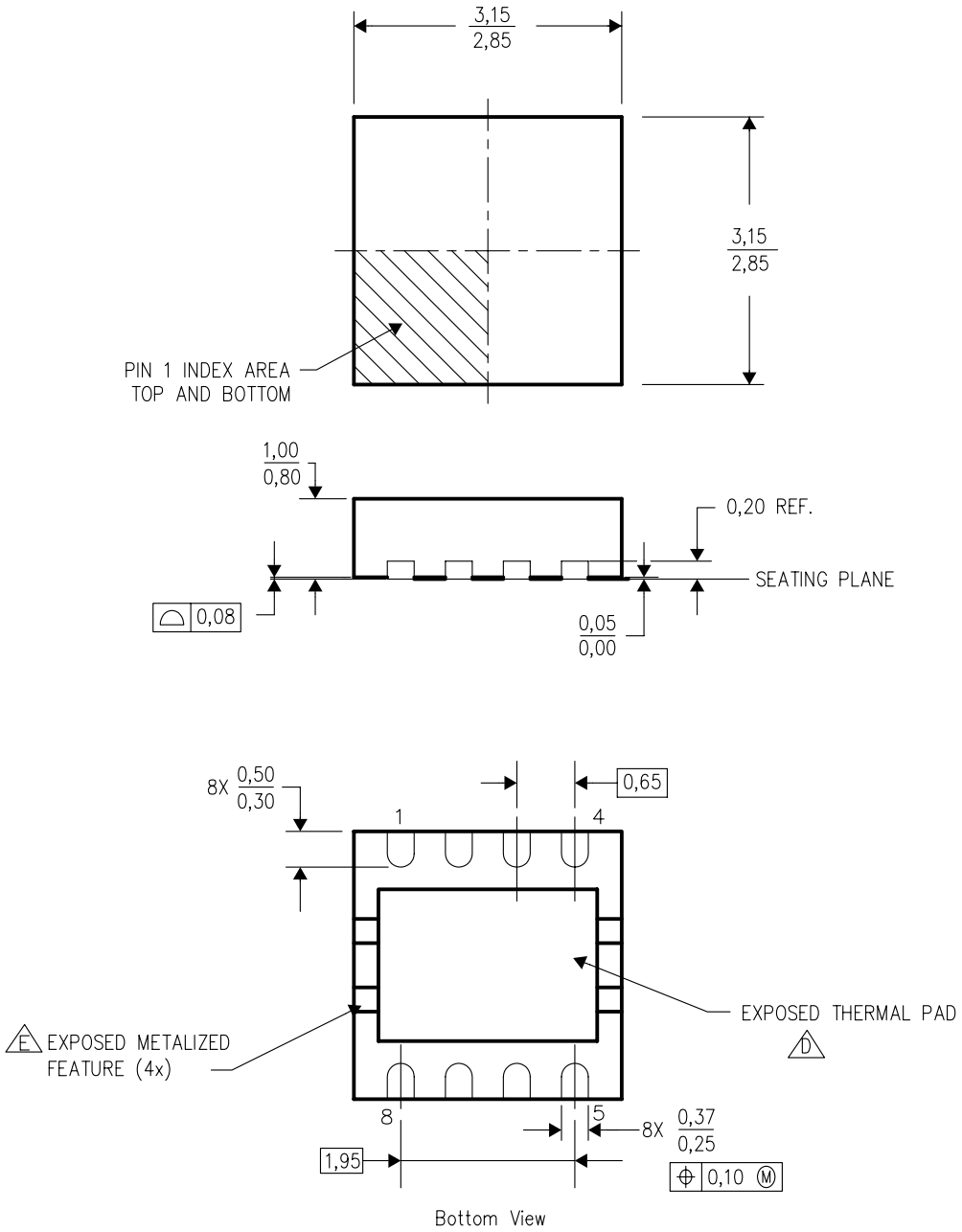
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DRB (S–PDSO–N8) PLASTIC SMALL OUTLINE



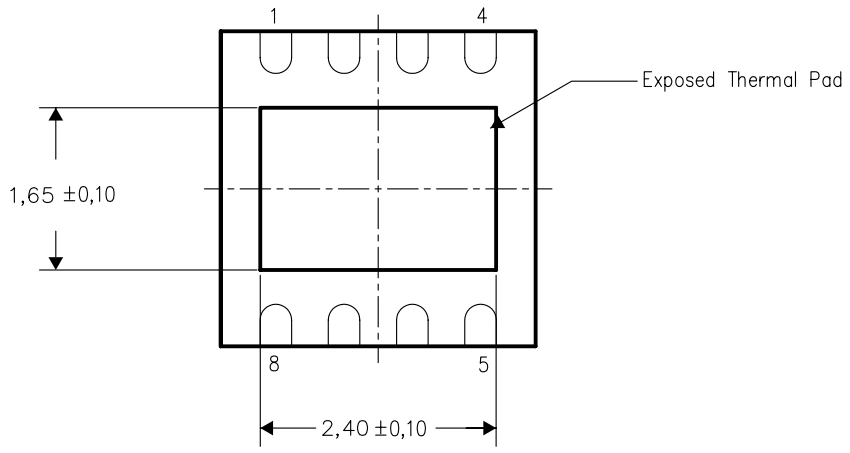
4203482/G 11/04

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

THERMAL INFORMATION

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.

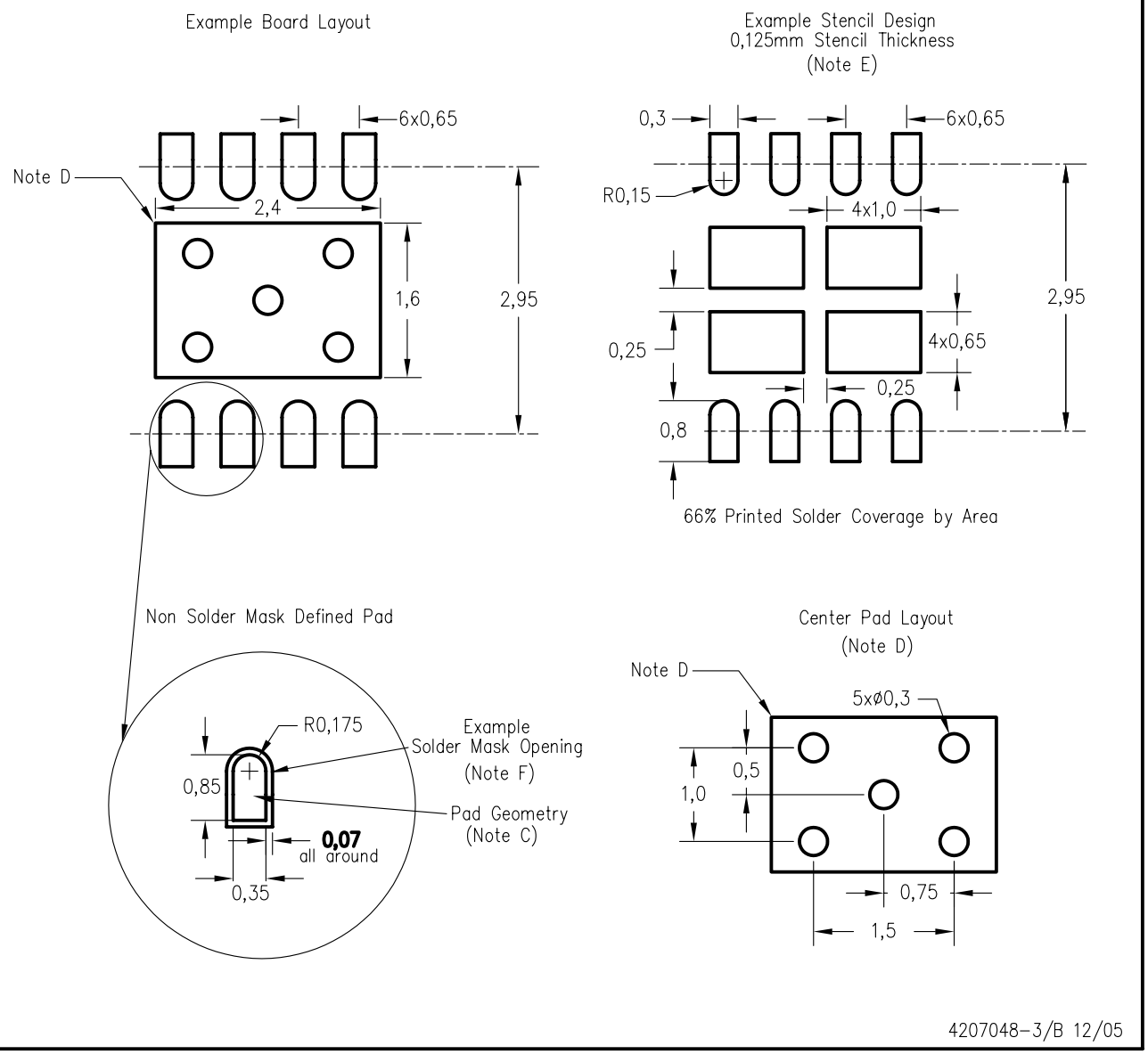


Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

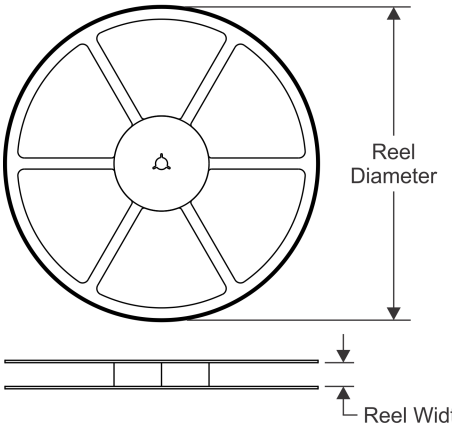
DRB (S–PDSO–N8)



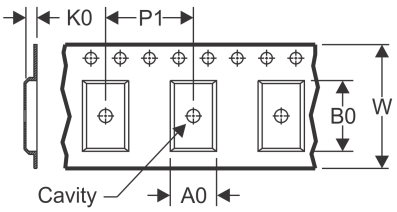
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SCBA017, SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for solder mask tolerances.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

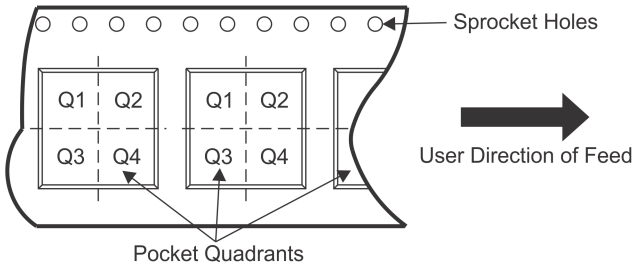


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

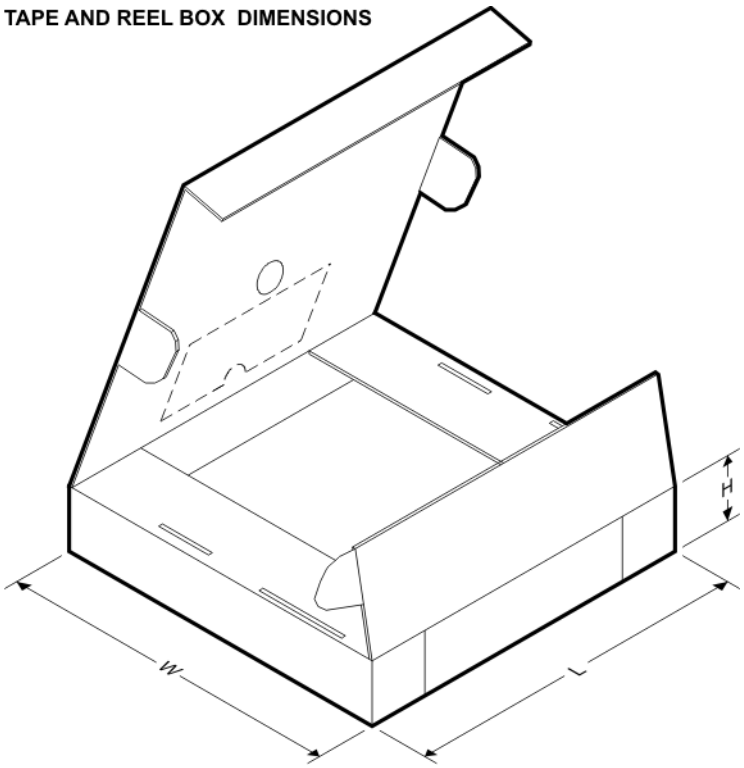
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS8325IBDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8325IBDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8325IBDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8325IDGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8325IDGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
ADS8325IDRBR	SON	DRB	8	2500	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
ADS8325IDRBT	SON	DRB	8	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS8325IBDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
ADS8325IBDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8325IBDRBT	SON	DRB	8	250	210.0	185.0	35.0
ADS8325IDGKR	VSSOP	DGK	8	2500	367.0	367.0	35.0
ADS8325IDGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
ADS8325IDRBR	SON	DRB	8	2500	367.0	367.0	35.0
ADS8325IDRBT	SON	DRB	8	250	210.0	185.0	35.0

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