THE DATASHEET OF

AFT18S290-13SR3

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RoHS

RF Power LDMOS Transistor

N−Channel Enhancement−Mode Lateral MOSFET

AFT18S290−13SR3

1805−1995 MHz, 63 W AVG., 28 V

This 63 watt RF power LDMOS transistor is designed for cellular base station applications covering the frequency range of 1805 to 1995 MHz.

- Typical Single−Carrier W−CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 2000 mA, P_{out} = 63 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1930 MHz	18.0	31.2	7.1	−36.0	−19
1960 MHz	18.2	31.2	7.1	−35.0	−19
1995 MHz	18.2	31.8	6.9	−35.0	−12

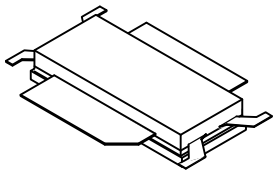
1800 MHz

- Typical Single−Carrier W−CDMA Performance: V_{DD} = 28 Volts, I_{DQ} = 2000 mA, P_{out} = 63 Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	G_{ps} (dB)	η_D (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
1805 MHz	18.0	33.3	7.1	−35.0	−13
1840 MHz	18.2	32.7	7.1	−35.0	−16
1880 MHz	18.3	32.6	7.1	−34.0	−13

Features

- Greater Negative Gate−Source Voltage Range for Improved Class C Operation
- Designed for Digital Predistortion Error Correction Systems
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 44 mm Tape Width, 13−inch Reel.



NI−880XS−2L4S

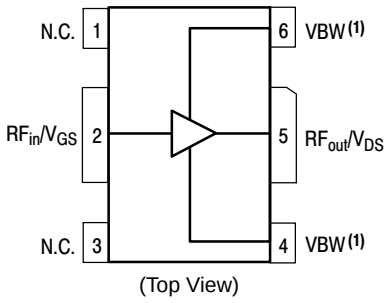


Figure 1. Pin Connections

1. Device cannot operate with the V_{DD} current supplied through pin 4 and pin 6.

freescale Airfast

Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain−Source Voltage	V_{DSS}	−0.5, +65	Vdc
Gate−Source Voltage	V_{GS}	−6.0, +10	Vdc
Operating Voltage	V_{DD}	32, +0	Vdc
Storage Temperature Range	T_{stg}	−65 to +150	°C
Case Operating Temperature Range	T_C	−40 to +150	°C
Operating Junction Temperature Range (1,2)	T_J	−40 to +225	°C
CW Operation @ T_C = 25°C Derate above 25°C	CW	245 1.6	W W/°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 80°C, 66 W CW, 28 Vdc, I_{DQ} = 2000 mA, 1960 MHz	$R_{\theta JC}$	0.42	°C/W

Table 3. ESD Protection Characteristics

Test Methodology	Class
Human Body Model (per JESD22−A114)	2
Machine Model (per EIA/JESD22−A115)	B
Charge Device Model (per JESD22−C101)	IV

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 65 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 28 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate−Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 389 μAdc)	$V_{GS(th)}$	1.5	2.0	2.5	Vdc
Gate Quiescent Voltage (V_{DD} = 28 Vdc, I_D = 2000 mAdc, Measured in Functional Test)	$V_{GS(Q)}$	2.3	2.8	3.3	Vdc
Drain−Source On−Voltage (V_{GS} = 10 Vdc, I_D = 5.0 Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

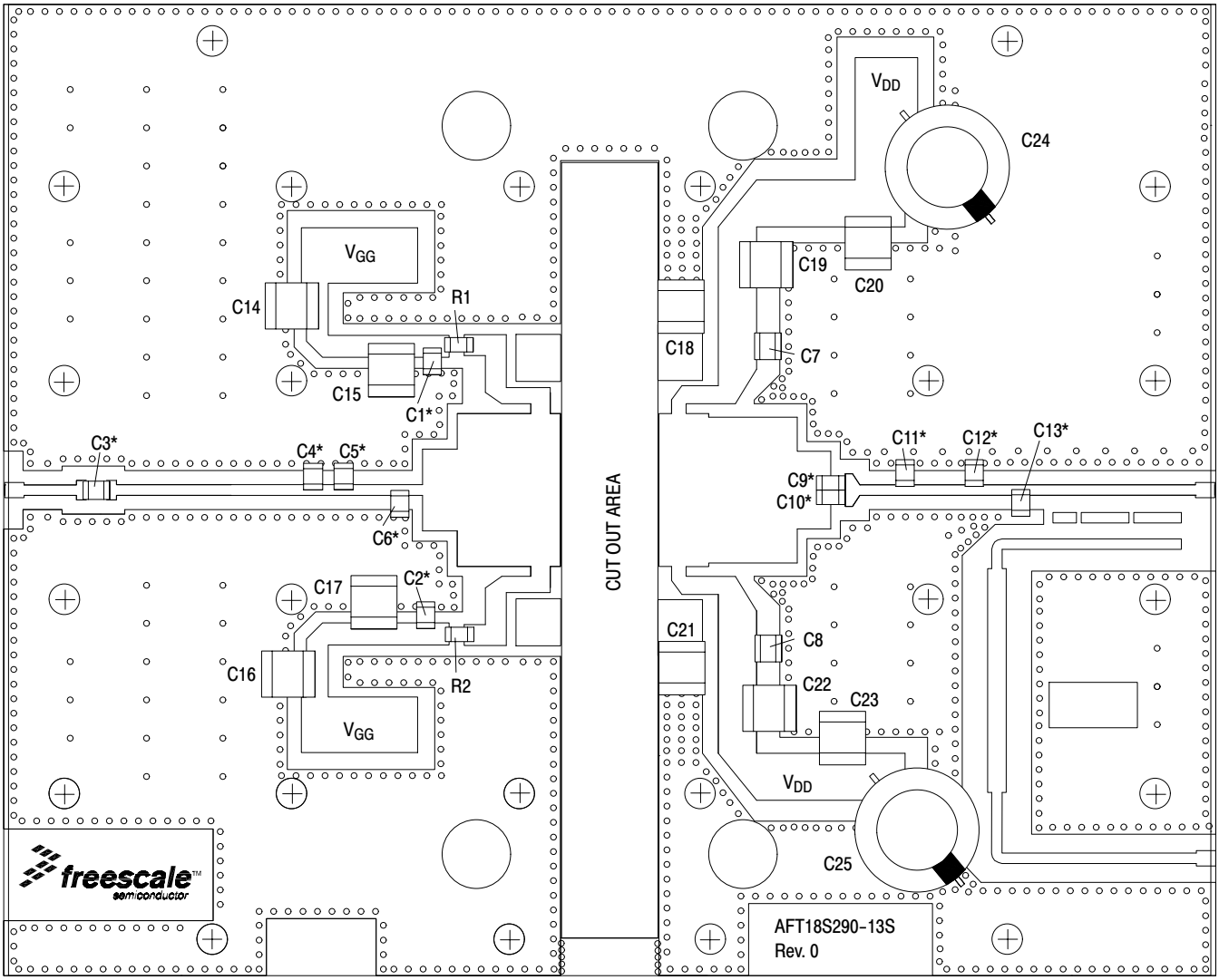
1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at http://www.freescale.com/rf. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers.* Go to http://www.freescale.com/rf. Select Documentation/Application Notes − AN1955.

(continued)

Table 4. Electrical Characteristics (T_A = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (1) (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 2000 mA, P_{out} = 63 W Avg., f = 1960 MHz, Single−Carrier W−CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @ ±5 MHz Offset.					
Power Gain	G_{ps}	17.2	18.2	20.2	dB
Drain Efficiency	η_D	29.5	31.2	—	%
Output Peak−to−Average Ratio @ 0.01% Probability on CCDF	PAR	6.6	7.1	—	dB
Adjacent Channel Power Ratio	ACPR	—	−35.0	−34.0	dBc
Input Return Loss	IRL	—	−19	−6	dB
Load Mismatch (In Freescale Test Fixture, 50 ohm system) I_{DQ} = 2000 mA, f = 1960 MHz					
VSWR 10:1 at 32 Vdc, 363 W CW (2) Output Power (3 dB Input Overdrive from 263 W CW (2) Rated Power)	No Device Degradation				
Typical Performance (In Freescale Test Fixture, 50 ohm system) V_{DD} = 28 Vdc, I_{DQ} = 2000 mA, 1930−1995 MHz Bandwidth					
P_{out} @ 1 dB Compression Point, CW	P1dB	—	263 (2)	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 1930−1995 MHz bandwidth)	Φ	—	15	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW_{res}	—	85	—	MHz
Gain Flatness in 65 MHz Bandwidth @ P_{out} = 63 W Avg.	G_F	—	0.2	—	dB
Gain Variation over Temperature (−30°C to +85°C)	ΔG	—	0.01	—	dB/°C
Output Power Variation over Temperature (−30°C to +85°C) (2)	ΔP1dB	—	0.003	—	dB/°C

1. Part internally matched both on input and output.
2. Exceeds recommended operating conditions. See CW operation data in Maximum Ratings table.



*C1, C2, C3, C4, C5, C6, C9, C10, C11, C12 and C13 are mounted vertically.

Figure 2. AFT18S290−13SR3 Test Circuit Component Layout — 1930−1995 MHz

Table 5. AFT18S290−13SR3 Test Circuit Component Designations and Values — 1930−1995 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C3, C7 C8	8.2 pF Chip Capacitors	ATC100B8R2BT500XT	ATC
C4	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C5	1.1 pF Chip Capacitor	ATC100B1R1BT500XT	ATC
C6	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
C9, C10	8.2 pF Chip Capacitors	ATC800B8R2BT500XT	ATC
C11, C12	0.4 pF Chip Capacitors	ATC100B0R4BT500XT	ATC
C13	0.5 pF Chip Capacitor	ATC100B0R5BT500XT	ATC
C14, C15, C16, C17, C18, C19, C20, C21, C22, C23	10 µF Chip Capacitors	C5750X7S2A106M230KB	TDK
C24, C25	470 µF, 63 V Electrolytic Capacitors	UVZ1J471MHD	Nichicon
R1, R2	2 Ω, 1/4 W Chip Resistors	CRCW12062R00FKEA	Vishay
PCB	0.020″, εr = 3.5	RO4350B	Rogers

TYPICAL CHARACTERISTICS — 1930−1995 MHz

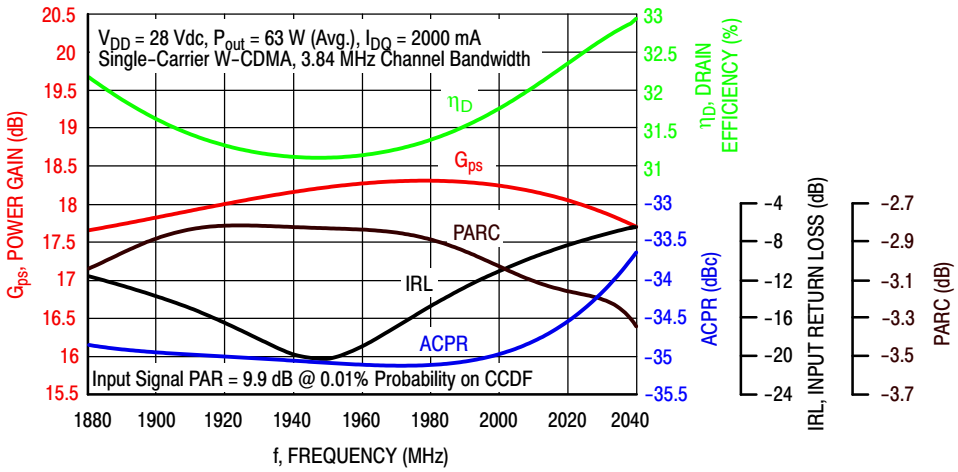


Figure 3. Single−Carrier Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

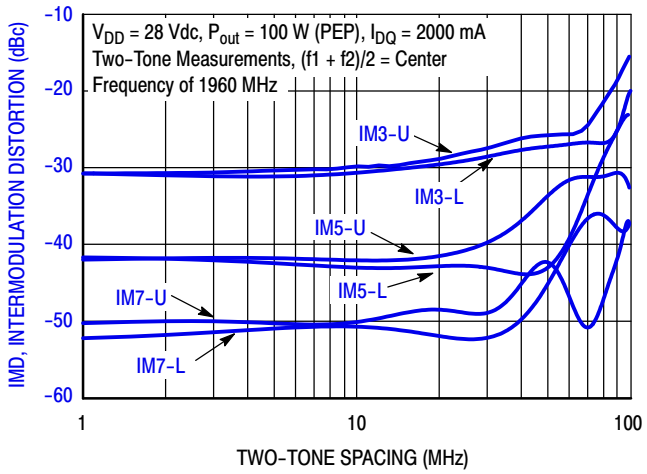


Figure 4. Intermodulation Distortion Products versus Two−Tone Spacing

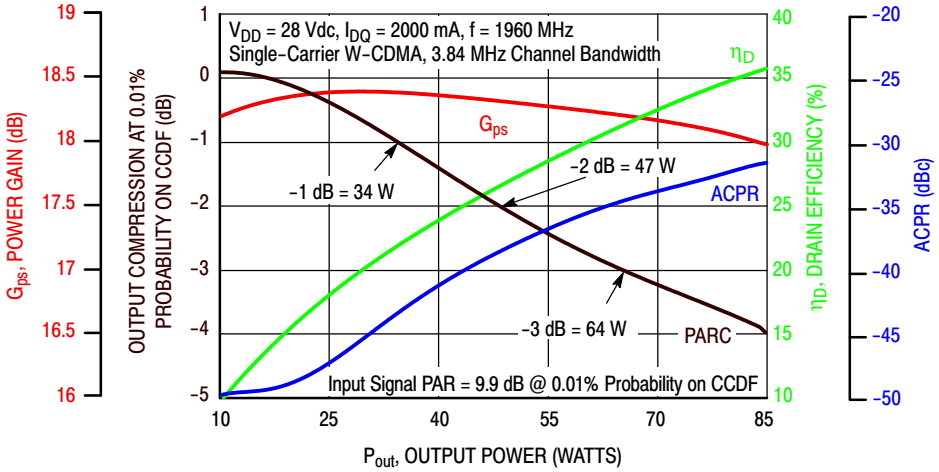


Figure 5. Output Peak−to−Average Ratio Compression (PARC) versus Output Power

TYPICAL CHARACTERISTICS — 1930−1995 MHz

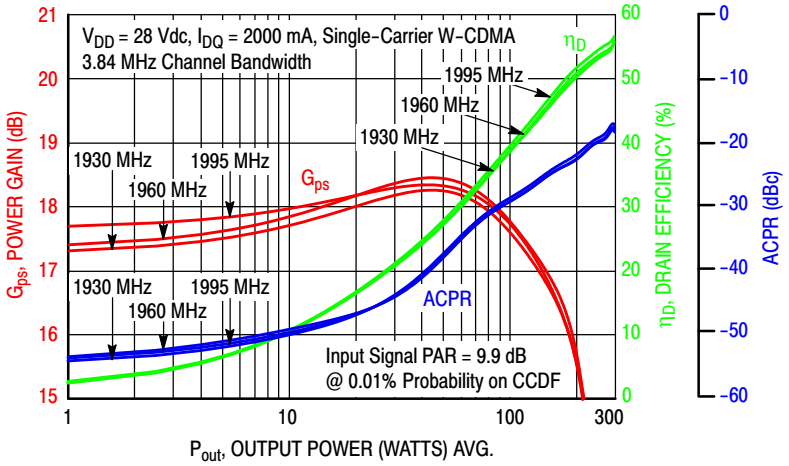


Figure 6. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

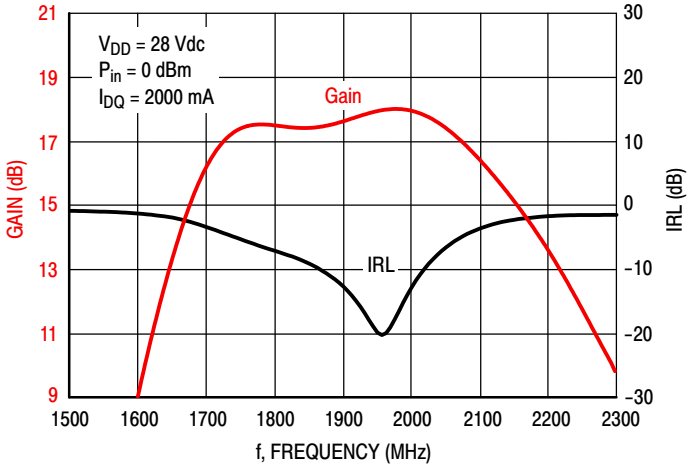


Figure 7. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 2077 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	4.65 − j5.42	4.26 + j5.36	1.01 − j2.59	17.2	55.4	344	53.8	−11
1960	5.36 − j4.16	6.21 + j4.97	1.07 − j2.68	17.2	55.2	334	53.5	−10
1990	8.71 − j2.52	8.15 + j2.81	1.09 − j2.82	17.2	55.3	338	53.1	−11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	4.65 − j5.42	4.49 + j5.53	1.07 − j2.75	15.0	56.2	419	57.1	−15
1960	5.36 − j4.16	6.63 + j5.03	1.11 − j2.85	15.0	56.1	407	55.9	−15
1990	8.71 − j2.52	8.59 + j2.49	1.16 − j2.99	15.0	56.1	411	55.8	−16

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 8. Load Pull Performance — Maximum Power Tuning

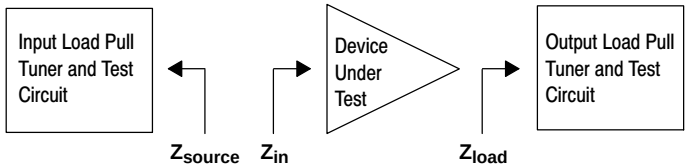
V_{DD} = 28 Vdc, I_{DQ} = 2077 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	4.65 − j5.42	4.89 + j5.31	1.71 − j1.45	19.7	53.5	224	65.3	−16
1960	5.36 − j4.16	6.97 + j4.39	1.64 − j1.37	19.7	53.1	205	64.5	−15
1990	8.71 − j2.52	8.27 + j1.78	1.57 − j1.60	19.6	53.4	220	64.0	−16

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1930	4.65 − j5.42	5.07 + j5.44	1.72 − j1.56	17.6	54.4	275	67.3	−23
1960	5.36 − j4.16	7.25 + j4.47	1.64 − j1.65	17.4	54.4	275	66.3	−22
1990	8.71 − j2.52	8.62 + j1.34	1.51 − j1.63	17.6	54.2	262	65.9	−24

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB − TYPICAL LOAD PULL CONTOURS — 1960 MHz

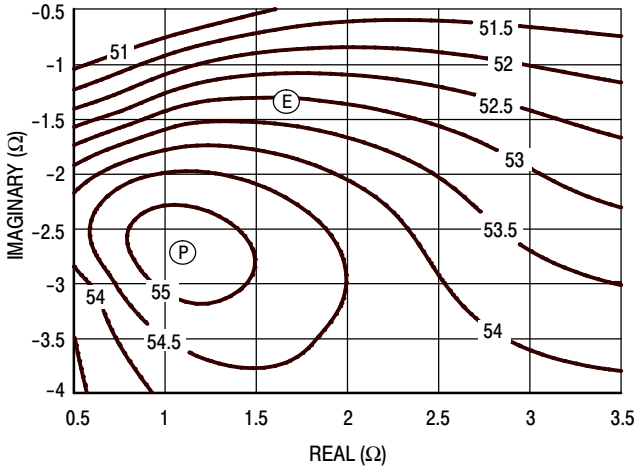


Figure 10. P1dB Load Pull Output Power Contours (dBm)

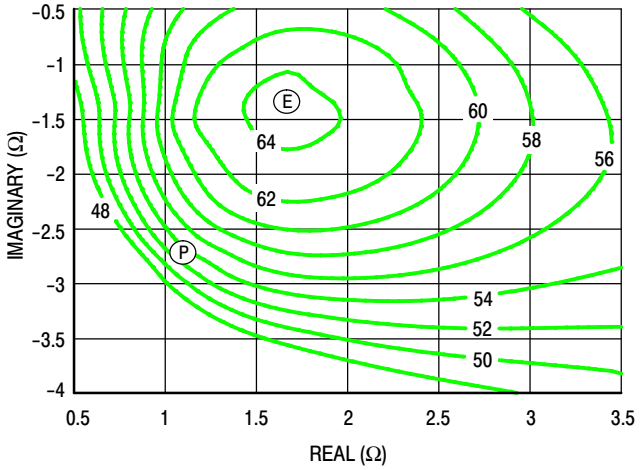


Figure 11. P1dB Load Pull Efficiency Contours (%)

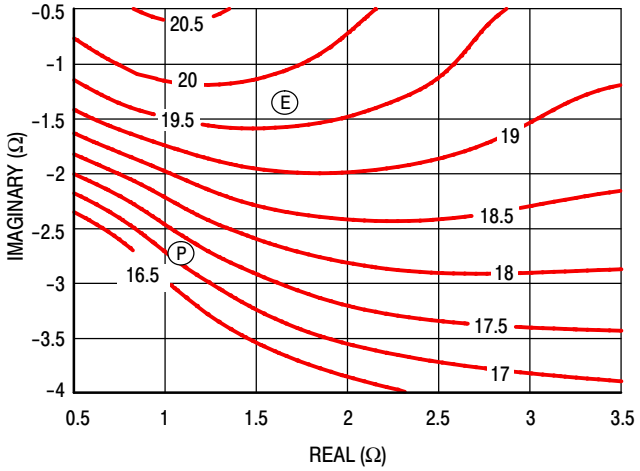


Figure 12. P1dB Load Pull Gain Contours (dB)

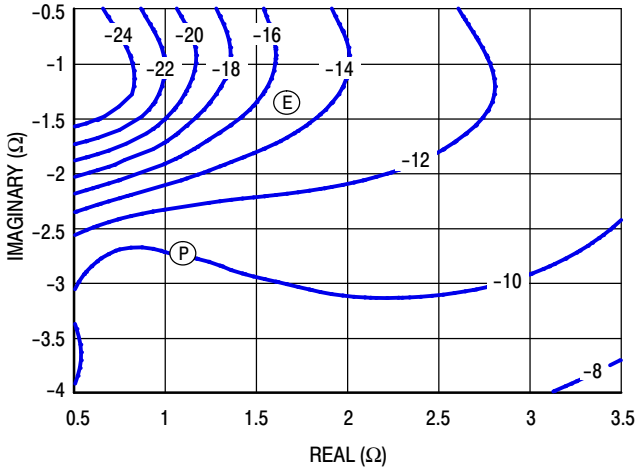


Figure 13. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB − TYPICAL LOAD PULL CONTOURS — 1960 MHz

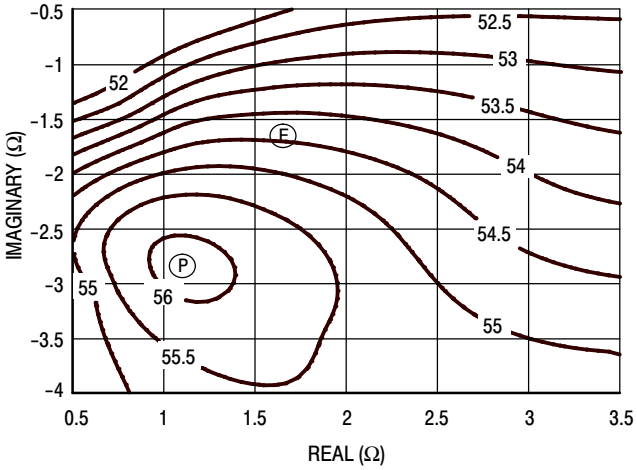


Figure 14. P3dB Load Pull Output Power Contours (dBm)

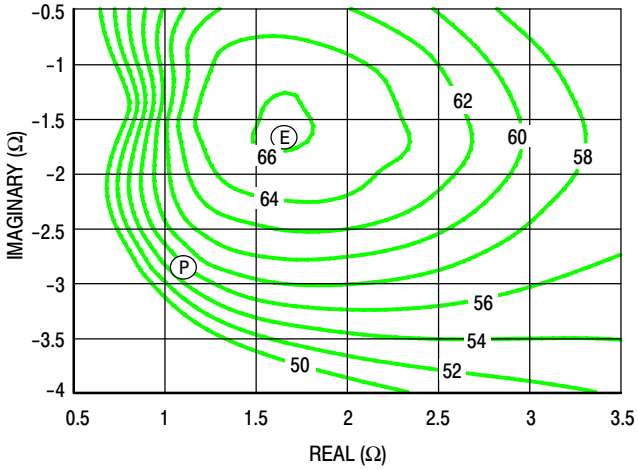


Figure 15. P3dB Load Pull Efficiency Contours (%)

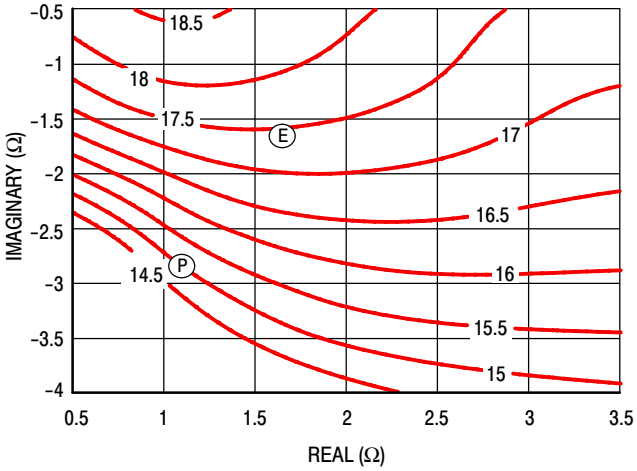


Figure 16. P3dB Load Pull Gain Contours (dB)

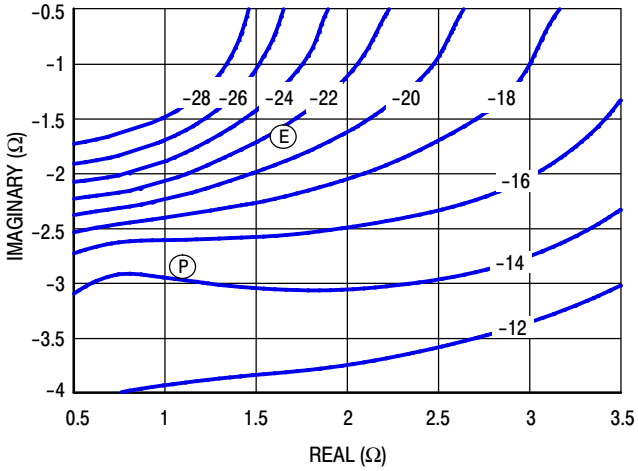


Figure 17. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

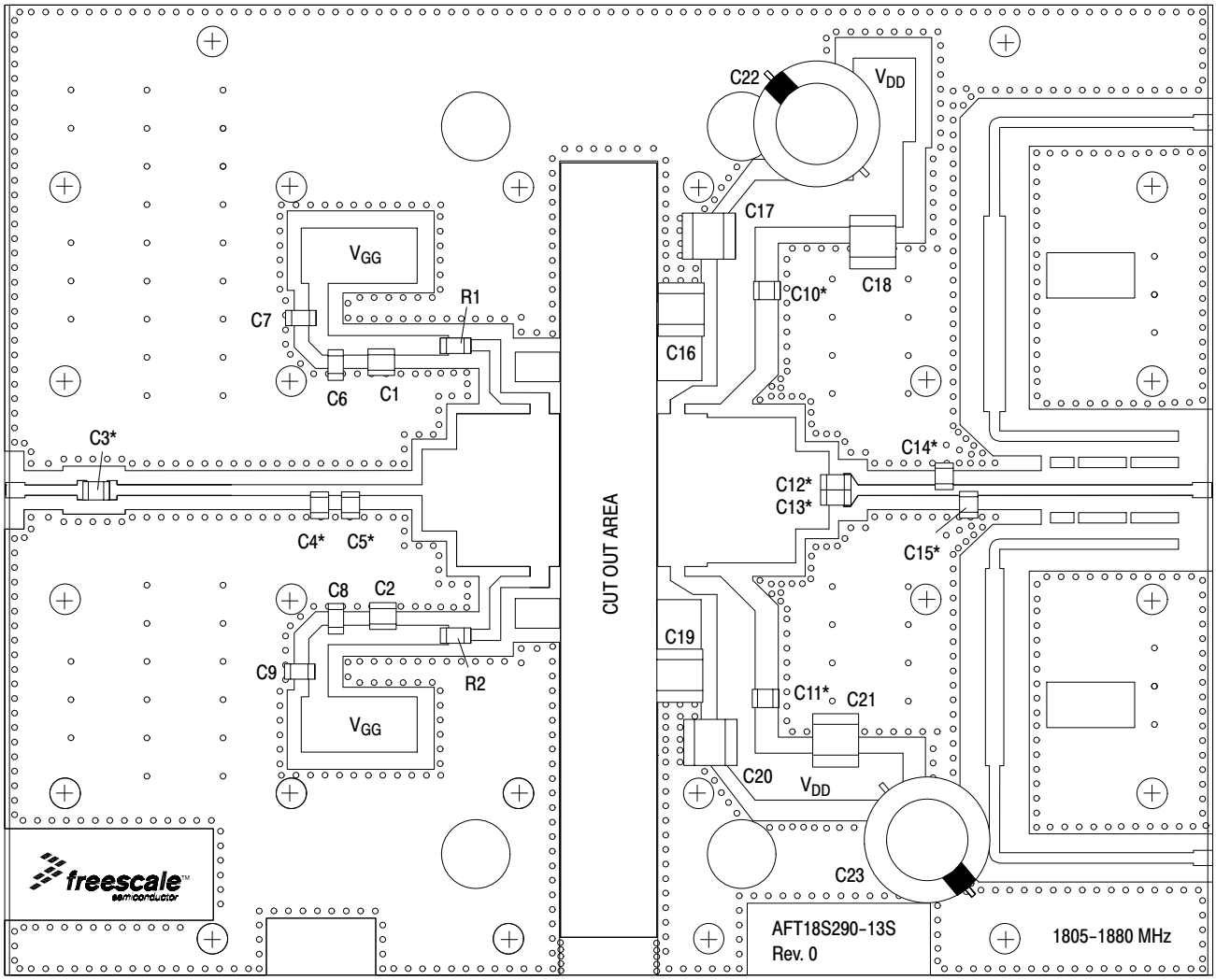
Power Gain

Drain Efficiency

Linearity

Output Power

ALTERNATIVE CHARACTERIZATION — 1805−1880 MHz



*C3, C4, C5, C10, C11, C12, C13, C14 and C15 are mounted vertically.

Figure 18. AFT18S290−13SR3 Test Circuit Component Layout — 1805−1880 MHz

Table 6. AFT18S290−13SR3 Test Circuit Component Designations and Values — 1805−1880 MHz

Part	Description	Part Number	Manufacturer
C1, C2, C10, C11	12 pF Chip Capacitors	ATC100B120JT500XT	ATC
C3	8.2 pF Chip Capacitor	ATC100B8R2CT500XT	ATC
C4	0.7 pF Chip Capacitor	ATC100B0R7BT500XT	ATC
C5	0.8 pF Chip Capacitor	ATC100B0R8BT500XT	ATC
C6, C7, C8, C9	10 μF Chip Capacitors	GRM31CR61H106KA12L	Murata
C12, C13	8.2 pF Chip Capacitors	ATC800B8R2BW500XT	ATC
C14, C15	0.4 pF Chip Capacitors	ATC100B0R4BT500XT	ATC
C16, C17, C18, C19, C20, C21	10 μF Chip Capacitors	C5750X7S2A106M230KB	TDK
C22, C23	470 μF, 63 V Electrolytic Capacitors	MCGPR63V477M13X26−RH	Multicomp
R1, R2	2 Ω, 1/4 W Chip Resistors	CRCW12062R00FKEA	Vishay
PCB	0.020″, εr = 3.5	RO4350B	Rogers

ALTERNATIVE CHARACTERIZATION — 1805−1880 MHz

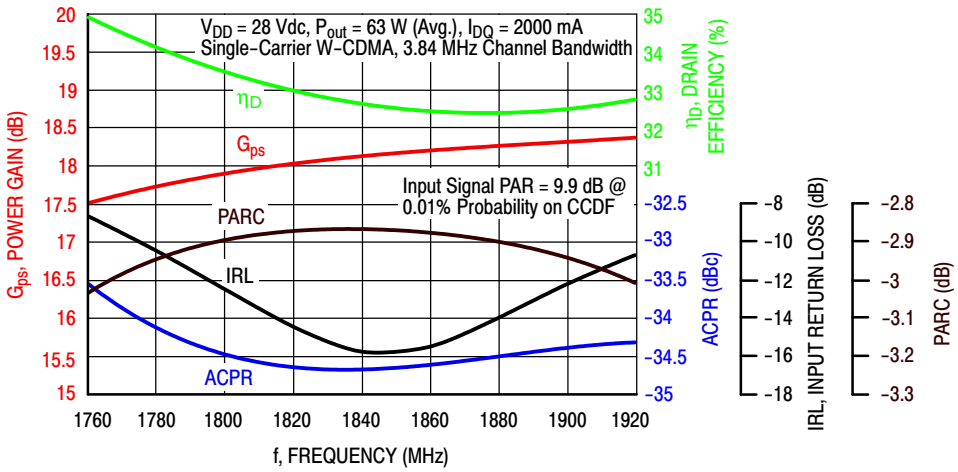


Figure 19. Single−Carrier Output Peak−to−Average Ratio Compression (PARC) Broadband Performance @ P_{out} = 63 Watts Avg.

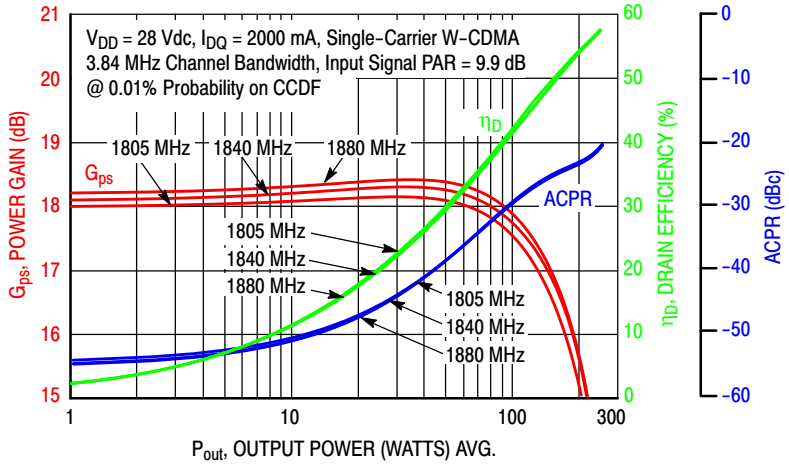


Figure 20. Single−Carrier W−CDMA Power Gain, Drain Efficiency and ACPR versus Output Power

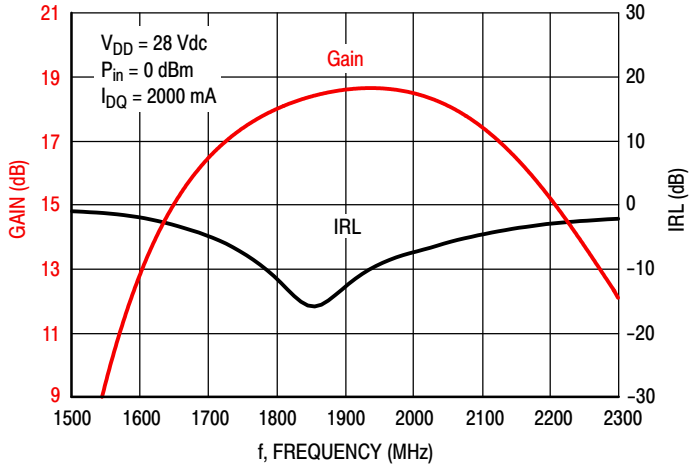


Figure 21. Broadband Frequency Response

V_{DD} = 28 Vdc, I_{DQ} = 2078 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1800	1.17 − j3.88	1.11 + j3.95	1.04 − j2.20	17.5	55.1	325	52.8	−9.8
1840	1.50 − j4.53	1.55 + j4.38	1.01 − j2.27	17.4	55.3	339	53.9	−11
1880	2.48 − j5.08	2.36 + j4.86	1.02 − j2.51	17.3	55.3	341	54.2	−11

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Output Power P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1800	1.17 − j3.88	1.10 + j4.01	1.03 − j2.36	15.3	56.1	405	57.0	−14
1840	1.50 − j4.53	1.56 + j4.47	1.03 − j2.53	15.1	56.2	417	57.3	−15
1880	2.48 − j5.08	2.39 + j5.03	1.02 − j2.62	15.1	56.2	418	57.0	−15

(1) Load impedance for optimum P1dB power.
(2) Load impedance for optimum P3dB power.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 22. Load Pull Performance — Maximum Power Tuning

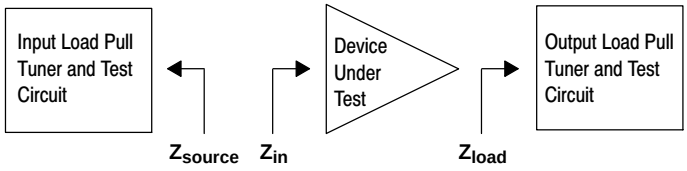
V_{DD} = 28 Vdc, I_{DQ} = 2078 mA, Pulsed CW, 10 μsec(on), 10% Duty Cycle

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P1dB Z_{load} (1) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1800	1.17 − j3.88	1.26 + j4.14	2.57 − j1.57	20.0	53.2	210	64.5	−13
1840	1.50 − j4.53	1.76 + j4.52	2.26 − j1.49	19.8	53.4	220	64.7	−14
1880	2.48 − j5.08	2.70 + j4.93	2.21 − j1.55	19.7	53.4	218	65.1	−14

f (MHz)	Z_{source} (Ω)	Z_{in} (Ω)	Max Drain Efficiency P3dB Z_{load} (2) (Ω)	Gain (dB)	(dBm)	(W)	η_D (%)	AM/PM (°)
1800	1.17 − j3.88	1.26 + j4.15	2.45 − j1.87	17.7	54.4	274	67.0	−19
1840	1.50 − j4.53	1.74 + j4.58	2.14 − j1.76	17.5	54.6	290	67.4	−21
1880	2.48 − j5.08	2.70 + j5.11	2.04 − j1.73	17.5	54.5	285	67.4	−21

(1) Load impedance for optimum P1dB efficiency.
(2) Load impedance for optimum P3dB efficiency.
Z_{source} = Measured impedance presented to the input of the device at the package reference plane.
Z_{in} = Impedance as measured from gate contact to ground.
Z_{load} = Measured impedance presented to the output of the device at the package reference plane.

Figure 23. Load Pull Performance — Maximum Drain Efficiency Tuning



P1dB − TYPICAL LOAD PULL CONTOURS — 1840 MHz

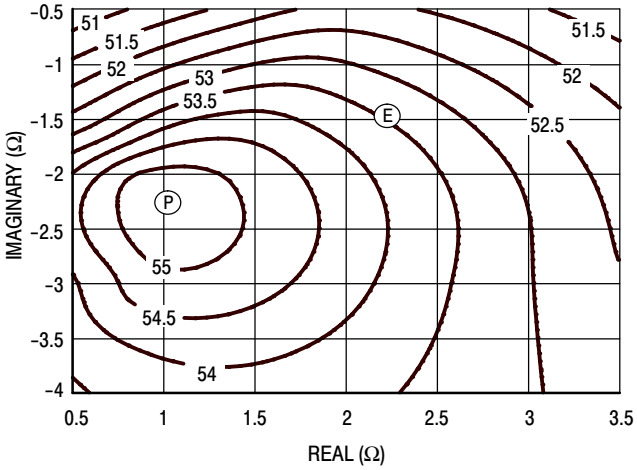


Figure 24. P1dB Load Pull Output Power Contours (dBm)

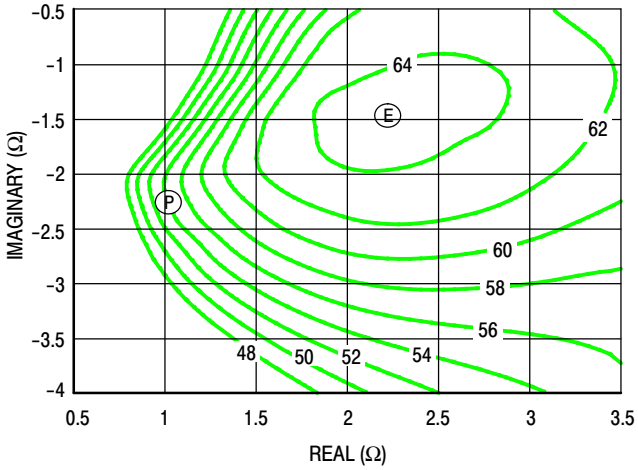


Figure 25. P1dB Load Pull Efficiency Contours (%)

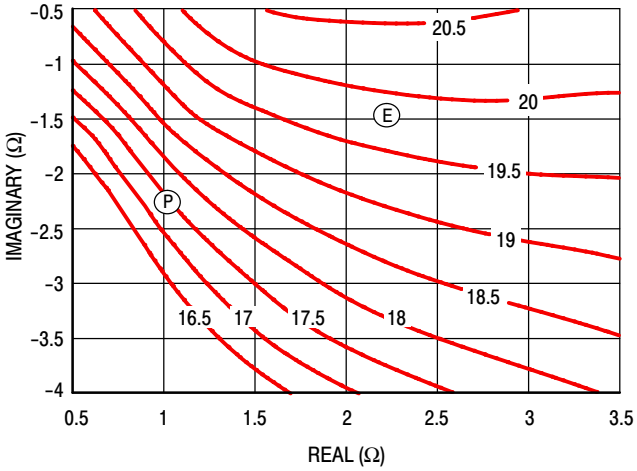


Figure 26. P1dB Load Pull Gain Contours (dB)

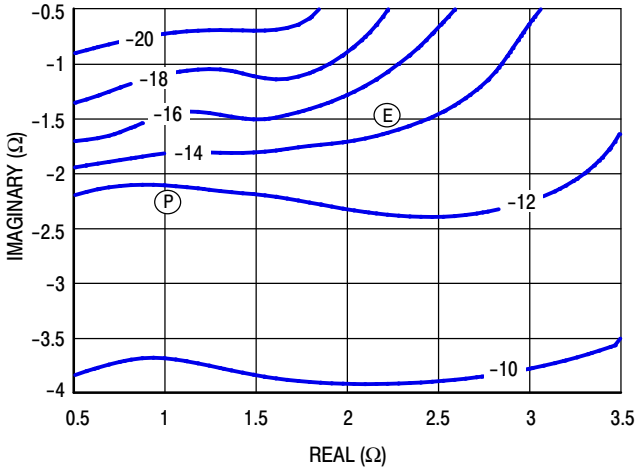


Figure 27. P1dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

Power Gain

Drain Efficiency

Linearity

Output Power

P3dB − TYPICAL LOAD PULL CONTOURS — 1840 MHz

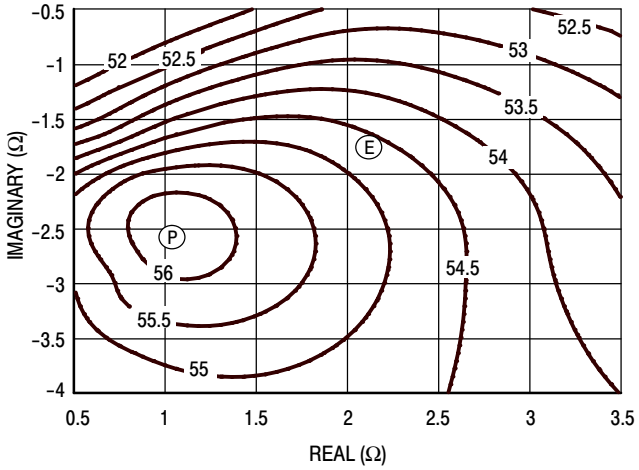


Figure 28. P3dB Load Pull Output Power Contours (dBm)

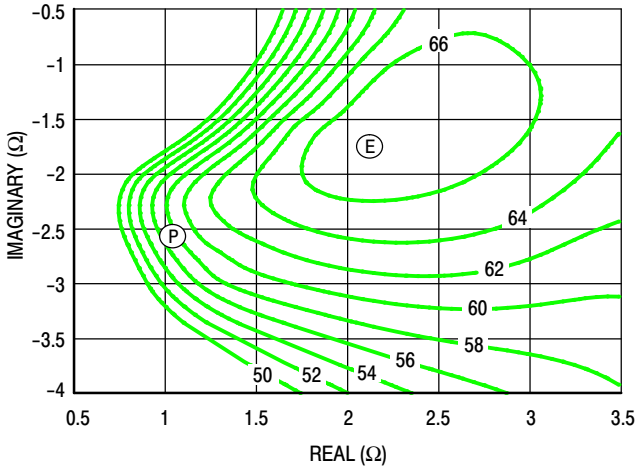


Figure 29. P3dB Load Pull Efficiency Contours (%)

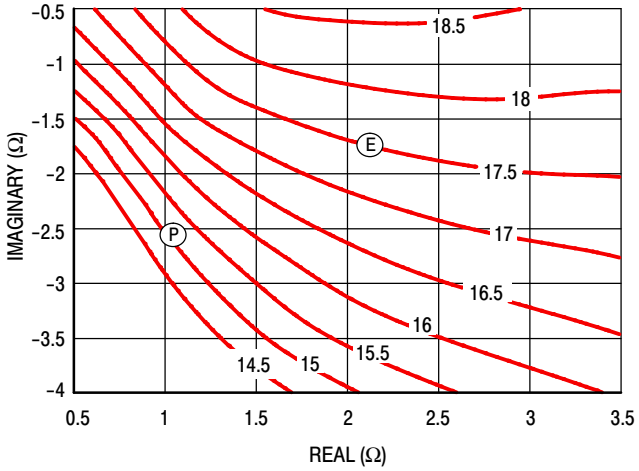


Figure 30. P3dB Load Pull Gain Contours (dB)

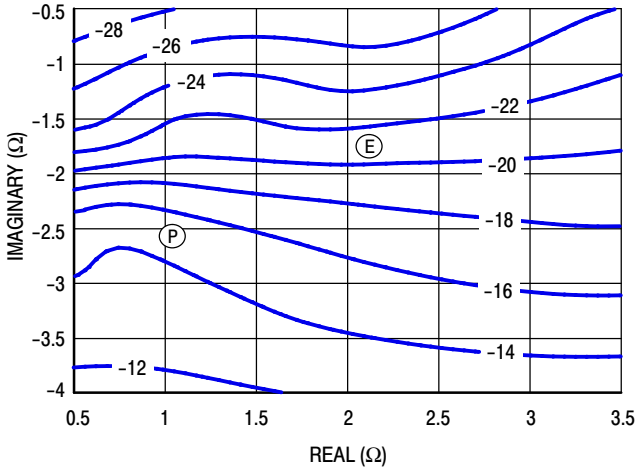


Figure 31. P3dB Load Pull AM/PM Contours (°)

NOTE: Ⓟ = Maximum Output Power

Ⓔ = Maximum Drain Efficiency

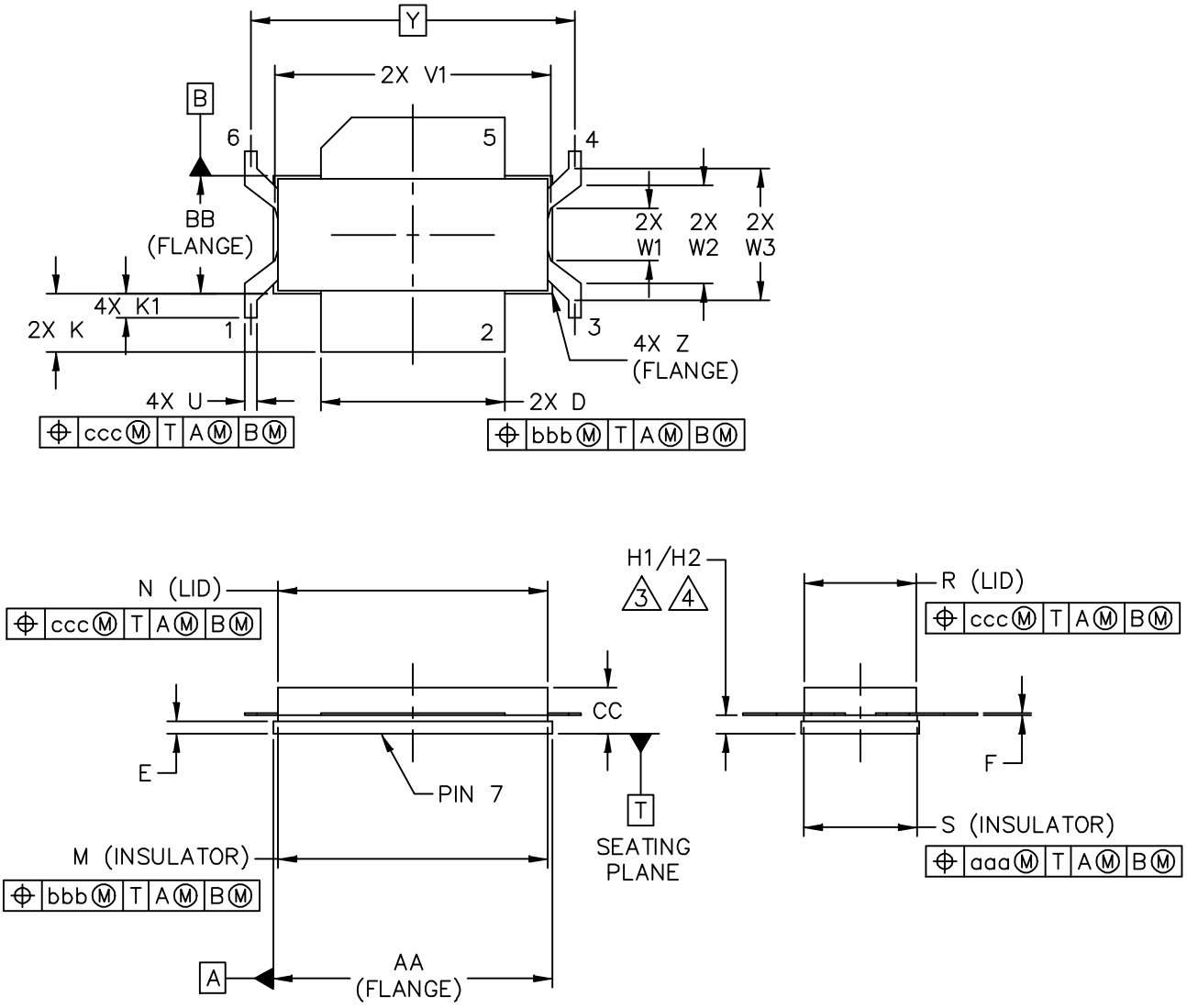
Power Gain

Drain Efficiency

Linearity

Output Power

PACKAGE DIMENSIONS



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NOTES:

1. CONTROLLING DIMENSION: INCH.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M–1994.

3. DIMENSIONS H1 AND H2 ARE MEASURED .030 INCH (0.762 MM) AWAY FROM FLANGE PARALLEL TO DATUM B. H1 APPLIES TO PINS 2 & 5. H2 APPLIES TO PINS 1, 3, 4 & 6.

4. TOLERANCE OF DIMENSION H2 IS TENTATIVE.

DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX	DIM	INCH MIN	INCH MAX	MILLIMETER MIN	MILLIMETER MAX
AA	.905	.915	22.99	23.24	R	.365	.375	9.27	9.53
BB	.380	.390	9.65	9.91	S	.365	.375	9.27	9.53
CC	.125	.170	3.18	4.32	U	.035	.045	0.89	1.14
D	.595	.605	15.11	15.37	V1	.895	.905	22.73	22.99
E	.035	.045	0.89	1.14	W1	.165	.175	4.19	4.45
F	.004	.007	0.10	0.18	W2	.315	.325	8.00	8.26
H1	.057	.067	1.45	1.70	W3	.425	.435	10.80	11.05
H2	.054	.070	1.37	1.78	Y	1.056 BSC		26.82 BSC	
K	.170	.210	4.32	5.33	Z	R.000	R.040	R.00	R1.02
K1	.070	.090	1.78	2.29	aaa	.005		0.13	
M	.874	.886	22.20	22.50	bbb	.010		0.25	
N	.872	.888	22.15	22.56	ccc	.015		0.38	

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PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at http://www.freescale.com, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	May 2013	• Initial Release of Data Sheet

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