



**THE DATASHEET OF  
AFT23S160W02SR3**





# RF Power LDMOS Transistors

## N-Channel Enhancement-Mode Lateral MOSFETs

These 45 watt RF power LDMOS transistors are designed for cellular base station applications requiring very wide instantaneous bandwidth capability covering the frequency range of 2300 to 2400 MHz.

- Typical Single-Carrier W-CDMA Performance:  $V_{DD} = 28$  Vdc,  $I_{DQ} = 1100$  mA,  $P_{out} = 45$  Watts Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)	IRL (dB)
2300 MHz	17.7	31.0	6.8	-34.6	-18
2350 MHz	17.8	30.5	6.7	-34.5	-25
2400 MHz	17.9	30.3	6.6	-33.9	-14

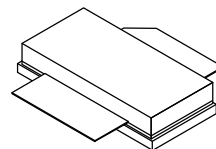
### Features

- Designed for Wide Instantaneous Bandwidth Applications
- Greater Negative Gate-Source Voltage Range for Improved Class C Operation
- Able to Withstand Extremely High Output VSWR and Broadband Operating Conditions
- Optimized for Doherty Applications
- In Tape and Reel. R3 Suffix = 250 Units, 56 mm Tape Width, 13-inch Reel.

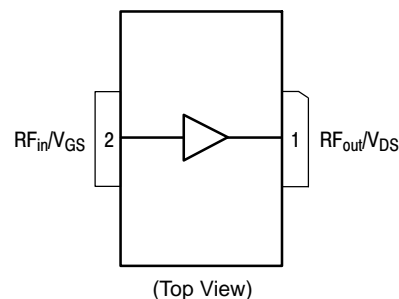
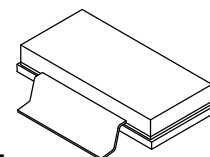
**AFT23S160W02SR3**  
**AFT23S160W02GSR3**

**2300-2400 MHz, 45 W AVG., 28 V**  
**AIRFAST RF POWER LDMOS**  
**TRANSISTORS**

NI-780S-2L  
AFT23S160W02SR3



NI-780GS-2L  
AFT23S160W02GSR3



**Figure 1. Pin Connections**

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain–Source Voltage	$V_{DSS}$	–0.5, +65	Vdc
Gate–Source Voltage	$V_{GS}$	–6.0, +10	Vdc
Operating Voltage	$V_{DD}$	32, +0	Vdc
Storage Temperature Range	$T_{stg}$	–65 to +150	°C
Case Operating Temperature Range	$T_C$	–40 to +125	°C
Operating Junction Temperature Range (1,2)	$T_J$	–40 to +225	°C

**Table 2. Thermal Characteristics**

Characteristic	Symbol	Value (2,3)	Unit
Thermal Resistance, Junction to Case Case Temperature 81°C, 45 W CW, 28 Vdc, $I_{DQ} = 1100$ mA, 2400 MHz	$R_{\theta JC}$	0.53	°C/W

**Table 3. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JESD22–A114)	2
Machine Model (per EIA/JESD22–A115)	B
Charge Device Model (per JESD22–C101)	IV

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
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**Off Characteristics**

Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 65$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	10	$\mu\text{Adc}$
Zero Gate Voltage Drain Leakage Current ( $V_{DS} = 28$ Vdc, $V_{GS} = 0$ Vdc)	$I_{DSS}$	—	—	5	$\mu\text{Adc}$
Gate–Source Leakage Current ( $V_{GS} = 5$ Vdc, $V_{DS} = 0$ Vdc)	$I_{GSS}$	—	—	1	$\mu\text{Adc}$

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10$ Vdc, $I_D = 219$ $\mu\text{Adc}$ )	$V_{GS(th)}$	0.9	1.3	1.7	Vdc
Gate Quiescent Voltage ( $V_{DD} = 28$ Vdc, $I_D = 1100$ mAdc, Measured in Functional Test)	$V_{GS(Q)}$	1.4	1.8	2.2	Vdc
Drain–Source On–Voltage ( $V_{GS} = 6$ Vdc, $I_D = 2.19$ Adc)	$V_{DS(on)}$	0.1	0.2	0.3	Vdc

**Functional Tests (4,5)** (In Freescale Test Fixture, 50 ohm system)  $V_{DD} = 28$  Vdc,  $I_{DQ} = 1100$  mA,  $P_{out} = 45$  W Avg.,  $f = 2400$  MHz, Single–Carrier W–CDMA, IQ Magnitude Clipping, Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF. ACPR measured in 3.84 MHz Channel Bandwidth @  $\pm 5$  MHz Offset.

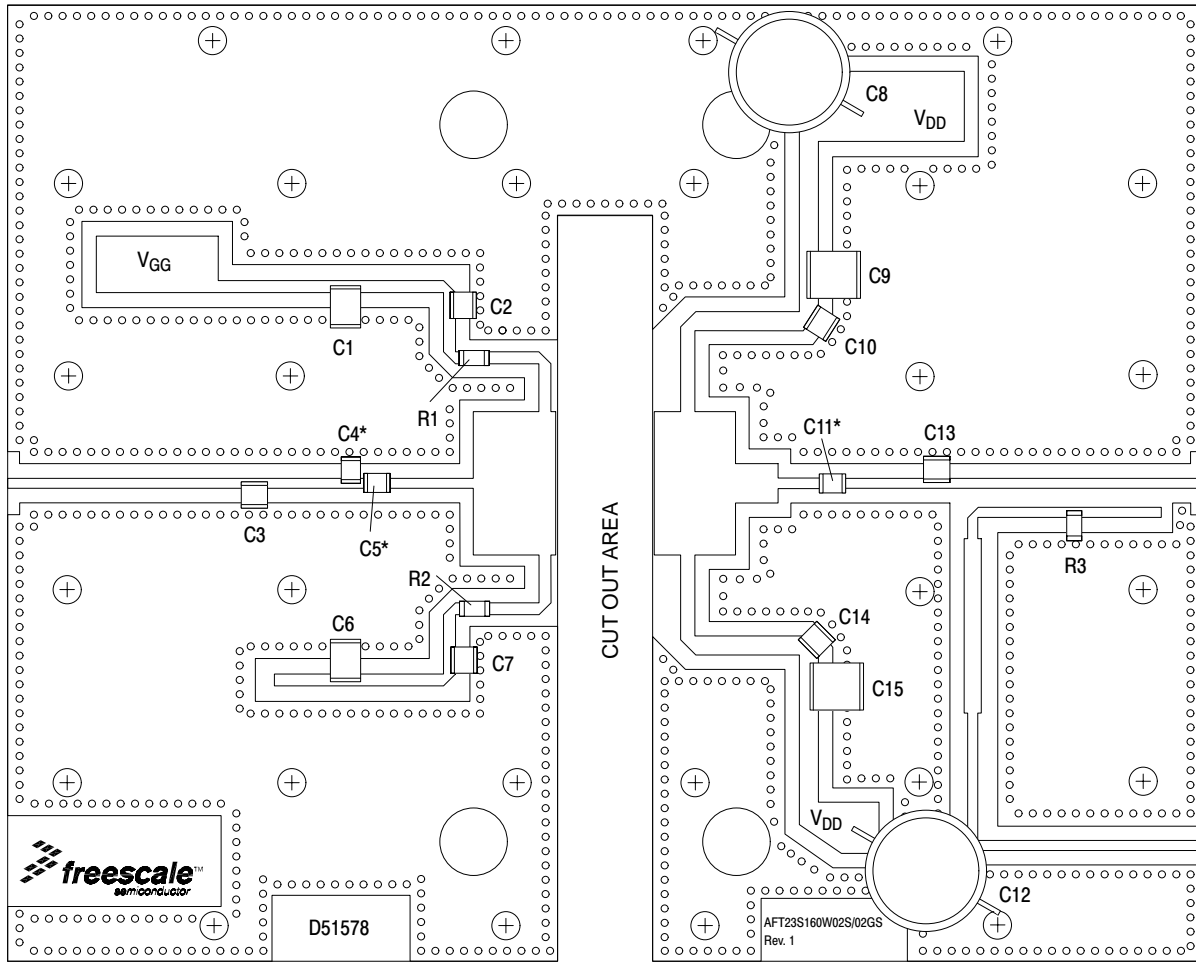
Power Gain	$G_{ps}$	17.0	17.9	19.0	dB
Drain Efficiency	$\eta_D$	28.0	30.3	—	%
Output Peak–to–Average Ratio @ 0.01% Probability on CCDF	PAR	6.1	6.6	—	dB
Adjacent Channel Power Ratio	ACPR	—	–33.9	–31.5	dBc
Input Return Loss	IRL	—	–14	–8	dB

1. Continuous use at maximum temperature will affect MTTF.
2. MTTF calculator available at <http://www.freescale.com/rf>. Select Software & Tools/Development Tools/Calculators to access MTTF calculators by product.
3. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.freescale.com/rf>. Select Documentation/Application Notes – AN1955.
4. Part internally matched both on input and output.
5. Measurements made with device in straight lead configuration before any lead forming operation is applied. Lead forming is used for gull wing (GS) parts.

(continued)

**Table 4. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Load Mismatch</b> (In Freescale Test Fixture, 50 ohm system) $I_{DQ} = 1100\text{ mA}$ , $f = 2350\text{ MHz}$					
VSWR 10:1 at 32 Vdc, 165 W CW Output Power (3 dB Input Overdrive from 210 W CW Rated Power)	No Device Degradation				
<b>Typical Performance</b> (In Freescale Test Fixture, 50 ohm system) $V_{DD} = 28\text{ Vdc}$ , $I_{DQ} = 1100\text{ mA}$ , 2300–2400 MHz Bandwidth					
$P_{out}$ @ 1 dB Compression Point, CW	P1dB	—	155	—	W
AM/PM (Maximum value measured at the P3dB compression point across the 2300–2400 MHz bandwidth)	$\Phi$	—	-15.5	—	°
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	VBW <sub>res</sub>	—	80	—	MHz
Gain Flatness in 100 MHz Bandwidth @ $P_{out} = 45\text{ W Avg.}$	$G_F$	—	0.14	—	dB
Gain Variation over Temperature (-30°C to +85°C)	$\Delta G$	—	0.018	—	dB/°C
Output Power Variation over Temperature (-30°C to +85°C)	$\Delta P1dB$	—	0.01	—	dB/°C



\*C4, C5 and C11 are mounted vertically.

**Figure 2. AFT23S160W02SR3 Test Circuit Component Layout**

**Table 5. AFT23S160W02SR3 Test Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C6	2.2 $\mu$ F Chip Capacitors	C3225X7R1H225M200AB	TDK
C2, C5, C7, C10, C11, C14	4.7 pF Chip Capacitors	ATC100B4R7BT500XT	ATC
C3	0.1 pF Chip Capacitor	ATC100B0R1BT500XT	ATC
C4, C13	0.3 pF Chip Capacitors	ATC100B0R3BT500XT	ATC
C8, C12	470 $\mu$ F, 63 V Electrolytic Capacitors	B41693A8477Q7	EPCOS
C9, C15	10 $\mu$ F Chip Capacitors	C5750X7S2A106M230KB	TDK
R1, R2	3.3 $\Omega$ , 1/4 W Chip Resistors	WCR1206-3R3FI	Welwyn
R3	0 $\Omega$ , 2 A Chip Jumper	WCR1206-R005JI	Welwyn
PCB	Rogers RO4350B, 0.020", $\epsilon_r = 3.5$	D51578	MTL

### TYPICAL CHARACTERISTICS

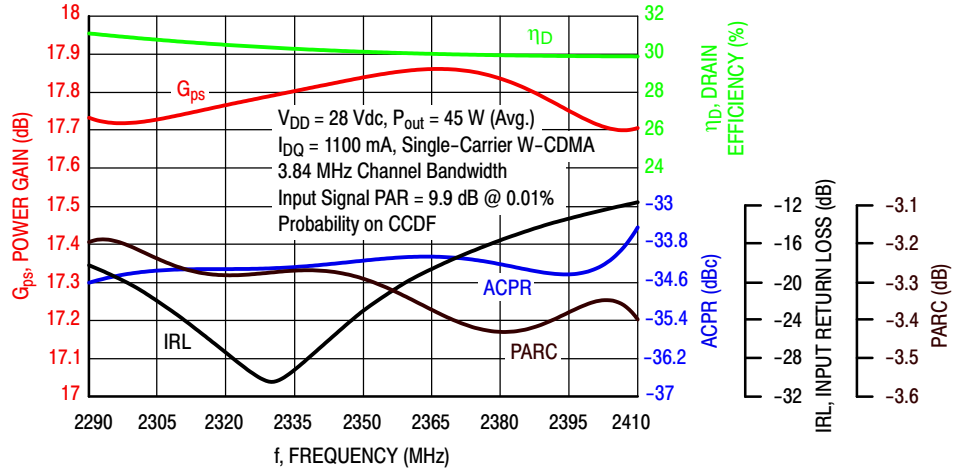


Figure 3. Single-Carrier Output Peak-to-Average Ratio Compression (PARC) Broadband Performance @  $P_{out} = 45 \text{ Watts Avg.}$

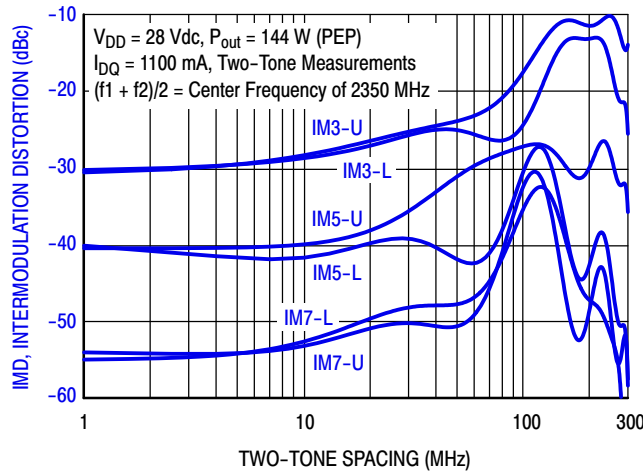


Figure 4. Intermodulation Distortion Products versus Two-Tone Spacing

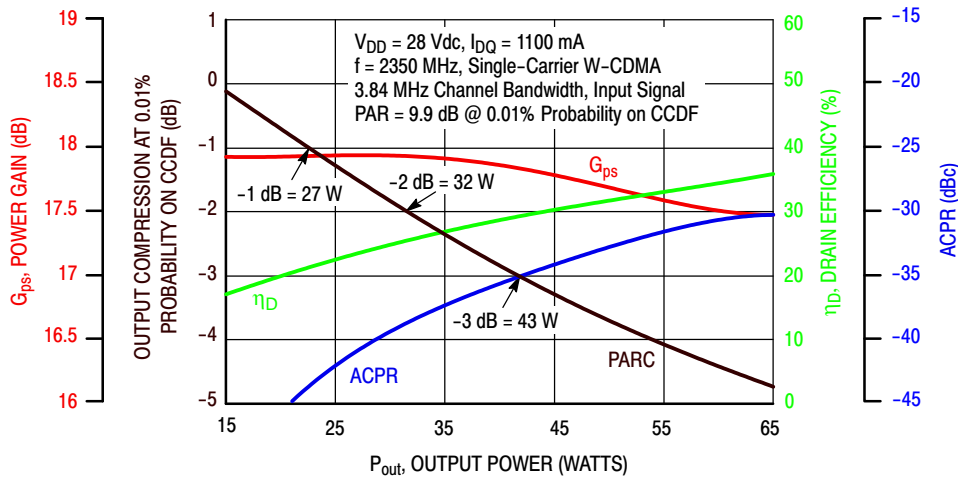
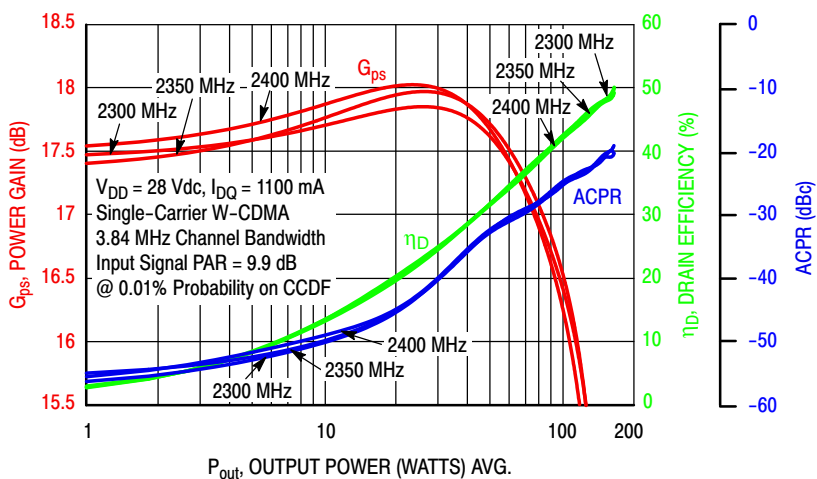
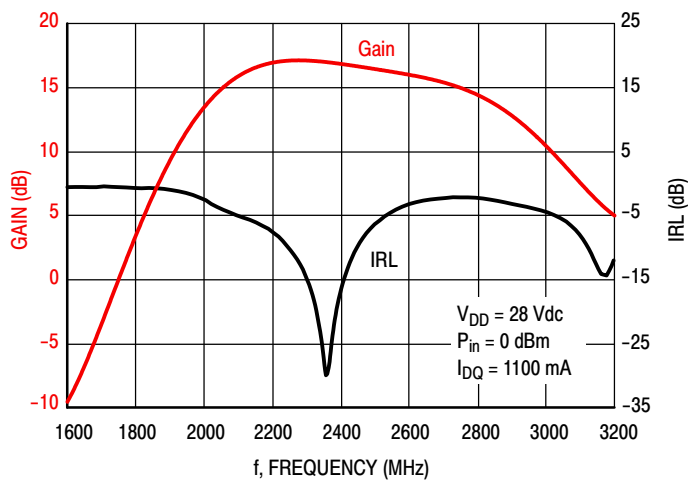


Figure 5. Output Peak-to-Average Ratio Compression (PARC) versus Output Power

### TYPICAL CHARACTERISTICS



**Figure 6. Single-Carrier W-CDMA Power Gain, Drain Efficiency and ACPR versus Output Power**



**Figure 7. Broadband Frequency Response**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1246 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2300	3.05 - j9.21	3.18 + j8.65	2.49 - j5.63	18.0	53.4	220	53.3	-11
2350	4.59 - j10.1	4.32 + j9.21	2.59 - j6.01	17.9	53.3	215	52.1	-11
2400	7.50 - j11.0	6.42 + j10.4	2.63 - j6.16	18.0	53.2	208	51.0	-12

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Output Power					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2300	3.05 - j9.21	3.21 + j9.07	2.46 - j5.99	15.7	54.2	264	53.7	-17
2350	4.59 - j10.1	4.52 + j9.79	2.64 - j6.20	15.8	54.1	257	53.2	-17
2400	7.50 - j11.0	6.97 + j11.1	2.79 - j6.34	16.0	54.0	252	52.8	-17

(1) Load impedance for optimum P1dB power.

(2) Load impedance for optimum P3dB power.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Figure 8. Load Pull Performance — Maximum Power Tuning**

$V_{DD} = 28 \text{ Vdc}$ ,  $I_{DQ} = 1246 \text{ mA}$ , Pulsed CW, 10  $\mu\text{sec}(\text{on})$ , 10% Duty Cycle

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P1dB					
			$Z_{\text{load}}^{(1)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2300	3.05 - j9.21	3.12 + j8.82	3.76 - j3.36	20.1	52.0	158	61.8	-17
2350	4.59 - j10.1	4.25 + j9.42	3.59 - j3.23	20.1	51.6	145	60.7	-18
2400	7.50 - j11.0	6.33 + j10.6	3.21 - j3.60	20.1	51.8	151	60.2	-17

f (MHz)	$Z_{\text{source}} (\Omega)$	$Z_{\text{in}} (\Omega)$	Max Drain Efficiency					
			P3dB					
			$Z_{\text{load}}^{(2)} (\Omega)$	Gain (dB)	(dBm)	(W)	$\eta_D$ (%)	AM/PM (°)
2300	3.05 - j9.21	3.12 + j9.19	3.83 - j3.50	18.0	52.8	189	63.5	-25
2350	4.59 - j10.1	4.42 + j9.93	3.59 - j3.43	18.1	52.5	180	62.5	-26
2400	7.50 - j11.0	6.85 + j11.3	3.33 - j3.72	18.0	52.7	186	62.1	-25

(1) Load impedance for optimum P1dB efficiency.

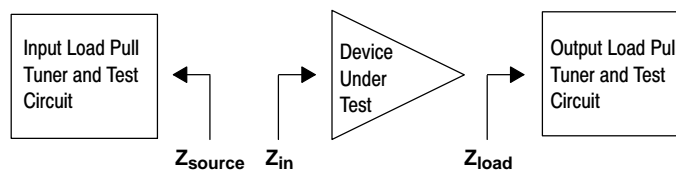
(2) Load impedance for optimum P3dB efficiency.

$Z_{\text{source}}$  = Measured impedance presented to the input of the device at the package reference plane.

$Z_{\text{in}}$  = Impedance as measured from gate contact to ground.

$Z_{\text{load}}$  = Measured impedance presented to the output of the device at the package reference plane.

**Figure 9. Load Pull Performance — Maximum Drain Efficiency Tuning**



### P1dB – TYPICAL SIDE LOAD PULL CONTOURS — 2350 MHz

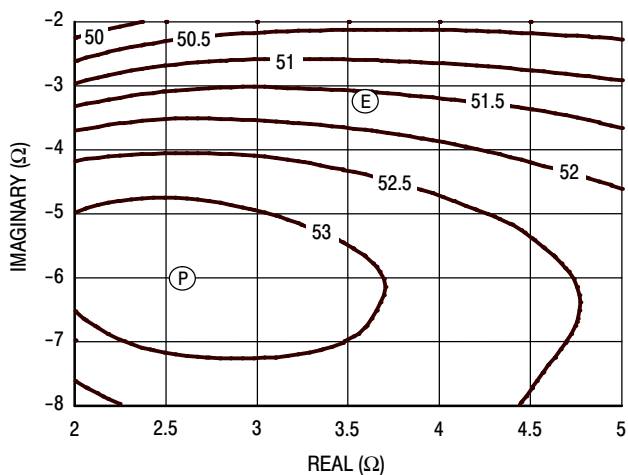


Figure 10. P1dB Load Pull Output Power Contours (dBm)

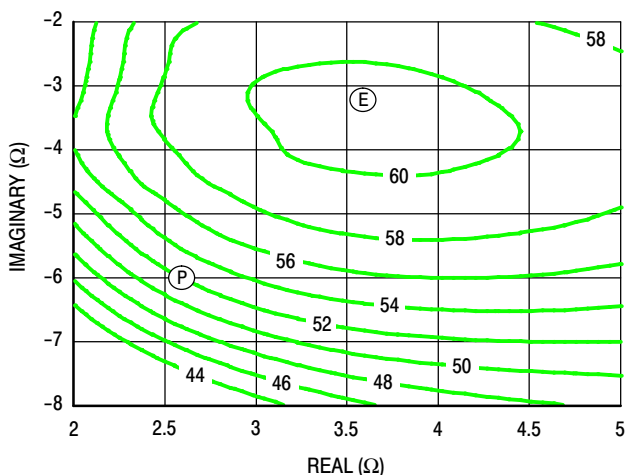


Figure 11. P1dB Load Pull Efficiency Contours (%)

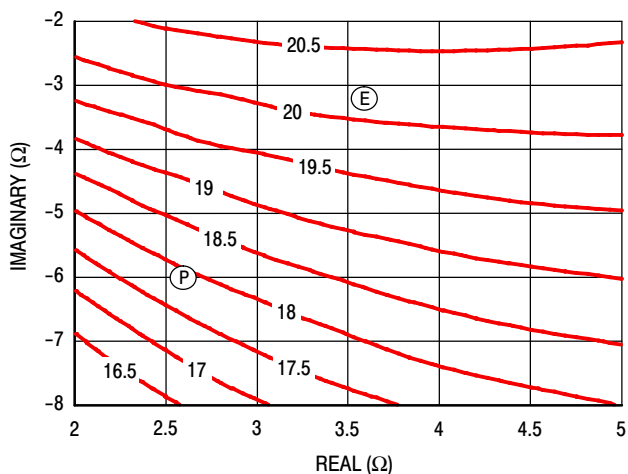


Figure 12. P1dB Load Pull Gain Contours (dB)

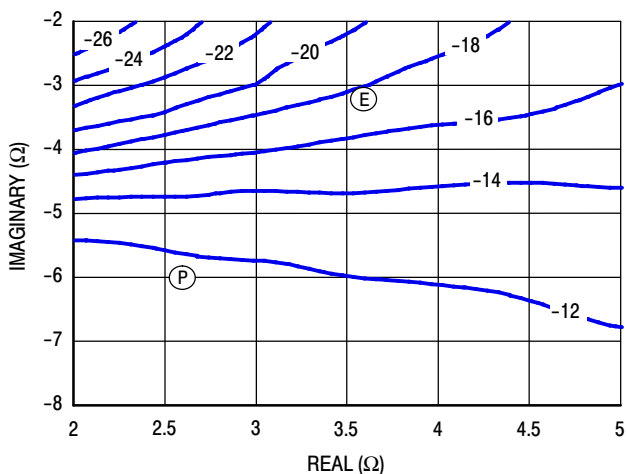


Figure 13. P1dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
 (E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### P3dB – TYPICAL SIDE LOAD PULL CONTOURS — 2350 MHz

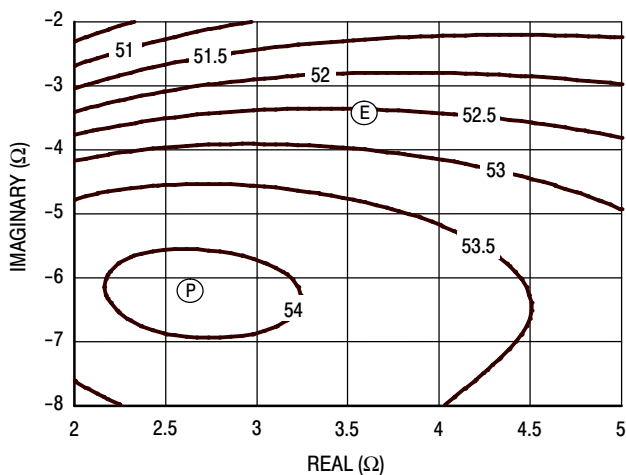


Figure 14. P3dB Load Pull Output Power Contours (dBm)

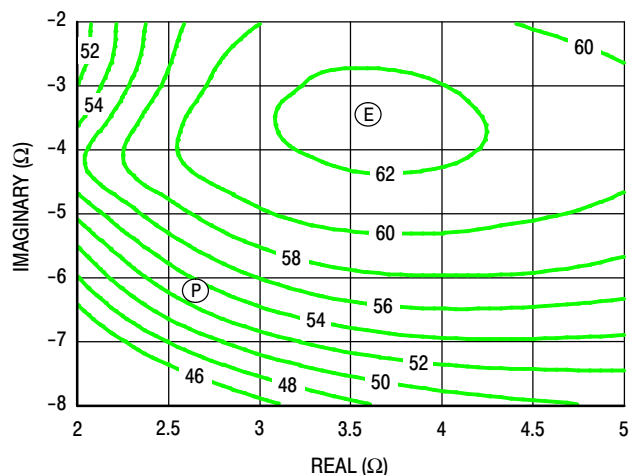


Figure 15. P3dB Load Pull Efficiency Contours (%)

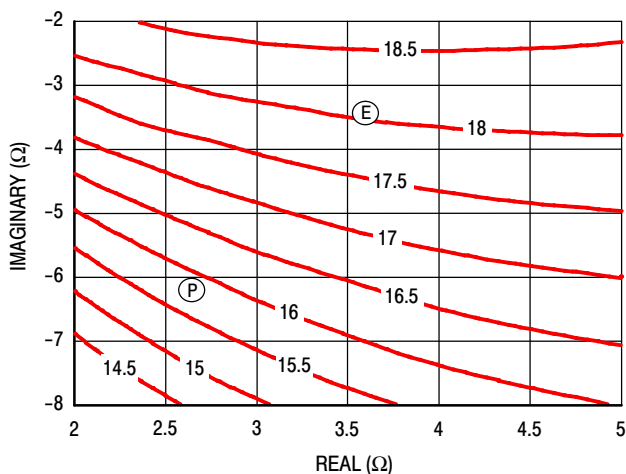


Figure 16. P3dB Load Pull Gain Contours (dB)

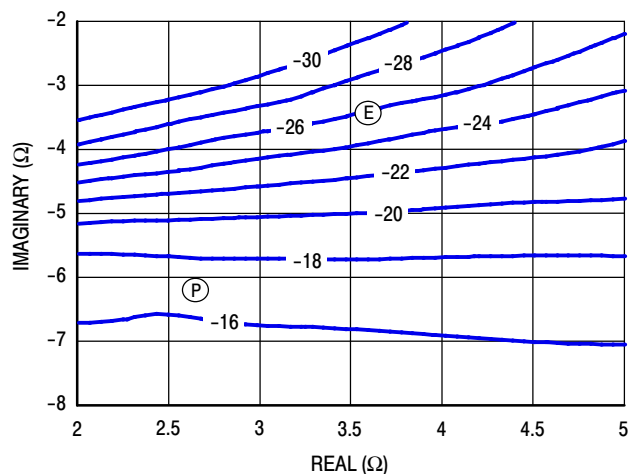
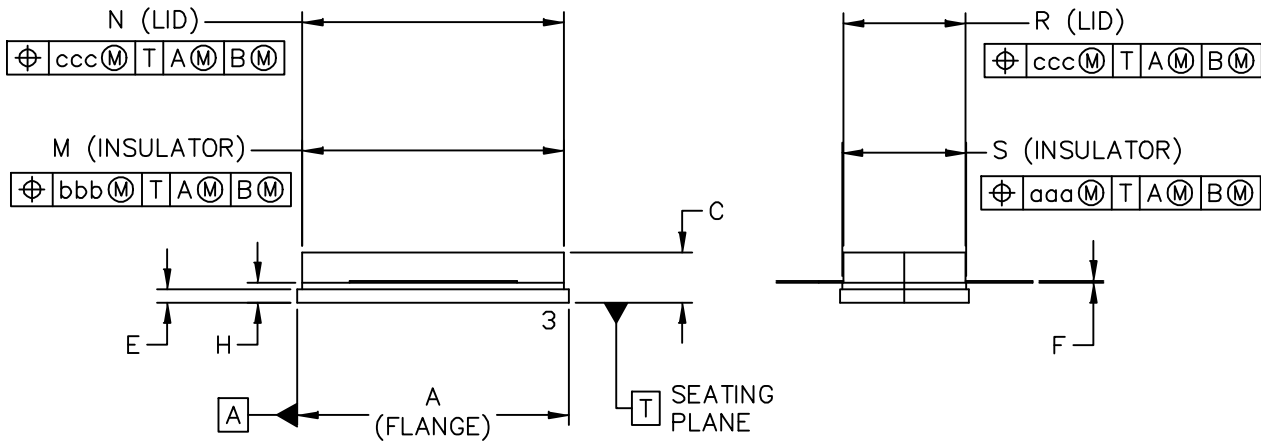
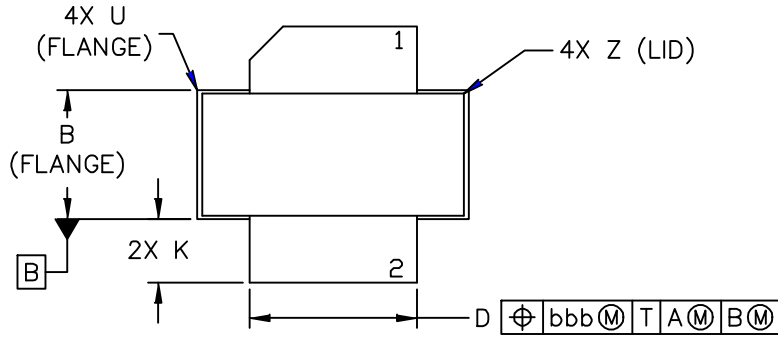


Figure 17. P3dB Load Pull AM/PM Contours (°)

**NOTE:** (P) = Maximum Output Power  
(E) = Maximum Drain Efficiency

- Gain
- Drain Efficiency
- Linearity
- Output Power

### PACKAGE DIMENSIONS



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	CASE NUMBER: 465A-06	31 MAR 2005
	STANDARD: NON-JEDEC	

NOTES:

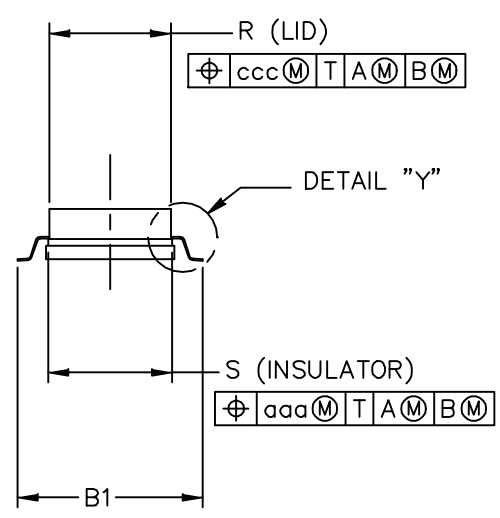
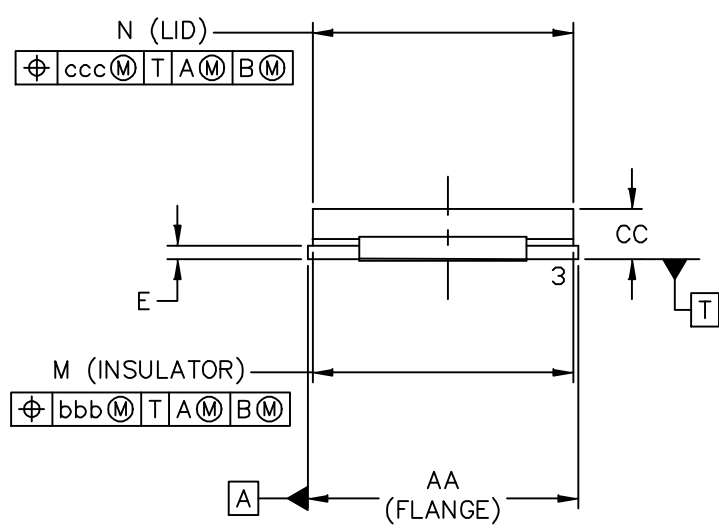
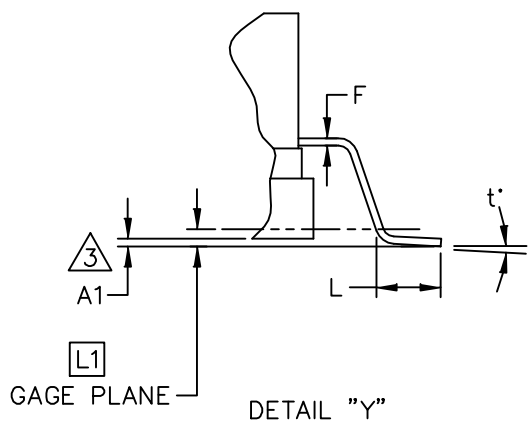
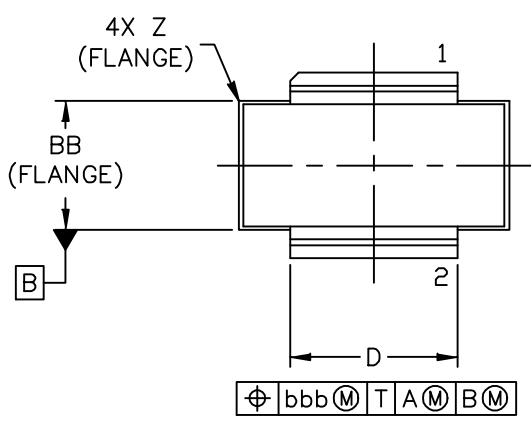
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.
3. DELETED
4. DIMENSION H IS MEASURED .030 (0.762) AWAY FROM PACKAGE BODY.

STYLE 1:

- PIN 1. DRAIN
2. GATE
3. SOURCE

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
A	.805	-.815	20.45	20.7	U	-.040	-	-	1.02
B	.380	-.390	9.65	9.91	Z	-.030	-	-	0.76
C	.125	-.170	3.18	4.32	aaa	-.005	-	-	0.127
D	.495	-.505	12.57	12.83	bbb	-.010	-	-	0.254
E	.035	-.045	0.89	1.14	ccc	-.015	-	-	0.381
F	.003	-.006	0.08	0.15	-	-	-	-	-
H	.057	-.067	1.45	1.7	-	-	-	-	-
K	.170	-.210	4.32	5.33	-	-	-	-	-
M	.774	-.786	19.61	20.02	-	-	-	-	-
N	.772	-.788	19.61	20.02	-	-	-	-	-
R	.365	-.375	9.27	9.53	-	-	-	-	-
S	.365	-.375	9.27	9.52	-	-	-	-	-

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	STANDARD: NON-JEDEC	



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TITLE:  NI-780GS-2L	DOCUMENT NO: 98ASA00193D	REV: B
	STANDARD: NON-JEDEC	
	05 SEP 2013	

NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M-1994.
2. CONTROLLING DIMENSION: INCH.

3. DIMENSION A1 IS MEASURED WITH REFERENCE TO DATUM T. THE POSITIVE VALUE IMPLIES THAT THE PACKAGE BOTTOM IS HIGHER THAN THE LEAD BOTTOM.

DIM	INCH		MILLIMETER		DIM	INCH		MILLIMETER	
	MIN	MAX	MIN	MAX		MIN	MAX	MIN	MAX
AA	.805	.815	20.45	20.70	Z	R.000	R.040	R0.00	R1.02
A1	.002	.008	0.05	0.20	t	0	8	0	8
BB	.380	.390	9.65	9.91					
B1	.546	.562	13.87	14.27					
CC	.125	.170	3.18	4.32	aaa	.005		0.13	
D	.495	.505	12.57	12.83	bbb	.010		0.25	
E	.035	.045	0.89	1.14	ccc	.015		0.38	
F	.003	.006	0.08	0.15					
L	.038	.046	0.97	1.17					
L1	.010 BSC		0.25 BSC						
M	.774	.786	19.66	19.96					
N	.772	.788	19.61	20.02					
R	.365	.375	9.27	9.53					
S	.365	.375	9.27	9.53					
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TITLE:					DOCUMENT NO: 98ASA00193D      REV: B				
NI-780GS-2L					STANDARD: NON-JEDEC				
					05 SEP 2013				

## PRODUCT DOCUMENTATION, SOFTWARE AND TOOLS

Refer to the following documents, software and tools to aid your design process.

### Application Notes

- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

### Software

- Electromigration MTTF Calculator
- RF High Power Model
- .s2p File

### Development Tools

- Printed Circuit Boards

For Software and Tools, do a Part Number search at <http://www.freescale.com>, and select the “Part Number” link. Go to the Software & Tools tab on the part’s Product Summary page to download the respective tool.

## REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
0	Nov. 2013	<ul style="list-style-type: none"> <li>• Initial Release of Data Sheet</li> </ul>

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## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management