THE DATASHEET OF

TLV320AIC3110EVM-U

TLV320AIC3110 Low-Power Audio Codec With Audio Processing and Stereo Class-D Speaker Amplifier

1 Device Overview

1.1 Features

- Stereo Audio DAC With 95-dB SNR
- Mono Audio ADC With 91-dB SNR
- Supports 8-kHz to 192-kHz Separate DAC and ADC Sample Rates
- Stereo 1.29-W Class-D BTL 8-Ω Speaker Driver With Direct Battery Connection
- One Differential and Three Single-Ended Inputs With Mixing and Level Controls
- Microphone With Bias, Preamp PGA, and AGC
- Built-in Digital Audio Processing Blocks (PRB) With User-Programmable Biquad, FIR Filters, and DRC
- Digital Mixing Capability
- Programmable Digital Audio Processor for Bass Boost/Treble/EQ With up to Five Biquads for Record and up to Six Biquads for Playback
- Pin Control or Register Control for Digital-Playback Volume-Control Settings
- Digital Sine-Wave Generator for Beeps and Key-Clicks
- Integrated PLL Used for Programmable Digital Audio Processor
- I^2S, Left-Justified, Right-Justified, DSP, and TDM Audio Interfaces
- I^2C Control With Register Auto-Increment
- Full Power-Down Control
- Power Supplies:
  - Analog: 2.7 V–3.6 V
  - Digital Core: 1.65 V–1.95 V
  - Digital I/O: 1.1 V–3.6 V
  - Class-D: 2.7 V–5.5 V (SPLVDD and SPRVDD ≥ AVDD)
- 5-mm × 5-mm 32-VQFN Package

1.2 Applications

- Portable Audio Devices
- Mobile Internet Devices
- e-Books

1.3 Description

The TLV320AIC3110 device is a low-power, highly integrated, high-performance codec that supports stereo audio DAC, and mono audio ADC.

The TLV320AIC3110 device features a high-performance audio codec with 24-bit stereo playback and monaural record functionality. The device integrates several analog features, such as a microphone interface, headphone drivers, and speaker drivers. The digital-audio data format is programmable to work with popular audio standard protocols (I^2S, left-justified and right-justified) in master, slave, DSP, and TDM modes. Bass boost, treble, or EQ is supported by the programmable digital-signal processing blocks (PRB). An on-chip PLL provides the high-speed clock required by the digital-signal processing block. The volume level is controlled either by pin control or by register control. The audio functions are controlled using the I^2C serial bus.

The TLV320AIC3110 device has a programmable digital sine-wave generator and is available in a 32-pin VQFN package.

Device Information[(1)]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TLV320AIC3110	VQFN (32)	5.00 mm × 5.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

1.4 Functional Block Diagram

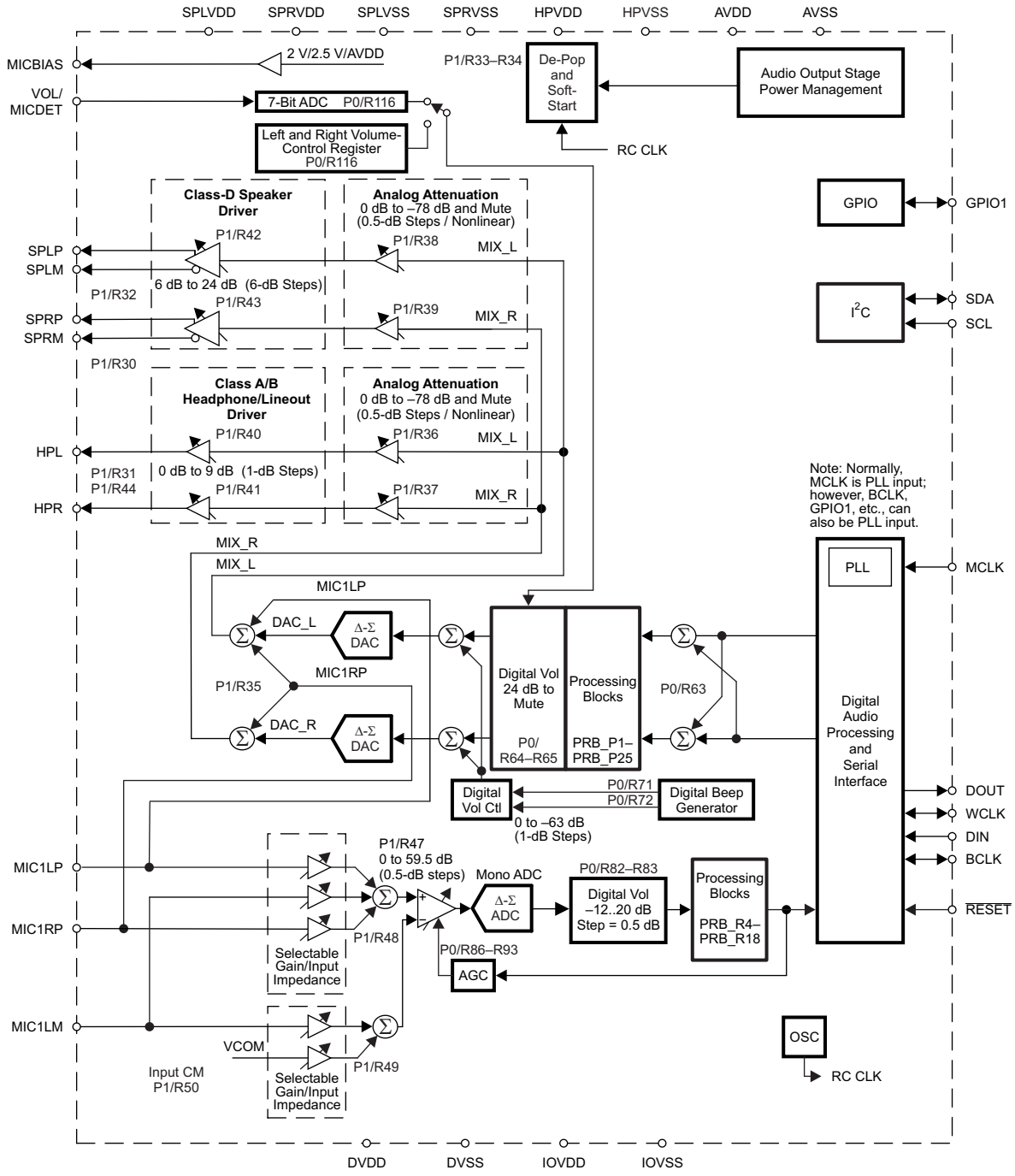


Table of Contents

2 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision B (May 2012) to Revision C **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Added *Power-Supply Sequence* section to the *Device Initialization* section 20
- Added the reference to the *PGA Gain Versus Input Impedance* table in the *MICBIAS and Microphone Preamplifier* section 27
- Changed units in Table 7-15 from k to kΩ 27
- Changed SDIN terminal to DIN in Figure 7-16 40
- Changed Section 7.3.10.1.2 diagrams for PRB_P2/5/8/10/13/15/18/21/24/25 to reflect that the DRC_HPF filter cannot be bypassed when the DRC is turned off 43
- Added sequence for inserting a beep in the middle of an already-playing signal and note text following script in the *Key-Click Functionality With Digital Sine-Wave Generator (PRB_P25)* section 59
- Added note to Register Map section 80
- Changed DOSR note in Page 0 / Register 14 by switching multiple value for Filter Type A and Filter Type C 83
- Added ADC OSR note to Page 0 / Register 20 84
- Changed values in *Page 0 / Register 69 (0x45): DRC Control 2* 95
- Changed Page 0, Register 70, bit D3-D0 decay rate value for 0000 from DR = $1.5625e^{-3}$ to DR = 0.015625 95
- Switched D1 and D0 descriptions so that D1 is for SP and D0 is for HP in Page 1 / Register 30 table 103
- Changed Page 1 / Register 40, D1 to reserved 106
- Changed Page 1 / Register 41, D1 to reserved 106

Changes from Revision A (April 2012) to Revision B **Page**

- Changed footnote in D7=1 table; added D6–D0 to the Register Value columns, and changed Analog Attenuation to Analog Gain. 62
- Updated AOSR values in *Clock Distribution Tree* image 66
- Deleted extra character from title of Page 0 / Register 75. 96
- Changed Description value in Page 0 / Register 83 for bits D6–D0. 97
- Removed extra cross-reference from Page 1 / Register 36–39. 105

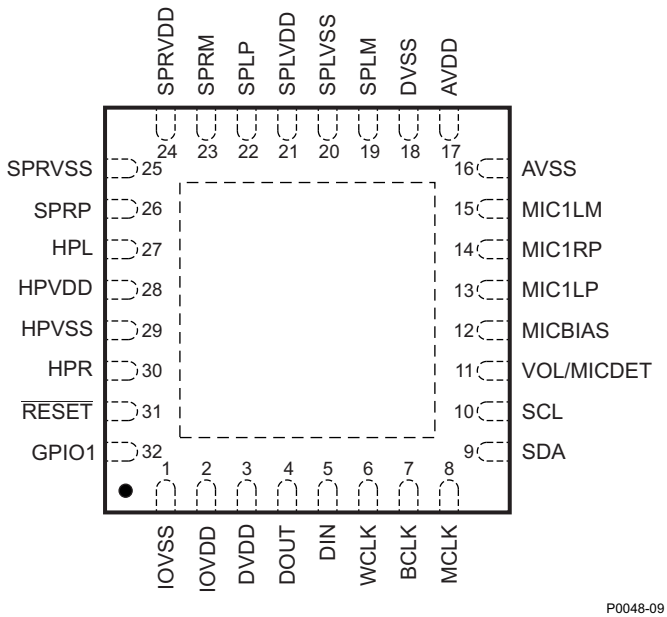
3 Device Comparison

Table 3-1. Device Features Comparison

FUNCTION	TLV320AIC3100	TLV320AIC3110	TLV320AIC3111	TLV320AIC3120
DACs	2	2	2	1
ADCs	1	1	1	1
Inputs / Outputs	3/3	3/4	3/4	3/2
Resolution (Bits)	16, 20, 24, 32	16, 20, 24, 32	16, 20, 24, 32	16, 20, 24, 32
Control Interface	I^2C	I^2C	I^2C	I^2C
Digital Audio Interface	LJ, RJ, I^2S, TDM, DSP	LJ, RJ, I^2S, TDM, DSP	LJ, RJ, I^2S, TDM, DSP	LJ, RJ, I^2S, TDM, DSP
Number of Digital Audio Interfaces	1	1	1	1
Speaker Amplifier Type	Mono Differential Class-D	Stereo Differential Class-D	Stereo Differential Class-D	Mono Differential Class-D
Configurable miniDSP	No	No	Yes	Yes
Headphone Driver	Yes	Yes	Yes	Yes

4 Pin Configuration and Functions

RHB Package
(Top View)



P0048-09

4.1 Pin Attributes

Table 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
AVDD	17	-	Analog power supply
AVSS	16	-	Analog ground
BCLK	7	I/O	Audio serial bit clock
DOUT	4	O	Audio serial data output
DVDD	3	-	Digital power – digital core
DVSS	18	-	Digital ground
GPIO1	32	I/O	General-purpose input/output pin and multifunction pin
HPL	27	O	Left-channel headphone and line driver output
HPR	30	O	Right-channel headphone and line driver output
HPVDD	28	-	Headphone and line driver and PLL power
HPVSS	29	-	Headphone and line driver and PLL ground
IOVDD	2	-	Interface power
IOVSS	1	-	Interface ground
MCLK	8	I	External master clock
MICBIAS	12	O	Microphone bias voltage
MIC1LM	15	I	Microphone and line input routed to M or P input mixer
MIC1LP	13	I	Microphone and line input routed to P input mixer and left output mixer
MIC1RP	14	I	Microphone and line input routed to P input mixer and left and right output mixer
$\overline{\text{RESET}}$	31	I	Device reset
SCL	10	I/O	I^2C control bus clock input
SDA	9	I/O	I^2C control-bus data input
SPLM	19	O	Left-channel class-D speaker driver inverting output

Table 4-1. Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
SPLP	22	O	Left-channel class-D speaker driver noninverting output
SPLVDD	21	-	Left-channel class-D speaker driver power supply
SPLVSS	20	-	Left-channel class-D speaker-amplifier power-supply ground
SPRM	23	O	Right-channel class-D speaker driver inverting output
SPRP	26	O	Right-channel class-D speaker driver noninverting output
SPRVDD	24	-	Right-channel class-D speaker driver power supply
SPRVSS	25	-	Right-channel class-D speaker driver power supply ground
VOL/MICDET	11	I	Volume control or microphone detection
WCLK	6	I/O	Audio serial word clock

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
AVDD to AVSS	–0.3	3.9	V
DVDD to DVSS	–0.3	2.5	V
HPVDD to HPVSS	–0.3	3.9	V
SPLVDD to SPLVSS	–0.3	6	V
SPRVDD to SPRVSS	–0.3	6	V
IOVDD to IOVSS	–0.3	3.9	V
Digital input voltage	IOVSS – 0.3	IOVDD + 0.3	V
Analog input voltage	AVSS – 0.3	AVDD + 0.3	V
Operating temperature	–40	85	°C
Junction temperature (T_J Max)		105	°C
Storage temperature, T_{stg}	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
AVDD (1)	Power-supply voltage range	Referenced to AVSS (2)	2.7	3.3	3.6	V
DVDD		Referenced to DVSS (2)	1.65	1.8	1.95	
HPVDD		Referenced to HPVSS (2)	2.7	3.3	3.6	
SPLVDD (1)		Referenced to SPLVSS (2)	2.7		5.5	
SPRVDD (1)		Referenced to SPRVSS (2)	2.7		5.5	
IOVDD		Referenced to IOVSS (2)	1.1	3.3	3.6	
	Speaker impedance	Resistance applied across class-D ouput pins (BTL)	8			Ω
	Headphone impedance	AC coupled to R_L	16			Ω
V_I	Analog audio full-scale input voltage	AVDD = 3.3 V, single-ended		0.707		V_{RMS}
	Stereo-line output load impedance	AC coupled to R_L		10		kΩ
MCLK (3)	Master clock frequency	IOVDD = 3.3 V			50	MHz
SCL	SCL clock frequency				400	kHz
T_A	Operating free-air temperature		–40		85	°C

(1) To minimize battery-current leakage, the SPLVDD and SPRVDD voltage levels must not be below the AVDD voltage level.
(2) All grounds on board are tied together, so they must not differ in voltage by more than 0.2-V maximum for any combination of ground signals. Ensure a low-impedance connection between HPVSS and DVSS through the use of a wide trace or ground plane,.
(3) The maximum input frequency must be 50 MHz for any digital pin used as a general-purpose clock.

5.4 Thermal Information

THERMAL METRIC[1]		TLV320AIC3110 RHB (VQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	32.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	6.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	6.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.0	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.5 Electrical Characteristics

At 25°C, AVDD = HPVDD = IOVDD = 3.3 V, SPLVDD = SPRVDD = 3.6 V; DVDD = 1.8 V; f_S (audio) = 48 kHz; CODEC_CLKIN = 256 × f_S; PLL = Off; VOL/MICDET pin disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INTERNAL OSCILLATOR-RC_CLK						
	Oscillator frequency for SAR			8.2		MHz
VOLUME CONTROL PIN (ADC); VOL/MICDET pin enabled						
	Input voltage range	VOL/MICDET pin configured as volume control (page 0 / register 116, bit D7 = 1 and page 0 / register 67, bit D7 = 0)	0		0.5 × AVDD	V
	Input capacitance			2		pF
	Volume control steps			128		Steps
AUDIO ADC						
Microphone Input to ADC, 984-Hz Sine-Wave Input, f_S = 48 kHz, AGC = OFF						
	Input signal level (0-dB)	MIC with R1 = 20 kΩ (page 1 / register 48 and register 49, bits D7-D6)		0.707		V_{RMS}
SNR	Signal-to-noise ratio	f_S = 48 kHz, 0-dB PGA gain, MIC input AC-shorted to ground; measured as idle-channel noise, A-weighted[1] [2]	80	91		dB
	Dynamic range	f_S = 48 kHz, 0-dB PGA gain, MIC input 1 kHz at –60-dBFS input applied, referenced to 0.707-V_{RMS} input, A-weighted[1] [2]		91		dB
THD+N	Total harmonic distortion + noise	f_S = 48 kHz, 0-dB PGA gain, MIC input 1 kHz at –2 dBFS input applied, referenced to 0.707-V_{RMS} input		–85	–70	dB
THD	Total harmonic distortion	f_S = 48 kHz, 0-dB PGA gain, MIC input 1 kHz at –2 dBFS input applied, referenced to 0.707-V_{RMS} input		–91		dB
	Input capacitance	MIC input		2		pF
Microphone Bias						
	Voltage output	Page 1 / register 46, bits D1–D0 = 10	2.25	2.5	2.75	V
		Page 1 / register 46, bits D1–D0 = 01		2		
	Voltage regulation	At 4-mA load current, page 1 / register 46, bits D1–D0 = 10 (MICBIAS = 2.5 V)		5		mV
		At 4-mA load current, page 1 / register 46, bits D1–D0 = 01 (MICBIAS = 2 V)		7		
Audio ADC Digital Decimation Filter Characteristics						
See Section 7.3.9.4.4 for audio ADC decimation filter characteristics.						
AUDIO DAC						
DAC HEADPHONE OUTPUT, AC-coupled load = 16 Ω (single-ended), driver gain = 0 dB, parasitic capacitance = 30 pF						
	Full-scale output voltage (0 dB)	Output common-mode setting = 1.65 V		0.707		V_{RMS}
SNR	Signal-to-noise ratio	Measured as idle-channel noise, A-weighted[1] [2]	80	95		dB
THD	Total harmonic distortion	0-dBFS input		–85	–65	dB
THD+N	Total harmonic distortion + noise	0-dBFS input		–82	–60	dB
	Mute attenuation			87		dB
PSRR	Power-supply rejection ratio[3]	Ripple on HPVDD (3.3 V) = 200 mVp-p at 1 kHz		–62		dB
P_O	Maximum output power	R_L = 32 Ω, THD+N = –60 dB		20		mW
		R_L = 16 Ω, THD+N = –60 dB		60		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the inputs short-circuited, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter may result in higher THD+N and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, may affect dynamic specification values.
(3) DAC to headphone-out PSRR measurement is calculated as PSRR = 20 × log(ΔV_{HPL} / ΔV_{HPVDD}).

Electrical Characteristics *(continued)*

At 25°C, AVDD = HPVDD = IOVDD = 3.3 V, SPLVDD = SPRVDD = 3.6 V; DVDD = 1.8 V; f_S (audio) = 48 kHz; CODEC_CLKIN = 256 × f_S; PLL = Off; VOL/MICDET pin disabled (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DAC LINEOUT (HP Driver in Lineout Mode)						
SNR	Signal-to-noise ratio	Measured as idle-channel noise, A-weighted		95		dB
THD	Total harmonic distortion	0-dBFS input, 0-dB gain		–86		dB
THD+N	Total harmonic distortion + noise	0-dBFS input, 0-dB gain		–83		dB
DAC Digital Interpolation Filter Characteristics						
See Section 7.3.10.1.4 for DAC interpolation filter characteristics.						
DAC OUTPUT to CLASS-D SPEAKER OUTPUT; Load = 8 Ω (differential), 50 pF						
	Output voltage	SPLVDD = SPRVDD = 3.6 V, BTL measurement, DAC input = 0 dBFS, DAC CM (page 1 / register 31, bits D4–D3) = 1.65 V, class-D gain = 6 dB, THD = –16.5 dB		2.2		V_{RMS}
		SPLVDD = SPRVDD = 3.6 V, BTL measurement, DAC input = –2 dBFS, DAC CM (page 1 / register 31, bits D4–D3) = 1.65 V, class-D gain = 6 dB, THD = –20 dB		2.1		
	Output, common-mode	SPLVDD = SPRVDD = 3.6 V, BTL measurement, DAC input = mute, class-D gain = 6 dB		1.8		V
SNR	Signal-to-noise ratio	SPLVDD = SPRVDD = 3.6 V, BTL measurement, class-D gain = 6 dB, measured as idle-channel noise, A-weighted (with respect to full-scale output value of 2.2 V_{RMS})(1)(2)		87		dB
THD	Total harmonic distortion	SPLVDD = SPRVDD = 3.6 V, BTL measurement, CM = 1.8 V, DAC input = –6 dBFS, class-D gain = 6 dB		–67		dB
THD+N	Total harmonic distortion + noise	SPLVDD = SPRVDD = 3.6 V, BTL measurement, CM = 1.8 V, DAC input = –6 dBFS, class-D gain = 6 dB		–66		dB
PSRR	Power-supply rejection ratio(4)	SPLVDD = SPRVDD = 3.6 V, BTL measurement, ripple on SPLVDD/SPRVDD = 200 mVp-p at 1 kHz		–44		dB
	Mute attenuation			110		dB
P_O	Maximum output power	SPLVDD = SPRVDD = 3.6 V, BTL measurement, CM = 1.8 V, class-D gain = 18 dB, THD = 10%		540		mW
		SPLVDD = SPRVDD = 4.3 V, BTL measurement, CM = 1.8 V, class-D gain = 18 dB, THD = 10%		790		mW
		SPLVDD = SPRVDD = 5.5 V, BTL measurement, CM = 1.8 V, class-D gain = 18 dB, THD = 10%		1.29		W
	Output-stage leakage current for direct battery connection	SPLVDD = SPRVDD = 4.3 V, device is powered down (power-up-reset condition)		80		nA
ADC and DAC POWER CONSUMPTION						
For ADC and DAC power consumption based per selected processing block, see Section 7.3.8.						
DIGITAL INPUT/OUTPUT						
	Logic family			CMOS		
V_{IH}	Logic Level	I_{IH} = 5 µA, IOVDD = 1.6 V	0.7 × IOVDD			V
		I_{IH} = 5 µA, IOVDD = 1.6 V	IOVDD			
V_{IL}		I_{IL} = 5 µA, IOVDD = 1.6 V	–0.3		0.3 × IOVDD	
		I_{IL} = 5 µA, IOVDD = 1.6 V			0	
V_{OH}		I_{OH} = 2 TTL loads	0.8 × IOVDD			
V_{OL}		I_{OL} = 2 TTL loads			0.1 × IOVDD	
	Capacitive load			10		pF

(4) DAC to speaker-out PSRR is a differential measurement calculated as PSRR = 20 × log($\Delta V_{SPL(P + M)}$ / ΔV_{SPLVDD}).

5.6 Power Dissipation Ratings

This data was taken using 2-oz. (0,071-mm thick) trace and copper pad that is soldered to a JEDEC high-K, standard 4-layer 3-inch × 3-inch (7,62-cm × 7,62-cm) PCB.

Power Rating at 25°C	Derating Factor	Power Rating at 70°C	Power Rating at 85°C
2.3 W	28.57 mW/°C	1 W	0.6 W

5.7 I²S, LJF, and RJF Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization but not tested at final test. See Figure 5-1.

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		45		20	ns
t_d(DO-WS)	WCLK to DOUT delay (for LJF mode only)		45		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay		45		20	ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		25		10	ns
t_f	Fall time		25		10	ns

5.8 I²S, LJF, and RJF Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization but not tested at final test. See Figure 5-2.

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		6		ns
t_h(WS)	WCLK hold	8		6		ns
t_d(DO-WS)	WCLK to DOUT delay (for LJF mode only)		45		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay		45		20	ns
t_s(DI)	DIN setup	8		6		ns
t_h(DI)	DIN hold	8		6		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

5.9 DSP Timing in Master Mode

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization but not tested at final test. See Figure 5-3.

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(WS)	WCLK delay		45		20	ns
t_d(DO-BCLK)	BCLK to DOUT delay		45		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		25		10	ns
t_f	Fall time		25		10	ns

5.10 DSP Timing in Slave Mode

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization but not tested at final test. See Figure 5-4.

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_H(BCLK)	BCLK high period	35		35		ns
t_L(BCLK)	BCLK low period	35		35		ns
t_s(WS)	WCLK setup	8		8		ns
t_h(WS)	WCLK hold	8		8		ns

DSP Timing in Slave Mode *(continued)*

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization but not tested at final test. See Figure 5-4.

PARAMETER		IOVDD = 1.1 V		IOVDD = 3.3 V		UNIT
		MIN	MAX	MIN	MAX	
t_d(DO-BCLK)	BCLK to DOUT delay		45		20	ns
t_s(DI)	DIN setup	8		8		ns
t_h(DI)	DIN hold	8		8		ns
t_r	Rise time		4		4	ns
t_f	Fall time		4		4	ns

5.11 I²C Interface Timing

All specifications at 25°C, DVDD = 1.8 V. **Note:** All timing specifications are measured at characterization.See Figure 5-5.

PARAMETER		Standard Mode			Fast Mode			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
f_{SCL}	SCL clock frequency	0		100	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			0.8			µs
t_{LOW}	LOW period of the SCL clock	4.7			1.3			µs
t_{HIGH}	HIGH period of the SCL clock	4			0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			0.8			µs
$t_{HD;DAT}$	Data hold time: for I²C bus devices	0		3.45	0		0.9	µs
$t_{SU;DAT}$	Data set-up time	250			100			ns
t_r	SDA and SCL rise time			1000	20 + 0.1C_b		300	ns
t_f	SDA and SCL fall time			300	20 + 0.1C_b		300	ns
$t_{SU;STO}$	Set-up time for STOP condition	4			0.8			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			1.3			µs
C_b	Capacitive load for each bus line			400			400	pF

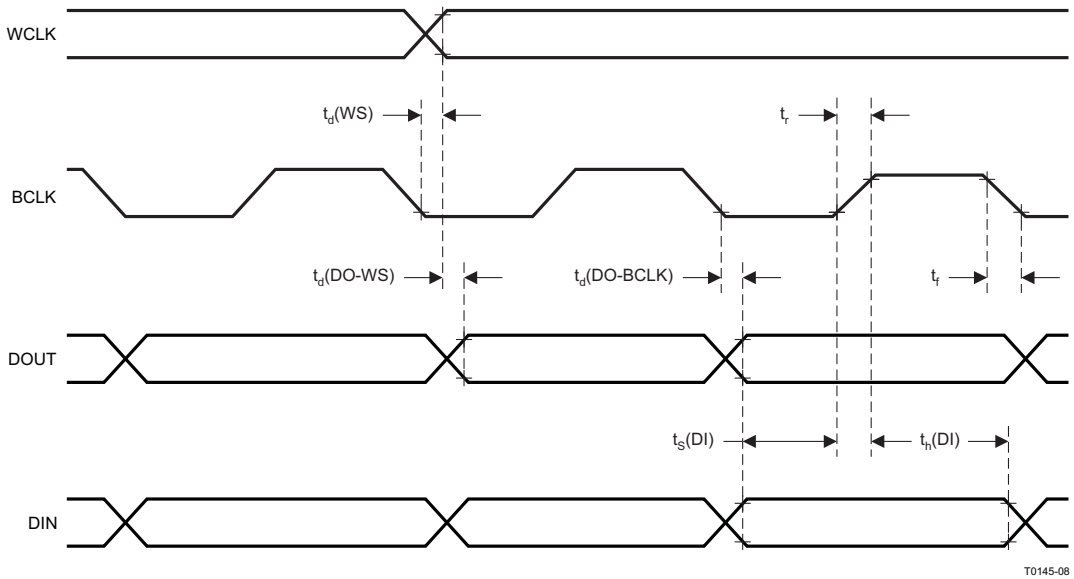


Figure 5-1. I²S/LJF/RJF Timing in Master Mode

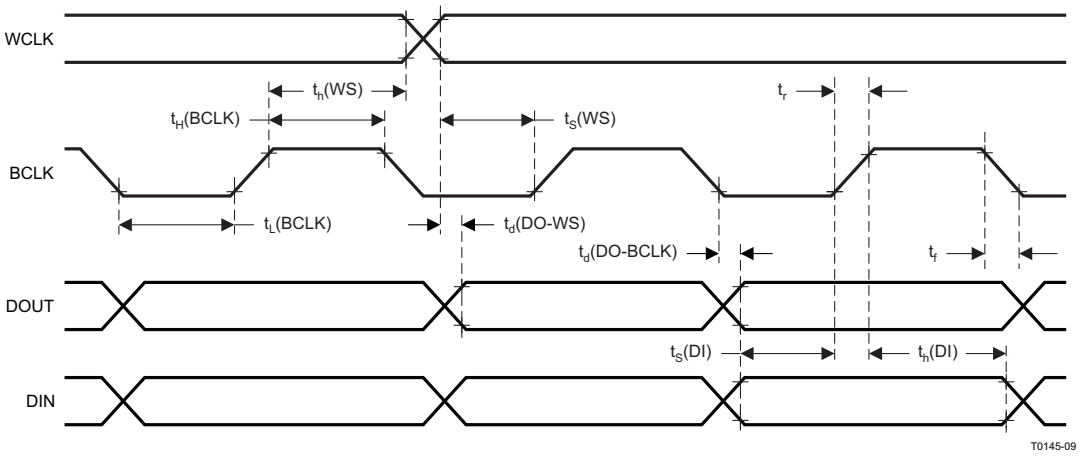


Figure 5-2. I²S/LJF/RJF Timing in Slave Mode

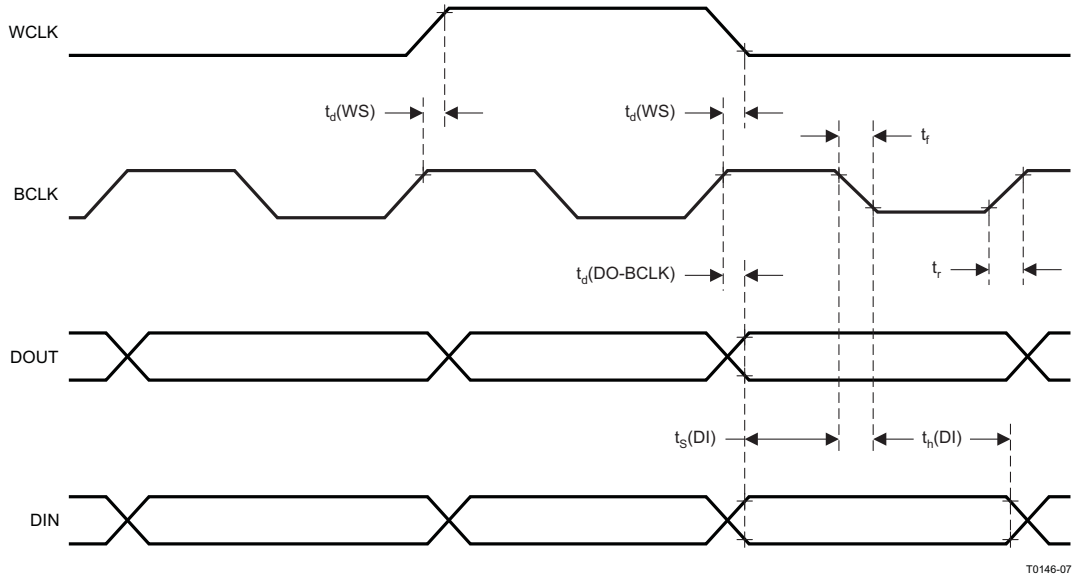


Figure 5-3. DSP Timing in Master Mode

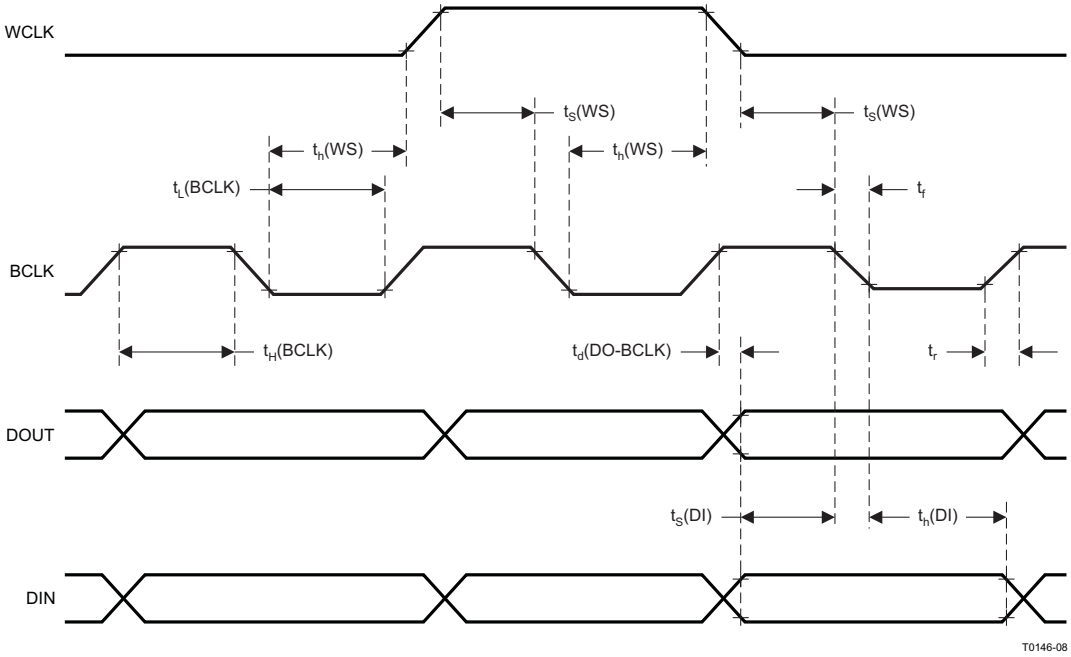


Figure 5-4. DSP Timing in Slave Mode

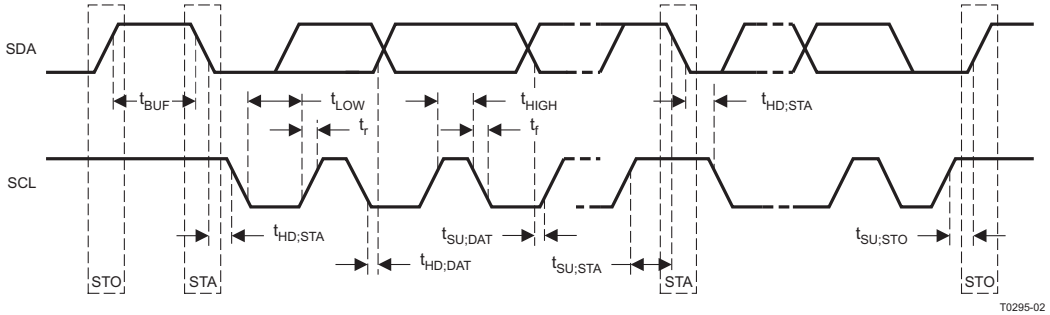


Figure 5-5. I^2C Interface Timing Diagram

5.12 Typical Characteristics

5.12.1 Audio ADC Performance

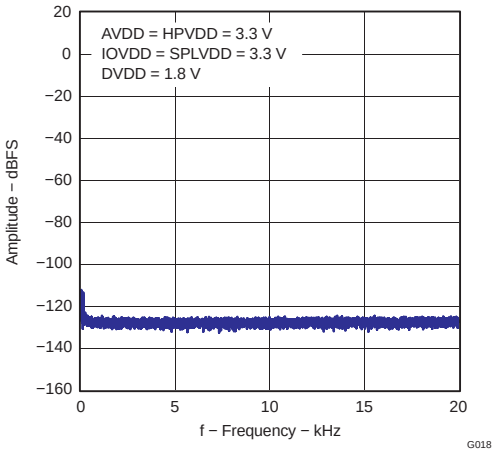


Figure 5-6. FFT – ADC Idle Channel Differential

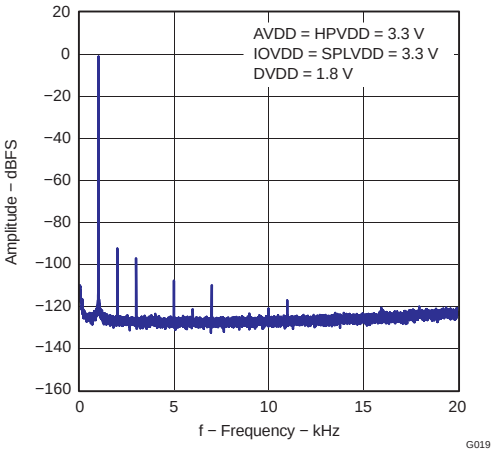


Figure 5-7. FFT – ADC Single-Ended Input

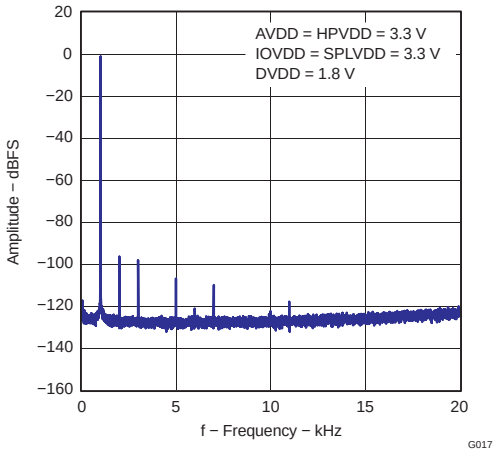


Figure 5-8. FFT – ADC Differential Input

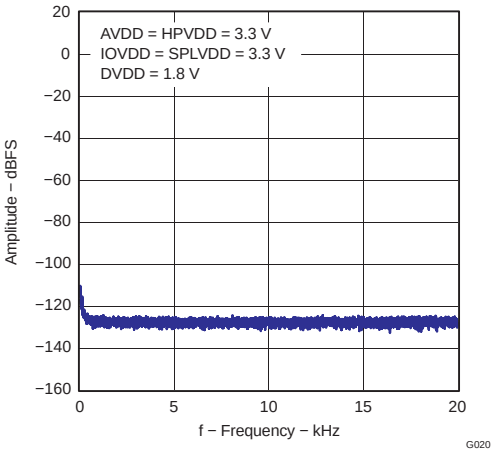


Figure 5-9. FFT – ADC Idle Channel, Single-Ended

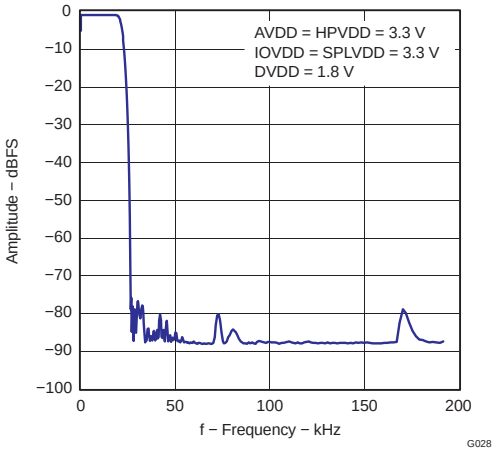


Figure 5-10. Frequency Response, Audio ADC Channel

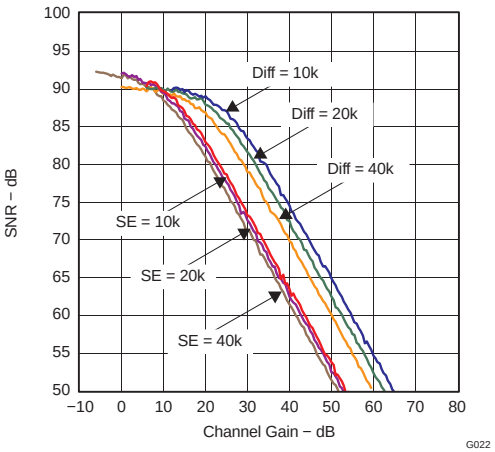


Figure 5-11. Audio ADC Channel

5.12.2 DAC Performance

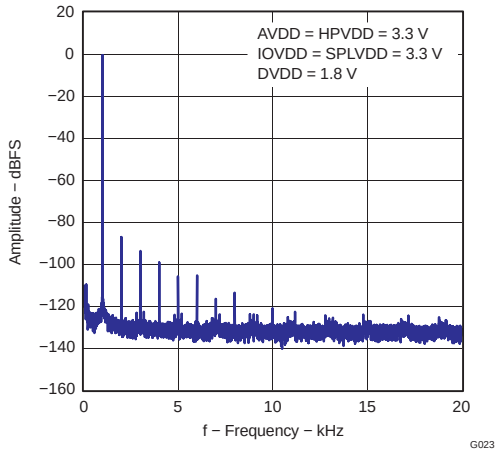


Figure 5-12. Amplitude vs Frequency FFT – DAC to Line Output

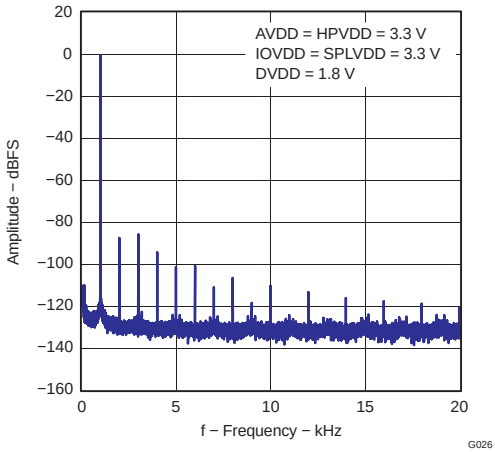


Figure 5-13. Amplitude vs Frequency FFT – DAC to Headphone Output

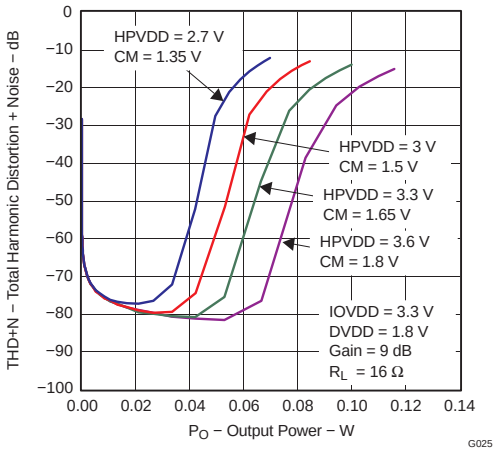


Figure 5-14. Total Harmonic Distortion + Noise vs Output Power Headphone Output Power

5.12.3 Class-D Speaker Driver Performance

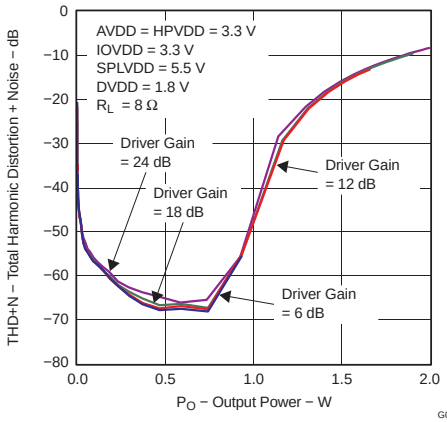


Figure 5-15. Total Harmonic Distortion + Noise vs Output Power Max Class-D Speaker-Driver Output Power

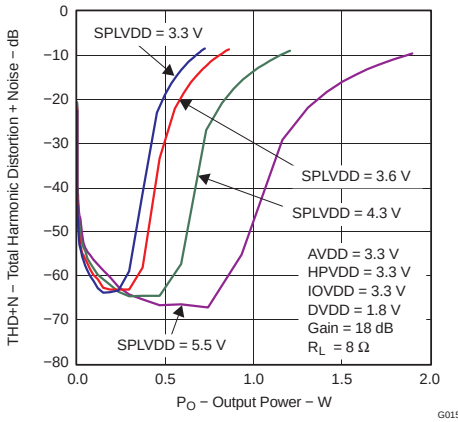


Figure 5-16. Total Harmonic Distortion + Noise vs Output Power Class-D Speaker-Driver Output Power

5.12.4 Analog Bypass Performance

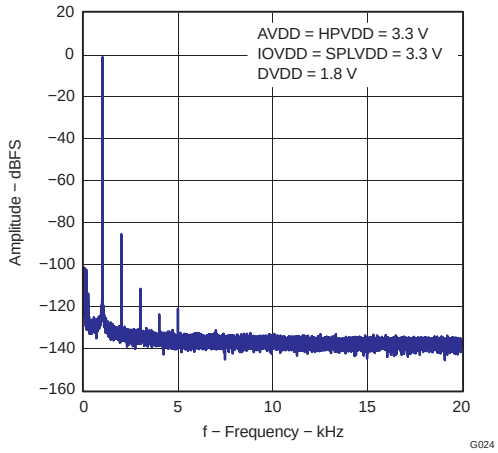


Figure 5-17. Amplitude vs Frequency FFT – Line-In Bypass to Line Output

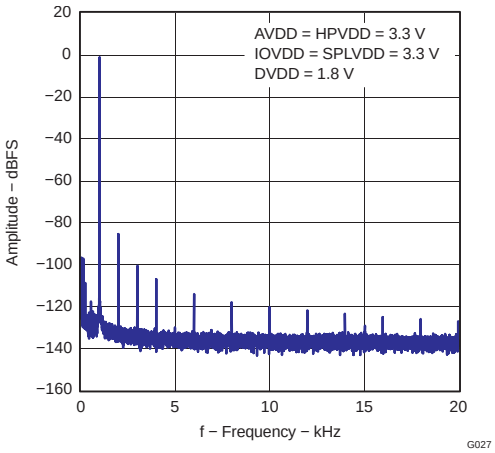


Figure 5-18. Amplitude vs Frequency FFT – Line-In Bypass to Headphone Output

5.12.5 MICBIAS Performance

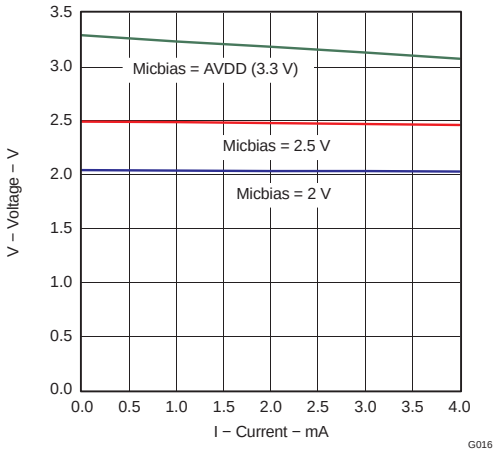


Figure 5-19. Voltage vs Current MICBIAS

6 Parameter Measurement Information

All parameters are measured according to the conditions described in *Section 5*.

7 Detailed Description

7.1 Overview

The TLV320AIC3110 device is a highly integrated stereo-audio DAC and monaural ADC for portable computing, communication, and entertainment applications. A register-based architecture eases integration with microprocessor-based systems through standard serial-interface buses. This device supports the two-wire I^2C bus interface which provides full register access. All peripheral functions are controlled through these registers and the onboard state machines.

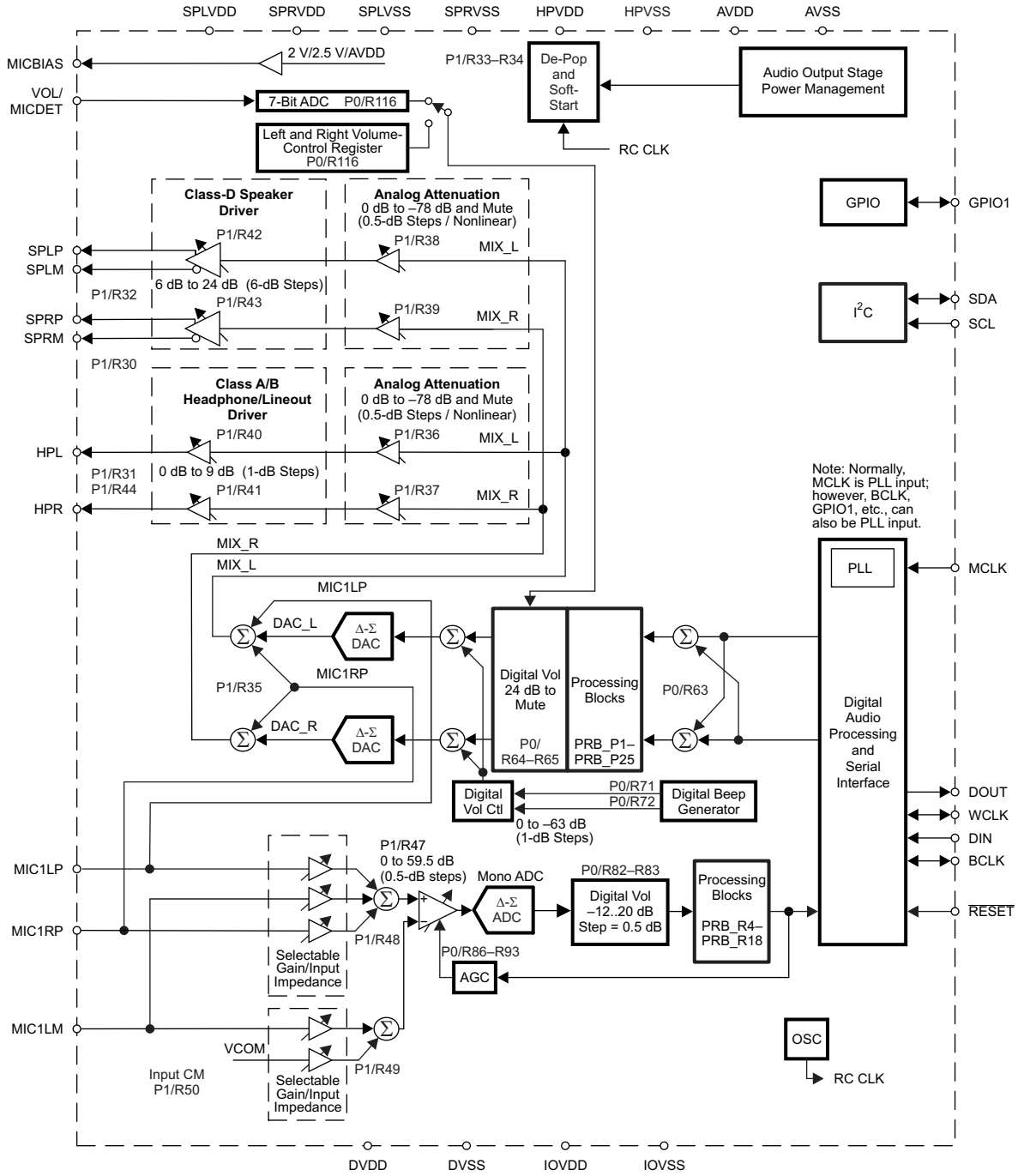
The TLV320AIC3110 device consists of the following blocks:

- Microphone interfaces (analog and digital)
- Audio codec (mono ADC and stereo DAC)
- AGC and DRC
- Digital audio processing blocks (PRB) for play and record paths
- Digital sine-wave generator for beeps
- Stereo headphone and lineout amplifier
- Class-D stereo amplifier for 8-Ω speakers
- Pin-controlled or register-controlled volume level
- Power-down de-pop and power-up soft start
- Analog inputs
- I^2C control interface
- Power-down control block

Following a toggle of the $\overline{\text{RESET}}$ pin or a software reset, the device operates in the default mode. The I^2C interface is used to write to the control registers to configure the device.

The I^2C address assigned to the TLV320AIC3110 device is 001 1000. This device always operates in an I^2C slave mode. All registers are 8-bit, and all writable registers have read-back capability. The device auto-increments to support sequential addressing and can be used with the I^2C fast mode. When the device is reset, all appropriate registers are updated by the host processor to configure the device as needed by the user.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Power-Supply Sequence

The TLV320AIC3110 requires multiple power supply rails for operation. All the power rails must be powered up for the device to operate at the fullest potention. The following is the recommended power-up sequencing for proper operation:

1. Power up SPLVDD and SPRVDD
2. Power up IOVDD

3. Power up DVDD shortly after IOVDD
4. Power up AVDD and HPVDD

Although not necessary, if the system requires, during shutdown, remove the power supplies in the reverse order of the above sequence.

7.3.2 Reset

The TLV320AIC3110 internal logic must be initialized to a known condition for proper device function. To initialize the device to its default operating condition, the hardware reset pin ($\overline{\text{RESET}}$) must be pulled low for at least 10 ns. For this initialization to work, both the IOVDD and DVDD supplies must be powered up. TI recommends that while the DVDD supply powers up, the $\overline{\text{RESET}}$ pin is pulled low.

The device can also be reset via software reset. Writing a 1 into page 0 / register 1, bit D0 resets the device.

7.3.3 Device Start-Up Lockout Times

After the TLV320AIC3110 is initialized through hardware reset at power up or software reset, the internal memories are initialized to default values. This initialization takes place within 1 ms after pulling the $\overline{\text{RESET}}$ signal high. During this initialization phase, no register-read or register-write operation should be performed on ADC or DAC coefficient buffers. Also, no block within the codec should be powered up during the initialization phase.

7.3.4 PLL Start-Up

Whenever the PLL is powered up, a start-up delay of approximately of 10 ms occurs after the power-up command of the PLL and before the clocks are available to the codec. This delay is to ensure stable operation of the PLL and clock-divider logic.

7.3.5 Power-Stage Reset

The power-stage-only reset is used to reset the device after an overcurrent latching shutdown has occurred. Using this reset re-enables the output stage without resetting all of the registers in the device. Each of the four power stages has its own dedicated reset bit. The headphone power-stage reset is performed by setting page 1 / register 31, bit D7 for HPL and by setting page 1 / register 31, bit D6 for HPR. The speaker power-stage reset is performed by setting page 1 / register 32, bit D7 for SPLP and SPLM, and by setting page 1 / register 32, bit D6 for SPRP and SPRM.

7.3.6 Software Power Down

By default, all circuit blocks are powered down following a reset condition. Hardware power up of each circuit block can be controlled by writing to the appropriate control register. This approach allows the lowest power-supply current for the functionality required. However, when a block is powered down, all of the register settings are maintained as long as power is still being applied to the device.

7.3.7 Audio Analog I/O

The TLV320AIC3110 has a stereo audio DAC and a monaural ADC. The device supports a wide range of analog interfaces to support different headsets and analog outputs. The TLV320AIC3110 has features to interface output drivers (8-Ω, 16-Ω, 32-Ω) and a microphone PGA with AGC control. A special circuit has also been included in the TLV320AIC3110 to insert a short key-click sound into the stereo audio output. The key-click sound is used to provide feedback to the user when a particular button is pressed or item is selected. The specific sound of the keyclick can be adjusted by varying several register bits that control its frequency, duration, and amplitude (see Section 7.3.10.7).

7.3.8 Digital Processing Low-Power Modes

The TLV320AIC3110 device can be tuned to minimize power dissipation, to maximize performance, or to an operating point between the two extremes to best fit the application. The choice of processing blocks, PRB_P1 to PRB_P25 for stereo playback and PRB_R4 to PRB_R18 for mono recording, also influences the power consumption. In fact, the numerous processing blocks have been implemented to offer a choice among configurations having a different balance of power optimization and signal-processing capabilities.

7.3.8.1 ADC, Mono, 48 kHz, DVDD = 1.8 V, AVDD = 3.3 V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

Power consumption = 9.01 mW

Table 7-1. PRB_R4 Alternative Processing Blocks, 9.01 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R5	A	0.23
PRB_R6	A	0.22

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

Power consumption = 7.99 mW

Table 7-2. PRB_R11 Alternative Processing Blocks, 7.99 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R4	A	0.43
PRB_R5	A	0.67
PRB_R6	A	0.66
PRB_R10	B	–0.14
PRB_R12	B	0.04

7.3.8.2 ADC, Mono, 8 kHz, DVDD = 1.8 V, AVDD = 3.3 V

AOSR = 128, Processing Block = PRB_R4 (Decimation Filter A)

Power consumption = 6.77 mW

Table 7-3. PRB_R4 Alternative Processing Blocks, 6.77 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R5	A	0.03
PRB_R6	A	0.03

AOSR = 64, Processing Block = PRB_R11 (Decimation Filter B)

Power consumption = 6.61 mW

Table 7-4. PRB_R11 Alternative Processing Blocks, 6.61 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_R4	A	0.07
PRB_R5	A	0.11
PRB_R6	A	0.11
PRB_R10	B	–0.02
PRB_R12	B	0.01

7.3.8.3 DAC Playback on Headphones, Stereo, 48 kHz, DVDD = 1.8 V, AVDD = 3.3 V, HPVDD = 3.3 V

DOSR = 128, Processing Block = PRB_P7 (Interpolation Filter B)

Power consumption = 24.28 mW

Table 7-5. PRB_P7 Alternative Processing Blocks, 24.28 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P1	A	1.34
PRB_P2	A	2.86
PRB_P3	A	2.11
PRB_P8	B	1.18
PRB_P9	B	0.53
PRB_P10	B	1.89
PRB_P11	B	0.87
PRB_P23	A	1.48
PRB_P24	A	2.89
PRB_P25	A	3.23

DOSR = 64, Processing Block = PRB_P7 (Interpolation Filter B)

Power consumption = 24.5 mW

Table 7-6. PRB_P7 Alternative Processing Blocks, 24.5 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P1	A	1.17
PRB_P2	A	2.62
PRB_P3	A	2
PRB_P8	B	0.99
PRB_P9	B	0.5
PRB_P10	B	1.46
PRB_P11	B	0.66
PRB_P23	A	1.43
PRB_P24	A	2.69
PRB_P25	A	2.92

7.3.8.4 DAC Playback on Headphones, Mono, 48 kHz, DVDD = 1.8 V, AVDD = 3.3 V, HPVDD = 3.3 V

DOSR = 128, Processing Block = PRB_P12 (Interpolation Filter B)

Power consumption = 15.4 mW

Table 7-7. PRB_P12 Alternative Processing Blocks, 15.4 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P4	A	0.57
PRB_P5	A	1.48
PRB_P6	A	1.08
PRB_P13	B	0.56
PRB_P14	B	0.27
PRB_P15	B	0.89
PRB_P16	B	0.31

DOSR = 64, Processing Block = PRB_P12 (Interpolation Filter B)

Power consumption = 15.54 mW

Table 7-8. PRB_P12 Alternative Processing Blocks, 15.54 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P4	A	0.37
PRB_P5	A	1.23
PRB_P6	A	1.15
PRB_P13	B	0.43
PRB_P14	B	0.13
PRB_P15	B	0.85
PRB_P16	B	0.21

7.3.8.5 DAC Playback on Headphones, Stereo, 8 kHz, DVDD = 1.8 V, AVDD = 3.3 V, HPVDD = 3.3 V

DOSR = 768, Processing Block = PRB_P7 (Interpolation Filter B)

Power consumption = 22.44 mW

Table 7-9. PRB_P7 Alternative Processing Blocks, 22.44 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P1	A	0.02
PRB_P2	A	0.31
PRB_P3	A	0.23
PRB_P8	B	0.28
PRB_P9	B	–0.03
PRB_P10	B	0.14
PRB_P11	B	0.05
PRB_P23	A	0.29
PRB_P24	A	0.26
PRB_P25	A	0.47

DOSR = 384, Processing Block = PRB_P7 (Interpolation Filter B)

Power consumption = 22.83 mW

Table 7-10. PRB_P7 Alternative Processing Blocks, 22.83 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P1	A	0.27
PRB_P2	A	0.4
PRB_P3	A	0.34
PRB_P8	B	0.2
PRB_P9	B	0.08
PRB_P10	B	0.24
PRB_P11	B	0.12
PRB_P23	A	0.23
PRB_P24	A	0.42
PRB_P25	A	0.46

7.3.8.6 DAC Playback on Headphones, Mono, 8 kHz, DVDD = 1.8 V, AVDD = 3.3 V, HPVDD = 3.3 V

DOSR = 768, Processing Block = PRB_P12 (Interpolation Filter B)

Power consumption = 14.49 mW

Table 7-11. PRB_P12 Alternative Processing Blocks, 14.49 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P4	A	–0.04
PRB_P5	A	0.2
PRB_P6	A	–0.01
PRB_P13	B	0.1
PRB_P14	B	0.05
PRB_P15	B	–0.03
PRB_P16	B	0.07

DOSR = 384, Processing Block = PRB_P12 (Interpolation Filter B)

Power consumption = 14.42 mW

Table 7-12. PRB_P12 Alternative Processing Blocks, 14.42 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P4	A	0.16
PRB_P5	A	0.3
PRB_P6	A	0.2
PRB_P13	B	0.15
PRB_P14	B	0.07
PRB_P15	B	0.18
PRB_P16	B	0.09

7.3.8.7 DAC Playback on Headphones, Stereo, 192 kHz, DVDD = 1.8 V, AVDD = 3.3 V, HPVDD = 3.3 V

DOSR = 32, Processing Block = PRB_P17 (Interpolation Filter C)

Power consumption = 27.05 mW

Table 7-13. PRB_P17 Alternative Processing Blocks, 27.05 mW

PROCESSING BLOCK	FILTER	ESTIMATED POWER CHANGE (mW)
PRB_P18	C	5.28
PRB_P19	C	1.98

7.3.8.8 DAC Playback on Line Out (10 k-Ω load), Stereo, 48 kHz, DVDD = 1.8 V, AVDD = 3 V, HPVDD = 3 V

DOSR = 64, Processing Block = PRB_P7 (Interpolation Filter B)

Power consumption = 12.85 mW

7.3.9 Audio ADC and Analog Inputs

7.3.9.1 MICBIAS and Microphone Preamplifier

The TLV320AIC3110 device includes a microphone bias circuit that sources up to 4 mA of current and is programmable to a 2-V, 2.5-V, or AVDD level. The level is controlled by writing to page 1 / register 46, bits D1–D0. Table 7-14 lists this functionality.

Table 7-14. MICBIAS Settings

D1	D0	FUNCTIONALITY
0	0	MICBIAS output is powered down
0	1	MICBIAS output is powered to 2 V
1	0	MICBIAS output is powered to 2.5 V
1	1	MICBIAS output is powered to AVDD

During normal operation, MICBIAS can be set to 2.5 V for better performance. However, based on the model of the selected microphone, optimal performance can be obtained at another setting and therefore the performance at a given setting must be verified.

The lowest current consumption occurs when MICBIAS is powered down. The next-lowest current consumption occurs when MICBIAS is set at AVDD.

Because of the oversampling nature of the audio ADC and the integrated digital-decimation filtering, requirements for analog anti-aliasing filtering are very relaxed. The TLV320AIC3110 device integrates a second-order analog anti-aliasing filter with 20-dB attenuation at 1 MHz. This filter, combined with the digital decimal filter, provides sufficient anti-aliasing filtering without requiring any external components.

The MIC PGA supports analog gain control from 0 dB to 59.5 dB in steps of 0.5 dB. These gain levels are controlled by writing to page 1 / register 47, bits D6–D0. The PGA gain changes are implemented with internal soft-stepping. This soft-stepping ensures that volume-control changes occur smoothly with no audible artifacts. On reset, the MIC PGA gain defaults to a mute condition, with soft-stepping enabled. The ADC soft-stepping control is enabled or disabled by writing to page 0 / register 81, bits D1–D0. ADC soft-stepping timing is provided by the internal oscillator and internal divider logic block.

The input feed-forward resistance for the MIC1LP input of the microphone PGA stage has three settings, 10 kΩ, 20 kΩ, and 40 kΩ, which are controlled by writing to page 1 / register 48, bits D7 and D6. The input feed-forward resistance value selected affects the gain of the microphone PGA. The ADC PGA gain for the MIC1LP input depends on the setting of page1 / register 48 and page 1 / register 49, bits D7–D6. If D7–D6 are set to 01, then the ADC PGA has 6 dB more gain with respect to the value programmed using page 1 / register 47. If D7–D6 are set to 10, then the ADC PGA has the same gain as programmed using page 1 / register 47. If D7–D6 are set to 11, then the ADC PGA has 6 dB less gain with respect to the value programmed using page 1 / register 47. The same gain scaling is also valid for the MIC1RP and MIC1LM input, based on the feed-forward resistance selected using page 1 / register 48, bits D5–D2.

Table 7-15 lists the effective gain applied by the PGA.

Table 7-15. PGA Gain Versus Input Impedance

PAGE 1 / REGISTER 47 D6–D0	EFFECTIVE GAIN APPLIED BY PGA					
	SINGLE-ENDED			DIFFERENTIAL		
	RIN = 10 kΩ	RIN = 20 kΩ	RIN = 40 kΩ	RIN = 10 kΩ	RIN = 20 kΩ	RIN = 40 kΩ
000 0000	6 dB	0 dB	–6 dB	12 dB	6 dB	0 dB
000 0001	6.5 dB	0.5 dB	–5.5 dB	12.5 dB	6.5 dB	0.5 dB
000 0010	7 dB	1 dB	–5 dB	13 dB	7 dB	1 dB
...	...	...	...	...	...	...

The MIC PGA gain is either controlled by an AGC loop or as a fixed gain. See for the various analog input routings to the MIC PGA that are supported in the single-ended and differential configurations. The AGC is enabled by writing to page 0 / register 86, bit D7. If the AGC is not enabled, then setting a fixed gain occurs by writing to page 1 / register 47, bits D6–D0. Because the TLV320AIC3110 device supports soft-stepping gain changes, a read-only flag on page 0 / register 36, bit D7 is set whenever the gain applied by PGA equals the desired value set by the gain register. The MIC PGA is enabled by writing to page 1 / register 47, bit D7. ADC muting occurs by writing to page 0 / register 82, bit D7 and page 1 / register 47, bit D7. Disabling the MIC PGA sets the gain to 0 dB. Muting the ADC causes the digital output to mute so that the output value remains fixed. When soft-stepping is enabled, the CODEC_CLKIN signal must stay active until after the ADC power-down register is written, in order to ensure that soft-stepping to mute has had time to complete. When the ADC POWER UP flag is no longer set, the CODEC_CLKIN signal can shut down.

7.3.9.2 Automatic Gain Control (AGC)

The TLV320AIC3110 includes automatic gain control (AGC) for the microphone inputs. AGC can be used to maintain nominally constant output-signal amplitude when recording speech signals. This circuitry automatically adjusts the MIC PGA gain as the input signal becomes overly loud or very weak, such as when a person speaking into a microphone moves closer to or farther from the microphone. The AGC algorithm has several programmable settings, including target gain, attack and decay time constants, noise threshold, and maximum PGA applicable, that allow the algorithm to be fine-tuned for any particular application. The algorithm uses the absolute average of the signal (which is the average of the absolute value of the signal) as a measure of the nominal amplitude of the output signal. Because the gain can be changed at the sample interval time, the AGC algorithm operates at the ADC_f_S clock rate.

Target level represents the nominal output level at which the AGC attempts to hold the ADC output signal. The TLV320AIC3110 allows programming of eight different target levels, which can be programmed from –5.5 dB to –24 dB relative to a full-scale signal. Because the TLV320AIC3110 reacts to the signal absolute average and not to peak levels, TI recommends that the target level be set with enough margin to avoid clipping at the occurrence of loud sounds.

An AGC low-pass filter is used to help determine the average level of the input signal. This average level is compared to the programmed detection levels in the AGC to provide the correct functionality. This low-pass filter is in the form of a first-order IIR filter. Programming this filter is done by writing to page 4 / register 2 through page 4 / register 7. Two 8-bit registers are used to form the 16-bit digital coefficient as shown on the register map. In this way, a total of six registers are programmed to form the three IIR coefficients.

Attack time determines how quickly the AGC circuitry reduces the PGA gain when the input signal is too loud. Programming the attack time is done by writing to page 0 / register 89, bits D7–D0.

Decay time determines how quickly the PGA gain is increased when the input signal is too low. Programming the decay time is done by writing to page 0 / register 90, bits D7–D0.

Noise threshold is a reference level. If the input speech average value falls below the noise threshold, the AGC considers it as a silence and hence brings down the gain to 0 dB in steps of 0.5 dB every sample period and sets the noise-threshold flag. The gain stays at 0 dB unless the input speech signal average rises above the noise-threshold setting. This ensures that noise is not amplified in the absence of speech. The noise-threshold level in the AGC algorithm is programmable from –30 dB to –90 dB for the microphone input. When the AGC noise threshold is set to –70 dB, –80 db, or –90 dB, the microphone input maximum PGA applicable setting must be greater than or equal to 11.5 dB, 21.5 dB, or 31.5 dB, respectively. This operation includes debounce and hysteresis to prevent the AGC gain from cycling between high gain and 0 dB when signals are near the noise threshold level. When the noise-threshold flag is set, the status of the gain applied by the AGC and the saturation flag has no meaning. Programming the noise debounce is done by writing to page 0 / register 91, bits D4–D0. Programming the signal debounce is done by writing to page 0 / register 92, bits D3–D0.

Max PGA applicable allows the user to restrict the maximum gain applied by the AGC. This can be used for limiting PGA gain in situations where environmental noise is greater than the programmed noise threshold. Microphone input maximum PGA can be programmed from 0 dB to 59.5 dB in steps of 0.5 dB. Programming the maximum PGA gain allowed by the AGC is done by writing to page 0 / register 88, bits D6–D0.

See Table 7-16 for various AGC programming options. AGC can be used only if the microphone input is routed to the ADC channel.

Table 7-16. AGC Settings(1)

CONTROL REGISTER	BIT	FUNCTION
36	D5 (read-only)	AGC saturation flag
39	D3 (read-only)	ADC saturation flag
45	D6 (read-only)	Signal to level setting of noise threshold
86	D7	AGC enable
86	D6–D4	Target level
87	D7–D6	Hysteresis
87	D5–D1	Noise threshold
88	D6–D0	Maximum PGA applicable
89	D7–D0	Time constants (attack time)
90	D7–D0	Time constants (decay time)
91	D4–D0	Debounce time (noise)
92	D3–D0	Debounce time (signal)
93	D7–D0 (read-only)	Gain applied by AGC

(1) All registers shown in this table are located on page 0.

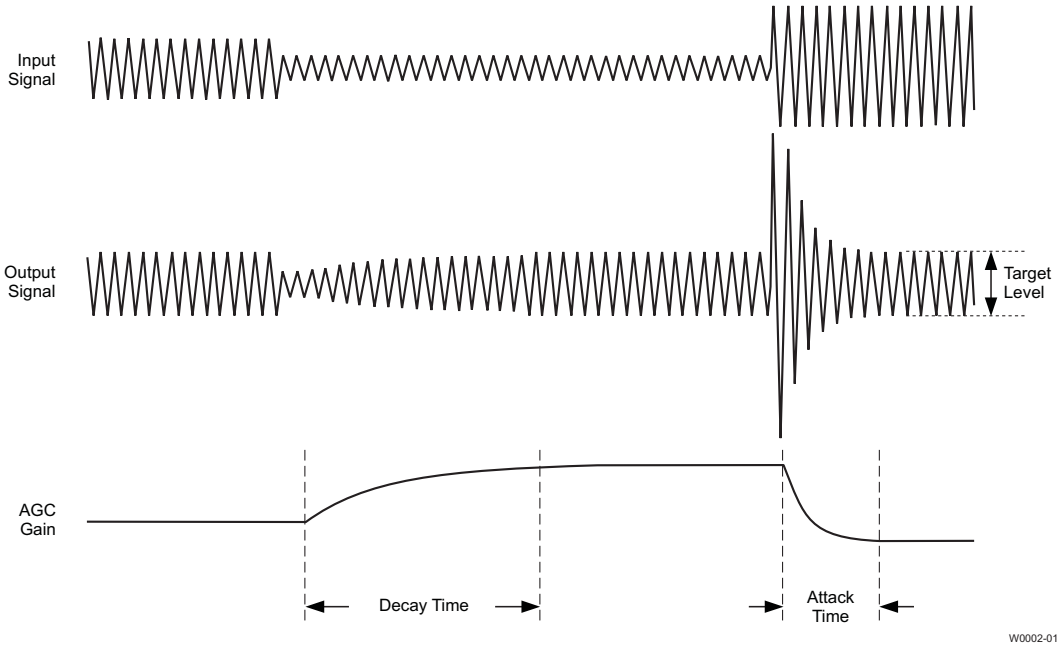


Figure 7-1. AGC Characteristics

The AGC settings should be set based on user and system conditions such as microphone selection and sensitivity, acoustics (plastics) around the microphone which affect the microphone pattern, expected distance and direction between microphone and sound source, and acoustic background noise.

One example of AGC code follows, but actual use of code should be verified based on application usage. Note that the AGC code should be set up before powering up the ADC.

```
###################### AGC ENABLE EXAMPLE CODE ###################
## Switch to page 0
w 30 00 00
# Set AGC enable and Target Level = -10 dB
# Target level can be set lower if clipping occurs during speech
# Target level is adjusted considering Max Gain also
w 30 56 A0 # AGC hysteresis=DISABLE, noise threshold = -90dB
# Noise threshold should be set at higher level if noisy background is present in application
w 30 57 FE # AGC maximum gain= 40 dB
# Higher Max gain is a trade off between gaining up a low sensitivity MIC, and the background
# acoustic noise
# Microphone bias voltage (MICBIAS) level can be used to change the Microphone Sensitivity
w 30 58 50
# Attack time=864/Fs w 30 59 68
# Decay time=22016/Fs
w 30 5A A8
# Noise debounce 0 ms
# Noise debounce time can be increased if needed
w 30 5B 00
# Signal debounce 0 ms
# Signal debounce time can be increased if needed
w 30 5C 00
####################### END of AGC SET UP ################################
```

7.3.9.3 Delta-Sigma ADC

The analog-to-digital converter has a delta-sigma modulator with an oversampling ratio (AOSR) up to 128. The ADC can support a maximum output rate of 192 kHz.

ADC power up is controlled by writing to page 0 / register 81, bit D7. An ADC power-up condition can be verified by reading page 0 / register 36, bit D6.

7.3.9.4 ADC Decimation Filtering and Signal Processing

The TLV320AIC3110 ADC channel includes built-in digital decimation filters to process the oversampled data from the delta-sigma modulator to generate digital data at the Nyquist sampling rate with high dynamic range. The decimation filter can be chosen from three different types, depending on the required frequency response, group delay, and sampling rate.

7.3.9.4.1 ADC Processing Blocks

The TLV320AIC3110 offers a range of processing blocks which implement various signal processing capabilities along with decimation filtering. These processing blocks give users the choice of how much and what type of signal processing they may use and which decimation filter is applied.

The choices among these processing blocks allow the system designer to balance power conservation and signal-processing flexibility. Less signal-processing capability reduces the power consumed by the device. Table 7-17 gives an overview of the available processing blocks of the ADC channel and their properties. The Resource Class (RC) column gives a relative indication of power consumption.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- Variable-tap FIR filter
- AGC

The processing blocks are tuned for common cases and can achieve high anti-alias filtering or low group delay in combination with various signal-processing effects such as audio effects and frequency shaping. The available first-order IIR, biquad, and FIR filters have fully user-programmable coefficients.

Table 7-17. ADC Processing Blocks

PROCESSING BLOCKS	CHANNEL	DECIMATION FILTER	1st-ORDER IIR AVAILABLE	NUMBER BIQUADS	FIR	REQUIRED AOSR VALUE	RESOURCE CLASS
PRB_R4	Mono	A	Yes	0	No	128, 64	3
PRB_R5	Mono	A	Yes	5	No	128, 64	4
PRB_R6	Mono	A	Yes	0	25-tap	128, 64	4
PRB_R10	Mono	B	Yes	0	No	64	2
PRB_R11	Mono	B	Yes	3	No	64	2
PRB_R12	Mono	B	Yes	0	20-tap	64	2
PRB_R16	Mono	C	Yes	0	No	32	2
PRB_R17	Mono	C	Yes	5	No	32	2
PRB_R18	Mono	C	Yes	0	25-tap	32	2

7.3.9.4.2 ADC Processing Blocks – Signal Chain Details

7.3.9.4.2.1 First-Order IIR, AGC, Filter A

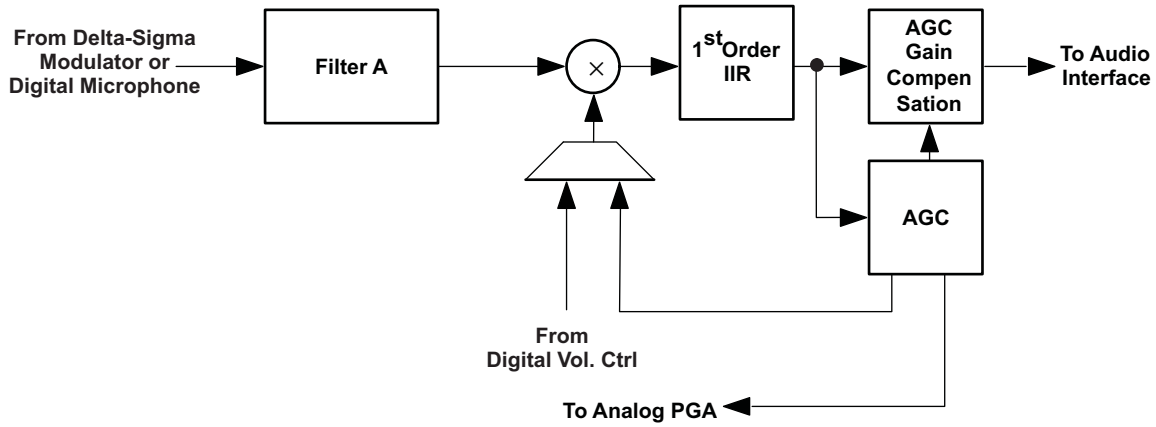


Figure 7-2. Signal Chain for PRB_R4

7.3.9.4.2.2 Five Biquads, First-Order IIR, AGC, Filter A

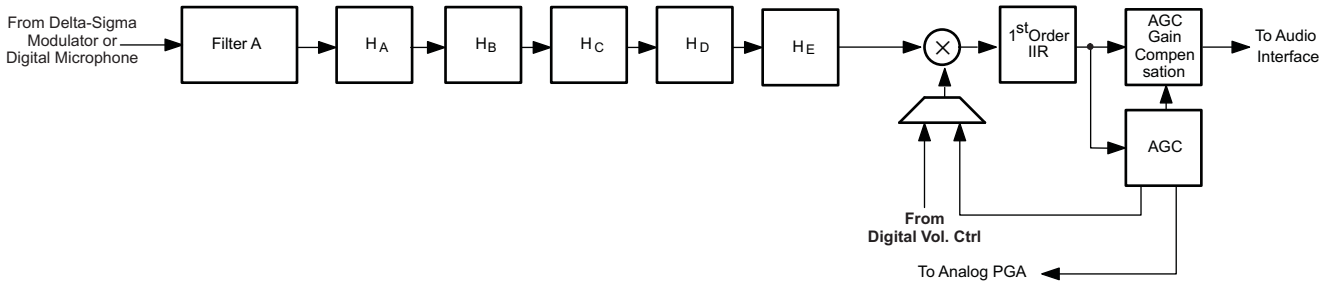


Figure 7-3. Signal Chain for PRB_R5

7.3.9.4.2.3 25-Tap FIR, First-Order IIR, AGC, Filter A

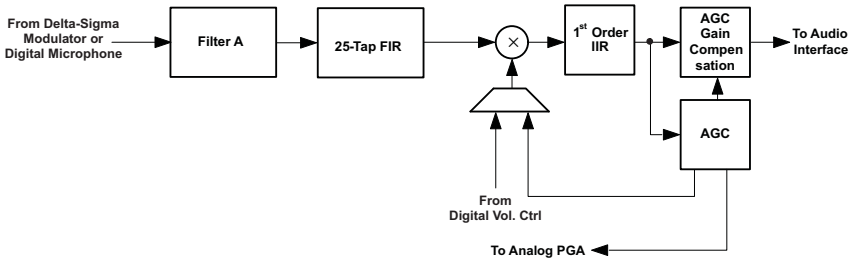


Figure 7-4. Signal Chain for PRB_R6

7.3.9.4.2.4 First-Order IIR, AGC, Filter B

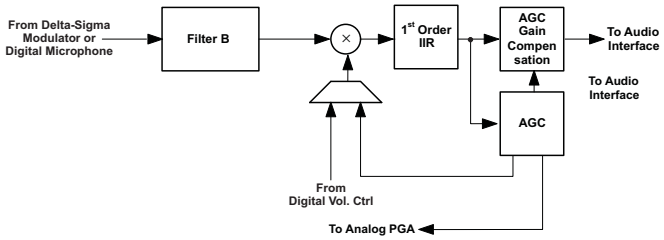


Figure 7-5. Signal Chain for PRB_R10

7.3.9.4.2.5 Three Biquads, First-Order IIR, AGC, Filter B

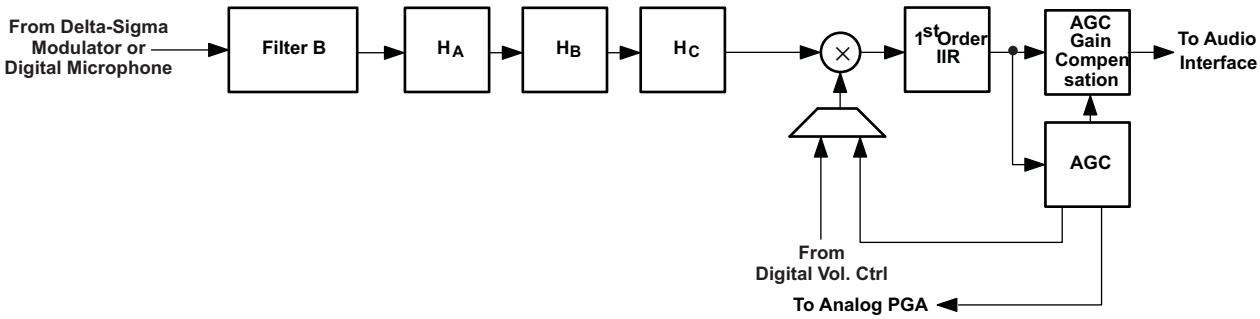


Figure 7-6. Signal Chain for PRB_R11

7.3.9.4.2.6 20-Tap FIR, First-Order IIR, AGC, Filter B

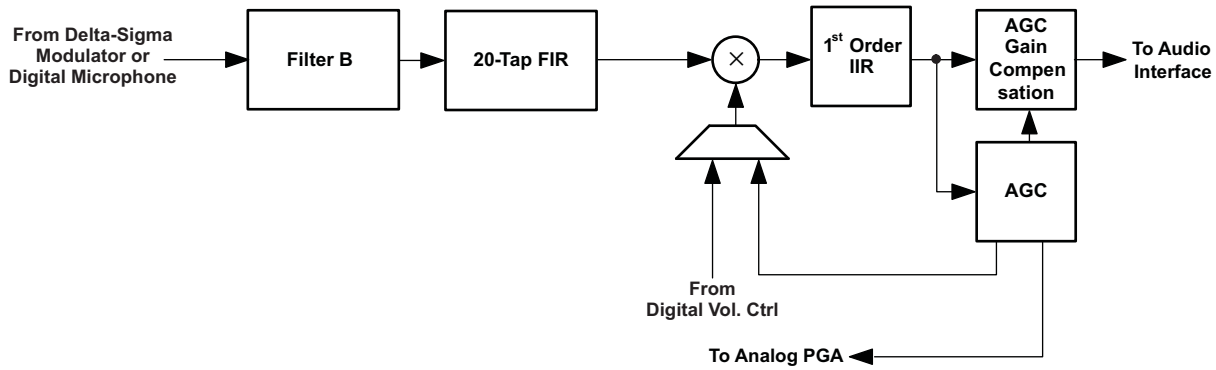


Figure 7-7. Signal Chain for PRB_R12

7.3.9.4.2.7 First-Order IIR, AGC, Filter C

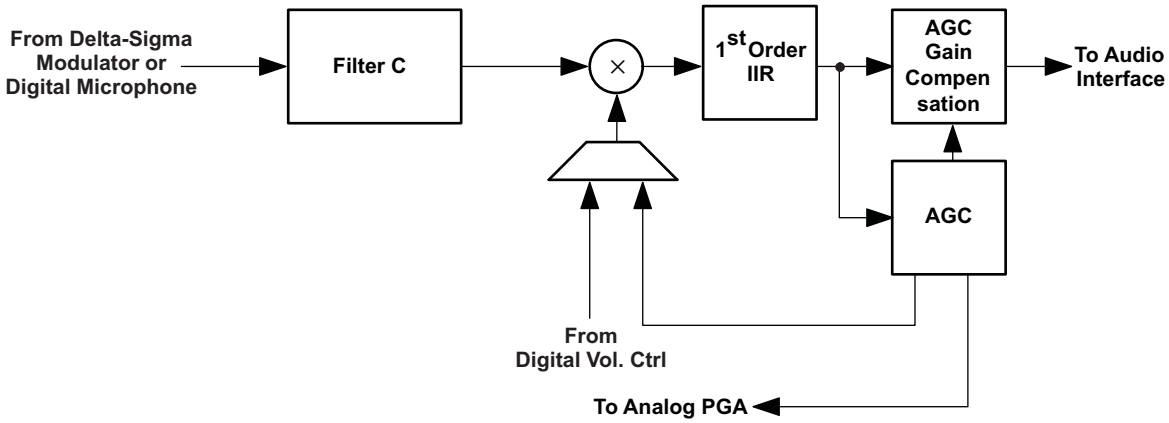


Figure 7-8. Signal Chain for PRB_R16

7.3.9.4.2.8 Five Biquads, First-Order IIR, AGC, Filter C

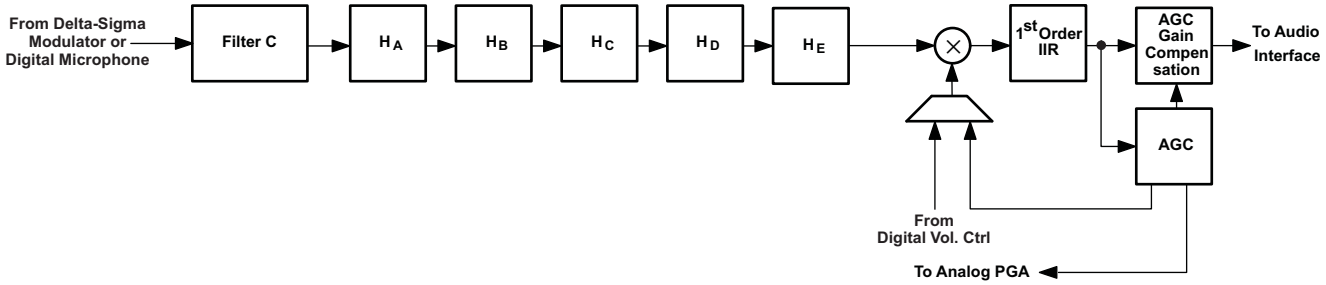


Figure 7-9. Signal Chain for PRB_R17

7.3.9.4.2.9 25-Tap FIR, First-Order IIR, AGC, Filter C

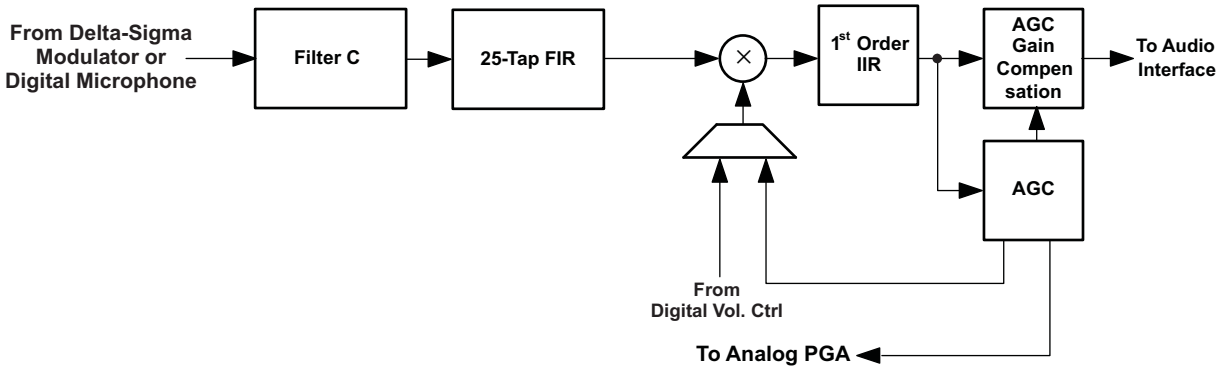


Figure 7-10. Signal Chain for PRB_R18

7.3.9.4.3 User-Programmable Filters

Depending on the selected processing block, different types and orders of digital filtering are available. A first-order IIR filter is always available, and is useful to filter out possible dc components of the signal efficiently. Up to five biquad sections or, alternatively, FIR filters of up to 25 taps are available for specific processing blocks. The coefficients of the available filters are arranged as sequentially indexed coefficients.

The coefficients of these filters are each 16 bits wide, in 2s-complement format, and occupy two consecutive 8-bit registers in the register space. Specifically, the filter coefficients are in 1.15 (one dot 15) format with a range from –1.0 (0x8000) to 0.999969482421875 (0x7FFF), as shown in Figure 7-11.

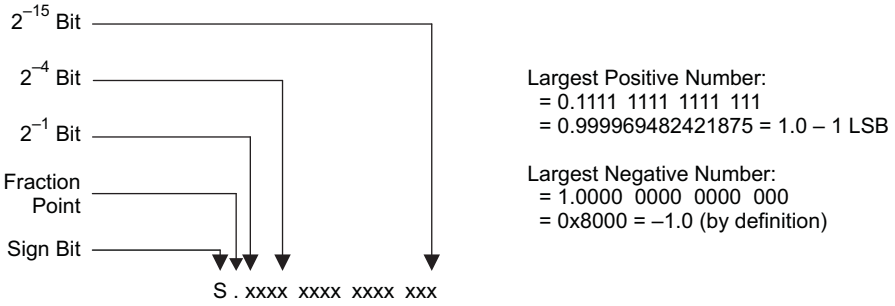


Figure 7-11. 1.15 2s-Complement Coefficient Format

7.3.9.4.3.1 First-Order IIR Section

The transfer function for the first-order IIR filter is given by Equation 1.

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (1)$$

The frequency response for the first-order IIR section with default coefficients is flat at a gain of 0 dB.

Table 7-18. ADC First-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	ADC COEFFICIENT	DEFAULT (RESET) VALUES
First-order IIR	N0	Page 4 / register 8 and page 4 / register 9	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 10 and page 4 / register 11	0x0000
	D1	Page 4 / register 12 and page 4 / register 13	0x0000

7.3.9.4.3.2 Biquad Section

The transfer function of each of the biquad filters is given by Equation 2.

$$H(z) = \frac{N_0 + 2 \times N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2 \times D_1 z^{-1} - D_2 z^{-2}} \quad (2)$$

The default values for each biquad section yield an all-pass (flat) frequency response at a gain of 0 dB.

Table 7-19. ADC Biquad Filter Coefficients

FILTER	FILTER COEFFICIENT	FILTER COEFFICIENT RAM LOCATION	DEFAULT (RESET) VALUES
Biquad A	N0	Page 4 / register 14 and page 4 / register 15	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 16 and page 4 / register 17	0x0000
	N2	Page 4 / register 18 and page 4 / register 19	0x0000
	D1	Page 4 / register 20 and page 4 / register 21	0x0000
	D2	Page 4 / register 22 and page 4 / register 23	0x0000
Biquad B	N0	Page 4 / register 24 and page 4 / register 25	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 26 and page 4 / register 27	0x0000
	N2	Page 4 / register 28 and page 4 / register 29	0x0000
	D1	Page 4 / register 30 and page 4 / register 31	0x0000
	D2	Page 4 / register 32 and page 4 / register 33	0x0000

Table 7-19. ADC Biquad Filter Coefficients (continued)

FILTER	FILTER COEFFICIENT	FILTER COEFFICIENT RAM LOCATION	DEFAULT (RESET) VALUES
Biquad C	N0	Page 4 / register 34 and page 4 / register 35	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 36 and page 4 / register 37	0x0000
	N2	Page 4 / register 38 and page 4 / register 39	0x0000
	D1	Page 4 / register 40 and page 4 / register 41	0x0000
	D2	Page 4 / register 42 and page 4 / register 43	0x0000
Biquad D	N0	Page 4 / register 44 and page 4 / register 45	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 46 and page 4 / register 47	0x0000
	N2	Page 4 / register 48 and page 4 / register 49	0x0000
	D1	Page 4 / register 50 and page 4 / register 51	0x0000
	D2	Page 4 / register 52 and page 4 / register 53	0x0000
Biquad E	N0	Page 4 / register 54 and page 4 / register 55	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 4 / register 56 and page 4 / register 57	0x0000
	N2	Page 4 / register 58 and page 4 / register 59	0x0000
	D1	Page 4 / register 60 and page 4 / register 61	0x0000
	D2	Page 4 / register 62 and page 4 / register 63	0x0000

7.3.9.4.3.3 FIR Section

Three of the available ADC processing blocks offer FIR filters for signal processing. Processing block PRB_R12 features a 20-tap FIR filter, whereas the processing blocks PRB_R6 and PRB_R18 each feature a 25-tap FIR filter.

$$H(z) = \sum_{n=0}^{M} FIR_n z^{-n}$$
$$M = 24 \text{ for } PRB\_R6, PRB\_R18$$
$$M = 19 \text{ for } PRB\_R12 \quad (3)$$

The coefficients of the FIR filters are 16-bit 2s-complement format (2 bytes each) and correspond to the ADC coefficient space as listed in Table 7-20. Note that the default (reset) coefficients are not valid for the FIR filter. When the FIR filter is used, all applicable coefficients must be reprogrammed by the user. To reprogram the FIR filter coefficients as an all-pass filter, write value 0x00 to page 4 / registers 24, 25, 34, 35, 44, 45, 54, and 55.

Table 7-20. ADC FIR Filter Coefficients

FILTER COEFFICIENT	FILTER COEFFICIENT RAM LOCATION	DEFAULT (RESET) VALUES – NOT VALID FOR THE FIR FILTER – MUST BE REPROGRAMMED BY USER
FIR0	Page 4 / register 14 and page 4 / register 15	0x7FFF (decimal 1.0 – LSB value)
FIR1	Page 4 / register 16 and page 4 / register 17	0x0000
FIR2	Page 4 / register 18 and page 4 / register 19	0x0000
FIR3	Page 4 / register 20 and page 4 / register 21	0x0000
FIR4	Page 4 / register 22 and page 4 / register 23	0x0000
FIR5	Page 4 / register 24 and page 4 / register 25	0x7FFF (decimal 1.0 – LSB value)
FIR6	Page 4 / register 26 and page 4 / register 27	0x0000
FIR7	Page 4 / register 28 and page 4 / register 29	0x0000
FIR8	Page 4 / register 30 and page 4 / register 31	0x0000
FIR9	Page 4 / register 32 and page 4 / register 33	0x0000
FIR10	Page 4 / register 34 and page 4 / register 35	0x7FFF (decimal 1.0 – LSB value)
FIR11	Page 4 / register 36 and page 4 / register 37	0x0000
FIR12	Page 4 / register 38 and page 4 / register 39	0x0000

Table 7-20. ADC FIR Filter Coefficients (continued)

FILTER COEFFICIENT	FILTER COEFFICIENT RAM LOCATION	DEFAULT (RESET) VALUES – NOT VALID FOR THE FIR FILTER – MUST BE REPROGRAMMED BY USER
FIR13	Page 4 / register 40 and page 4 / register 41	0x0000
FIR14	Page 4 / register 42 and page 4 / register 43	0x0000
FIR15	Page 4 / register 44 and page 4 / register 45	0x7FFF (decimal 1.0 – LSB value)
FIR16	Page 4 / register 46 and page 4 / register 47	0x0000
FIR17	Page 4 / register 48 and page 4 / register 49	0x0000
FIR18	Page 4 / register 50 and page 4 / register 51	0x0000
FIR19	Page 4 / registe 52 and page 4 / register 53	0x0000
FIR20	Page 4 / register 54 and page 4 / register 55	0x7FFF (decimal 1.0 – LSB value)
FIR21	Page 4 / register 56 and page 4 / register 57	0x0000
FIR22	Page 4 / register 58 and page 4 / register 59	0x0000
FIR23	Page 4 / register 60 and page 4 / register 61	0x0000
FIR24	Page 4 / register 62 and page 4 / register 63	0x0000

7.3.9.4.4 ADC Digital Decimation Filter Characteristics

The TLV320AIC3110 offers three different types of decimation filters. The integrated digital decimation filter removes high-frequency content and downsamples the audio data from an initial sampling rate of AOSR × f_S to the final output sampling rate of f_S. The decimation filtering is achieved using a higher-order CIC filter followed by linear-phase FIR filters. The decimation filter cannot be chosen by itself; it is implicitly set through the chosen processing block.

The following subsections describe the properties of the available filters A, B, and C.

7.3.9.4.4.1 Decimation Filter A

This filter is intended for use at sampling rates up to 48 kHz. When configuring this filter, the oversampling ratio of the ADC can either be 128 or 64. For highest performance, the oversampling ratio must be set to 128.

Filter A can also be used for 96 kHz at an AOSR of 64.

Table 7-21. ADC Decimation-Filter-A Specifications

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
AOSR = 128			
Filter gain pass band	0…0.39 f_S	0.062	dB
Filter gain stop band	0.55…64 f_S	–73	dB
Filter group delay		17/f_S	s
Pass-band ripple, 8 ksps	0…0.39 f_S	0.062	dB
Pass-band ripple, 44.1 ksps	0…0.39 f_S	0.05	dB
Pass-band ripple, 48 ksps	0…0.39 f_S	0.05	dB
AOSR = 64			
Filter gain pass band	0…0.39 f_S	0.062	dB
Filter gain stop band	0.55…32 f_S	–73	dB
Filter group delay		17/f_S	s
Pass-band ripple, 8 ksps	0…0.39 f_S	0.062	dB
Pass-band ripple, 44.1 ksps	0…0.39 f_S	0.05	dB
Pass-band ripple, 48 ksps	0…0.39 f_S	0.05	dB
Pass-band ripple, 96 ksps	0…20 kHz	0.1	dB

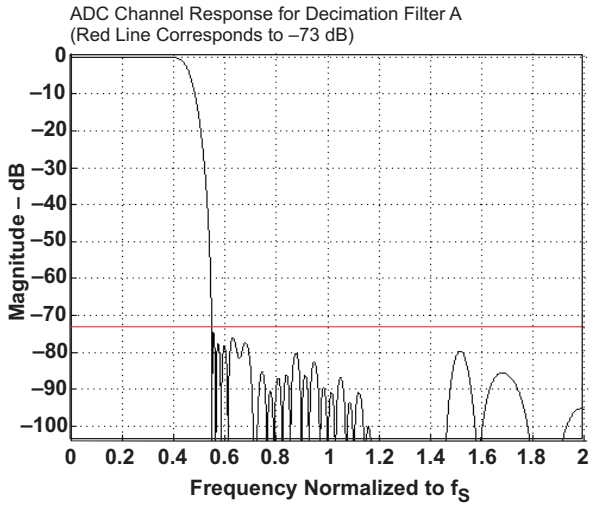


Figure 7-12. ADC Decimation-Filter-A Frequency Response

7.3.9.4.4.2 Decimation Filter B

Filter B is intended to support sampling rates up to 96 kHz at an oversampling ratio of 64.

Table 7-22. ADC Decimation-Filter-B Specifications

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
AOSR = 64			
Filter gain pass band	0…0.39 f_S	±0.077	dB
Filter gain stop band	0.60 f_S…32 f_S	–46	dB
Filter group delay		11/f_S	s
Pass-band ripple, 8 ksps	0…0.39 f_S	0.076	dB
Pass-band ripple, 44.1 ksps	0…0.39 f_S	0.06	dB
Pass-band ripple, 48 ksps	0…0.39 f_S	0.06	dB
Pass-band ripple, 96 ksps	0…20 kHz	0.11	dB

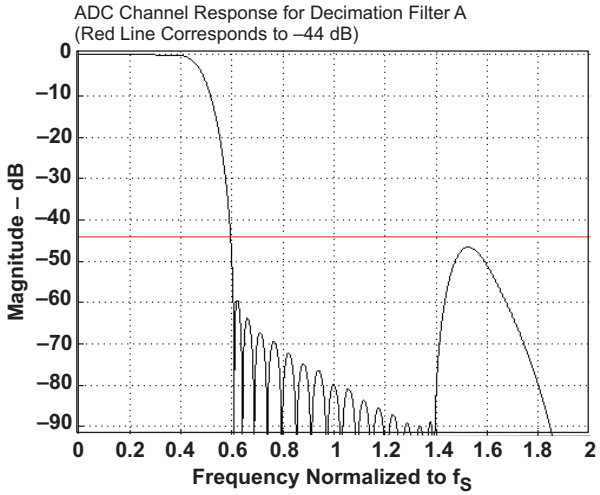


Figure 7-13. ADC Decimation-Filter-B Frequency Response

7.3.9.4.4.3 Decimation Filter C

Filter C along with an AOSR of 32 is specially designed for 192-ksps operation for the ADC. The pass band, which extends up to 0.11 × f_S (corresponding to 21 kHz), is suited for audio applications.

Table 7-23. ADC Decimation-Filter-C Specifications

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
Filter gain from 0 to 0.11 f_S	0…0.11 f_S	±0.033	dB
Filter gain from 0.28 f_S to 16 f_S	0.28 f_S…16 f_S	–60	dB
Filter group delay		11/f_S	s
Pass-band ripple, 8 ksps	0…0.11 f_S	0.033	dB
Pass-band ripple, 44.1 ksps	0…0.11 f_S	0.033	dB
Pass-band ripple, 48 ksps	0…0.11 f_S	0.032	dB
Pass-band ripple, 96 ksps	0…0.11 f_S	0.032	dB
Pass-band ripple, 192 ksps	0…20 kHz	0.086	dB

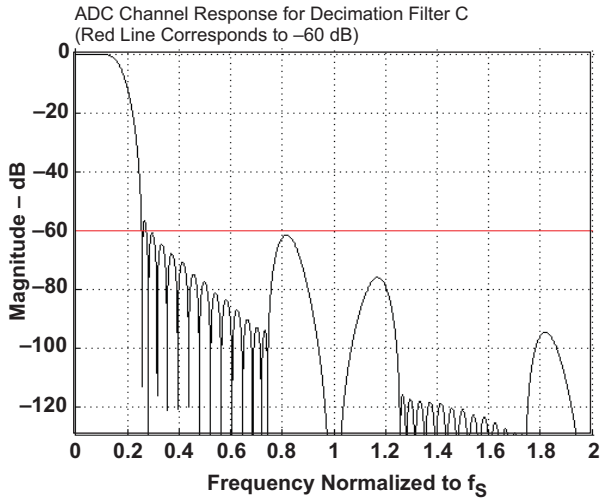


Figure 7-14. ADC Decimation-Filter-C Frequency Response

7.3.9.4.5 ADC Data Interface

The decimation filter and signal processing block in the ADC channel pass 32-bit data words to the audio serial interface once every cycle of ADC_f_S. During each cycle of ADC_f_S, a pair of data words (for left and right channel) is passed. The audio serial interface rounds the data to the required word length of the interface before converting to serial data. Because the TLV320AIC3110 has only a mono ADC, it passes the same data to both the left and right channels of the audio serial interface.

7.3.9.5 Updating ADC Digital Filter Coefficients During Record

When it is required to update the ADC digital filter coefficients during record, care must be taken to avoid click and pop noise or even a possible oscillation noise. These artifacts can occur if the ADC coefficients are updated without following the proper update sequence. The correct sequence is shown in Figure 7-15. The values for the times listed are conservative and should be used for software purposes.

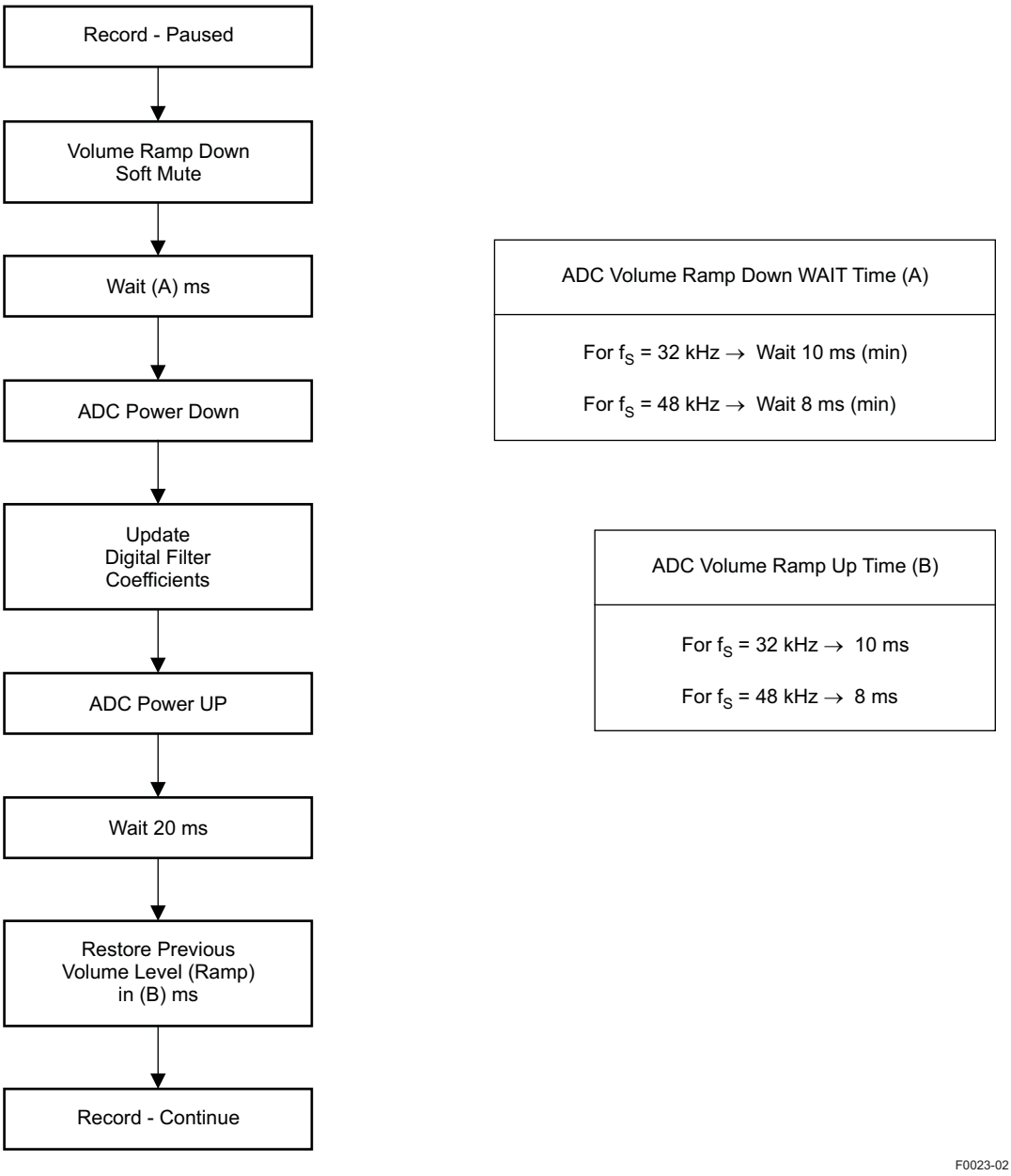


Figure 7-15. Updating ADC Digital Filter Coefficients During Record

7.3.9.6 Digital Microphone Function

In addition to supporting analog microphones, the TLV320AIC3110 can also interface to one digital microphone using the mono ADC channel. Figure 7-16 shows the digital microphone interface block diagram and Figure 7-17 shows the timing diagram for the digital microphone interface.

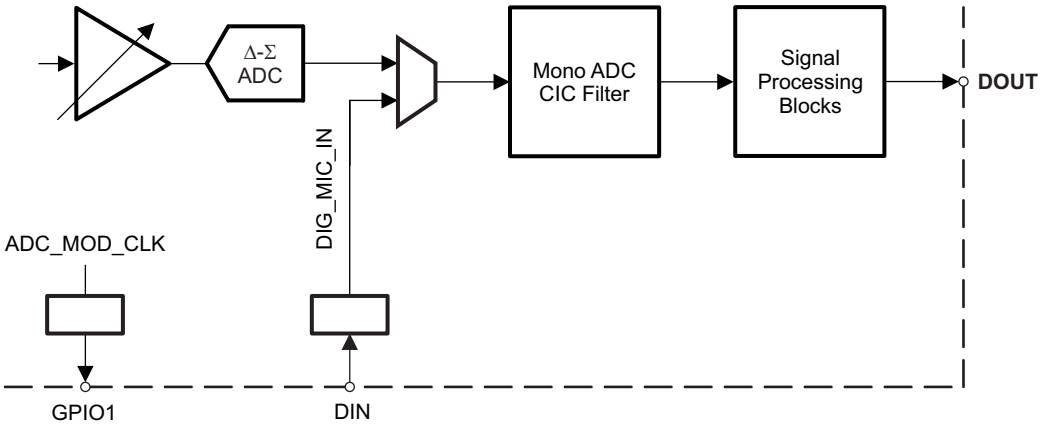


Figure 7-16. Digital Microphone in the TLV320AIC3110

The TLV320AIC3110 outputs internal clock ADC_MOD_CLK on the GPIO1 pin (page 0 / register 51, bits D5–D2 = 1010). This clock can be connected to the external digital microphone device. The single-bit output of the external digital microphone device can be connected to the DIN pin. Internally, the TLV320AIC3110 latches the steady value of the mono ADC data on the rising edge of ADC_MOD_CLK.

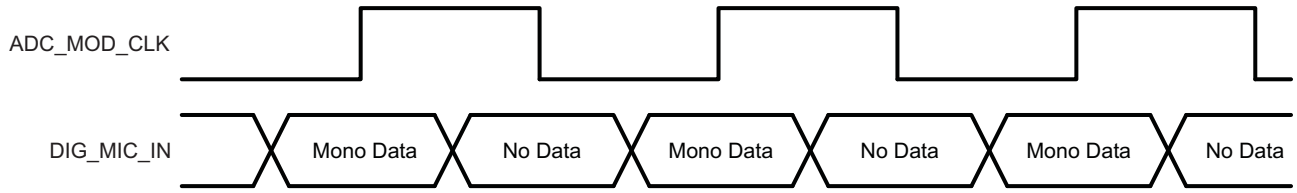


Figure 7-17. Timing Diagram for Digital Microphone Interface

When the digital microphone mode is enabled, the analog section of the ADC can be powered down and bypassed for power efficiency. The AOSR value for the ADC channel must be configured to select the desired decimation ratio to be achieved, based on the external digital microphone properties.

7.3.9.7 DC Measurement

The TLV320AIC3110 supports a highly flexible dc-measurement feature using the high-resolution oversampling and noise-shaping ADC. This mode can be used when the ADC channel is not used for the voice/audio record function. This mode can be enabled by programming page 0 / register 102, bit D7. The converted data is 24 bits, using the 2.22 numbering format. The value of the converted data for the ADC channel can be read back from page 0 / register 104 through page 1 / register 106. Before reading back the converted data, page 0 / register 103, bit D6 must be programmed to 1 in order to latch the converted data into the read-back registers. After the converted data is read back, page 0 / register 103, bit D6 must be immediately reset to 0. In dc-measurement mode, two measurement modes are supported.

Mode A

In dc-measurement mode A, a variable-length averaging filter is used. The length of averaging filter D can be programmed from 1 to 20 by programming page 0 / register 102, bits D4–D0. To choose mode A, page 0 / register 102, bit D5 must be programmed to 0.

Mode B

To choose mode B, page 0 / register 102, bit D5 must be programmed to 1. In dc-measurement mode B, a first-order IIR filter is used. The coefficients of this filter are determined by D, page 0 / register 102, bits D4–D0. The nature of the filter is given in Table 7-24.

Table 7-24. DC Measurement Bandwidth Settings

D: PAGE 0 / REGISTER 102, BITS D4–D0	–3 dB BW (kHz)	–0.5 dB BW (kHz)
1	688.440	236.500
2	275.970	96.334
3	127.400	44.579
4	61.505	21.532
5	30.248	10.590
6	15.004	5.253
7	7.472	2.616
8	3.729	1.305
9	1.862	652
10	931	326
11	465	163
12	232.6	81.5
13	116.3	40.7
14	58.1	20.3
15	29.1	10.2
16	14.54	5.09
17	7.25	2.54
18	3.63	1.27
19	1.8	0.635
20	0.908	0.3165

By programming page 0 / register 103, bit D5 to 1, the averaging filter is periodically reset after 2^R number of ADC_MOD_CLK periods, where R is programmed in page 0 / register 103, bits D4–D0. When page 0 / register 103, bit D5 is set to 1, then the value of D should be less than the value of R. When page 0 / register 103, bit D5 is programmed to 0, the averaging filter is never reset.

7.3.10 Audio DAC and Audio Analog Outputs

Each channel of the stereo audio DAC consists of a digital-audio processing block, a digital interpolation filter, a digital delta-sigma modulator, and an analog reconstruction filter. This high oversampling ratio (typically DOSR is between 32 and 128) exhibits good dynamic range by ensuring that the quantization noise generated within the delta-sigma modulator stays outside of the audio frequency band. Audio analog outputs include stereo headphone, or lineouts, and stereo class-D speaker outputs.

7.3.10.1 DAC

The TLV320AIC3110 stereo-audio DAC supports data rates from 8 kHz to 192 kHz. Each channel of the stereo audio-DAC consists of a signal-processing engine with fixed processing blocks, a digital interpolation filter, a multibit digital delta-sigma modulator, and an analog reconstruction filter. The DAC is designed to provide enhanced performance at low sampling rates through increased oversampling and image filtering, thereby keeping quantization noise generated within the delta-sigma modulator and signal

images strongly suppressed within the audio band to beyond 20 kHz. To handle multiple input rates and optimize power dissipation and performance, the TLV320AIC3110 device allows the system designer to program the oversampling rates over a wide range from 1 to 1024 by configuring page 0 / register 13 and page 0 / register 14. The system designer can choose higher oversampling ratios for lower input data rates and lower oversampling ratios for higher input data rates.

The TLV320AIC3110 DAC channel includes a built-in digital interpolation filter to generate oversampled data for the delta-sigma modulator. The interpolation filter can be chosen from three different types, depending on required frequency response, group delay, and sampling rate.

DAC power up is controlled by writing to page 0 / register 63, bit D7 for the left channel and bit D6 for the right channel. The left-channel DAC clipping flag is provided as a read-only bit on page 0 / register 39, bit D7. The right-channel DAC clipping flag is provided as a read-only bit on page 0 / register 39, bit D6.

7.3.10.1.1 DAC Processing Blocks

The TLV320AIC3110 device implements signal-processing capabilities and interpolation filtering through processing blocks. These fixed processing blocks give users the choice of how much and what type of signal processing they use and which interpolation filter is applied.

The choices among these processing blocks allow the system designer to balance power conservation and signal-processing flexibility. Table 7-25 gives an overview of all available processing blocks of the DAC channel and their properties. The resource-class column gives an approximate indication of power consumption for the digital (DVDD) supply; however, based on the out-of-band noise spectrum, the analog power consumption of the drivers (HPVDD) may differ.

The signal processing blocks available are:

- First-order IIR
- Scalable number of biquad filters
- 3D effect
- Digital sine-wave (beep) generator

The processing blocks are tuned for common cases and can achieve high image rejection or low group delay in combination with various signal-processing effects such as audio effects and frequency shaping. The available first-order IIR and biquad filters have fully user-programmable coefficients.

Table 7-25. Overview – DAC Predefined Processing Blocks

PROCESSING BLOCK NO.	INTERPOLATION FILTER	CHANNEL	FIRST-ORDER IIR AVAILABLE	NUMBER OF BIQUADS	DRC	3D	BEEP GENERATOR	RESOURCE CLASS
PRB_P1	A	Stereo	No	3	No	No	No	8
PRB_P2	A	Stereo	Yes	6	Yes	No	No	12
PRB_P3	A	Stereo	Yes	6	No	No	No	10
PRB_P4	A	Left	No	3	No	No	No	4
PRB_P5	A	Left	Yes	6	Yes	No	No	6
PRB_P6	A	Left	Yes	6	No	No	No	6
PRB_P7	B	Stereo	Yes	0	No	No	No	6
PRB_P8	B	Stereo	No	4	Yes	No	No	8
PRB_P9	B	Stereo	No	4	No	No	No	8
PRB_P10	B	Stereo	Yes	6	Yes	No	No	10
PRB_P11	B	Stereo	Yes	6	No	No	No	8
PRB_P12	B	Left	Yes	0	No	No	No	3
PRB_P13	B	Left	No	4	Yes	No	No	4
PRB_P14	B	Left	No	4	No	No	No	4
PRB_P15	B	Left	Yes	6	Yes	No	No	6
PRB_P16	B	Left	Yes	6	No	No	No	4
PRB_P17	C	Stereo	Yes	0	No	No	No	3
PRB_P18	C	Stereo	Yes	4	Yes	No	No	6
PRB_P19	C	Stereo	Yes	4	No	No	No	4

Table 7-25. Overview – DAC Predefined Processing Blocks (continued)

PROCESSING BLOCK NO.	INTERPOLATION FILTER	CHANNEL	FIRST-ORDER IIR AVAILABLE	NUMBER OF BIQUADS	DRC	3D	BEEP GENERATOR	RESOURCE CLASS
PRB_P20	C	Left	Yes	0	No	No	No	2
PRB_P21	C	Left	Yes	4	Yes	No	No	3
PRB_P22	C	Left	Yes	4	No	No	No	2
PRB_P23	A	Stereo	No	2	No	Yes	No	8
PRB_P24	A	Stereo	Yes	5	Yes	Yes	No	12
PRB_P25	A	Stereo	Yes	5	Yes	Yes	Yes	12

7.3.10.1.2 DAC Processing Blocks — Details

7.3.10.1.2.1 Three Biquads, Filter A

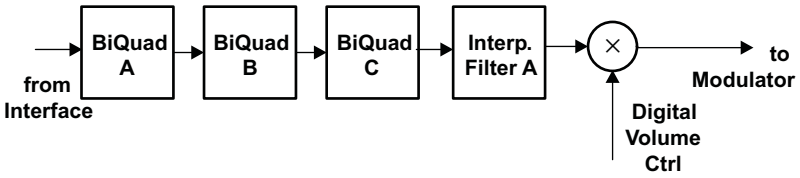


Figure 7-18. Signal Chain for PRB_P1 and PRB_P4

7.3.10.1.2.2 Six Biquads, First-Order IIR, DRC, Filter A or B

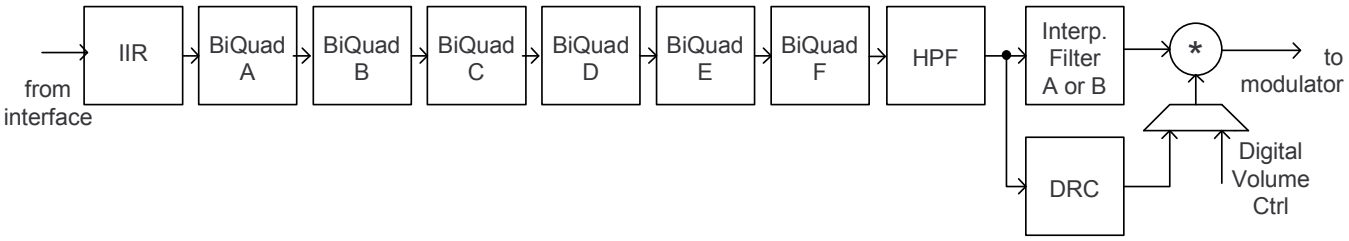


Figure 7-19. Signal Chain for PRB_P2, PRB_P5, PRB_P10, and PRB_P15

7.3.10.1.2.3 Six Biquads, First-Order IIR, Filter A or B

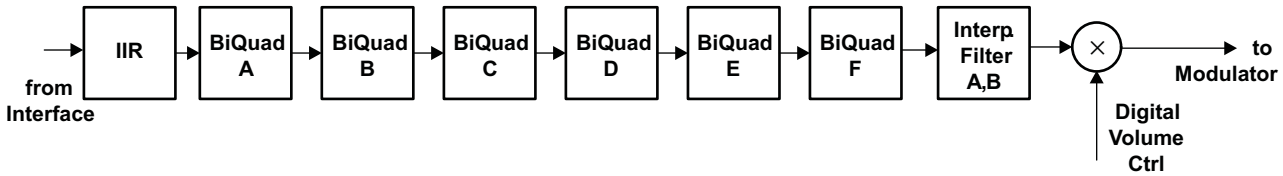


Figure 7-20. Signal Chain for PRB_P3, PRB_P6, PRB_P11, and PRB_P16

7.3.10.1.2.4 IIR, Filter B or C

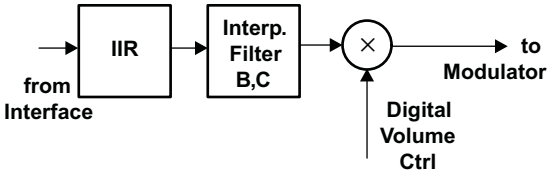


Figure 7-21. Signal Chain for PRB_P7, PRB_P12, PRB_P17, and PRB_P20

7.3.10.1.2.5 Four Biquads, DRC, Filter B

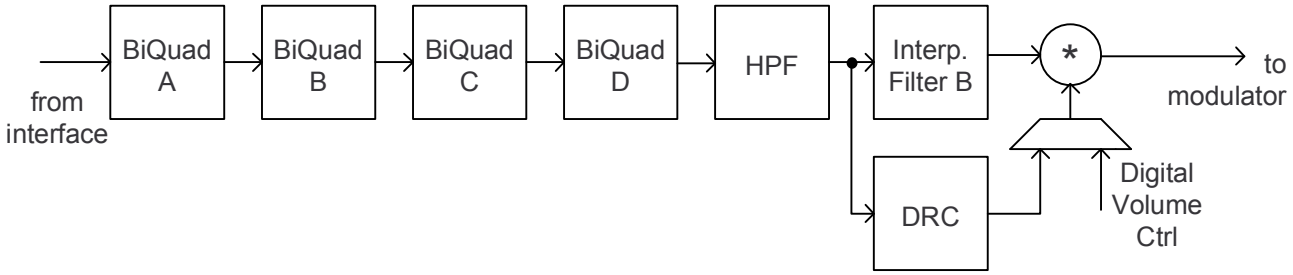


Figure 7-22. Signal Chain for PRB_P8 and PRB_P13

7.3.10.1.2.6 Four Biquads, Filter B

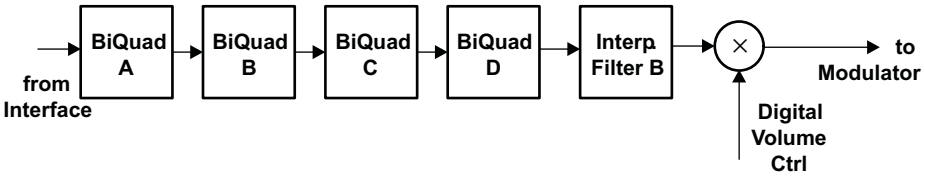


Figure 7-23. Signal Chain for PRB_P9 and PRB_P14

7.3.10.1.2.7 Four Biquads, First-Order IIR, DRC, Filter C

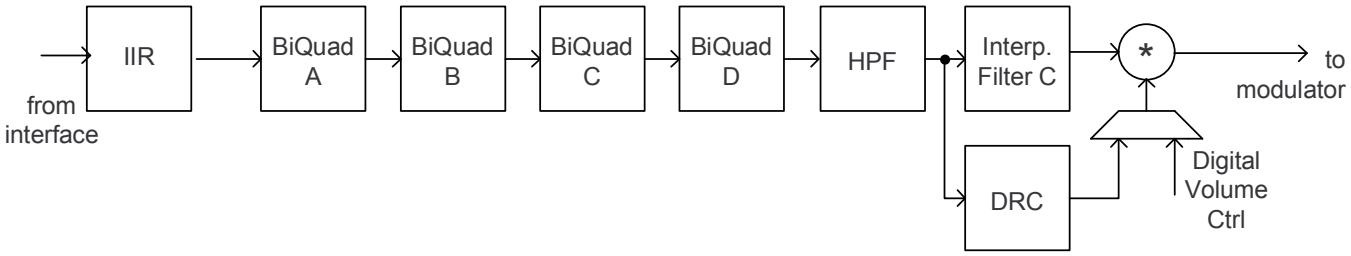


Figure 7-24. Signal Chain for PRB_P18 and PRB_P21

7.3.10.1.2.8 Four Biquads, First-Order IIR, Filter C

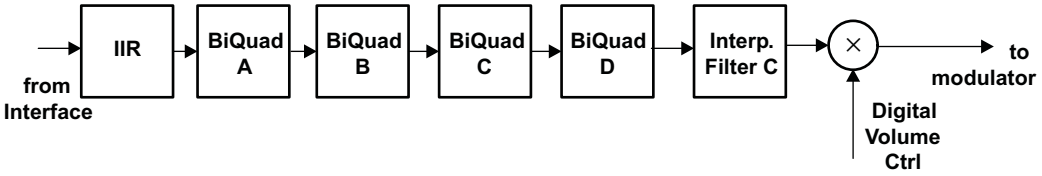
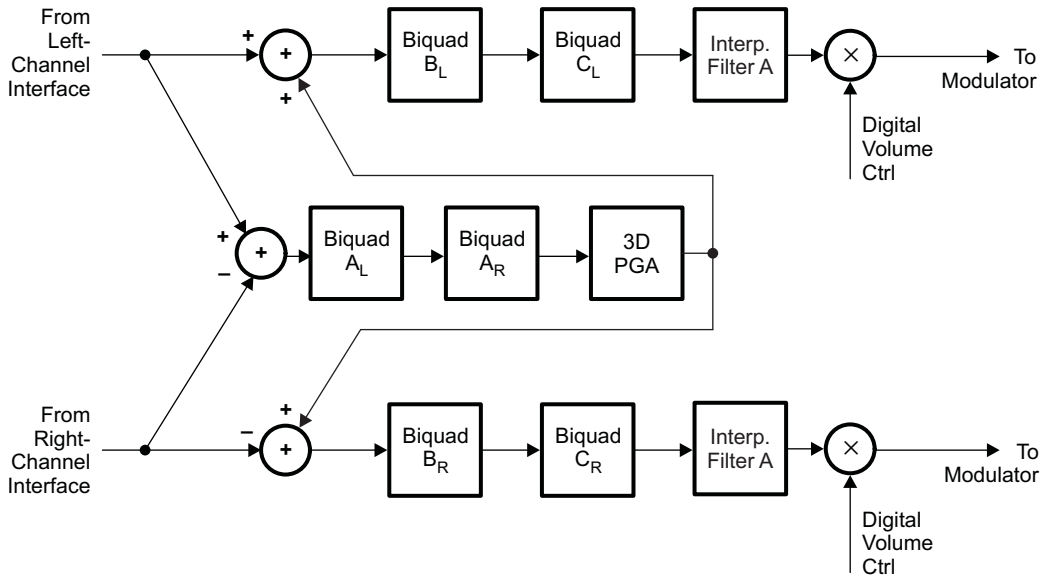


Figure 7-25. Signal Chain for PRB_P19 and PRB_P22

7.3.10.1.2.9 Two Biquads, 3D, Filter A



NOTE: A_L means biquad A of the left channel, and similarly, B_R means biquad B of the right channel.

Figure 7-26. Signal Chain for PRB_P23

7.3.10.1.2.10 Five Biquads, DRC, 3D, Filter A

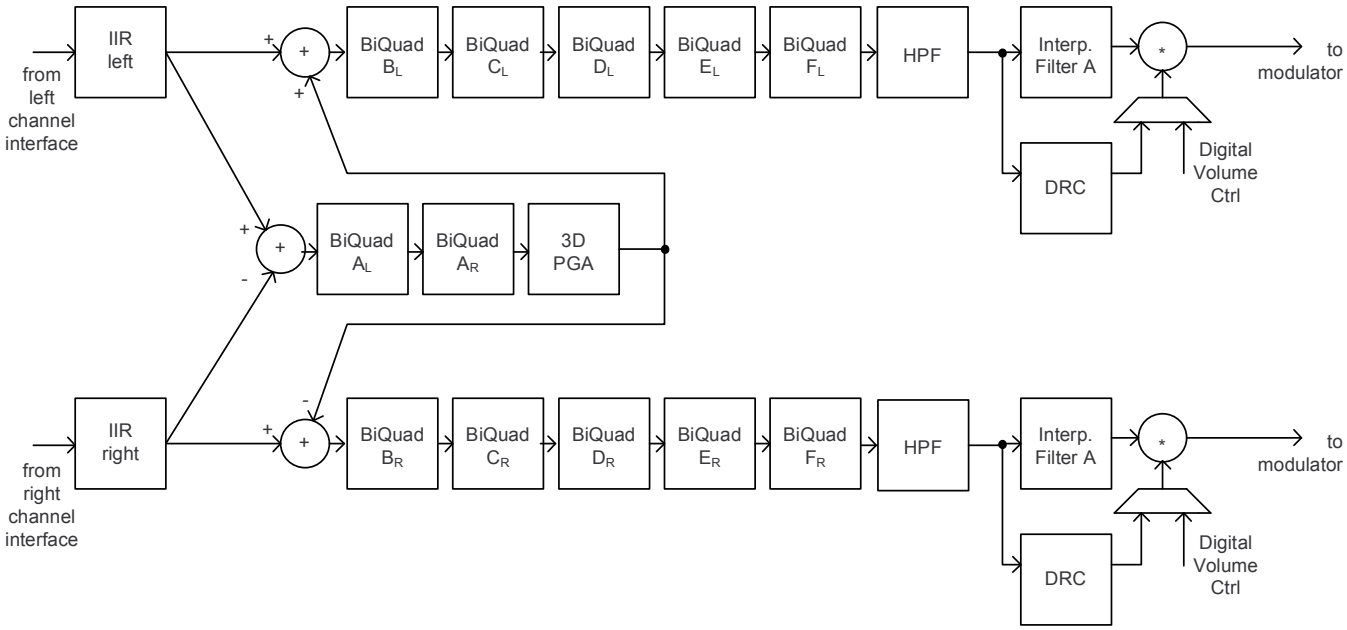


Figure 7-27. Signal Chain for PRB_P24

7.3.10.1.2.11 Five Biquads, DRC, 3D, Beep Generator, Filter A

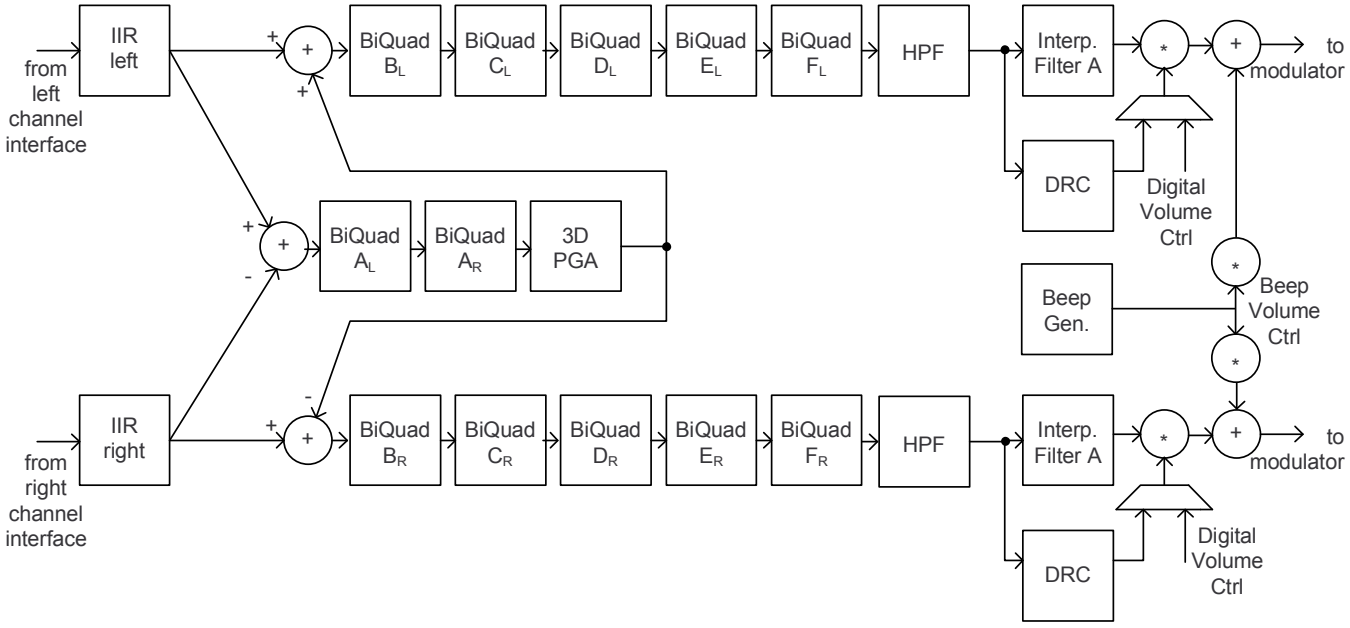


Figure 7-28. Signal Chain for PRB_P25

7.3.10.1.3 DAC User-Programmable Filters

Based on the selected processing block, different types and orders of digital filtering are available. Up to six biquad sections are available for specific processing blocks.

The coefficients of the available filters are arranged as sequentially-indexed coefficients in two banks. If adaptive filtering is chosen, the coefficient banks can be switched in real time.

When the DAC is running, the user-programmable filter coefficients are locked and cannot be accessed for either read or write.

However, the TLV320AIC3110 device offers an adaptive filter mode as well. Setting page 8 / register 1, bit D2 = 1 turns on double buffering of the coefficients. In this mode, filter coefficients are updated through the host and activated without stopping and restarting the DAC which enables advanced adaptive filtering applications.

In the double-buffering scheme, all coefficients are stored in two buffers (buffers A and B). When the DAC is running and the adaptive filtering mode is turned on, setting page 8 / register 1, bit D0 = 1 switches the coefficient buffers at the next start of a sampling period. This bit is set back to 0 after the switch occurs. At the same time, page 8 / register 1, bit D1 toggles.

The flag in page 8 / register 1, bit D1 indicates which of the two buffers is actually in use.

Page 8 / register 1, bit D1 = 0: buffer A is in use by the DAC engine; bit D1 = 1: buffer B is in use.

While the device is running, coefficient updates are always made to the buffer not in use by the DAC, regardless of the buffer to which the coefficients have been written.

Table 7-26. Adaptive-Mode Filter-Coefficient Buffer Switching

DAC POWERED UP	PAGE 8 / REGISTER 1, BIT D1	COEFFICIENT BUFFER IN USE	WRITING TO	UPDATES
No	0	None	Page 8, Reg 2–3, buffer A	Page 8, Reg 2–3, buffer A
No	0	None	Page 12, Reg 2–3, buffer B	Page 12, Reg 2–3, buffer B

Table 7-26. Adaptive-Mode Filter-Coefficient Buffer Switching (continued)

DAC POWERED UP	PAGE 8 / REGISTER 1, BIT D1	COEFFICIENT BUFFER IN USE	WRITING TO	UPDATES
Yes	0	Buffer A	Page 8, Reg 2–3, buffer A	Page 12, Reg 2–3, buffer B
Yes	0	Buffer A	Page 12, Reg 2–3, buffer B	Page 12, Reg 2–3, buffer B
Yes	1	Buffer B	Page 8, Reg 2–3, buffer A	Page 8, Reg 2–3, buffer A
Yes	1	Buffer B	Page 12, Reg 2–3, buffer B	Page 8, Reg 2–3, buffer A

The user-programmable coefficients for the DAC Processing Blocks are defined on page 8 and page 9 for buffer A and page 12 and page 13 for buffer B.

The coefficients of these filters are each 16-bit, 2s-complement format, occupying two consecutive 8-bit registers in the register space. Specifically, the filter coefficients are in 1.15 (one dot 15) format with a range from –1.0 (0x8000) to 0.999969482421875 (0x7FFF) as shown in Figure 7-11.

7.3.10.1.3.1 First-Order IIR Section

The IIR is of first order and its transfer function is given by Equation 4.

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \tag{4}$$

The frequency response for the first-order IIR section with default coefficients is flat.

Table 7-27. DAC IIR Filter Coefficients

FILTER	COEFFICIENT	LEFT DAC CHANNEL	RIGHT DAC CHANNEL	DEFAULT (RESET) VALUE
First-order IIR	N0	Page 9 / register 2 and page 9 / register 3	Page 9 / register 8 and page 9 / register 9	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 9 / register 4 and page 9 / register 5	Page 9 / register 10 and page 9 / register 11	0x0000
	D1	Page 9 / register 6 and page 9 / register 7	Page 9 / register 12 and page 9 / register 13	0x0000

7.3.10.1.3.2 Biquad Section

The transfer function of each of the biquad filters is given by Equation 5.

$$H(z) = \frac{N_0 + 2 \times N_1 z^{-1} + N_2 z^{-2}}{2^{15} - 2 \times D_1 z^{-1} - D_2 z^{-2}} \tag{5}$$

Table 7-28. DAC Biquad Filter Coefficients

FILTER	COEFFICIENT	LEFT DAC CHANNEL	RIGHT DAC CHANNEL	DEFAULT (RESET) VALUE
Biquad A	N0	Page 8 / register 2 and page 8 / register 3	Page 8 / register 66 and page 8 / register 67	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 4 and page 8 / register 5	Page 8 / register 68 and page 8 / register 69	0x0000
	N2	Page 8 / register 6 and page 8 / register 7	Page 8 / register 70 and page 8 / register 71	0x0000
	D1	Page 8 / register 8 and page 8 / register 9	Page 8 / register 72 and page 8 / register 73	0x0000
	D2	Page 8 / register 10 and page 8 / register 11	Page 8 / register 74 and page 8 / register 75	0x0000

Table 7-28. DAC Biquad Filter Coefficients (continued)

FILTER	COEFFICIENT	LEFT DAC CHANNEL	RIGHT DAC CHANNEL	DEFAULT (RESET) VALUE
Biquad B	N0	Page 8 / register 12 and page 8 / register 13	Page 8 / register 76 and page 8 / register 77	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 14 and page 8 / register 15	Page 8 / register 78 and page 8 / register 79	0x0000
	N2	Page 8 / register 16 and page 8 / register 17	Page 8 / register 80 and page 8 / register 81	0x0000
	D1	Page 8 / register 18 and page 8 / register 19	Page 8 / register 82 and page 8 / register 83	0x0000
	D2	Page 8 / register 20 and page 8 / register 21	Page 8 / register 84 and page 8 / register 85	0x0000
Biquad C	N0	Page 8 / register 22 and page 8 / register 23	Page 8 / register 86 and page 8 / register 87	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 24 and page 8 / register 25	Page 8 / register 88 and page 8 / register 89	0x0000
	N2	Page 8 / register 26 and page 8 / register 27	Page 8 / register 90 and page 8 / register 91	0x0000
	D1	Page 8 / register 28 and page 8 / register 29	Page 8 / register 92 and page 8 / register 93	0x0000
	D2	Page 8 / register 30 and page 8 / register 31	Page 8 / register 94 and page 8 / register 95	0x0000
Biquad D	N0	Page 8 / register 32 and page 8 / register 33	Page 8 / register 96 and page 8 / register 97	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 34 and page 8 / register 35	Page 8 / register 98 and page 8 / register 99	0x0000
	N2	Page 8 / register 36 and page 8 / register 37	Page 8 / register 100 and page 8 / register 101	0x0000
	D1	Page 8 / register 38 and page 8 / register 39	Page 8 / register 102 and page 8 / register 103	0x0000
	D2	Page 8 / register 40 and page 8 / register 41	Page 8 / register 104 and page 8 / register 105	0x0000
Biquad E	N0	Page 8 / register 42 and page 8 / register 43	Page 8 / register 106 and page 8 / register 107	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 44 and page 8 / register 45	Page 8 / register 108 and page 8 / register 109	0x0000
	N2	Page 8 / register 46 and page 8 / register 47	Page 8 / register 110 and page 8 / register 111	0x0000
	D1	Page 8 / register 48 and page 8 / register 49	Page 8 / register 112 and page 8 / register 113	0x0000
	D2	Page 8 / register 50 and page 8 / register 51	Page 8 / register 114 and page 8 / register 115	0x0000
Biquad F	N0	Page 8 / register 52 and page 8 / register 53	Page 8 / register 116 and page 8 / register 117	0x7FFF (decimal 1.0 – LSB value)
	N1	Page 8 / register 54 and page 8 / register 55	Page 8 / register 118 and page 8 / register 119	0x0000
	N2	Page 8 / register 56 and page 8 / register 57	Page 8 / register 120 and page 8 / register 121	0x0000
	D1	Page 8 / register 58 and page 8 / register 59	Page 8 / register 122 and page 8 / register 123	0x0000
	D2	Page 8 / register 60 and page 8 / register 61	Page 8 / register 124 and page 8 / register 125	0x0000

7.3.10.1.4 DAC Interpolation Filter Characteristics

7.3.10.1.4.1 Interpolation Filter A

Filter A is designed for an f_S up to 48 ksps with a flat passband of 0 to 20 kHz.

Table 7-29. Specification for DAC Interpolation Filter A

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
Filter-gain pass band	0 … 0.45 f_S	±0.015	dB
Filter-gain stop band	0.55… 7.455 f_S	–65	dB
Filter group delay		21 / f_S	s

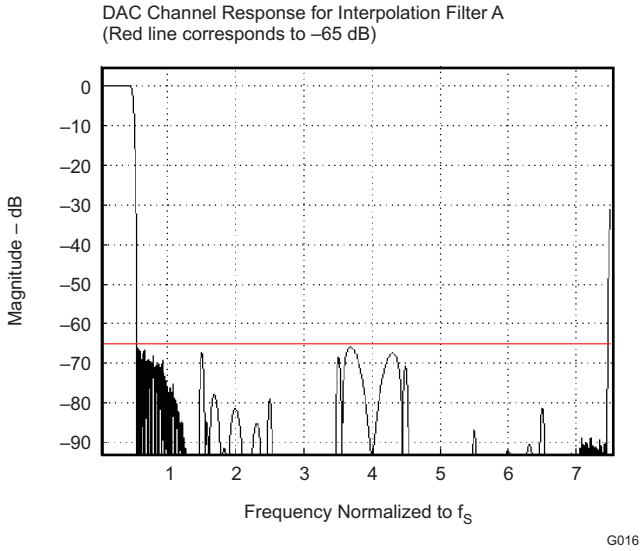


Figure 7-29. Frequency Response of DAC Interpolation Filter A

7.3.10.1.4.2 Interpolation Filter B

Filter B is specifically designed for an f_S of up to 96 ksps. Thus, the flat passband region easily covers the required audio band of 0 to 20 kHz.

Table 7-30. Specification for DAC Interpolation Filter B

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
Filter-gain pass band	0 … 0.45 f_S	±0.015	dB
Filter-gain stop band	0.55… 3.45 f_S	–58	dB
Filter group delay		18 / f_S	s

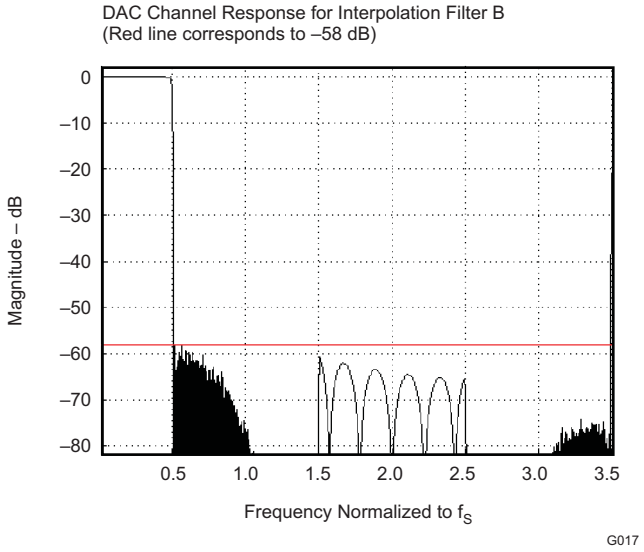


Figure 7-30. Frequency Response of Channel Interpolation Filter B

7.3.10.1.4.3 Interpolation Filter C

Filter C is specifically designed for the 192-ksps mode. The pass band extends up to 0.4 × f_S (corresponds to 80 kHz), more than sufficient for audio applications.

Table 7-31. Specification for DAC Interpolation Filter C

PARAMETER	CONDITION	VALUE (TYPICAL)	UNIT
Filter-gain pass band	0 … 0.35 f_S	±0.03	dB
Filter-gain stop band	0.6… 1.4 f_S	–43	dB
Filter group delay		13 / f_S	s

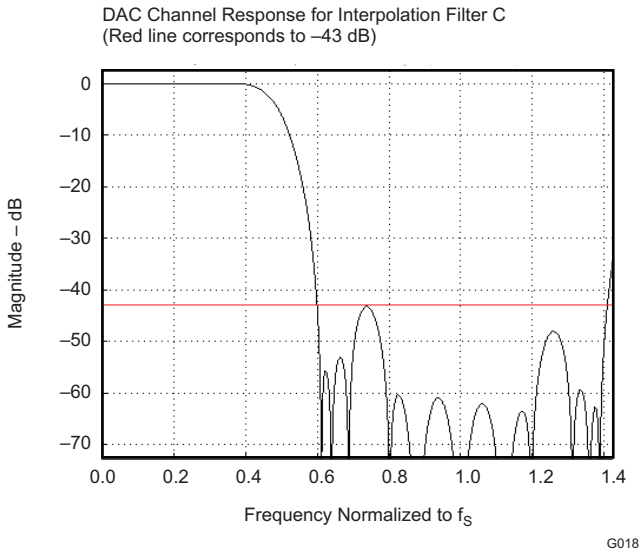


Figure 7-31. Frequency Response of DAC Interpolation Filter C

7.3.10.2 DAC Digital-Volume Control

The DAC has a digital-volume control block which implements programmable gain. Each channel has an independent volume control that can be varied from 24 dB to –63.5 dB in 0.5-dB steps. The left-channel DAC volume is controlled by writing to page 0 / register 65, bits D7–D0. The right-channel DAC volume can be controlled by writing to page 0 / register 66, bits D7–D0. DAC muting and setting up a master gain control to control both channels occurs by writing to page 0 / register 64, bits D3–D0. The gain is implemented with a soft-stepping algorithm, which only changes the actual volume by 0.125 dB per input sample, either up or down, until the desired volume is reached. The rate of soft-stepping is slowed to one step per two input samples by writing to page 0 / register 63, bits D1–D0. Note that the default source for volume-control level settings is control by register writes (page 0 / register 65 and page 0 / register 66 to control volume). Use of the VOL/MICDET pin to control the DAC volume is ignored until the volume control source selected has been changed to pin control (page 0 / register 116, bit D7 = 1). This functionality is shown in .

During soft-stepping, the host does not receive a signal when the DAC has been completely muted. This may be important if the host must mute the DAC before making a significant change, such as changing sample rates. In order to help with this situation, the device provides a flag back to the host through a read-only register, page 0 / register 38, bit D4 for the left channel and bit D0 for the right channel. This information alerts the host when the part has completed the soft-stepping and the actual volume has reached the desired volume level. The soft-stepping feature can be disabled by writing to page 0 / register 63, bits D1–D0.

If soft-stepping is enabled, the CODEC_CLKIN signal must be kept active until the DAC power-up flag is cleared. When this flag is cleared, the internal DAC soft-stepping process is complete, and CODEC_CLKIN can be stopped if desired. (The analog volume control can be ramped down using an internal oscillator.)

7.3.10.3 Volume Control Pin

The range of voltages used by the 7-bit SAR ADC is shown in Section 5.5.

The volume-control pin is not enabled by default but is enabled by writing 1 to page 0 / register 116, bit D7. The default DAC volume control uses software control of the volume, which occurs if page 0 / register 116, bit D7 = 0. Soft-stepping the volume level is set up by writing to page 0 / register 63, bits D1–D0.

When the volume-pin function is used, a 7-bit Vol ADC reads the voltage on the VOL/MICDET pin and updates the digital volume control by overwriting the current value of the volume control. The new volume setting which has been applied because of a change of voltage on the volume control pin is read on page 0 / register 117, bits D6–D0. The 7-bit Vol ADC clock source is selected on page 0 / register 116, bit D6. The update rate is programmed on page 0 / register 116, bits D2–D0 for this 7-bit SAR ADC.

Table 7-32 lists The VOL/MICDET pin gain mapping.

Table 7-32. VOL/MICDET Pin Gain Mapping

VOL/MICDET PIN SAR OUTPUT	DIGITAL GAIN APPLIED
0	18 dB
1	17.5 dB
2	17 dB
:	:
35	0.5 dB
36	0.0 dB
37	–0.5 dB
:	:
89	–26.5 dB
90	–27 dB
91	–28 dB
:	:
125	–62 dB
126	–63 dB
127	Mute

Figure 7-32 shows the VOL/MICDET pin connection and functionality.

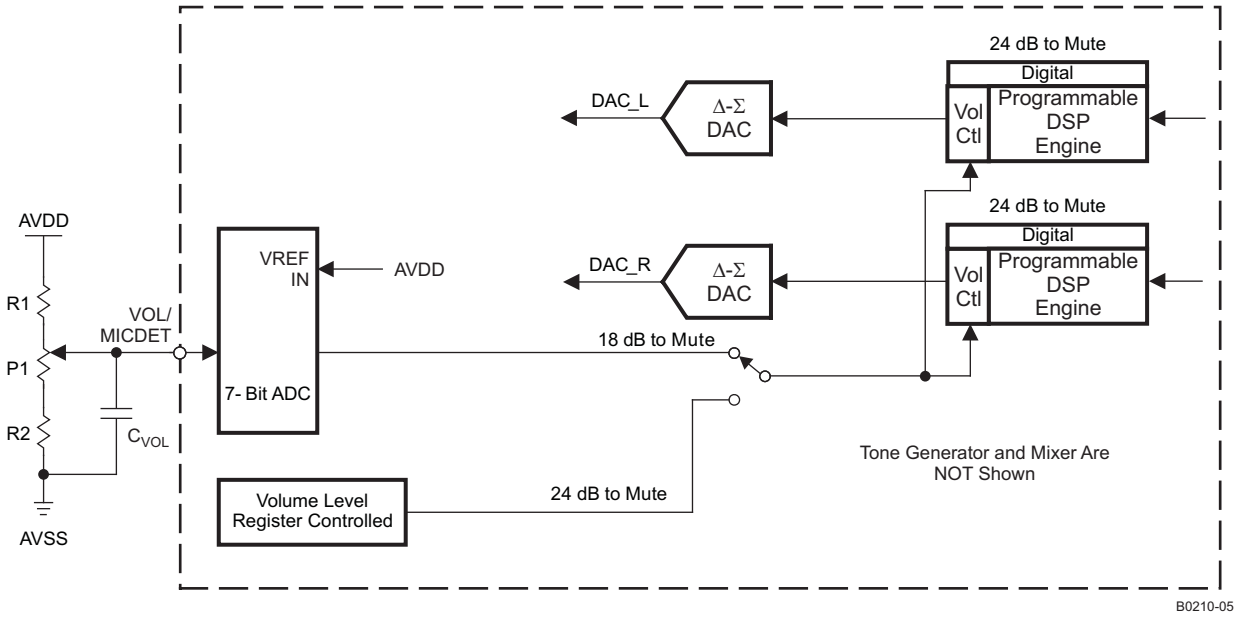


Figure 7-32. Digital Volume Controls for Beep Generator and DAC Play Data

As shown in Table 7-32, the VOL/MICDET pin has a range of volume control from 18 dB down to –63 dB, and mute. However, if less maximum gain is required, then a smaller range of voltage must be applied to the VOL/MICDET pin. Applying a smaller range of voltage occurs by increasing the value of R2 relative to the value of (P1 + R1), so that more voltage is available at the bottom of P1. The circuit must also be designed such that for the values of R1, R2, and P1 chosen, the maximum voltage (top of the potentiometer) does not exceed AVDD/2 (see Figure 7-32). The recommended values for R1, R2, and P1 for several maximum gains are shown in Table 7-33.

Table 7-33. VOL/MICDET Pin Gain Scaling

R1 (kΩ)	P1 (kΩ)	R2 (kΩ)	ADC VOLTAGE for AVDD = 3.3 V (V)	DIGITAL GAIN RANGE (dB)
25	25	0	0 to 1.65	18 to –63
33	25	7.68	0.386 to 1.642	3 to –63
34.8	25	9.76	0.463 to 1.649	0 to –63

7.3.10.4 Dynamic Range Compression

Typical music signals are characterized by crest factors, the ratio of peak signal power to average signal power, of 12 dB or more. To avoid audible distortions due to clipping of peak signals, the gain of the DAC channel must be adjusted so as not to cause hard clipping of peak signals. As a result, during nominal periods, the applied gain is low, causing the perception that the signal is not loud enough. To overcome this problem, dynamic range conpression (DRC) in the TLV320AIC3110 continuously monitors the output of the DAC digital volume control to detect its power level relative to 0 dBFS. When the power level is low, DRC increases the input signal gain to make it sound louder. At the same time, if a peaking signal is detected, it autonomously reduces the applied gain to avoid hard clipping. This results in sounds more pleasing to the ear as well as sounding louder during nominal periods.

The DRC functionality in the TLV320AIC3110 is implemented by a combination of processing blocks in the DAC channel as described in Section 7.3.10.1.2.

DRC can be disabled by writing to page 0 / register 68, bits D6–D5.

DRC typically works on the filtered version of the input signal. The input signals have no audio information at dc and extremely low frequencies; however, they can significantly influence the energy estimation function in the dynamic range compressor (the DRC). Also, most of the information about signal energy is concentrated in the low-frequency region of the input signal.

To estimate the energy of the input signal, the signal is first fed to the DRC high-pass filter and then to the DRC low-pass filter. These filters are implemented as first-order IIR filters given by

$$H_{HPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (6)$$

$$H_{LPF}(z) = \frac{N_0 + N_1 z^{-1}}{2^{15} - D_1 z^{-1}} \quad (7)$$

The coefficients for these filters are 16 bits wide in 2s-complement format and are user-programmable through register write as given in Table 7-34.

Table 7-34. The DRC HPF and LPF Coefficients

COEFFICIENT	LOCATION
HPF N0	C71 page 9 / register 14 and page 9 / register 15
HPF N1	C72 page 9 / registers 16 and page 9 / register 17
HPF D1	C73 page 9 / registers 18 and page 9 / register 19

Table 7-34. The DRC HPF and LPF Coefficients (continued)

COEFFICIENT	LOCATION
LPF N0	C74 page 9 / registers 20 and page 9 / register 21
LPF N1	C75 page 9 / registers 22 and page 9 / register 23
LPF D1	C76 page 9 / registers 24 and page 9 / register 25

The default values of these coefficients implement a high-pass filter with a cutoff at 0.00166 × DAC_f_S, and a low-pass filter with a cutoff at 0.00033 × DAC_f_S.

The output of the DRC high-pass filter is fed to the processing block selected for the DAC channel. The absolute value of the DRC LPF filter is used for energy estimation within the DRC.

The gain in the DAC digital volume control is controlled by page 0 / register 65 and page 0 / register 66. When the DRC is enabled, the applied gain is a function of the digital volume control register setting and the output of the DRC.

The DRC parameters are described in sections that follow.

7.3.10.4.1 DRC Threshold

DRC threshold represents the level of the DAC playback signal at which the gain compression becomes active. The output of the digital volume control in the DAC is compared with the set threshold. The threshold value is programmable by writing to page 0 / register 68, bits D4–D2. The threshold value can be adjusted between –3 dBFS and –24 dBFS in steps of 3 dB. Keeping the DRC threshold value too high may not leave enough time for the DRC block to detect peaking signals, and can cause excessive distortion at the outputs. Keeping the DRC threshold value too low can limit the perceived loudness of the output signal.

The recommended DRC threshold value is –24 dB.

When the output signal exceeds the set DRC threshold, the interrupt flag bits at page 0 / register 44, bits D3–D2 are updated. These flag bits are *sticky* in nature, and are reset only after they are read back by the user. The non-sticky versions of the interrupt flags are also available at page 0 / register 46, bits D3–D2.

7.3.10.4.2 DRC Hysteresis

DRC hysteresis is programmable by writing to page 0 / register 68, bits D1–D0. These bits can be programmed to represent values between 0 dB and 3 dB in steps of 1dB. DRC hysteresis provides a programmable window around the programmed DRC threshold that must be exceeded for the *disabled* DRC to become enabled, or the *enabled* DRC to become disabled. For example, if the DRC threshold is set to –12 dBFS and the DRC hysteresis is set to 3 dB, then if the gain compression in the DRC is inactive, the output of the DAC digital volume control must exceed –9 dBFS before gain compression due to the DRC is activated. Similarly, when the gain compression in the DRC is active, the output of the DAC digital volume control must fall below –15 dBFS for gain compression in the DRC to be deactivated. The DRC hysteresis feature prevents the rapid activation and de-activation of gain compression in the DRC in cases when the output of the DAC digital volume control rapidly fluctuates in a narrow region around the programmed DRC threshold. By programming the DRC hysteresis as 0 dB, the hysteresis action is disabled.

The recommended value of DRC hysteresis is 3 dB.

7.3.10.4.3 DRC Hold Time

DRC hold time is intended to slow the start of decay for a specified period of time in response to a decrease in energy level. To minimize audible artifacts, TI recommends to set the DRC hold time to 0 through programming page 0 / register 69, bits D6–D3 = 0000.

7.3.10.4.4 DRC Attack Rate

When the output of the DAC digital volume control exceeds the programmed DRC threshold, the gain applied in the DAC digital volume control is progressively reduced to avoid the signal from saturating the channel. This process of reducing the applied gain is called *attack*. To avoid audible artifacts, the gain is reduced slowly with a rate equaling the attack rate, programmable via page 0 / register 70, bits D7–D4. Attack rates can be programmed from 4-dB gain change per 1 / DAC_f_S to 1.2207e–5-dB gain change per 1 / DAC_f_S.

Attack rates should be programmed such that before the output of the DAC digital volume control can clip, the input signal should be sufficiently attenuated. High attack rates can cause audible artifacts, and too-slow attack rates may not be able to prevent the input signal from clipping.

The recommended DRC attack rate value is 1.9531e–4 dB per 1 / DAC_f_S.

7.3.10.4.5 DRC Decay Rate

When the DRC detects a reduction in output signal swing beyond the programmed DRC threshold, the DRC enters a decay state, where the applied gain in the digital-volume control is gradually increased to programmed values. To avoid audible artifacts, the gain is slowly increased with a rate equal to the decay rate programmed through page 0 / register 70, bits D3–D0. The decay rates can be programmed from 1.5625e–3 dB per 1 / DAC_f_S to 4.7683e–7 dB per 1 / DAC_f_S. If the decay rates are programmed too fast, then sudden gain changes can cause audible artifacts. However, if it is programmed too slow, then the output may be perceived as too low for a long time after the peak signal has passed.

The recommended value of DRC decay rate is 2.4414e–5 dB per 1 / DAC_f_S.

7.3.10.4.6 Example Setup for DRC

- PGA gain = 12 dB
- Threshold = –24 dB
- Hysteresis = 3 dB
- Hold time = 0 ms
- Attack rate = 1.9531e–4 dB per 1 / DAC_f_S
- Decay rate = 2.4414e–5 dB per 1 / DAC_f_S

Script

```
#Go to Page 0
w 30 00 00
#DAC => 12 db gain left
w 30 41 18
#DAC => 12 db gain right
w 30 42 18
#DAC => DRC Enabled for both channels, Threshold = -24 db, Hysteresis = 3 dB
w 30 44 7F
#DRC Hold = 0 ms, Rate of Changes of Gain = 0.5 dB/Fs'
w 30 45 00
#Attack Rate = 1.9531e-4 dB/Frame , DRC Decay Rate =2.4414e-5 dB/Frame
w 30 46 B6
#Go to Page 9
w 30 00 09
#DRC HPF
w 30 0E 7F AB 80 55 7F 56
#DRC LPF W 30 14 00 11 00 11 7F DE
```

7.3.10.5 Headset Detection

The TLV320AIC3110 device includes extensive capability to monitor a headphone, microphone, or headset jack, to determine if a plug has been inserted into the jack, and then determine what type of headset or headphone is wired to the plug. The device also includes the capability to detect a button press, even, for example, when starting calls on mobile phones with headsets. Figure 7-33 shows the circuit configuration to enable this feature.

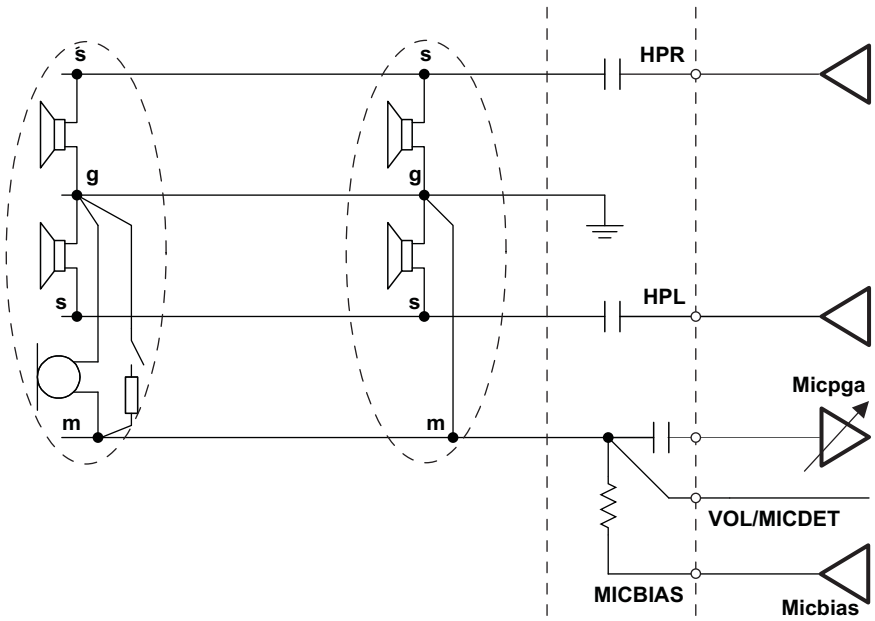


Figure 7-33. Jack Connections for Headset Detection

Headset Detection is enabled by programming page 0 / register 67, bit D1. In order to avoid false detections because of mechanical vibrations in headset jacks or microphone buttons, a debounce function is provided for glitch rejection. For the case of headset insertion, a debounce function with a range of 32 ms to 512 ms is provided. This can be programmed through page 0 / register 67, bits D4–D2. For improved button-press detection, the debounce function has a range of 8 ms to 32 ms by programming page 0 / register 67, bits D1–D0.

The TLV320AIC3110 device also provides feedback to the user when a button press or a headset insertion or removal event is detected through the register-readable flags as well as an interrupt on the I/O pins. The value in page 0 / register 46, bits D5–D4 provides the instantaneous state of button press and headset insertion. Page 0 / register 44, bit D5 is a sticky (latched) flag that is set when the button-press event is detected. Page 0 / register 44, bit D4 is a sticky flag which is set when the headset insertion or removal event is detected. These sticky flags are set by the event occurrence, and are reset only when read. This requires polling page 0 / register 44. To avoid polling and the associated overhead, the TLV320AIC3110 device also provides an interrupt feature, whereby events can trigger the INT1, the INT2, or both interrupts. These interrupt events can be routed to one of the digital output pins. See Section 7.3.10.6 for details.

The TLV320AIC3110 device not only detects a headset insertion event, but also is able to distinguish between the different headsets inserted, such as stereo headphones or cellular headphones. After the headset-detection event, the user can read page 0 / register 67, bits D6–D5 to determine the type of headset inserted.

Table 7-35. Headset Detection Block Registers

REGISTER	DESCRIPTION
Page 0 / register 67, bit D1	Headset-detection enable/disable
Page 0 / register 67, bits D4–D2	Debounce programmability for headset detection
Page 0 / register 67, bits D1–D0	Debounce programmability for button press
Page 0 / register 44, bit D5	Sticky flag for button-press event
Page 0 / register 44, bit D4	Sticky flag for headset-insertion or -removal event
Page 0 / register 46, bit D5	Status flag for button-press event
Page 0 / register 46, bit D4	Status flag for headset insertion and removal
Page 0 / register 67, bits D6–D5	Flags for type of headset detected

The headset detection block requires AVDD to be powered. The headset detection feature in the TLV320AIC3110 device is achieved with very low power overhead, requiring less than 20 µA of additional current from the AVDD supply.

7.3.10.6 Interrupts

Some specific events in the TLV320AIC3110 device that can require host processor intervention are used to trigger interrupts to the host processor. This avoids polling the status-flag registers continuously. The TLV320AIC3110 device has two defined interrupts, INT1 and INT2, that are configured by programming page 0 / register 48 and page 0 / register 49. A user can configure interrupts INT1 and INT2 to be triggered by one or many events, such as:

- Headset detection
- Button press
- DAC DRC signal exceeding threshold
- Noise detected by AGC
- Overcurrent condition in headphone drivers and speaker drivers
- Data overflow in the ADC and DAC processing blocks and filters
- DC measurement data available

Each of these INT1 and INT2 interrupts can be routed to output pins GPIO1 or DOUT. These interrupt signals can either be configured as a single pulse or a series of pulses by programming page 0 / register 48, bit D0 and page 0 / register 49, bit D0. If the user configures the interrupts as a series of pulses, the events trigger the start of pulses that stop when the flag registers in page 0 / registers 44, 45, and 50 are read by the user to determine the cause of the interrupt.

7.3.10.7 Key-Click Functionality With Digital Sine-Wave Generator (PRB_P25)

A special algorithm has been included in the digital signal processing block PRB_P25 for generating a digital sine-wave signal that is sent to the DAC. The digital sine-wave generator is also referred to as the beep generator in this document.

This functionality is intended for generating key-click sounds for user feedback. The sine-wave generator is very flexible (see Table 7-36) and is completely register programmable. Programming page 0 / register 71 through page 0 / register 79 (8 bits each) completely controls the functionality of this generator and allows for differentiating sounds.

The two registers used for programming the 16-bit sine-wave coefficient are page 0 / register 76 and page 0 / register 77. The two registers used for programming the 16-bit cosine-wave coefficient are page 0 / register 78 and page 0 / register 79. This coefficient resolution allows virtually any frequency of sine wave in the audio band to be generated, up to f_S / 2.

The three registers used to control the length of the sine-burst waveform are page 0 / register 73 through page 0 / register 75. The resolution (bit) in the registers of the sine-burst length is one sample time, so this allows great control on the overall time of the sine-burst waveform. This 24-bit length timer supports 16 777 215 sample times. For example, if f_S is set at 48 kHz, and the register value equals 96 000 d (01 7700h), then the sine burst lasts exactly 2 seconds. The default settings for the tone generator, based on using a sample rate of 48 kHz, are 1-kHz (approximately) sine wave, with a sine-burst length of five cycles (5 ms).

Table 7-36. Beep Generator Register Locations (Page 00h)

	LEFT BEEP CONTROL	RIGHT BEEP CONTROL	BEEP LENGTH			SINE		COSINE	
			MSB	MID	LSB	MSB	LSB	MSB	LSB
REGISTER	71	72	73	74	75	76	77	78	79

Table 7-37. Example Beep-Generator Settings for a 1000-Hz Tone

BEEP FREQUENCY	BEEP LENGTH			SINE		COSINE		SAMPLE RATE
Hz	MSB (hex)	MID (hex)	LSB (hex)	MSB (hex)	LSB (hex)	MSB (hex)	LSB (hex)	Hz
1000[1]	0	0	EE	10	D8	7E	E3	48 000

(1) These are the default settings.

Two registers are used to control the left sine-wave volume and the right sine-wave volume independently. The 6-bit digital volume control used allows level control of 2 dB to –61 dB in 1-dB steps. The left-channel volume is controlled by writing to page 0 / register 71, bits D5–D0. The right-channel volume is controlled by writing to page 0, register 72, bits D5–D0. A master volume control that controls the left and right channels of the beep generator are set up by writing to page 0 / register 72, bits D7–D6. The default volume control setting is 2 dB, which provides the maximum tone-generator output level.

For generating other tones, the three tone-generator coefficients are found by running the following script using MATLAB™ :

```
Sine = dec2hex(round(sin(2*π*Fin/Fs)*2^15))
Cosine = dec2hex(round(cos(2*π*Fin/Fs)*2^15))
Beep Length = dec2hex(floor(Fs*Cycle/Fin))
```

where,

Fin = Beep frequency desired
Fs = Sample rate
Cycle = Number of beep (sine wave) cycles that are required
dec2hex = Decimal to hexadecimal conversion function

NOTES:

1. Fin must be less than Fs / 4.
2. For the sine and cosine values, if the number of bits is less than the full 16-bit value, then the unused MSBs must be written as 0s.
3. For the beep-length values, if number of bits is less than the full 24-bit value, then the unused MSBs must be written as 0s.

Following the beep-volume control is a digital mixer that mixes in a playback data stream whose level has already been set by the DAC volume control. Therefore, once the key-click volume level is set, the key-click volume is not affected by the DAC volume control, which is the main control available to the end user. shows this functionality.

Following the DAC, the signal can be further scaled by the analog output volume control and power-amplifier level control.

To insert a beep in the middle of an already-playing signal over DAC, use the following sequence.

Before the beep is desired, program the desired beep frequency, volume, and length in the configuration registers. When a beep is desired, use the example configuration script.

```
w 30 00 00          # change to Page 0
w 30 40 0C          # mute DACs
f  30 26 xxx1xxx1   # wait for DAC gain flag to be set
w 30 0B 02          # power down NDAC divider
w 30 47 80          # enable beep generator with left channel volume = 0dB, volume level could
                    # be different as per requirement
w 30 0B 82          # power up NDAC divider, in this specific example NDAC = 2, but NDAC could
                    # be different value as per overall setup
w 30 40 00          # un-mute DAC to resume playing audio
```

Note that in this scheme the audio signal on the DAC is temporarily muted to enable beep generation. Because powering down of NDAC clock divider is required, do not use the DAC_CLK or DAC_MOD_CLK for generation of I^2S clocks.

7.3.10.8 Programming DAC Digital Filter Coefficients

The digital filter coefficients must be programmed through the I^2C interface. All digital filtering for the DAC signal path must be loaded into the RAM before the DAC is powered on. Note that default ALLPASS filter coefficients for programmable biquads are located in boot ROM. The boot ROM automatically loads the default values into the RAM following a hardware reset (toggling the $\overline{\text{RESET}}$ pin) or after a software reset. After resetting the device, loading boot ROM coefficients into the digital filters requires 100 µs of programming time. During this time, reading or writing to page 8 through page 15 for updating DAC filter coefficient values is not permitted. The DAC should not be powered up until after all of the DAC configurations have been done by the system microprocessor.

7.3.10.9 Updating DAC Digital Filter Coefficients During PLAY

When it is required to update the DAC digital filter coefficients or beep generator during play, care must be taken to avoid click and pop noise or even a possible oscillation noise. These artifacts can occur if the DAC coefficients are updated without following the proper update sequence. The correct sequence is shown in Figure 7-34. The values for times listed in Figure 7-34 are conservative and should be used for software purposes.

There is also an adaptive mode, in which DAC coefficients can be updated while the DAC is on. For details, see Section 7.3.10.1.3.

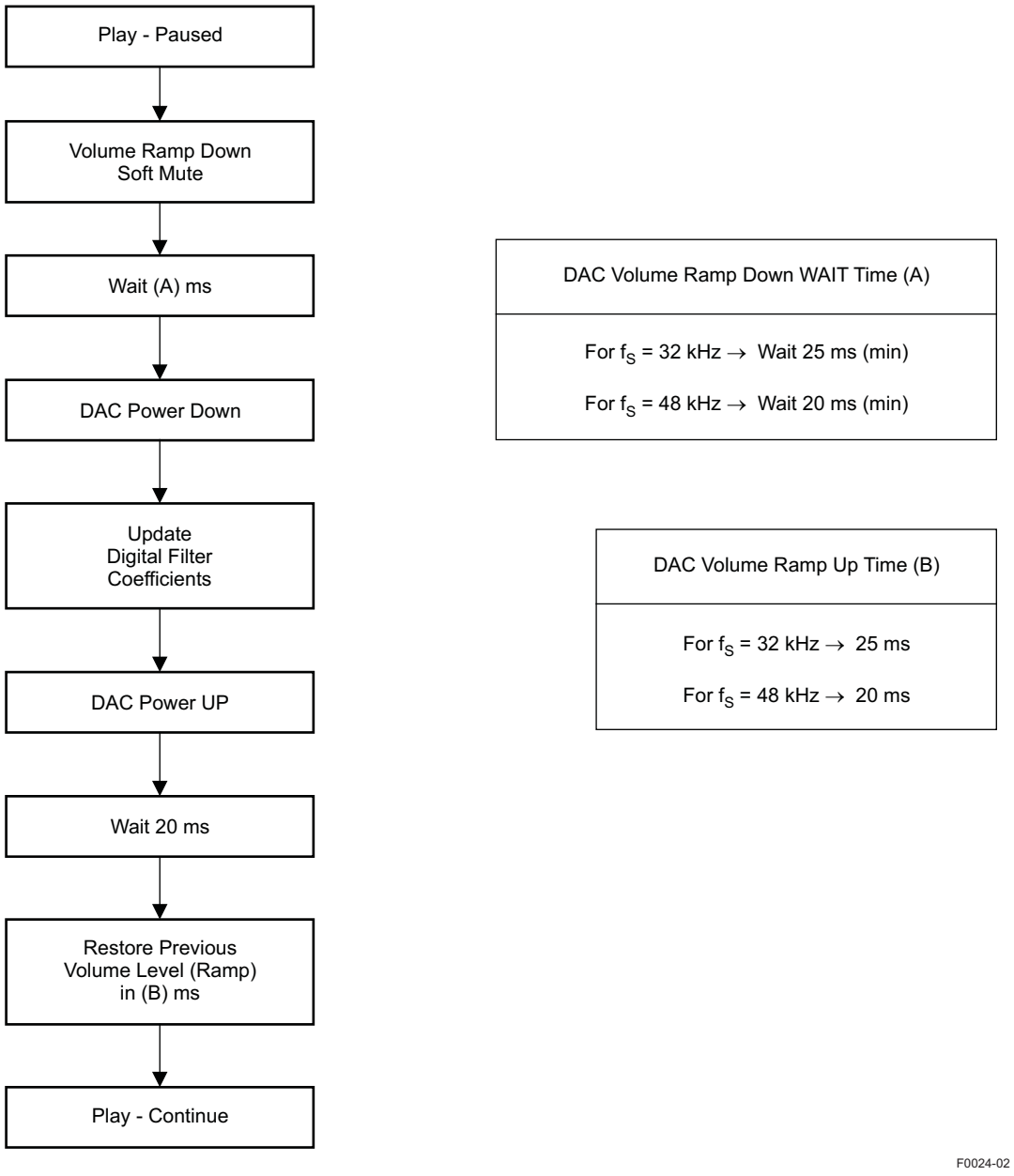


Figure 7-34. Example Flow For Updating DAC Digital Filter Coefficients During Play

7.3.10.10 Digital Mixing and Routing

The TLV320AIC3110 has four digital mixing blocks. Each mixer can provide either mixing or multiplexing of the digital audio data. This arrangement of digital mixers allows independent volume control for both the playback data and the key-click sound. The first set of mixers can be used to make monaural signals from left and right audio data, or they can be used to swap channels to the DAC. This function is accomplished by selecting left audio data for the right DAC input, and right data for the left DAC input. The second set of mixers provides mixing of the audio data stream and the key-click sound. The digital routing can be configured by writing to page 0 / register 63, bits D5–D4 for the left channel and bits D3–D2 for the right channel.

Because the key-click function uses the digital signal processing block, the CODEC_CLKIN, DAC, analog volume control, and output driver must be powered on for the key-click sound to occur.

7.3.10.11 Analog Audio Routing

The TLV320AIC3110 has the capability to route the DAC output to either the headphone or the speaker output. If desirable, both output drivers can operate at the same time while playing at different volume levels. The TLV320AIC3110 provides various digital routing capabilities, allowing digital mixing or even channel swapping in the digital domain. All analog outputs other than the selected ones can be powered down for optimal power consumption.

7.3.10.11.1 Analog Output Volume Control

The output volume control fine tunes the level of the mixer amplifier signal supplied to the headphone driver or the speaker driver. This architecture supports separate and concurrent volume levels for each of the four output drivers. This volume control is also used as part of the output pop-noise reduction scheme. This feature is available even if the ADC and DAC are powered down.

7.3.10.11.2 Headphone Analog-Output Volume Control

For the headphone outputs, the analog volume control has a range from 0 dB to –78 dB in 0.5-dB steps for most of the useful range plus mute, which is shown in Table 7-38. This volume control includes soft-stepping logic. Routing the left-channel DAC output signal to the left-channel analog volume control occurs by writing to page 1 / register 35, bit D6. Routing the right-channel DAC output signal to the right-channel analog volume control occurs by writing to page 1 / register 35, bit D2.

Changing the left-channel analog volume for the headphone is controlled by writing to page 1 / register 36, bits D6–D0. Changing the right-channel analog volume for the headphone is controlled by writing to page 1 / register 37, bits D6–D0. Routing the signal from the output of the left-channel analog volume control to the input of the left-channel headphone power amplifier occurs by writing to page 1 / register 36, bit D7. Routing the signal from the output of the right-channel analog volume control to the input of the right-channel headphone power amplifier occurs by writing to page 1 / register 37, bit D7.

The analog volume-control soft-stepping time is based on the setting in page 0 / register 63, bits D1–D0.

Table 7-38. Analog Volume Control for Headphone and Speaker Outputs (for D7 = 1)(1)

REGISTER VALUE (D6–D0)	ANALOG GAIN (dB)	REGISTER VALUE (D6–D0)	ANALOG GAIN (dB)	REGISTER VALUE (D6–D0)	ANALOG GAIN (dB)	REGISTER VALUE (D6–D0)	ANALOG GAIN (dB)
0	0	30	–15	60	–30.1	90	–45.2
1	–0.5	31	–15.5	61	–30.6	91	–45.8
2	–1	32	–16	62	–31.1	92	–46.2
3	–1.5	33	–16.5	63	–31.6	93	–46.7
4	–2	34	–17	64	–32.1	94	–47.4
5	–2.5	35	–17.5	65	–32.6	95	–47.9
6	–3	36	–18.1	66	–33.1	96	–48.2
7	–3.5	37	–18.6	67	–33.6	97	–48.7
8	–4	38	–19.1	68	–34.1	98	–49.3
9	–4.5	39	–19.6	69	–34.6	99	–50
10	–5	40	–20.1	70	–35.2	100	–50.3
11	–5.5	41	–20.6	71	–35.7	101	–51
12	–6	42	–21.1	72	–36.2	102	–51.4
13	–6.5	43	–21.6	73	–36.7	103	–51.8
14	–7	44	–22.1	74	–37.2	104	–52.2
15	–7.5	45	–22.6	75	–37.7	105	–52.7
16	–8	46	–23.1	76	–38.2	106	–53.7
17	–8.5	47	–23.6	77	–38.7	107	–54.2
18	–9	48	–24.1	78	–39.2	108	–55.3
19	–9.5	49	–24.6	79	–39.7	109	–56.7
20	–10	50	–25.1	80	–40.2	110	–58.3
21	–10.5	51	–25.6	81	–40.7	111	–60.2
22	–11	52	–26.1	82	–41.2	112	–62.7
23	–11.5	53	–26.6	83	–41.7	113	–64.3
24	–12	54	–27.1	84	–42.1	114	–66.2
25	–12.5	55	–27.6	85	–42.7	115	–68.7
26	–13	56	–28.1	86	–43.2	116	–72.2
27	–13.5	57	–28.6	87	–43.8	117–127	–78.3
28	–14	58	–29.1	88	–44.3		
29	–14.5	59	–29.6	89	–44.8		

(1) Mute when D7 = 0 and D6–D0 = 127 (0x7F).

7.3.10.11.3 Class-D Speaker Analog Output Volume Control

For the speaker outputs, the analog volume control has a range from 0 dB to –78 dB in 0.5-dB steps for most of the useful range plus mute, as seen in Table 7-38. The implementation includes soft-stepping logic.

Routing the left-channel DAC output signal to the left-channel analog volume control is done by writing to page 1 / register 35, bit D6. Routing the right-channel DAC output signal to the right-channel analog volume control is done by writing to page 1 / register 35, bit D2. Changing the left-channel analog volume for the speaker is controlled by writing to page 1 / register 38, bits D6–D0. Changing the right-channel analog volume for the speaker is controlled by writing to page 1 / register 39, bits D6–D0.

Routing the signal from the output of the left-channel analog volume control to the input of the left-channel speaker amplifier is done by writing to page 1 / register 38, bit D7. Routing the signal from the output of the right-channel analog volume control to the input of the right-channel speaker amplifier is done by writing to page 1 / register 39, bit D7.

The analog volume-control soft-stepping time is based on the setting in page 0 / register 63, bits D1–D0.

7.3.10.12 Analog Outputs

Various analog routings are supported for playback. All the options can be conveniently viewed on the functional block diagram, .

7.3.10.12.1 Headphone Drivers

The TLV320AIC3110 device features a stereo headphone driver (HPL and HPR) that delivers up to 30 mW per channel, at 3.3-V supply voltage, into a 16-Ω load. The headphones are used in a single-ended configuration where an ac-coupling capacitor (dc-blocking) is connected between the device output pins and the headphones. The headphone driver also supports 32-Ω and 10-kΩ loads without changing any control register settings.

The headphone drivers can be configured to optimize the power consumption in the lineout-drive mode by writing 11 to page 1 / register 44, bits D2–D1.

The output common mode of the headphone and lineout drivers is programmed to 1.35 V, 1.5 V, 1.65 V, or 1.8 V by setting page 1 / register 31, bits D4–D3. Set the common-mode voltage to ≤ AVDD / 2.

The left headphone driver powers on by writing to page 1 / register 31, bit D7. The right headphone driver powers on by writing to page 1 / register 31, bit D6. The left-output driver gain is controlled by writing to page 1 / register 40, bits D6–D3, and it is muted by writing to page 1 / register 40, bit D2. The right-output driver gain is controlled by writing to page 1 / register 41, bits D6–D3, and it is muted by writing to page 1 / register 41, bit D2.

The TLV320AIC3110 device has a short-circuit protection feature for the headphone drivers, which is always enabled to provide protection. The output condition of the headphone driver during short circuit is programmed by writing to page 1 / register 31, bit D1. If D1 = 0 when a short circuit is detected, the device limits the maximum current to the load. If D1 = 1 when a short circuit is detected, the device powers down the output driver. The default condition for headphones is the current-limiting mode. In case of a short circuit on either channel, the output is disabled and a status flag is provided as read-only bits on page 1 / register 31, bit D0. If shutdown mode is enabled, then as soon as the short circuit is detected, page 1 / register 31, bit D7 (for HPL) or page 1 / register 31, bit D6, or both (for HPR) clear automatically. Next, the device requires a reset to re-enable the output stage. Resetting occurs in two ways. First, the device master reset can be used, which requires either toggling the $\overline{\text{RESET}}$ pin or using the software reset. If master reset is used, it resets all of the registers. Second, a dedicated headphone power-stage reset can also be used to re-enable the output stage, and that keeps all of the other device settings. The headphone power stage reset occurs by setting page 1 / register 31, bit D7 for HPL and by setting page 1 / register 31, bit D6 for HPR. If the fault condition has been removed, then the device returns to normal operation. If the fault is still present, then another shutdown occurs. Repeated resetting (more than three times) is not recommended, as this could lead to overheating.

7.3.10.12.2 Speaker Drivers

The TLV320AIC3110 device has an integrated class-D stereo speaker driver (SPLP / SPLM and SPRP / SPRM) capable of driving an 8-Ω differential load. The speaker driver can be powered directly from the battery supply (2.7 V to 5.5 V) on the SPLVDD and SPRVDD pins; however, the voltage (including spike voltage) must be limited below the absolute-maximum voltage of 6 V.

The speaker driver is capable of supplying 400 mW per channel with a 3.6-V power supply. Through the use of digital mixing, the device can connect one or both digital-audio playback data-channels to either speaker driver which also allows for digital channel swapping if needed.

The left class-D speaker driver can be powered on by writing to page 1 / register 32, bit D7. The right class-D speaker driver can be powered on by writing to page 1 / register 32, bit D6. The left-output driver gain can be controlled by writing to page 1 / register 42, bits D4–D3, and it can be muted by writing to page 1 / register 42, bit D2. The right-output driver gain can be controlled by writing to page 1 / register 43, bits D4–D3, and it can be muted by writing to page 1 / register 43, bit D2.

The TLV320AIC3110 device has a short-circuit protection feature for the speaker drivers that is always enabled to provide protection. If the output is shorted, the output stage shuts down on the overcurrent condition. (Current limiting is not an available option for the higher-current speaker driver output stage.) In case of a short circuit on either channel, the output is disabled and a status flag is provided as a read-only bit on page 1 / register 32, bit D0.

If shutdown occurs because of an overcurrent condition, then the device requires a reset to re-enable the output stage. Resetting occurs in two ways. First, the device master reset can be used, which requires either toggling the $\overline{\text{RESET}}$ pin or using the software reset. If master reset is used, it resets all of the registers. Second, a dedicated speaker power-stage reset can be used that keeps all of the other device settings. The speaker power-stage reset occurs by setting page 1 / register 32, bit D7 for SPLP and SPLM and by setting page 1 / register 32, bit D6 for SPRP and SPRM. If the fault condition has been removed, then the device returns to normal operation. If the fault is still present, then another shutdown occurs. Repeated resetting (more than three times) is not recommended as this could lead to overheating.

To minimize battery current leakage, the SPLVDD and SPRVDD voltage levels must not be less than the AVDD voltage level.

The TLV320AIC3110 device has a thermal protection (OTP) feature for the speaker drivers which is always enabled to provide protection. If the device overheats, then the output stops switching. When the device cools down, the device resumes switching. An overtemperature status flag is provided as a read-only bit on page 0 / register 3, bit D1. The OTP feature is for self-protection of the device. If die temperature can be controlled at the system or board level, then overtemperature does not occur.

7.3.10.13 Audio-Output Stage-Power Configurations

After the device has been configured (following a $\overline{\text{RESET}}$) and the circuitry has been powered up, the audio output stage can be powered up and powered down by register control.

These functions soft-start automatically. By using these register controls, controlling all four output stages independently is possible.

See Table 7-39 for register control of audio output stage power configurations.

Table 7-39. Audio-Output Stage-Power Configurations

AUDIO OUTPUT PINS	DESIRED FUNCTION	PAGE 1 / REGISTER, BIT VALUES
HPL	Power down HPL driver	Page 1 / register 31, bit D7 = 0
	Power up HPL driver	Page 1 / register 31, bit D7 = 1
HPR	Power down HPR driver	Page 1 / register 31, bit D6 = 0
	Power up HPR driver	Page 1 / register 31, bit D6 = 1
SPLP / SPLM	Power down left class-D drivers	Page 1 / register 32, bit D7 = 0
	Power up left class-D drivers	Page 1 / register 32, bit D7 = 1
SPRP / SPRM	Power down right class-D drivers	Page 1 / register 32, bit D6 = 0
	Power up right class-D drivers	Page 1 / register 32, bit D6 = 1

7.3.10.14 Example Register Setup to Play Digital Data Through DAC and Headphone/Speaker Outputs

A typical EVM I^2C register control script follows to show how to set up the TLV320AIC3110 in playback mode with f_S = 44.1 kHz and MCLK = 11.2896 MHz.

```
# I2C Script to Setup TLV320AIC3110 in Playback Mode
# Key: w 30 XX YY ==> write to I2C address 0x30, to register 0xXX, data 0xYY
#               # ==> comment delimiter
#
# Select Page 0
w 30 00 00
# Software reset
w 30 01 01
# PLL_clkin = MCLK, codec_clkin = PLL_CLK
w 30 04 03
```

```
# PLL Power up, P = 1, R = 1
w 30 05 91
# J = 8
w 30 06 08
# D = 0000, D(13:8) = 0, D(7:0) = 0
w 30 07 00 00
# Mode is I2S, Wordlength is 16
w 30 1B 00
# NDAC is powered up and set to 4
w 30 0B 84
# MDAC is powered up and set to 4
w 30 0C 84
# DOSR = 128, DOSR(9:8) = 0, DOSR(7:0) = 128
w 30 0D 00 80
# DAC => volume control thru pin disable
w 30 74 00
# DAC => DRC disable,
w 30 44 00
# DAC => -22 db gain left
w 30 41 D4
# DAC => -22 db gain right
w 30 42 D4
# Select Page 1
w 30 00 01
# De-pop, Power on = 800 ms, Step time = 4 ms
w 30 21 4E
# HPL and HPR powered up
w 30 1F C2
# LDAC routed to HPL, RDAC routed to HPR
w 30 23 44
# HPL unmute and gain = 0db
w 30 28 06
# HPR unmute and gain = 0db
w 30 29 06
# Unmute Class-D Left
w 30 2A 1C
# Unmute Class-D Right
w 30 2B 1C
# Power-up Class-D drivers
w 30 20 C6
# Enable HPL output analog volume, set = -9 dB
w 30 24 92
# Enable HPR output analog volume, set = -9 dB
w 30 25 92
# Enable HPL output analog volume, set = -9 dB
w 30 26 92
# Enable HPR output analog volume, set = -9 dB
w 30 27 92
# Select Page 0
w 30 00 00
# Select DAC DSP Processing Block PRB_P11
w 30 3C 0B
w 30 00 08
w 30 01 04
w 30 00 00
# Powerup DAC left and right channels (soft step disable)
w 30 3F D6
# Unmute DAC left and right channels
w 30 40 00
```

7.3.11 CLOCK Generation and PLL

The TLV320AIC3110 device supports a wide range of options for generating clocks for the ADC and DAC sections as well as interface and other control blocks as shown in Figure 7-35. The clocks for the ADC and DAC require a source reference clock. This clock is provided on a variety of device pins, such as the MCLK, BCLK, or GPIO1 pins. The source reference clock for the codec is chosen by programming the CODEC_CLKIN value on page 0 / register 4, bits D1–D0. The CODEC_CLKIN is then routed through highly-flexible clock dividers shown in Figure 7-35 to generate the various clocks required for the DAC,

and digital processing sections. In the event that the desired audio clocks cannot be generated from the reference clocks on MCLK, BCLK, or GPIO1, the TLV320AIC3110 device also provides the option of using the on-chip PLL which supports a wide range of fractional multiplication values to generate the required clocks. Starting from CODEC_CLKIN, the TLV320AIC3110 device provides several programmable clock dividers to help achieve a variety of sampling rates for the ADC, DAC.

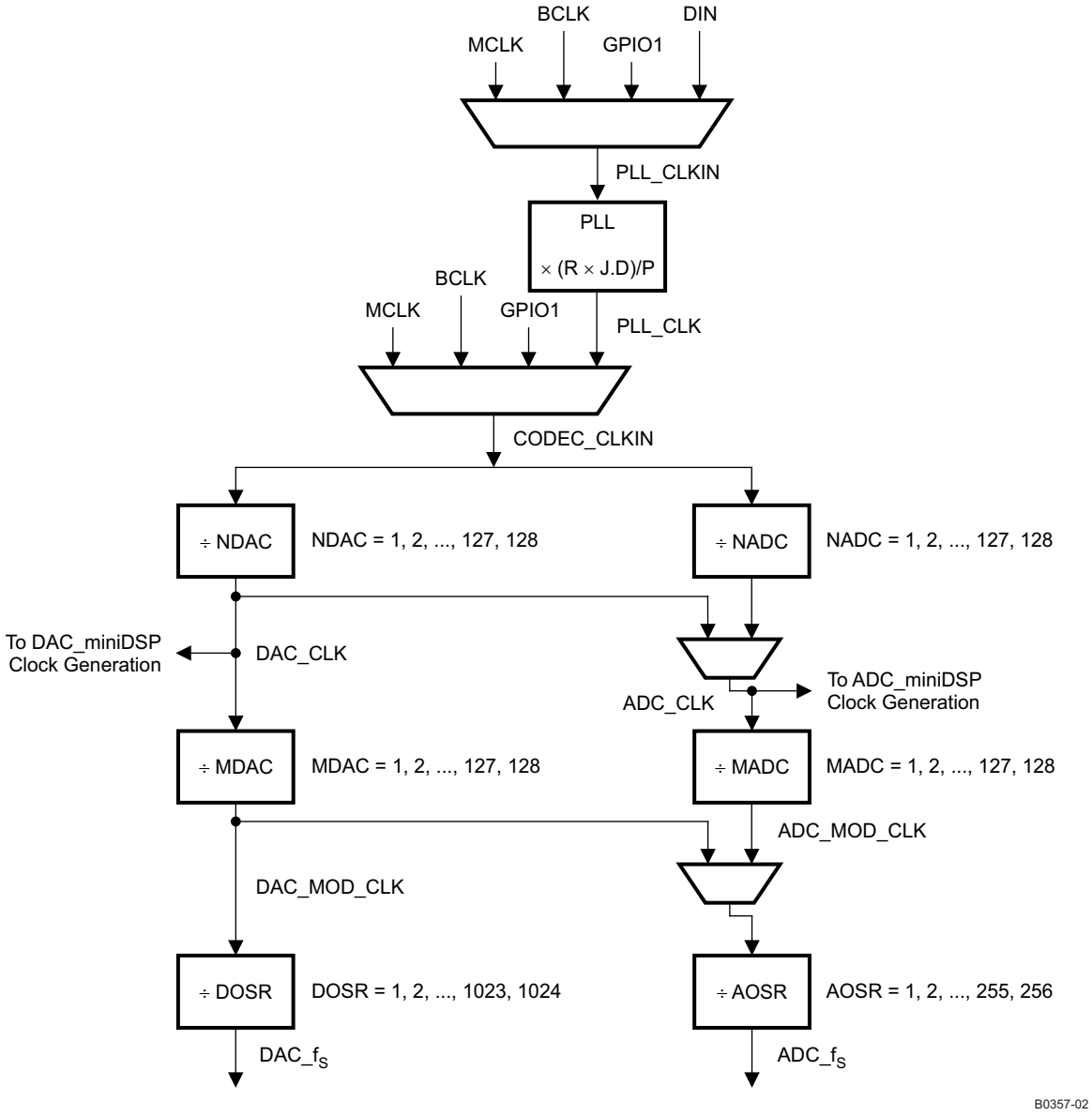


Figure 7-35. Clock Distribution Tree

$$DAC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NDAC \times MDAC} \qquad ADC\_MOD\_CLK = \frac{CODEC\_CLKIN}{NADC \times MADC}$$

$$DAC\_f_S = \frac{CODEC\_CLKIN}{NDAC \times MDAC \times DOSR} \qquad ADC\_f_S = \frac{CODEC\_CLKIN}{NADC \times MADC \times AOSR} \quad (8)$$

Table 7-40. CODEC CLKIN Clock Dividers

DIVIDER	BITS
NDAC	Page 0 / register 11, bits D6–D0
MDAC	Page 0 / register 12, bits D6–D0
DOSR	Page 0 / register 13, bits D1–D0 and page 0 / register 14, bits D7–D0
NADC	Page 0 / register 18, bits D6–D0
MADC	Page 0 / register 19, bits D6–D0
AOSR	Page 0 / register 20, bits D7–D0

The DAC modulator is clocked by DAC_MOD_CLK. For proper power-up operation of the DAC channel, these clocks must be enabled by configuring the NDAC and MDAC clock dividers (page 0 / register 11, bit D7 = 1 and page 0 / register 12, bit D7 = 1). When the DAC channel is powered down, the device internally initiates a power-down sequence for proper shutdown. During this shutdown sequence, the NDAC and MDAC dividers must not be powered down, or else a proper low-power shutdown may not take place. The user can read back the power-status flag at page 0 / register 37, bit D7 and page 0 / register 37, bit D3. When both of the flags indicate power-down, the MDAC divider may be powered down, followed by the NDAC divider. Note that when the ADC clock dividers are powered down, the ADC clock is derived from the DAC clocks.

The ADC modulator is clocked by ADC_MOD_CLK. For proper power-up of the ADC channel, these clocks are enabled by the NADC and MADC clock dividers (page 0 / register 18, bit D7 = 1 and page 0 / register 19, bit D7 = 1). When the ADC channel is powered down, the device internally initiates a power-down sequence for proper shutdown. During this shutdown sequence, the NADC and MADC dividers must not be powered down, or else a proper low-power shutdown may not take place. The user can read back the power-status flag from page 0 / register 36, bit D6. When this flag indicates power down, the MADC divider may be powered down, followed by NADC divider.

When ADC_CLK (ADC processing clock) is derived from the NDAC divider output, the NDAC must be kept powered up until the power-down status flags for ADC do not indicate power down. When the input to the AOSR clock divider is derived from DAC_MOD_CLK, then MDAC must be powered up when ADC_f_S is needed (for example, when WCLK is generated by the TLV320AIC3110 device or AGC is enabled) and can be powered down only after the ADC power-down flags indicate power-down status.

In general, for proper operation, all the root clock dividers must power down only after the child clock dividers have powered down.

The TLV320AIC3110 device also has options for routing some of the internal clocks to the output pins of the device to be used as general-purpose clocks in the system. The feature is shown in Figure 7-37.

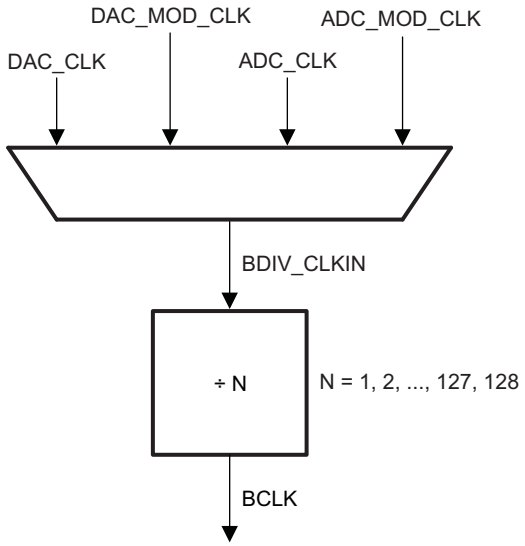


Figure 7-36. BCLK Output Options

In the mode when the TLV320AIC3110 device is configured to drive the BCLK pin (page 0 / register 27, bit D3 = 1), the device is driven as the divided value of BDIV_CLKIN. The division value is programmed in page 0 / register 30, bits D6–D0 from 1 to 128. The BDIV_CLKIN is configurable to be one of DAC_CLK (DAC processing clock), DAC_MOD_CLK, ADC_CLK (ADC DSP clock) or ADC_MOD_CLK by configuring the BDIV_CLKIN multiplexer in page 0 / register 29, bits D1–D0. Additionally, a general-purpose clock can be driven out on either GPIO1 or DOUT.

This clock can be a divided-down version of CDIV_CLKIN. The value of this clock divider can be programmed from 1 to 128 by writing to page 0 / register 26, bits D6–D0. CDIV_CLKIN can also be programmed as one of the clocks among the list shown in Figure 7-37. This is controlled by programming the multiplexer in page 0 / register 25, bits D2–D0.

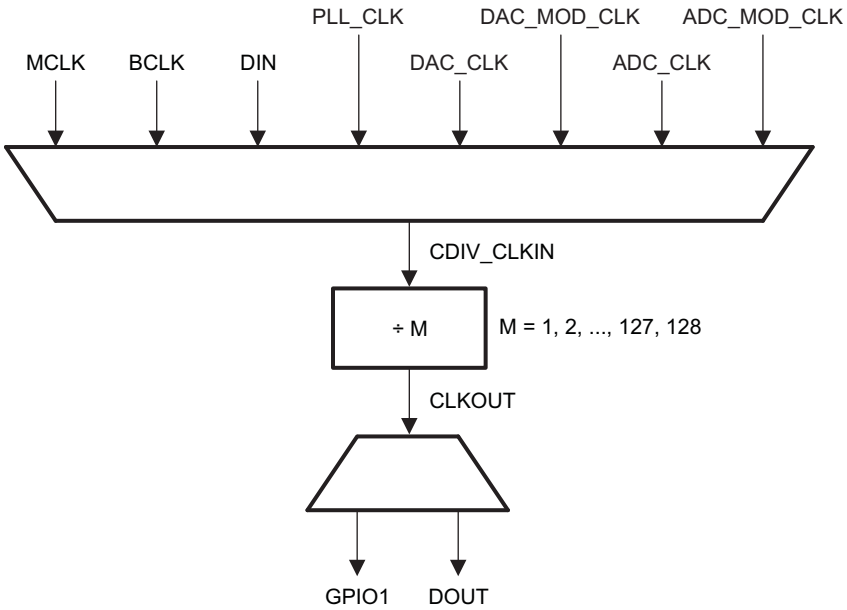


Figure 7-37. General-Purpose Clock Output Options

Table 7-41. Maximum TLV320AIC3110 Clock Frequencies

CLOCK	DVDD ≥ 1.65 V
CODEC_CLKIN	≤ 110 MHz
ADC_CLK (ADC processing clock)	≤ 49.152 MHz
ADC_PRB_CLK	≤ 24.576 MHz
ADC_MOD_CLK	6.758 MHz
ADC_f_S	0.192 MHz
DAC_CLK (DAC processing clock)	≤ 49.152 MHz
DAC_PRB_CLK	≤ 49.152 MHz with DRC disabled ≤ 48 MHz with DRC enabled
DAC_MOD_CLK	6.758 MHz
DAC_f_S	0.192 MHz
BDIV_CLKIN	55 MHz
CDIV_CLKIN	100 MHz when M is odd 110 MHz when M is even

7.3.11.1 PLL

For lower power consumption, the best process is to derive the internal audio processing clocks using the simple dividers. When the input MCLK or other source clock is not an integer multiple of the audio processing clocks then using the on-board PLL is necessary. The TLV320AIC3110 fractional PLL generates an internal *master clock* that produces the processing clocks required by the ADC, DAC, and digital processing blocks. The programmability of this PLL allows operation from a wide variety of clocks that may be available in the system.

The PLL input supports clocks varying from 512 kHz to 20 MHz and is register-programmable to enable generation of the required sampling rates with fine resolution. The PLL turns on by writing to page 0 / register 5, bit D7. When the PLL is enabled, the PLL output clock, PLL_CLK, is given by Equation 9.

$$PLL\_CLK = \frac{PLL\_CLKIN \times R \times J.D}{P} \quad (9)$$

where

- R = 1, 2, 3, ..., 16 (page 0 / register 5, default value = 1)
- J = 1, 2,3, … , 63, (page 0 / register 6, default value = 4)
- D = 0, 1, 2, …, 9999 (page 0 / register 7 and page 0 / register 8, default value = 0)
- P = 1, 2, 3, …, 8 (page 0 / register 5, default value = 1)

The PLL turns on through page 0 / register 5, bit D7. The variable P is programmed through page 0 / register 5, bits D6–D4. The variable R is programmed through page 0 / register 5, bits D3–D0. The variable J is programmed through page 0 / register 6, bits D5–D0. The variable D is 14 bits and is programmed into two registers. The MSB portion is programmed through page 0 / register 7, bits D5–D0, and the LSB portion is programmed thrugh page 0 / register 8, bits D7–D0. For proper update of the D-divider value, page 0 / register 7 must be programmed first, followed immediately by page 0 / register 8. The new value of D does not take effect unless the write to page 0 / register 8 is complete.

When the PLL is enabled, the following conditions must be satisfied:

- When the PLL is enabled and D = 0, the following conditions must be satisfied for PLL_CLKIN:

$$512\ kHz \le \frac{PLL\_CLKIN}{P} \le 20\ MHz \quad (10)$$

$$80\ MHz \le (PLL\_CLKIN \times J.D. \times R / P) \le 110\ MHz$$

$$4 \le R \times J \le 259$$

- When the PLL is enabled and D ≠ 0, the following conditions must be satisfied for PLL_CLKIN:

$$10\ \text{MHz} \le \frac{\text{PLL\_CLKIN}}{P} \le 20\ \text{MHz}$$
$$80\ \text{MHz} \le \text{PLL\_CLKIN} \times \text{J.D.} \times R / P \le 110\ \text{MHz} \quad (11)$$

$$R = 1$$

The PLL can power up independently from the ADC and DAC blocks, and can also be used as a general-purpose PLL by routing the PLL output to the GPIO output. After powering up the PLL, PLL_CLK is available typically after 10 ms.

The clocks for the codec and various signal processing blocks, CODEC_CLKIN, are generated from the MCLK input, BCLK input, GPIO input, or PLL_CLK (page 0 / register 4, bits D1–D0).

If CODEC_CLKIN is derived from the PLL, then the PLL must be powered up first and powered down last.

Table 7-42 lists several example cases of typical PLL_CLKIN rates and how to program the PLL to achieve a sample rate f_S of either 44.1 kHz or 48 kHz.

Table 7-42. PLL Example Configurations

PLL_CLKIN (MHz)	PLLP	PLLR	PLLJ	PLLD	MADC	NADC	AOSR	MDAC	NDAC	DOSR
f_S = 44.1 kHz										
2.8224	1	3	10	0	3	5	128	3	5	128
5.6448	1	3	5	0	3	5	128	3	5	128
12	1	1	7	560	3	5	128	3	5	128
13	1	1	6	3504	2	9	104	6	3	104
16	1	1	5	2920	3	5	128	3	5	128
19.2	1	1	4	4100	3	5	128	3	5	128
48	4	1	7	560	3	5	128	3	5	128
f_S = 48 kHz										
2.048	1	3	14	0	2	7	128	7	2	128
3.072	1	4	7	0	2	7	128	7	2	128
4.096	1	3	7	0	2	7	128	7	2	128
6.144	1	2	7	0	2	7	128	7	2	128
8.192	1	4	3	0	2	8	128	4	4	128
12	1	1	7	1680	2	7	128	7	2	128
16	1	1	5	3760	2	7	128	7	2	128
19.2	1	1	4	4800	2	7	128	7	2	128
48	4	1	7	1680	2	7	128	7	2	128

7.3.12 Timer

The internal clock runs nominally at 8.2 MHz. This is used for various internal timing intervals, de-bounce logic, and interrupts. The MCLK divider must be set in such a way that the divider output is approximately 1 MHz for the timers to be closer to the programmed value.

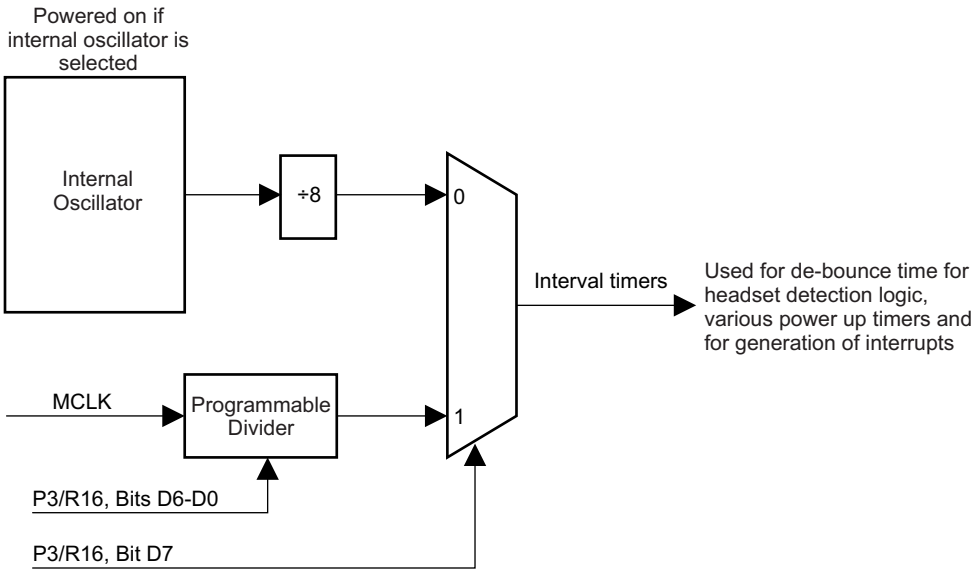


Figure 7-38. Interval Timer Clock Selection

7.3.13 Digital Audio and Control Interface

7.3.13.1 Digital Audio Interface

Audio data is transferred between the host processor and the TLV320AIC3110 device through the digital audio data, serial interface, or audio bus. The audio bus on this device is very flexible, including left- or right-justified data options, support for I^2S or DSP protocols, programmable data length options, a TDM mode for multichannel operation, very flexible master and slave configurability for each bus-clock line, and the ability to communicate with multiple devices within a system directly.

The audio bus of the TLV320AIC3110 device can be configured for left-justified or right-justified, I^2S, DSP, or TDM modes of operation, where communication with standard telephony interfaces is supported within the TDM mode. These modes are all MSB-first, with data width programmable as 16, 20, 24, or 32 bits by configuring page 0 / register 27, bits D5–D4. In addition, the word clock and bit clock can be independently configured in either master or slave mode, for flexible connectivity to a wide variety of processors. The word clock defines the beginning of a frame, and can be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC and DAC sampling frequencies.

The bit clock is used to clock-in and clock-out the digital audio data across the serial bus. When in master mode, this signal can be programmed to generate variable clock pulses by controlling the bit-clock divider in page 0 / register 30 (see Figure 7-35). The number of bit-clock pulses in a frame can require adjustment to accommodate various word lengths as well as to support the case when multiple TLV320AIC3110s share the same audio bus.

The TLV320AIC3110 device also includes a feature to offset the position of start-of-data transfer with respect to the word clock. This offset is controlled in terms of number of bit-clocks and can be programmed in page 0 / register 28.

The TLV320AIC3110 device also has the feature of inverting the polarity of the bit clock used for transferring the audio data as compared to the default clock polarity used. This feature can be used independently of the mode of audio interface chosen. This can be configured through page 0 / register 29, bit D3.

The TLV320AIC3110 device further includes programmability (page 0 / register 27, bit D0) to place the DOUT line in the high-impedance state during all bit clocks when valid data is not being sent. By combining this capability with the ability to program at what bit clock in a frame the audio data begins, time-division multiplexing (TDM) is accomplished, enabling the use of multiple codecs on a single audio serial data bus. When the audio serial data bus is powered down while configured in master mode, the pins associated with the interface are put into a high-impedance output condition.

By default, when the word clocks and bit clocks are generated by the TLV320AIC3110 device, these clocks are active only when the codecs (ADC, DAC or both) are powered up within the device. This is done to save power. However, it also supports a feature when both the word clocks and bit clocks can be active even when the codec in the device is powered down. This is useful when using the TDM mode with multiple codecs on the same bus, or when word clocks or bit clocks are used in the system as general-purpose clocks.

7.3.13.1.1 Right-Justified Mode

The audio interface of the TLV320AIC3110 can enter the right-justified mode by programming page 0 / register 27, bits D7–D6 = 10. In right-justified mode, the LSB of the left channel is valid on the rising edge of the bit clock preceding the falling edge of the word clock. Similarly, the LSB of the right channel is valid on the rising edge of the bit clock preceding the rising edge of the word clock.

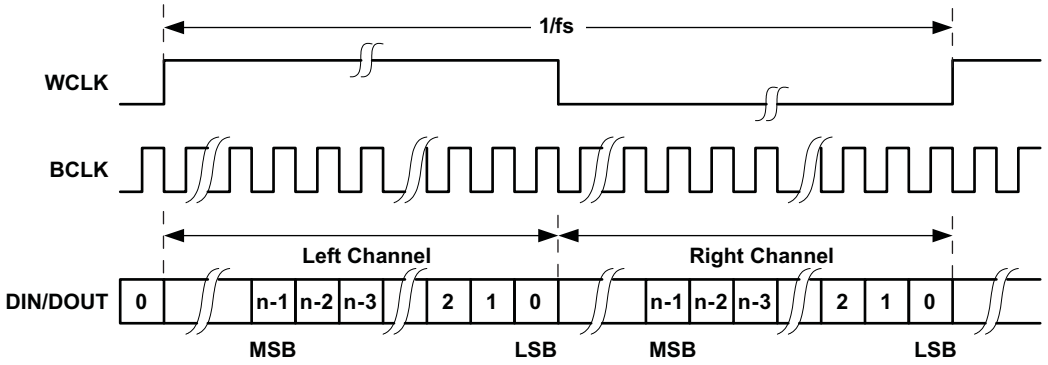


Figure 7-39. Timing Diagram for Right-Justified Mode

For the right-justified mode, the number of bit clocks per frame should be greater-than or equal-to twice the programmed word length of the data.

7.3.13.1.2 Left-Justified Mode

The audio interface of the TLV320AIC3110 can enter the left-justified mode by programming page 0 / register 27, bits D7–D6 = 11. In left-justified mode, the MSB of the right channel is valid on the rising edge of the bit clock following the falling edge of the word clock. Similarly, the MSB of the left channel is valid on the rising edge of the bit clock following the rising edge of the word clock.

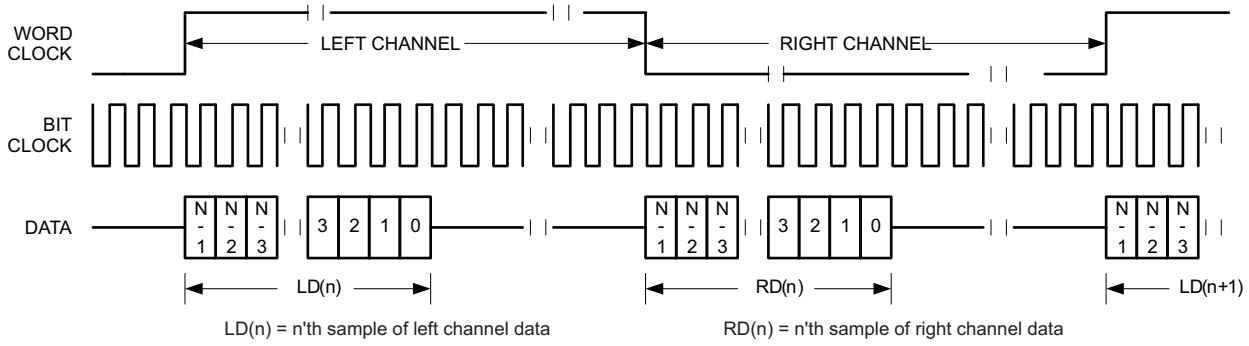


Figure 7-40. Timing Diagram for Left-Justified Mode

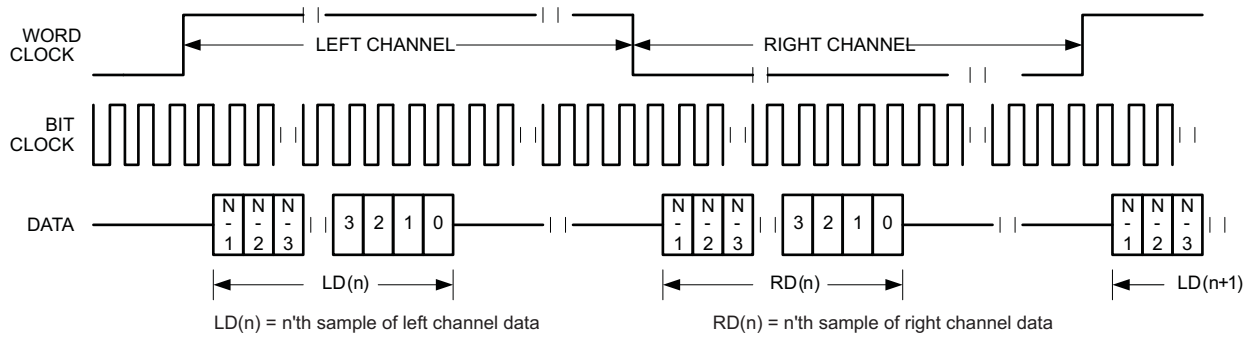


Figure 7-41. Timing Diagram for Left-Justified Mode With Offset = 1

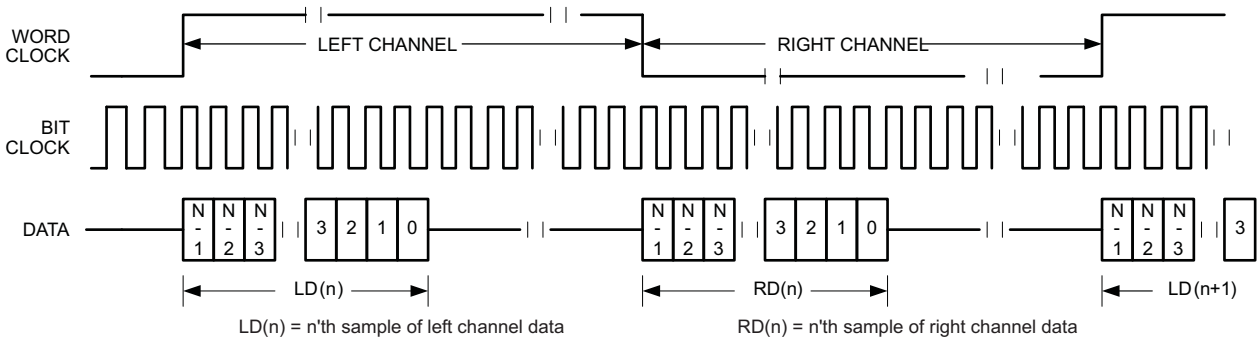


Figure 7-42. Timing Diagram for Left-Justified Mode With Offset = 0 and Inverted Bit Clock

For the left-justified mode, the number of bit clocks per frame should be greater-than or equal-to twice the programmed word length of the data. Also, the programmed offset value should be less than the number of bit clocks per frame by at least the programmed word length of the data.

7.3.13.1.3 I^2S Mode

The audio interface of the TLV320AIC3110 device enters I^2S mode by programming page 0 / register 27, bits D7–D6 = to 00. In I^2S mode, the MSB of the left channel is valid on the second rising edge of the bit clock after the falling edge of the word clock. Similarly, the MSB of the right channel is valid on the second rising edge of the bit clock after the rising edge of the word clock.

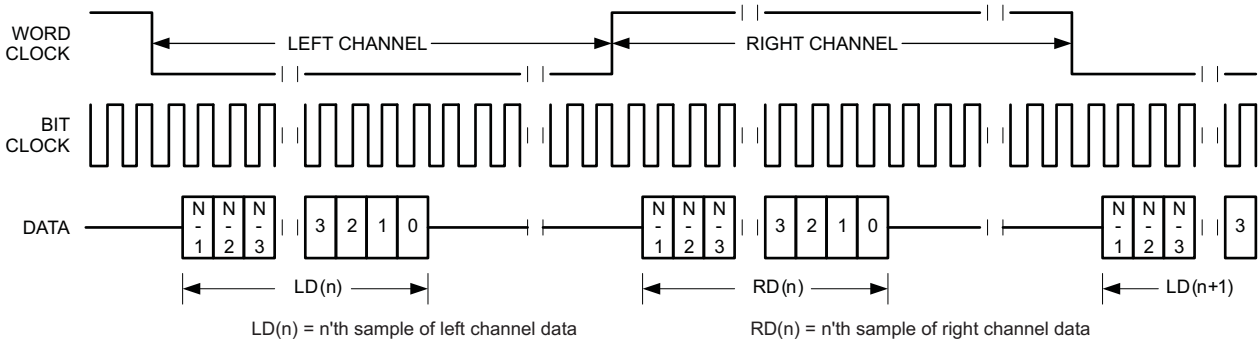


Figure 7-43. Timing Diagram for I^2S Mode

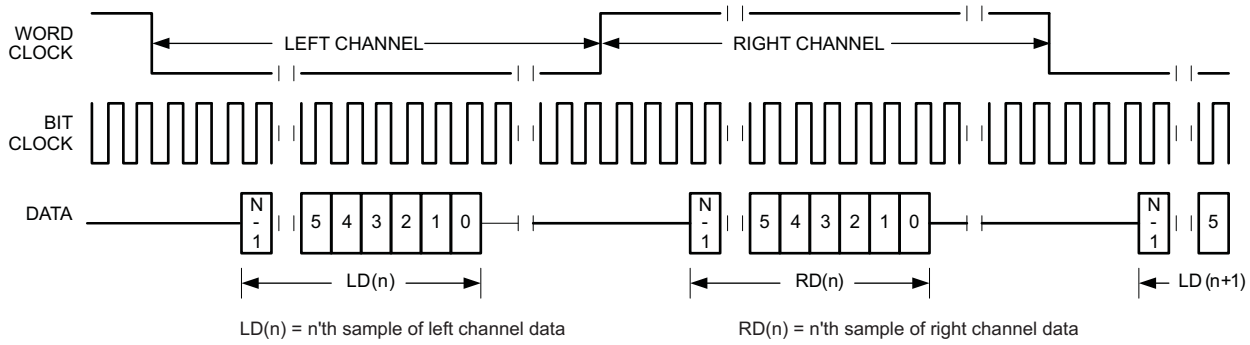


Figure 7-44. Timing Diagram for I²S Mode With Offset = 2

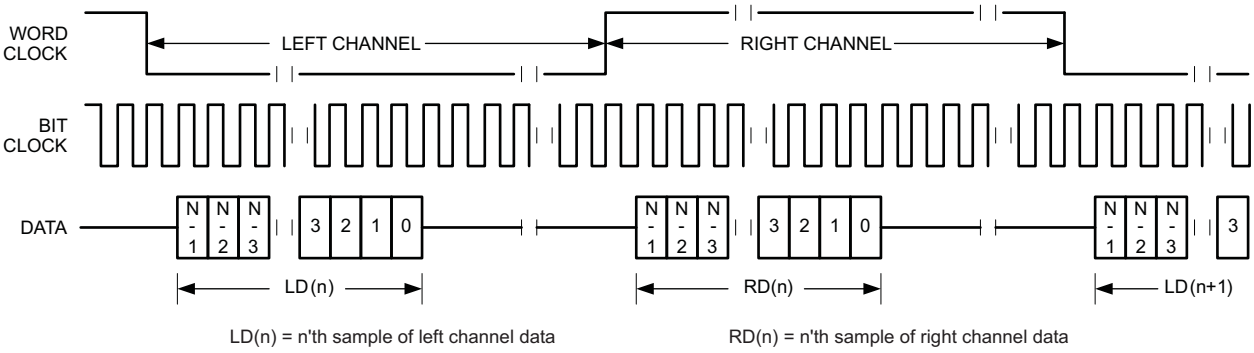


Figure 7-45. Timing Diagram for I²S Mode With Offset = 0 and Bit Clock Inverted

For I²S mode, the number of bit clocks per channel should be greater-than or equal-to the programmed word length of the data. Also, the programmed offset value should be less than the number of bit clocks per frame by at least the programmed word length of the data.

Figure 7-46 shows the timing diagram for I²S mode for the monaural audio ADC.

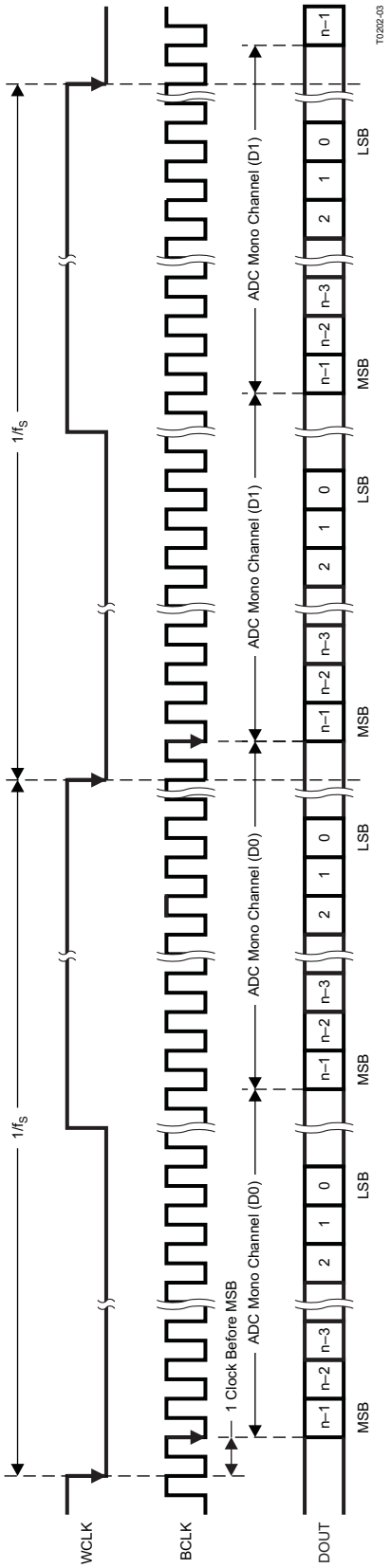


Figure 7-46. Timing Diagram for I²S Mode for Monaural Audio ADC

7.3.13.1.4 DSP Mode

The audio interface of the TLV320AIC3110 can enter DSP mode by programming page 0 / register 27, bits D7–D6 = 01. In DSP mode, the falling edge of the word clock starts the data transfer with the left-channel data first and immediately followed by the right-channel data. Each data bit is valid on the falling edge of the bit clock.

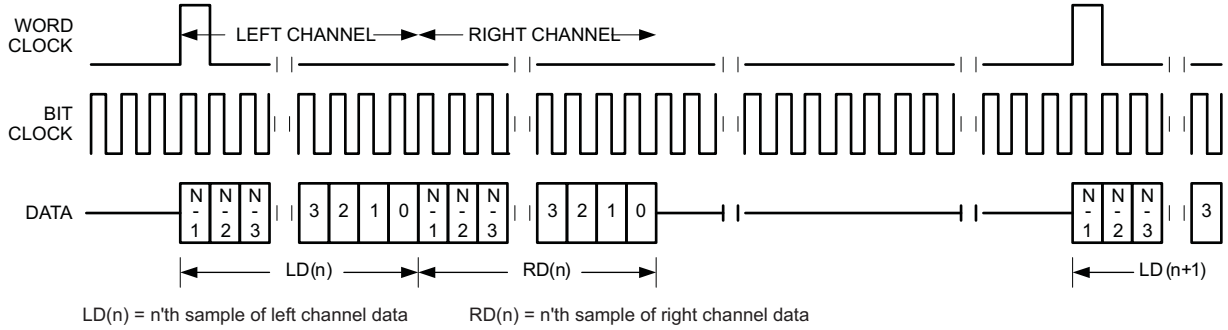


Figure 7-47. Timing Diagram for DSP Mode

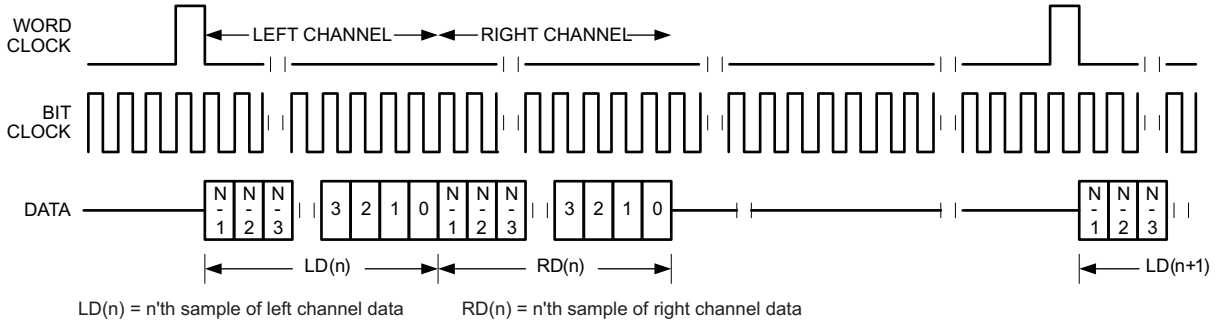


Figure 7-48. Timing Diagram for DSP Mode With Offset = 1

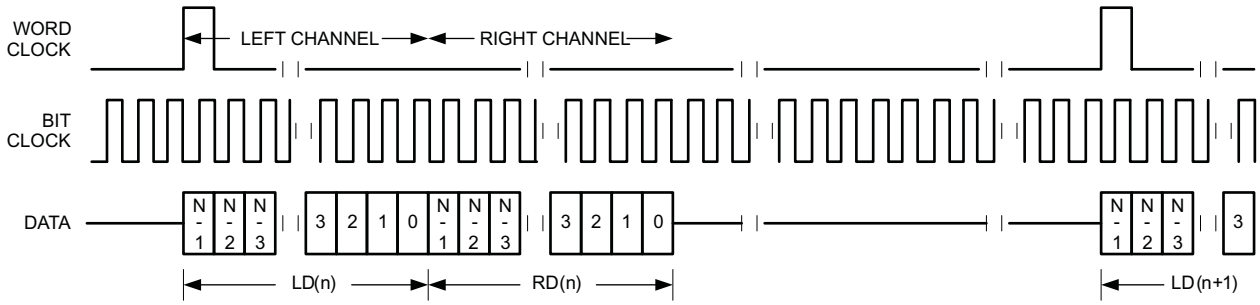


Figure 7-49. Timing Diagram for DSP Mode With Offset = 0 and Bit Clock Inverted

For the DSP mode, the number of bit clocks per frame should be greater-than or equal-to twice the programmed word length of the data. Also, the programmed offset value should be less than the number of bit clocks per frame by at least the programmed word length of the data.

7.3.13.2 Primary and Secondary Digital Audio Interface Selection

The audio serial interface on the TLV320AIC3110 has extensive I/O control to allow communication with two independent processors for audio data. The processors can communicate with the device one at a time. This feature is enabled by register programming of the various pin selections. Table 7-43 shows the primary and secondary audio interface selection and registers. Table 7-44 shows the selection criteria for generating ADC_WCLK. Figure 7-50 is a high-level diagram showing the general signal flow and multiplexing for the primary and secondary audio interfaces. For detailed information, see Table 7-43, Table 7-44, and the register definitions in .

Table 7-43. Primary and Secondary Audio Interface Selection

DESIRED PIN FUNCTION	POSSIBLE PINS	PAGE 0 REGISTERS	COMMENT
Primary WCLK (OUT)	WCLK	R27/D2 = 1	Primary WCLK is output from codec
		R33/D5–D4	Select source of primary WCLK (DAC_fs, ADC_fs, or secondary WCLK)
Primary WCLK (IN)	WCLK	R27/D2 = 0	Primary WCLK is input to codec
Primary BCLK (OUT)	BCLK	R27/D3 = 1	Primary BCLK is output from codec
		R33/D7	Select source of primary WCLK (internal BCLK or secondary BCLK)
Primary BCLK (IN)	BCLK	R27/D3 = 0	Primary BCLK is input to codec
Primary DIN (IN)	DIN	R32/D0	Select DIN to internal interface (0 = primary DIN; 1 = secondary DIN)
Primary DOUT (OUT)	DOUT	R53/D3–D1 = 001	DOUT = primary DOUT for codec interface
		R33/D1	Select source for DOUT (0 = DOUT from interface block; 1 = secondary DIN)
Secondary WCLK (OUT)	GPIO1	R31/D4–D2 = 000	Secondary WCLK obtained from GPIO1 pin
		R51/D5–D2 = 1001	GPIO1 = secondary WCLK output
		R33/D3–D2	Select source of secondary WCLK (DAC_fs, ADC_fs, or primary WCLK)
	DOUT	R31/D4–D2 = 011	Secondary WCLK obtained from DOUT pin
		R53/D3–D1 = 111	DOUT = secondary WCLK output
		R33/D3–D2	Select source of secondary WCLK (DAC_fs, ADC_fs, or primary WCLK)
Secondary WCLK (IN)	GPIO1	R31/D4–D2 = 000	Secondary WCLK obtained from GPIO1 pin
		R51/D5–D2 = 0001	GPIO1 enabled as secondary input
Secondary BCLK (OUT)	GPIO1	R31/D7–D5 = 000	Secondary BCLK obtained from GPIO1 pin
		R51/D5–D2 = 1000	GPIO1 = secondary BCLK output
		R33/D6	Select source of secondary BCLK (primary BCLK or internal BCLK)
	DOUT	R31/D7–D5 = 011	Secondary BCLK obtained from DOUT pin
		R53/D3–D1 = 110	DOUT = secondary BCLK output
		R33/D6	Select source of secondary BCLK (primary BCLK or internal BCLK)
Secondary BCLK (IN)	GPIO1	R31/D7–D5 = 000	Secondary BCLK obtained from GPIO1 pin
		R51/D5–D2 = 0001	GPIO1 enabled as secondary input
Secondary DIN (IN)	GPIO1	R31/D1–D0 = 00	Secondary DIN obtained from GPIO1 pin
		R51/D5–D2 = 0001	GPIO1 enabled as secondary input
Secondary DOUT (OUT)	GPIO1	R51/D5–D2 = 1011	GPIO1 = secondary DOUT
		R33/D0	Select source for secondary DOUT (0 = primary DIN; 1 = DOUT from interface block)

Table 7-44. Generation of ADC_WCLK

ADC_WCLK DIRECTION	POSSIBLE PINS	PAGE 0 REGISTERS	COMMENT
OUTPUT	GPIO1	R32/D7–D5 = 000	ADC_WCLK obtained from GPIO1 pin
		R51/D5–D2 = 0111	GPIO1 = ADC_WCLK
		R32/D1	Select source of Internal ADC_WCLK (0 = DAC_WCLK; 1 = ADC_WCLK)
INPUT	GPIO1	R32/D7–D5 = 000	ADC_WCLK obtained from GPIO1 pin
		R51/D5–D2 = 0001	GPIO1 enabled as secondary input
		R32/D1	Select source of internal ADC_WCLK (0 = DAC_WCLK; 1 = ADC_WCLK)

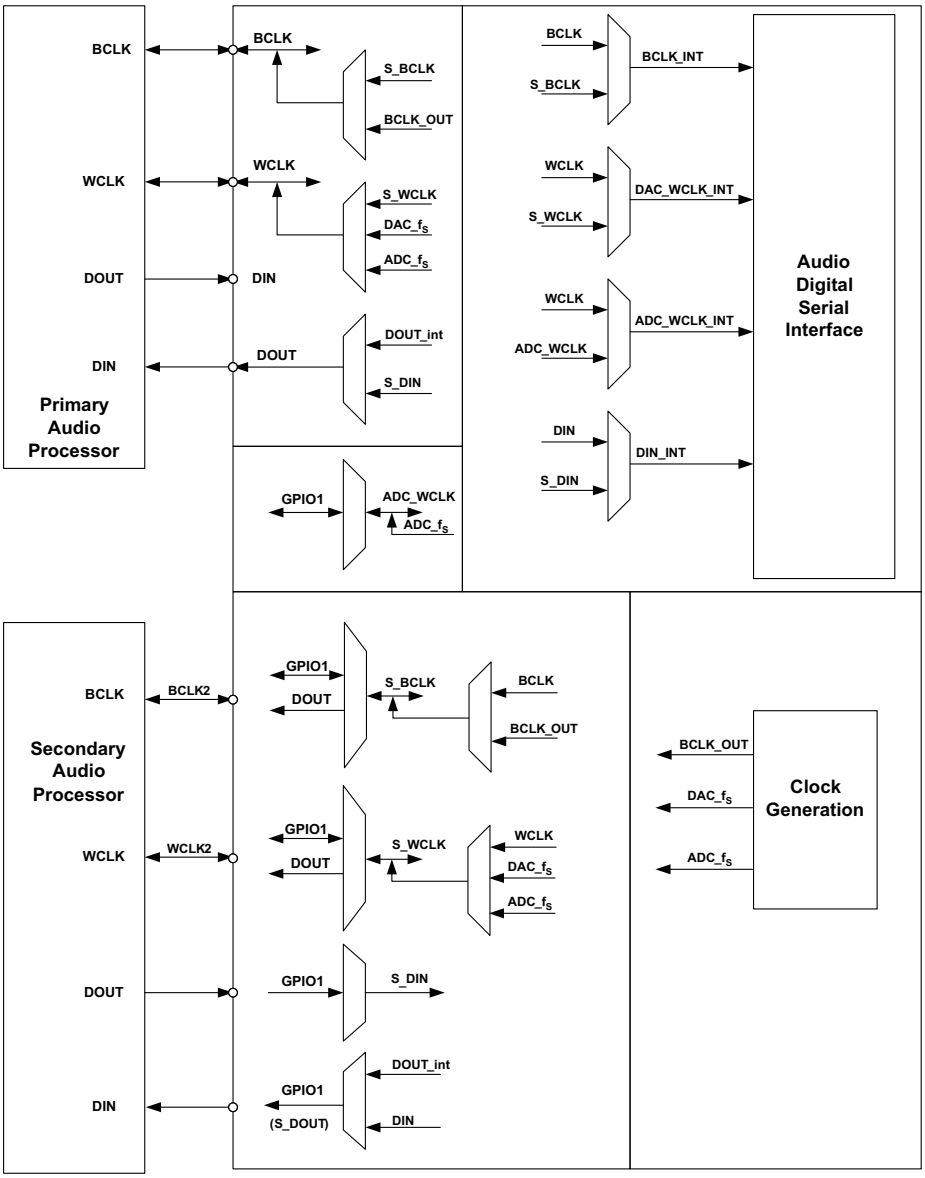


Figure 7-50. Audio Serial Interface Multiplexing

7.3.13.3 Control Interface

The TLV320AIC3110 control interface supports the I^{2}C communication protocol.

7.3.13.3.1 I^{2}C Control Mode

The TLV320AIC3110 supports the I^{2}C control protocol, and responds to the I^{2}C address of 0011 000. I^{2}C is a two-wire, open-drain interface supporting multiple devices and masters on a single bus. Devices on the I^{2}C bus only drive the bus lines LOW by connecting them to ground; they never drive the bus lines HIGH. Instead, the bus wires are pulled HIGH by pullup resistors, so the bus wires are HIGH when no device is driving them LOW. This way, two devices cannot conflict; if two devices drive the bus simultaneously, there is no driver contention.

Communication on the I^{2}C bus always takes place between two devices, one acting as the master and the other acting as the slave. Both masters and slaves can read and write, but slaves can only do so under the direction of the master. Some I^{2}C devices can act as masters or slaves, but the TLV320AIC3110 can only act as a slave device.

An I^{2}C bus consists of two lines, SDA and SCL. SDA carries data, and the SCL signal provides the clock. All data is transmitted across the I^{2}C bus in groups of eight bits. To send a bit on the I^{2}C bus, the SDA line is driven to the appropriate level while SCL is LOW (a LOW on SDA indicates the bit is zero, while a HIGH indicates the bit is one).

Once the SDA line has settled, the SCL line is brought HIGH, then LOW. This pulse on the SCL line clocks the SDA bit into the receiver shift register.

The I^{2}C bus is bidirectional: the SDA line is used both for transmitting and receiving data. When a master reads from a slave, the slave drives the data line; when a master sends to a slave, the master drives the data line.

Most of the time the bus is idle, no communication is taking place, and both lines are HIGH. When communication is taking place, the bus is active. Only master devices can start communication on the bus. Generally, the data line is only allowed to change state while the clock line is LOW. If the data line changes state while the clock line is HIGH, it is either a START condition or the counterpart, a STOP condition. A START condition is when the clock line is HIGH and the data line goes from HIGH to LOW. A STOP condition is when the clock line is HIGH and the data line goes from LOW to HIGH.

After the master issues a START condition, it sends a byte that selects the slave device for communication. This byte is called the address byte. Each device on an I^{2}C bus has a unique 7-bit address to which it responds. (Slaves can also have 10-bit addresses; see the I^{2}C specification for details.) The master sends an address in the address byte, together with a bit that indicates whether it is to read from or write to the slave device.

Every byte transmitted on the I^{2}C bus, whether it is address or data, is acknowledged with an acknowledge bit. When a master has finished sending a byte (eight data bits) to a slave, it stops driving SDA and waits for the slave to acknowledge the byte. The slave acknowledges the byte by pulling SDA LOW. The master then sends a clock pulse to clock the acknowledge bit. Similarly, when a master has finished reading a byte, it pulls SDA LOW to acknowledge this to the slave. It then sends a clock pulse to clock the bit. (Remember that the master always drives the clock line.)

A not-acknowledge is performed by simply leaving SDA HIGH during an acknowledge cycle. If a device is not present on the bus, and the master attempts to address the device, the master receives a not-acknowledge because no device is present at that address to pull the line LOW.

When a master has finished communicating with a slave, it may issue a STOP condition. When a STOP condition is issued, the bus becomes idle again. A master may also issue another START condition. When a START condition is issued while the bus is active, it is called a repeated START condition.

The TLV320AIC3110 can also respond to and acknowledge a general call, which consists of the master issuing a command with a slave address byte of 00h. This feature is disabled by default, but can be enabled through page 0 / register 34, bit D5.

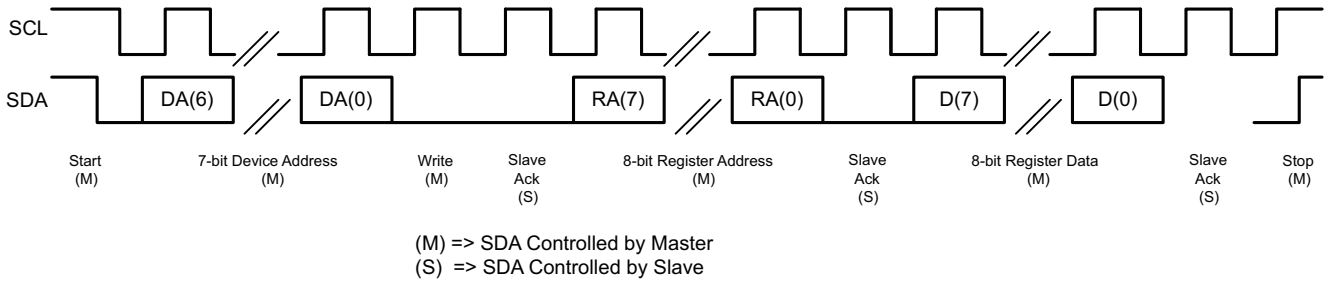


Figure 7-51. I²C Write

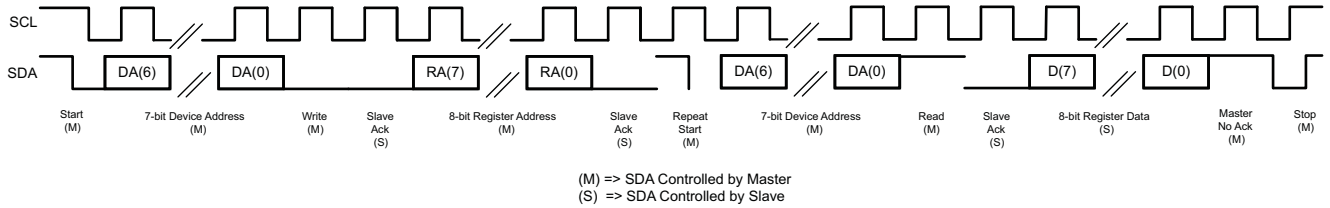


Figure 7-52. I²C Read

In the case of an I²C register write, if the master does not issue a STOP condition, then the device enters auto-increment mode. So in the next eight clocks, the data on SDA is treated as data for the next incremental register.

Similarly, in the case of an I²C register read, after the device has sent out the 8-bit data from the addressed register, if the master issues a ACKNOWLEDGE, the slave takes over control of the SDA bus and transmits for the next eight clocks the data of the next incremental register.

7.4 Register Map

7.4.1 TLV320AIC3110 Register Map

All features on this device are addressed using the I²C bus. All of the writable registers can be read back. However, some registers contain status information or data, and are only available for reading.

The TLV320AIC3110 device contains several pages of 8-bit registers, and each page can contain up to 128 registers. The register pages are divided up based on functional blocks for this device. Page 0 is the default home page after $\overline{\text{RESET}}$. Page control occurs by writing a new page value into register 0 of the current page.

The control registers for the TLV320AIC3110 device are described in detail as follows. All registers are 8 bits in width, with D7 referring to the most-significant bit of each register, and D0 referring to the least-significant bit.

Pages 0, 1, 3, 4, 8–9, 12–13 are available for use. All other pages and registers are reserved. Do not read from or write to reserved pages and registers. Also, do not write other than the reset values for the reserved bits and read-only bits of non-reserved registers; otherwise, device functionality failure can occur.

NOTE

Note that the page and register numbers are shown in decimal format. For use in microcode, these decimal values may need to be converted to hexadecimal format. For convenience, the register numbers are shown in both formats, whereas the page numbers are shown only in decimal format.

Table 7-45. Summary of Register Map

PAGE NUMBER	DESCRIPTION
0	Page 0 is the default page on power up. Configuration for serial interface, digital I/O, clocking, ADC, DAC settings, and other circuitry.
1	Configuration for analog PGAs, ADC, DAC, output drivers, volume controls, and other circuitry.
3	Register 16 controls the MCLK divider that controls the interrupt pulse duration, debounce timing, and detection block clock.
4	ADC AGC and filter coefficients
8–9	DAC Buffer A filter and DRC coefficients
12–13	DAC Buffer B filter and DRC coefficients

7.4.2 Registers

7.4.2.1 Control Registers, Page 0 (Default Page): Clock Multipliers, Dividers, Serial Interfaces, Flags, Interrupts, and GPIOs

Table 7-46. Page 0 / Register 0 (0x00): Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

Table 7-47. Page 0 / Register 1 (0x01): Software Reset

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D1	R/W	0000 000	Reserved. Write only zeros to these bits.
D0	R/W	0	0: Don't care 1: Self-clearing software reset for control register

Table 7-48. Page 0 / Register 2 (0x02): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Do not write to this register.

Table 7-49. Page 0 / Register 3 (0x03): OT FLAG

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D2	R	XXXX XX	Reserved. Do not write to these bits.
D1	R	1	0: Overtemperature protection flag (active-low). Valid only if speaker amplifier is powered up 1: Normal operation
D0	R/W	X	Reserved. Do not write to these bits.

Table 7-50. Page 0 / Register 4 (0x04): Clock-Gen Muxing(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.
D3–D2	R/W	00	00: PLL_CLKIN = **MCLK** (device pin) 01: PLL_CLKIN = BCLK (device pin) 10: PLL_CLKIN = GPIO1 (device pin) 11: PLL_CLKIN = DIN (can be used for the system where DAC is not used)

(1) See Section 7.3.11 for more details on clock generation mutiplexing and dividers.

Table 7-50. Page 0 / Register 4 (0x04): Clock-Gen Muxing[1] (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1–D0	R/W	00	00: CODEC_CLKIN = **MCLK** (device pin) 01: CODEC_CLKIN = BCLK (device pin) 10: CODEC_CLKIN = GPIO1 (device pin) 11: CODEC_CLKIN = PLL_CLK (generated on-chip)

Table 7-51. Page 0 / Register 5 (0x05): PLL P and R Values

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: PLL is powered down. 1: PLL is powered up.
D6–D4	R/W	001	000: PLL divider P = 8 001: PLL divider P = 1 010: PLL divider P = 2 ... 110: PLL divider P = 6 111: PLL divider P = 7
D3–D0	R/W	0001	0000: PLL multiplier R = 16 0001: PLL multiplier R = 1 0010: PLL multiplier R = 2 ... 1110: PLL multiplier R = 14 1111: PLL multiplier R = 15

Table 7-52. Page 0 / Register 6 (0x06): PLL J-Value

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 0100	00 0000: Do not use (reserved) 00 0001: PLL multiplier J = 1 00 0010: PLL multiplier J = 2 ... 11 1110: PLL multiplier J = 62 11 1111: PLL multiplier J = 63

Table 7-53. Page 0 / Register 7 (0x07): PLL D-Value MSB[1]

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only zeros to these bits.
D5–D0	R/W	00 0000	PLL fractional multiplier D-value MSB bits D[13:8]

(1) Note that this register is updated only when Page 0 / Register 8 is written immediately after Page 0 / Register 7.

Table 7-54. Page 0 / Register 8 (0x08): PLL D-Value LSB[1]

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	PLL fractional multiplier D-value LSB bits D[7:0]

(1) Note that Page 0 / Register 8 must be written immediately after Page 0 / Register 7.

Table 7-55. Page 0 / Register 9 (0x09) and Page 0 / Register 10 (0x0A): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only zeros to these bits.

Table 7-56. Page 0 / Register 11 (0x0B): DAC NDAC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DAC NDAC divider is powered down. 1: DAC NDAC divider is powered up.
D6–D0	R/W	000 0001	000 0000: DAC NDAC divider = 128 000 0001: DAC NDAC divider = 1 000 0010: DAC NDAC divider = 2 ... 111 1110: DAC NDAC divider = 126 111 1111: DAC NDAC divider = 127

Table 7-57. Page 0 / Register 12 (0x0C): DAC MDAC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DAC MDAC divider is powered down. 1: DAC MDAC divider is powered up.
D6–D0	R/W	000 0001	000 0000: DAC MDAC divider = 128 000 0001: DAC MDAC divider = 1 000 0010: DAC MDAC divider = 2 ... 111 1110: DAC MDAC divider = 126 111 1111: DAC MDAC divider = 127

Table 7-58. Page 0 / Register 13 (0x0D): DAC DOSR_VAL MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 00	Reserved. Write only reset vlaues.
D1–D0	R/W	00	DAC OSR (DOSR) Setting **DAC OSR(MSB)** & DAC OSR(LSB) **00** 0000 0000: DOSR=1024 **00** 0000 0001: DOSR=1 **00** 0000 0010: DOSR=2 ... **11** 1111 1110: DOSR=1022 **11** 1111 1111: DOSR=1023 **Note**: This register is updated when Page-0, Reg-14 is written to immediately after Page-0, Reg-13 **Note**: DOSR should be a multiple of 2 while using DAC Filter Type A, Multiple of 4 while using DAC Filter Type B and Multiple of 8 while using DAC Filter Type C

Table 7-59. Page 0 / Register 14 (0x0E): DAC DOSR_VAL LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	DAC OSR (DOSR) (7:0) 0000 0000: DAC DOSR (7:0) = 1024 (MSB page 0 / register 13, bits D1-D0 = 00) 0000 0001: Reserved. Do not use 0000 0010: DAC DOSR (7:0) = 2 (MSB page 0 / register 13, bits D1-D0 = 00) 0000 0100: : DAC DOSR (7:0) = 4 (MSB page 0 / register 13, bits D1-D0 = 00) ... 1111 1110: DAC DOSR (7:0) = 1022 (MSB page 0 / register 13, bits D1-D0 = 00) 1111 1111: Reserved. Do not use **Note**: This register must be written immediately after Page 0 / Register 13 **Note**: DOSR must be a multiple of 8 while using DAC Filter Type A, a multiple of 4 while using DAC Filter Type B and a multiple of 2 while using DAC Filter Type C

Table 7-60. Page 0 / Register 15 (0x0F) through Page 0 / Register 17: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-61. Page 0 / Register 18 (0x12): ADC NADC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC NADC divider is powered down and ADC_CLK = DAC_CLK. 1: ADC NADC divider is powered up.
D6–D0	R/W	000 0001	000 0000: ADC NADC divider = 128 000 0001: ADC NADC divider = 1 000 0010: ADC NADC divider = 2 ... 111 1110: ADC NADC divider = 126 111 1111: ADC NADC divider = 127

Table 7-62. Page 0 / Register 19 (0x13): ADC MADC_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC MADC divider is powered down and ADC_MOD_CLK = DAC_MOD_CLK. 1: ADC MADC divider is powered up.
D6–D0	R/W	000 0001	000 0000: ADC MADC divider = 128 000 0001: ADC MADC divider = 1 000 0010: ADC MADC divider = 2 ... 111 1110: ADC MADC divider = 126 111 1111: ADC MADC divider = 127

Table 7-63. Page 0 / Register 20 (0x14): ADC AOSR_VAL(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1000 0000	0000 0000: ADC OSR AOSR divider = 256 0000 0001: ADC OSR AOSR divider = 1 0000 0010: ADC OSR AOSR divider = 2 ... 1111 1110: ADC OSR AOSR divider = 254 1111 1111: ADC OSR AOSR divider = 255

(1) ADC OSR must be an integral multiple of the decimation in the ADC PRB engine (specified in register 22). When PRB modes are used, decimation ratio is 4 while using Filter-A, 2 while using Filter-B and 1 while using Filter-C

Table 7-64. Page 0 / Register 21 through Page 0 / Register 24: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-65. Page 0 / Register 25 (0x19): CLKOUT MUX

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Reserved
D2–D0	R/W	000	000: CDIV_CLKIN = MCLK (device pin) 001: CDIV_CLKIN = BCLK (device pin) 010: CDIV_CLKIN = DIN (can be used for the systems where DAC is not required) 011: CDIV_CLKIN = PLL_CLK (generated on-chip) 100: CDIV_CLKIN = DAC_CLK (DAC DSP clock - generated on-chip) 101: CDIV_CLKIN = DAC_MOD_CLK (generated on-chip) 110: CDIV_CLKIN = ADC_CLK (ADC DSP clock - generated on-chip) 111: CDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

Table 7-66. Page 0 / Register 26 (0x1A): CLKOUT M_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: CLKOUT M divider is powered down. 1: CLKOUT M divider is powered up.

Table 7-66. Page 0 / Register 26 (0x1A): CLKOUT M_VAL (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6–D0	R/W	000 0001	000 0000: CLKOUT divider M = 128 000 0001: CLKOUT divider M = 1 000 0010: CLKOUT divider M = 2 ... 111 1110: CLKOUT divider M = 126 111 1111: CLKOUT divider M = 127

Table 7-67. Page 0 / Register 27 (0x1B): Codec Interface Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Codec interface = I^2S 01: Codec Interface = DSP 10: Codec interface = RJF 11: Codec interface = LJF
D5–D4	R/W	00	00: Codec interface word length = 16 bits 01: Codec interface word length = 20 bits 10: Codec interface word length = 24 bits 11: Codec interface word length = 32 bits
D3	R/W	0	0: BCLK is input 1: BCLK is output
D2	R/W	0	0: WCLK is input 1: WCLK is output
D1	R/W	0	Reserved
D0	R/W	0	Driving **DOUT** to High-Impedance for the Extra BCLK Cycle When Data Is Not Being Transferred 0: Disabled 1: Enabled

Table 7-68. Page 0 / Register 28 (0x1C): Data-Slot Offset Programmability

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	Offset (Measured With Respect to WCLK Rising Edge in DSP Mode) 0000 0000: Offset = 0 BCLKs 0000 0001: Offset = 1 BCLK 0000 0010: Offset = 2 BCLKs ... 1111 1110: Offset = 254 BCLKs 1111 1111: Offset = 255 BCLKs

Table 7-69. Page 0 / Register 29 (0x1D): Codec Interface Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved
D5	R/W	0	0: DIN-to-DOUT loopback is disabled 1: DIN-to-DOUT loopback is enabled
D4	R/W	0	0: ADC-to-DAC loopback is disabled 1: ADC-to-DAC loopback is enabled
D3	R/W	0	0: BCLK is not inverted (valid for both primary and secondary BCLK) 1: BCLK is inverted (valid for both primary and secondary BCLK)
D2	R/W	0	BCLK and WCLK Active Even With Codec Powered Down (Valid for Both Primary and Secondary BCLK) 0: Disabled 1: Enabled
D1–D0	R/W	00	00: BDIV_CLKIN = DAC_CLK (generated on-chip) 01: BDIV_CLKIN = DAC_MOD_CLK (generated on-chip) 10: BDIV_CLKIN = ADC_CLK (ADC DSP clock - generated on-chip) 11: BDIV_CLKIN = ADC_MOD_CLK (generated on-chip)

Table 7-70. Page 0 / Register 30 (0x1E): BCLK N_VAL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: BCLK N-divider is powered down. 1: BCLK N-divider is powered up.
D6–D0	R/W	000 0001	000 0000: BCLK divider N = 128 000 0001: BCLK divider N = 1 000 0010: BCLK divider N = 2 ... 111 1110: BCLK divider N = 126 111 1111: BCLK divider N = 127

Table 7-71. Page 0 / Register 31 (0x1F): Codec Secondary Interface Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	000: Secondary BCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Secondary BCLK is obtained from DOUT pin. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D4–D2	R/W	000	000: Secondary WCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Secondary WCLK is obtained from DOUT pin. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D1–D0	R/W	00	00: Secondary DIN is obtained from the GPIO1 pin. 01: Reserved. 10: Reserved. 11: Reserved.

Table 7-72. Page 0 / Register 32 (0x20): Codec Secondary Interface Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	000: ADC_WCLK is obtained from GPIO1 pin. 001: Reserved. 010: Reserved. 011: Reserved. 100: Reserved. 101: Reserved. 110: Reserved. 111: Reserved.
D4	R/W	0	Reserved
D3	R/W	0	0: Primary BCLK is fed to codec serial-interface and ClockGen blocks. 1: Secondary BCLK is fed to codec serial-interface and ClockGen blocks.
D2	R/W	0	0: Primary WCLK is fed to codec serial-interface block. 1: Secondary WCLK is fed to codec serial-interface block.
D1	R/W	0	0: ADC_WCLK used in the codec serial-interface block is the same as DAC_WCLK. 1: ADC_WCLK used in the codec serial-interface block = ADC_WCLK.
D0	R/W	0	0: Primary DIN is fed to codec serial-interface block. 1: Secondary DIN is fed to codec serial-interface block.

Table 7-73. Page 0 / Register 33 (0x21): Codec Secondary Interface Control 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Primary BCLK output = internally generated BCLK clock 1: Primary BCLK output = secondary BCLK
D6	R/W	0	0: Secondary BCLK output = primary BCLK 1: Secondary BCLK output = internally generated BCLK clock
D5–D4	R/W	00	00: Primary WCLK output = internally generated DAC_f_S 01: Primary WCLK output = internally generated ADC_f_S clock 10: Primary WCLK output = secondary WCLK 11: Reserved
D3–D2	R/W	00	00: Secondary WCLK output = primary WCLK 01: Secondary WCLK output = internally generated DAC_f_S clock 10: Secondary WCLK output = internally generated ADC_f_S clock 11: Reserved
D1	R/W	0	0: Primary DOUT = DOUT from codec serial-interface block 1: Primary DOUT = secondary DIN
D0	R/W	0	0: Secondary DOUT = primary DIN 1: Secondary DOUT = DOUT from codec serial interface block

Table 7-74. Page 0 / Register 34 (0x22): I^2C Bus Condition

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	Reserved. Write only the reset value to these bits.
D5	R/W	0	0: I^2C general-call address is ignored. 1: Device accepts I^2C general-call address.
D4–D0	R/W	0 0000	Reserved. Write only zeros to these bits.

Table 7-75. Page 0 / Register 35: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only zeros to these bits.

Table 7-76. Page 0 / Register 36 (0x24): ADC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: ADC PGA applied gain ≠ programmed gain 1: ADC PGA applied gain = programmed gain
D6	R	0	0: ADC powered down 1: ADC powered up
D5(1)	R	0	0: AGC not saturated 1: AGC applied gain = maximum applicable gain by AGC
D4–D0	R/W	X XXXX	Reserved. Write only zeros to these bits.

(1) Sticky flag bIt. These is a read-only bit. This bit is automatically cleared once it is read and is set only if the source trigger occurs again.

Table 7-77. Page 0 / Register 37 (0x25): DAC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: Left-channel DAC powered down 1: Left-channel DAC powered up
D6	R/W	X	Reserved. Write only zero to this bit.
D5	R	0	0: HPL driver powered down 1: HPL driver powered up
D4	R	0	0: Left-channel class-D driver powered down 1: Left-channel class-D driver powered up

Table 7-77. Page 0 / Register 37 (0x25): DAC Flag Register (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3	R	0	0: Right-channel DAC powered down 1: Right-channel DAC powered up
D2	R/W	X	Reserved. Write only zero to this bit.
D1	R	0	0: HPR driver powered down 1: HPR driver powered up
D0	R	0	0: Right-channel class-D driver powered down 1: Right-channel class-D driver powered up

Table 7-78. Page 0 / Register 38 (0x26): DAC Flag Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	XXX	Reserved. Do not write to these bits.
D4	R	0	0: Left-channel DAC PGA applied gain ≠ programmed gain 1: Left-channel DAC PGA applied gain = programmed gain
D3–D1	R/W	XXX	Reserved. Write only zeros to these bits.
D0	**R**	0	0: Right-channel DAC PGA applied gain ≠ programmed gain 1: Right-channel DAC PGA applied gain = programmed gain

Table 7-79. Page 0 / Register 39 (0x27): Overflow Flags

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7(1)	R	0	Left-Channel DAC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D6(1)	R	0	Right-Channel DAC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D5(1)	R	0	DAC Barrel Shifter Output Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D4	R/W	0	Reserved. Write only zeros to these bits.
D3(1)	R	0	Delta-Sigma Mono ADC Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D2	R/W	0	Reserved. Write only zero to this bit.
D1(1)	R	0	ADC Barrel Shifter Output Overflow Flag 0: Overflow has not occurred. 1: Overflow has occurred.
D0	R/W	0	Reserved. Write only zero to this bit.

(1) Sticky flag bIt. These is a read-only bit. This bit is automatically cleared once it is read and is set only if the source trigger occurs again.

Table 7-80. Page 0 / Register 40 (0x28) Through Page 0 / Register 43 (0x2B): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-81. Page 0 / Register 44 (0x2C): Interrupt Flags—DAC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7(1)	R	0	0: No short circuit is detected at HPL / left class-D driver. 1: Short circuit is detected at HPL / left class-D driver.

(1) Sticky flag bIt. These is a read-only bit. This bit is automatically cleared once it is read and is set only if the source trigger occurs again.

Table 7-81. Page 0 / Register 44 (0x2C): Interrupt Flags—DAC (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D6(1)	R	0	0: No short circuit is detected at HPR / right class-D driver. 1: Short circuit is detected at HPR / right class-D driver.
D5(1)	**R**	X	0: No headset button pressed. 1: Headset button pressed.
D4(1)	**R**	X	0: No headset insertion or removal is detected. 1: Headset insertion or removal is detected.
D3(1)	**R**	0	0: Left DAC signal power is less than or equal to the signal threshold of DRC. 1: Left DAC signal power is above the signal threshold of DRC.
D2(1)	**R**	0	0: Right DAC signal power is less than or equal to the signal threshold of DRC. 1: Right DAC signal power is above the signal threshold of DRC.
D1-D0	**R**	0	Reserved. Do not write to these registers.

Table 7-82. Page 0 / Register 45 (0x2D): Interrupt Flags—ADC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6(1)	R	0	0: ADC signal power greater than noise threshold for AGC. 1: ADC signal power less than noise threshold for AGC.
D5-D3	R	0	Reserved. Write only zeros to these bits.
D2	R	0	0: DC measurement using delta-sigma audio ADC is not available. 1: DC measurement using delta-sigma audio ADC is not available.
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

(1) Sticky flag bIt. These is a read-only bit. This bit is automatically cleared once it is read and is set only if the source trigger occurs again.

Table 7-83. Page 0 / Register 46 (0x2E): Interrupt Flags—DAC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R	0	0: No short circuit detected at HPL / left class-D driver. 1: Short circuit detected at HPL / left class-D driver.
D6	R	0	0: No short circuit detected at HPR / right class-D driver 1: Short circuit detected at HPR / right class-D driver
D5	R	X	0: No headset button pressed. 1: Headset button pressed.
D4	R	X	0: Headset removal detected. 1: Headset insertion detected.
D3	R	0	0: Left DAC signal power is below signal threshold of DRC. 1: Left DAC signal power is above signal threshold of DRC.
D2	R	0	0: Right DAC signal power is below signal threshold of DRC. 1: Right DAC signal power is above signal threshold of DRC.
D1–D0	R	00	Reserved.

Table 7-84. Page 0 / Register 47 (0x2F): Interrupt Flags – ADC

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved
D6	R	0	0: Delta-sigma mono ADC signal power greater than noise threshold for left AGC 1: Delta-sigma mono ADC signal power less than noise threshold for left AGC
D5	R/W	0	Reserved
D4–D3	R	00	Reserved.
D2	R	0	0: DC measurement using delta-sigma audio ADC is not available 1: DC measurement using delta-sigma audio ADC is not available
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

Table 7-85. Page 0 / Register 48 (0x30): INT1 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset-insertion detect interrupt is not used in the generation of INT1 interrupt. 1: Headset-insertion detect interrupt is used in the generation of INT1 interrupt.
D6	R/W	0	0: Button-press detect interrupt is not used in the generation of INT1 interrupt. 1: Button-press detect interrupt is used in the generation of INT1 interrupt.
D5	R/W	0	0: DAC DRC signal-power interrupt is not used in the generation of INT1 interrupt. 1: DAC DRC signal-power interrupt is used in the generation of INT1 interrupt.
D4	R/W	0	0: ADC AGC noise interrupt is not used in the generation of INT1 interrupt. 1: ADC AGC noise interrupt is used in the generation of INT1 interrupt.
D3	R/W	0	0: Short-circuit interrupt is not used in the generation of INT1 interrupt. 1: Short-circuit interrupt is used in the generation of INT1 interrupt.
D2	R/W	0	0: DAC data overflow does not result in an INT1 interrupt. 1: DAC data overflow results in an INT1 interrupt.
D2	R	0	Reserved. Write only zero.
D1	R/W	0	0: DC measurement using delta-sigma audio ADC data-available interrupt is not used in the generation of INT1 interrupt 1: DC measurement using delta-sigma audio ADC data-available interrupt is used in the generation of INT1 interrupt
D0	R/W	0	0: INT1 is only one pulse (active-high) of typical 2-ms duration. 1: INT1 is multiple pulses (active-high) of typical 2-ms duration and 4-ms period, until flag registers 44 and 45 are read by the user.

Table 7-86. Page 0 / Register 49 (0x31): INT2 Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset-insertion detect interrupt is not used in the generation of INT2 interrupt. 1: Headset-insertion detect interrupt is used in the generation of INT2 interrupt.
D6	R/W	0	0: Button-press detect interrupt is not used in the generation of INT2 interrupt. 1: Button-press detect interrupt is used in the generation of INT2 interrupt.
D5	R/W	0	0: DAC DRC signal-power interrupt is not used in the generation of INT2 interrupt. 1: DAC DRC signal-power interrupt is used in the generation of INT2 interrupt.
D4	R/W	0	0: ADC AGC noise interrupt is not used in the generation of INT2 interrupt. 1: ADC AGC noise interrupt is used in the generation of INT2 interrupt.
D3	R/W	0	0: Short-circuit interrupt is not used in the generation of INT2 interrupt. 1: Short-circuit interrupt is used in the generation of INT2 interrupt.
D2	R	0	Reserved. Write only zero.
D1	R/W	0	0: DC measurement using delta-sigma audio ADC data-available interrupt is not used in the generation of INT2 interrupt 1: DC measurement using delta-sigma audio ADC data-available interrupt is used in the generation of INT2 interrupt
D0	R/W	0	0: INT2 is only one pulse (active-high) of typical 2-ms duration. 1: INT2 is multiple pulses (active-high) of typical 2-ms duration and 4-ms period, until flag registers 44 and 45 are read by the user.

Table 7-87. Page 0 / Register 50 (0x32): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7-D0	R/W	0000 0000	Reserved. Write only reset values.

Table 7-88. Page 0 / Register 52 (0x34): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write any value other than reset value.

Table 7-89. Page 0 / Register 53 (0x35): DOUT (OUT Pin) Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved
D4	R/W	1	0: DOUT bus keeper enabled 1: DOUT bus keeper disabled
D3–D1	R/W	001	000: DOUT disabled (output buffer powered down) 001: DOUT = primary DOUT output for codec interface 010: DOUT = general-purpose output 011: DOUT = CLKOUT output 100: DOUT = INT1 output 101: DOUT = INT2 output 110: DOUT = secondary BCLK output for codec interface 111: DOUT = secondary WCLK output for codec interface
D0	R/W	0	0: DOUT general-purpose output value = 0 1: DOUT general-purpose output value = 1

Table 7-90. Page 0 / Register 54 (0x36): DIN (IN Pin) Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	Reserved
D2–D1	R/W	01	00: DIN disabled (input buffer powered down) 01: DIN enabled (can be used as DIN for codec interface, Dig_Mic_In or into ClockGen block) 10: DIN is used as general-purpose input (GPI) 11: Reserved
D0	R	X	DIN input-buffer value

Table 7-91. Page 0 / Register 55 (0x37) through Page 0 / Register 59 (0x3B): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-92. Page 0 / Register 60 (0x3C): DAC Processing Blocks Selection

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only default value.
D4–D0	R/W	00 0001	0 0000: Reserved. Write only reset value. 0 0001: DAC signal-processing block PRB_P1 0 0010: DAC signal-processing block PRB_P2 0 0011: DAC signal-processing block PRB_P3 0 0100: DAC signal-processing block PRB_P4 ... 1 1000: DAC signal-processing block PRB_P24 1 1001: DAC signal-processing block PRB_P25 1 1010–1 1111: Reserved. Do not use.

Table 7-93. Page 0 / Register 61 (0x3D): ADC Processing Blocks Selection

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only default values.

Table 7-93. Page 0 / Register 61 (0x3D): ADC Processing Blocks Selection (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D4–D0	R/W	0 0100	0 0000: Reserved. Write only reset value. 0 0001–0 0011: Reserved 0 0100: ADC signal-processing block PRB_R4 0 0101: ADC signal-processing block PRB_R5 0 0110: ADC signal-processing block PRB_R6 0 0111–01001: Reserved 0 1010: ADC signal-processing block PRB_R10 0 1011: ADC signal-processing block PRB_R11 0 1100: ADC signal-processing block PRB_R12 0 1101–0 1111: Reserved 1 0000: ADC signal-processing block PRB_R16 1 0001: ADC signal-processing block PRB_R17 1 0010: ADC signal-processing block PRB_R18 1 0011–1 1111: Reserved. Do not write these sequences to these bits.

Table 7-94. Page 0 / Register 62 (0x3E): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	Reserved. write only reset values.

Table 7-95. Page 0 / Register 63 (0x3F): DAC Data-Path Setup

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel DAC is powered down. 1: Left-channel DAC is powered up.
D6	R/W	0	0: Right-channel DAC is powered down. 1: Right-channel DAC is powered up.
D5–D4	R/W	01	00: Left-channel DAC data path = off 01: Left-channel DAC data path = left data 10: Left-channel DAC data path = right data 11: Left-channel DAC data path = left-channel and right-channel data [(L + R) / 2]
D3–D2	R/W	01	00: Right-channel DAC data path = off 01: Right-channel DAC data path = right data 10: Right-channel DAC data path = left data 11: Right-channel DAC data path = left-channel and right-channel data [(L + R) / 2]
D1–D0	R/W	00	00: DAC-channel volume-control soft-stepping is enabled for one step per sample period. 01: DAC-channel volume-control soft-stepping is enabled for one step per two sample periods. 10: DAC-channel volume-control soft-stepping is disabled. 11: Reserved. Do not write this sequence to these bits.

Table 7-96. Page 0 / Register 64 (0x40): DAC Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.
D3	R/W	1	0: Left-channel DAC not muted 1: Left-channel DAC muted
D2	R/W	1	0: Right-channel DAC not muted 1: Right-channel DAC muted
D1–D0	R/W	00	00: Left and right channels have independent volume control.(1) 01: Left-channel volume control Is the programmed value of right-channel volume control. 10: Right-channel volume control is the programmed value of left-channel volume control. 11: Same as 00

(1) When DRC is enabled, left and right channel volume controls are always independent. Program bits D1–D0 to 00.

Table 7-97. Page 0 / Register 65 (0x41): DAC Left Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0111 1111–0011 0001: Do not use. 0011 0000: Left-channel DAC digital volume = 24 dB 0010 1111: Left-channel DAC digital volume = 23.5 dB ... 0000 0001: Left-channel DAC digital volume = 0.5 dB 0000 0000: Left-channel DAC digital volume = 0 dB 1111 1111: Left-channel DAC digital volume = –0.5 dB ... 1000 0010: Left-channel DAC digital volume = –63 dB 1000 0001: Left-channel DAC digital volume = –63.5 dB 1000 0000: Reserved. Do not use.

Table 7-98. Page 0 / Register 66 (0x42): DAC Right Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0111 1111–0011 0001: Do not use. 0011 0000: Right-channel DAC digital volume = 24 dB 0010 1111: Right-channel DAC digital volume = 23.5 dB ... 0000 0001: Right-channel DAC digital volume = 0.5 dB 0000 0000: Right-channel DAC digital volume = 0 dB 1111 1111: Right-channel DAC digital volume = –0.5 dB ... 1000 0010: Right-channel DAC digital volume = –63 dB 1000 0001: Right-channel DAC digital volume = –63.5 dB 1000 0000: Reserved. Do not use.

Table 7-99. Page 0 / Register 67 (0x43): Headset Detection

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Headset detection disabled 1: Headset detection enabled
D6–D5	R	XX	00: No headset detected 01: Headset without microphone is detected 10: Reserved 11: Headset with microphone is detected
D4–D2	R/W	000	Debounce Programming for Glitch Rejection During Headset Detection(1) 000: 16 ms (sampled with 2-ms clock) 001: 32 ms (sampled with 4-ms clock) 010: 64 ms (sampled with 8-ms clock) 011: 128 ms (sampled with 16-ms clock) 100: 256 ms (sampled with 32-ms clock) 101: 512 ms (sampled with 64-ms clock) 110: Reserved 111: Reserved
D1–D0	R/W	00	Debounce programming for glitch rejection during headset button-press detection 00: 0 ms 01: 8 ms (sampled with 1-ms clock) 10: 16 ms (sampled with 2-ms clock) 11: 32 ms (sampled with 4-ms clock)

(1) Note that these times are generated using the 1 MHz reference clock which is defined in Page 3 / Register 16.

Table 7-100. Page 0 / Register 68 (0x44): DRC Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only the reset value to these bits.
D6	R/W	0	0: DRC disabled for left channel 1: DRC enabled for left channel
D5	R/W	0	0: DRC disabled for right channel 1: DRC enabled for right channel
D4–D2	R/W	011	000: DRC threshold = –3 dB 001: DRC threshold = –6 dB 010: DRC threshold = –9 dB 011: DRC threshold = –12 dB 100: DRC threshold = –15 dB 101: DRC threshold = –18 dB 110: DRC threshold = –21 dB 111: DRC threshold = –24 dB
D1–D0	R/W	11	00: DRC hysteresis = 0 dB 01: DRC hysteresis = 1 dB 10: DRC hysteresis = 2 dB 11: DRC hysteresis = 3 dB

Table 7-101. Page 0 / Register 69 (0x45): DRC Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D	R	0	Reserved. Write only the reset value to these bits.
D6–D3	R/W	0111	DRC Hold Time 0000: DRC Hold Disabled 0001: DRC Hold Time = 32 DAC Word Clocks 0010: DRC Hold Time = 64 DAC Word Clocks 0011: DRC Hold Time = 128 DAC Word Clocks 0100: DRC Hold Time = 256 DAC Word Clocks 0101: DRC Hold Time = 512 DAC Word Clocks 0110: DRC Hold Time = 1024 DAC Word Clocks 0111: DRC Hold Time = 2048 DAC Word Clocks 1000: DRC Hold Time = 4096 DAC Word Clocks 1001: DRC Hold Time = 8192 DAC Word Clocks 1010: DRC Hold Time = 16 384 DAC Word Clocks 1011: DRC Hold Time = 32 768 DAC Word Clocks 1100: DRC Hold Time = 65 536 DAC Word Clocks 1101: DRC Hold Time = 98 304 DAC Word Clocks 1110: DRC Hold Time = 131 072 DAC Word Clocks 1111: DRC Hold Time = 163 840 DAC Word Clocks
D2-D0	R	000	Reserved. Write only the reset value to these bits.

Table 7-102. Page 0 / Register 70 (0x46): DRC Control 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	0000: DRC attack rate = 4 dB per DAC Word Clock 0001: DRC attack rate = 2 dB per DAC word clock 0010: DRC attack rate = 1 dB per DAC word clock ... 1110: DRC attack rate = 2.4414e–5 dB per DAC word clock 1111: DRC attack rate = 1.2207e–5 dB per DAC word clock
D3–D0	R/W	0000	Decay Rate is defined as DR / $2^{[\text{bits D3-D0 value}]}$ dB per DAC Word Clock, where DR = 0.015625 dB 0000: DRC decay rate (DR) = 0.015625 dB per DAC Word Clock 0001: DRC decay rate = DR / 2 dB per DAC Word Clock 0010: DRC decay rate = DR / 2^2 dB per DAC Word Clock 0011: DRC decay rate = DR / 2^3 dB per DAC Word Clock 0100: DRC decay rate = DR / 2^4 dB per DAC Word Clock 0101: DRC decay rate = DR / 2^5 dB per DAC Word Clock 0110: DRC decay rate = DR / 2^6 dB per DAC Word Clock 0111: DRC decay rate = DR / 2^7 dB per DAC Word Clock 1000: DRC decay rate = DR / 2^8 dB per DAC Word Clock 1001: DRC decay rate = DR / 2^9 dB per DAC Word Clock 1010: DRC decay rate = DR / 2^{10} dB per DAC Word Clock 1011: DRC decay rate = DR / 2^{11} dB per DAC Word Clock 1100: DRC decay rate = DR / 2^{12} dB per DAC Word Clock 1101: DRC decay rate = DR / 2^{13} dB per DAC Word Clock 1110: DRC decay rate = DR / 2^{14} dB per DAC Word Clock 1111: DRC decay rate = DR / 2^{15} dB per DAC Word Clock

Table 7-103. Page 0 / Register 71 (0x47): Left Beep Generator (1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Beep generator is disabled. 1: Beep generator is enabled (self-clearing based on beep duration).
D6	R/W	0	Reserved. Write only reset value.
D5–D0	R/W	00 0000	00 0000: Left-channel beep volume control = 2 dB 00 0001: Left-channel beep volume control = 1 dB 00 0010: Left-channel beep volume control = 0 dB 00 0011: Left-channel beep volume control = –1 dB ... 11 1110: Left-channel beep volume control = –60 dB 11 1111: Left-channel beep volume control = –61 dB

(1) The beep generator is only available in PRB_P25 DAC processing mode.

Table 7-104. Page 0 / Register 72 (0x48): Right Beep Generator(1)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: Left and right channels have independent beep volume control. 01: Left-channel beep volume control is the programmed value of right-channel beep volume control. 10: Right-channel beep volume control is the programmed value of left-channel beep volume control. 11: Same as 00
D5–D0	R/W	00 0000	00 0000: Right-channel beep volume control = 2 dB 00 0001: Right-channel beep volume control = 1 dB 00 0010: Right-channel beep volume control = 0 dB 00 0011: Right-channel beep volume control = –1 dB ... 11 1110: Right-channel beep volume control = –60 dB 11 1111: Right-channel beep volume control = –61 dB

(1) The beep generator is only available in PRB_P25 DAC processing mode.

Table 7-105. Page 0 / Register 73 (0x49): Beep Length MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	8 MSBs out of 24 bits for the number of samples for which the beep must be generated.

Table 7-106. Page 0 / Register 74 (0x4A): Beep-Length Middle Bits

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	8 middle bits out of 24 bits for the number of samples for which the beep must be generated.

Table 7-107. Page 0 / Register 75 (0x4B): Beep Length LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 1110	8 LSBs out of 24 bits for the number of samples for which beep must be generated.

Table 7-108. Page 0 / Register 76 (0x4C): Beep Sin(x) MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0001 0000	8 MSBs out of 16 bits for $\sin(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-109. Page 0 / Register 77 (0x4D): Beep Sin(x) LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1101 1000	8 LSBs out of 16 bits for $\sin(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-110. Page 0 / Register 78 (0x4E): Beep Cos(x) MSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0111 1110	8 MSBs out of 16 bits for $\cos(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-111. Page 0 / Register 79 (0x4F): Beep Cos(x) LSB

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	1110 0011	8 LSBs out of 16 bits for $\cos(2\pi \times f_{in} / f_S)$, where f_{in} is the beep frequency and f_S is the DAC sample rate.

Table 7-112. Page 0 / Register 80 (0x50): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-113. Page 0 / Register 81 (0x51): ADC Digital Mic

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: ADC channel is powered down. 1: ADC channel is powered up.
D6	R/W	0	Reserved
D5–D4	R/W	00	00: Digital microphone input is obtained from GPIO1 pin. 01: Reserved. 10: Digital microphone input is obtained from DIN pin. 11: Reserved.
D3	R/W	0	0: Digital microphone is not enabled for delta-sigma mono ADC channel. 1: Digital microphone is enabled for delta-sigma mono ADC channel
D2	R/W	0	Reserved
D1–D0	R/W	00	00: ADC channel volume control soft-stepping is enabled for one step per sample period. 01: ADC channel volume control soft-stepping is enabled for one step per two sample periods. 10: ADC channel volume control soft-stepping is disabled. 11: Reserved. Do not write this sequence to these bits.

Table 7-114. Page 0 / Register 82 (0x52): ADC Digital Volume Control Fine Adjust

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: ADC channel not muted 1: ADC channel muted
D6–D4	R/W	000	Delta-Sigma Mono ADC Channel Volume Control Fine Gain 000: 0 dB 001: –0.1 dB 010: –0.2 dB 011: –0.3 dB 100: –0.4 dB 101–111: Reserved
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

Table 7-115. Page 0 / Register 83 (0x53): ADC Digital Volume Control Coarse Adjust

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved
D6–D0		000 0000	100 0000–110 0111: Reserved 110 1000: –12 dB 110 1001: –11.5 dB ... 111 1111: –0.5 dB 000 0000: 0 dB 000 0001: 0.5 dB ... 010 0111: 19.5 dB 010 1000: 20 dB 010 1001–011 1111: Reserved

Table 7-116. Page 0 / Register 84 and Page 0 / Register 85: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

Table 7-117. Page 0 / Register 86 (0x56): AGC Control 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: AGC disabled 1: AGC enabled
D6–D4	R/W	000	000: AGC target level = –5.5 dB 001: AGC target level = –8 dB 010: AGC target level = –10 dB 011: AGC target level = –12 dB 100: AGC target level = –14 dB 101: AGC target level = –17 dB 110: AGC target level = –20 dB 111: AGC target level = –24 dB
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

Table 7-118. Page 0 / Register 87 (0x57): AGC Control 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: AGC hysterysis setting of 1 dB 01: AGC hysterysis setting of 2 dB 10: AGC hysterysis setting of 4 dB 11: AGC hysterysis disabled
D5–D1	R/W	00 000	00 000: AGC noise and silence detection is disabled. 00 001: AGC noise threshold = –30 dB 00 010: AGC noise threshold = –32 dB 00 011: AGC noise threshold = –34 dB ... 11 101: AGC noise threshold = –86 dB 11 110: AGC noise threshold = –88 dB 11 111: AGC noise threshold = –90 dB
D0	R/W	0	Reserved. Write only zero to this bit.

Table 7-119. Page 0 / Register 88 (0x58): AGC Maximum Gain

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D0	R/W	111 1111	000 0000: AGC maximum gain = 0 dB 000 0001: AGC maximum gain = 0.5 dB 000 0010: AGC maximum gain = 1 dB ... 111 0011: AGC maximum gain = 57.5 dB 111 0100: AGC maximum gain = 58 dB 111 0101: AGC maximum gain = 58.5 dB 111 0110: AGC maximum gain = 59 dB 111 0111: AGC maximum gain = 59.5 dB 111 1000–111 1111: Reserved. Do not write these sequences to these bits.

Table 7-120. Page 0 / Register 89 (0x59): AGC Attack Time

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	0000 0: AGC attack time = 1 × (32 / f_S) where f_S is the ADC sample rate 0000 1: AGC attack time = 3 × (32 / f_S) where f_S is the ADC sample rate 0001 0: AGC attack time = 5 × (32 / f_S) where f_S is the ADC sample rate 0001 1: AGC attack time = 7 × (32 / f_S) where f_S is the ADC sample rate 0010 0: AGC attack time = 9 × (32 / f_S) where f_S is the ADC sample rate ... 1111 0: AGC attack time = 61 × (32 / f_S) where f_S is the ADC sample rate 1111 1: AGC attack time = 63 × (32 / f_S) where f_S is the ADC sample rate

Table 7-120. Page 0 / Register 89 (0x59): AGC Attack Time (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D2–D0	R/W	000	000: Multiply factor for the programmed AGC attack time = 1 001: Multiply factor for the programmed AGC attack time = 2 010: Multiply factor for the programmed AGC attack time = 4 ... 111: Multiply factor for the programmed AGC attack time = 128

Table 7-121. Page 0 / Register 90 (0x5A): AGC Decay Time

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D3	R/W	0000 0	0000 0: AGC decay time = 1 × (512 / f_S) 0000 1: AGC decay time = 3 × (512 / f_S) 0001 0: AGC decay time = 5 × (512 / f_S) 0001 1: AGC decay time = 7 × (512 / f_S) 0010 0: AGC decay time = 9 × (512 / f_S) ... 1111 0: AGC decay time = 61 × (512 / f_S) 1111 1: AGC decay time = 63 × (512 / f_S)
D2–D0	R/W	000	000: Multiply factor for the programmed AGC decay time = 1 001: Multiply factor for the programmed AGC decay time = 2 010: Multiply factor for the programmed AGC decay time = 4 ... 111: Multiply factor for the programmed AGC decay time = 128

Table 7-122. Page 0 / Register 91 (0x5B): AGC Noise Debounce

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D0	R/W	0 0000	0 0000: AGC noise debounce = 0 / f_S 0 0001: AGC noise debounce = 4 / f_S 0 0010: AGC noise debounce = 8 / f_S 0 0011: AGC noise debounce = 16 / f_S 0 0100: AGC noise debounce = 32 / f_S 0 0101: AGC noise debounce = 64 / f_S 0 0110: AGC noise debounce = 128 / f_S 0 0111: AGC noise debounce = 256 / f_S 0 1000: AGC noise debounce = 512 / f_S 0 1001: AGC noise debounce = 1024 / f_S 0 1010: AGC noise debounce = 2048 / f_S 0 1011: AGC noise debounce = 4096 / f_S 0 1100: AGC noise debounce = 2 × 4096 / f_S 0 1101: AGC noise debounce = 3 × 4096 / f_S 0 1110: AGC noise debounce = 4 × 4096 / f_S ... 1 1110: AGC noise debounce = 20 × 4096 / f_S 1 1111: AGC noise debounce = 21 × 4096 / f_S

Table 7-123. Page 0 / Register 92 (0x5C): AGC Signal Debounce

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only zeros to these bits.

Table 7-123. Page 0 / Register 92 (0x5C): AGC Signal Debounce (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D3–D0	R/W	0000	0000: AGC signal debounce = 0 / f_S 0001: AGC signal debounce = 4 / f_S 0010: AGC signal debounce = 8 / f_S 0011: AGC signal debounce = 16 / f_S 0100: AGC signal debounce = 32 / f_S 0101: AGC signal debounce = 64 / f_S 0110: AGC signal debounce = 128 / f_S 0111: AGC signal debounce = 256 / f_S 1000: AGC signal debounce = 512 / f_S 1001: AGC signal debounce = 1024 / f_S 1010: AGC signal debounce = 2048 / f_S 1011: AGC signal debounce = 2 × 2048 / f_S 1100: AGC signal debounce = 3 × 2048 / f_S 1101: AGC signal debounce = 4 × 2048 / f_S 1110: AGC signal debounce = 5 × 2048 / f_S 1111: AGC signal debounce = 6 × 2048 / f_S

Table 7-124. Page 0 / Register 93 (0x5D): AGC Gain-Applied Reading

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	XXXX XXXX	1110 1000: Gain applied by AGC = –12 dB 1110 1001: Gain applied by AGC = –11.5 dB ... 0000 0000: Gain applied by AGC = 0 dB ... 0111 0011: Gain applied by AGC = 57.5 dB 0111 0100: Gain applied by AGC = 58 dB 0111 0101: Gain applied by AGC = 58.5 dB 0111 0110: Gain applied by AGC = 59 dB 0111 0111: Gain applied by AGC = 59.5 dB

Table 7-125. Page 0 / Register 94 Through Page 0 / Register 101: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-126. Page 0 / Register 102 (0x66): ADC DC Measurement 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: DC measurement is disabled for mono ADC channel 1: DC measurement is enabled for mono ADC channel
D6	R/W	0	Reserved. Write only reset value.
D5	R/W	0	0: DC measurement occurs based on first-order sync filter with averaging of 2^D 1: DC measurement occurs based on first-order low-pass IIR filter whose coefficients are calculated based on D value
D4–D0	R/W	00000	DC Measurement D setting: 00000: Reserved. Don't use. 00001: D = 1 00010: D = 2 ... 10011: D = 19 10100: D = 20 10101 to 11111: Reserved. Don't use.

Table 7-127. Page 0 / Register 103 (0x67): ADC DC Measurement 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only reset value.
D6	R/W	0	0: DC measurement data update is enabled. 1: DC measurement data update is disabled. User can read the last updated data without any data corruption.
D5	R/W	0	0: For IIR based DC measurement, the measurement value is the instantaneous output of the IIR filter 1: For IIR based DC measurement, the measurement value is update before periodic clearing of the IIR filter
D4–D0	R/W	00000	IIR based DC measurement, average time setting: 00000: Infinite average is used 00001: Averaging time is 2^1 ADC modulator clock periods 00010: Averaging time is 2^2 ADC modulator clock periods ... 10011: Averaging time is 2^{19} ADC modulator clock periods 10100: Averaging time is 2^{20} ADC modulator clock periods 10101 to 11111: Reserved. Don't use.

Table 7-128. Page 0 / Register 104 (0x67): ADC DC Measurement Output 1

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (23:16)

Table 7-129. Page 0 / Register 105 (0x68): ADC DC Measurement Output 2

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (15:8)

Table 7-130. Page 0 / Register 106 (0x69): ADC DC Measurement Output 3

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R	0000 0000	ADC DC Measurement Output (7:0)

Table 7-131. Page 0 / Register 107 Through Page 0 / Register 115: Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-132. Page 0 / Register 116 (0x74): VOL/MICDET-Pin SAR ADC — Volume Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION		
D7	R/W	0	0: DAC volume control is controlled by control register. (7-bit Vol ADC is powered down) 1: DAC volume control is controlled by pin.		
D6	R/W	0	0: Internal on-chip RC oscillator is used for the 7-bit Vol ADC for pin volume control. 1: MCLK is used for the 7-bit Vol ADC for pin volume control.		
D5–D4	R/W	00	00: No hysteresis for volume control ADC output 01: Hysteresis of ±1 bit 10: Hysteresis of ±2 bits 11: Reserved. Do not write this sequence to these bits.		
D3	R/W	0	Reserved. Write only reset value.		
D2–D0	R/W	000	Throughput of the 7-bit Vol ADC for pin volume control, frequency based on MCLK or internal oscillator.		
				MCLK = 12 MHz	**Internal Oscillator Source**
			000: Throughput = 001: Throughput = 010: Throughput = 011: Throughput = 100: Throughput = 101: Throughput = 110: Throughput = 111: Throughput =	15.625 Hz 31.25 Hz 62.5 Hz 125 Hz 250 Hz 500 Hz 1 kHz 2 kHz	10.68 Hz 21.35 Hz 42.71 Hz 8.2 Hz 170 Hz 340 Hz 680 Hz 1.37 kHz **Note**: These values are based on a nominal oscillator frequency of 8.2 MHz. The values scale to the actual oscillator frequency.

Table 7-133. Page 0 / Register 117 (0x75): VOL/MICDET-Pin Gain

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D0	R	XXX XXXX	000 0000: Gain applied by pin volume control = 18 dB 000 0001: Gain applied by pin volume control = 17.5 dB 000 0010: Gain applied by pin volume control = 17 dB ... 010 0011: Gain applied by pin volume control = 0.5 dB 010 0100: Gain applied by pin volume control = 0 dB 010 0101: Gain applied by pin volume control = –0.5 dB ... 101 1001: Gain applied by pin volume control = –26.5 dB 101 1010: Gain applied by pin volume control = –27 dB 101 1011: Gain applied by pin volume control = –28 dB ... 111 1101: Gain applied by pin volume control = –62 dB 111 1110: Gain applied by pin volume control = –63 dB 111 1111: Reserved.

Table 7-134. Page 0 / Register 118 (0x76) Through Page 0 / Register 127 (0x7F): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

7.4.2.2 Control Registers, Page 1: DAC and ADC Routing, PGA, Power-Controls, and MISC Logic-Related Programmability

Table 7-135. Page 1 / Register 0 (0x00): Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

Table 7-136. Page 1 / Register 1 (0x01) Through Page 1 / Register 29 (0x1D): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-137. Page 1 / Register 30 (0x1E): Headphone and Speaker Amplifier Error Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D2	R/W	0000 00	Reserved
D1	R/W	0	0: Reset SPL and SPR power-up control bits on short-circuit detection. 1: SPL and SPR power-up control bits remain unchanged on short-circuit detection.
D0	R/W	0	0: Reset HPL and HPR power-up control bits on short-circuit detection if page 1 / register 31, D1 = 1. 1: HPL and HPR power-up control bits remain unchanged on short-circuit detection.

Table 7-138. Page 1 / Register 31 (0x1F): Headphone Drivers

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: HPL output driver is powered down. 1: HPL output driver is powered up.
D6	R/W	0	0: HPR output driver is powered down. 1: HPR output driver is powered up.
D5	R/W	0	Reserved. Write only zero to this bit.
D4–D3	R/W	00	00: Output common-mode voltage = 1.35 V 01: Output common-mode voltage = 1.5 V 10: Output common-mode voltage = 1.65 V 11: Output common-mode voltage = 1.8 V
D2	R/W	1	Reserved. Write only 1 to this bit.
D1	R/W	0	0: If short-circuit protection is enabled for headphone driver and short circuit detected, device limits the maximum current to the load. 1: If short-circuit protection is enabled for headphone driver and short circuit detected, device powers down the output driver.
D0	R	0	0: Short circuit is not detected on the headphone driver. 1: Short circuit is detected on the headphone driver.

Table 7-139. Page 1 / Register 32 (0x20): Class-D Speaker Amplifier

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel class-D output driver is powered down. 1: Left-channel class-D output driver is powered up.
D6	R/W	0	0: Right-channel class-D output driver is powered down. 1: Right-channel class-D output driver is powered up.
D5–D1	R/W	00 011	Reserved. Write only the reset value to this bit.

Table 7-139. Page 1 / Register 32 (0x20): Class-D Speaker Amplifier (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R	0	0: Short circuit is not detected on the class-D driver. Valid only if class-D amplifier is powered up. For short-circuit flag sticky bit, see page 0 / register 44. 1: Short circuit is detected on the class-D driver. Valid only if class-D amp is powered-up. For short-circuit flag sticky bit, see page 0 / register 44.

Table 7-140. Page 1 / Register 33 (0x21): HP Output Drivers POP Removal Settings

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: If the power down sequence is activated by device software, power down using page 1 / register 46, bit D7, then power down the DAC simultaneously with the HP and SP amplifiers. 1: If the power down sequence is activated by device software, power down using page 1 / register 46, bit D7, then power down DAC only after HP and SP amplifiers are completely powered down. This is to optimize power-down POP.
D6–D3	R/W	0111	0000: Driver power-on time = 0 µs 0001: Driver power-on time = 15.3 µs 0010: Driver power-on time = 153 µs 0011: Driver power-on time = 1.53 ms 0100: Driver power-on time = 15.3 ms 0101: Driver power-on time = 76.2 ms 0110: Driver power-on time = 153 ms 0111: Driver power-on time = 304 ms 1000: Driver power-on time = 610 ms 1001: Driver power-on time = 1.22 s 1010: Driver power-on time = 3.04 s 1011: Driver power-on time = 6.1 s 1100–1111: Reserved. Do not write these sequences to these bits. **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D2–D1	R/W	11	00: Driver ramp-up step time = 0 ms 01: Driver ramp-up step time = 0.98 ms 10: Driver ramp-up step time = 1.95 ms 11: Driver ramp-up step time = 3.9 ms **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D0	R/W	0	0: Weakly driven output common-mode voltage is generated from resistor divider of the AVDD supply. 1: Reserved

Table 7-141. Page 1 / Register 34 (0x22): Output Driver PGA Ramp-Down Period Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only the reset value to this bit.
D6–D4	R/W	000	Speaker power-up wait time (duration based on using internal oscillator) 000: Wait time = 0 ms 001: Wait time = 3.04 ms 010: Wait time = 7.62 ms 011: Wait time = 12.2 ms 100: Wait time = 15.3 ms 101: Wait time = 19.8 ms 110: Wait time = 24.4 ms 111: Wait time = 30.5 ms **Note**: These values are based on typical oscillator frequency of 8.2 MHz. Scale according to the actual oscillator frequency.
D3–D0	R/W	0000	Reserved. Write only the reset value to these bits.

Table 7-142. Page 1 / Register 35 (0x23): DAC_L and DAC_R Output Mixer Routing

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6	R/W	00	00: DAC_L is not routed anywhere. 01: DAC_L is routed to the left-channel mixer amplifier. 10: DAC_L is routed directly to the HPL driver. 11: Reserved
D5	R/W	0	0: MIC1LP input is not routed to the left-channel mixer amplifier. 1: MIC1LP input is routed to the left-channel mixer amplifier.
D4		0	0: MIC1RP input is not routed to the left-channel mixer amplifier. 1: MIC1RP input is routed to the left-channel mixer amplifier.
D3–D2	R/W	00	00: DAC_R is not routed anywhere. 01: DAC_R is routed to the right-channel mixer amplifier. 10: DAC_R is routed directly to the HPR driver. 11: Reserved
D1	R/W	0	0: MIC1RP input is not routed to the right-channel mixer amplifier. 1: MIC1RP input is routed to the right-channel mixer amplifier.
D0	R/W	0	0: HPL driver output is not routed to the HPR driver. 1: HPL driver output is routed to the HPR driver input (used for differential output mode).

Table 7-143. Page 1 / Register 36 (0x24): Left Analog Volume to HPL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel analog volume to left-channel headphone output driver is muted if bits D6–D0 are also 111 1111. 1: Left-channel analog volume control is routed to HPL output driver.
D6–D0	R/W	111 1111	Left-channel analog volume control gain (non-linear) for the HPL output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-144. Page 1 / Register 37 (0x25): Right Analog Volume to HPR

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right-channel analog volume to right-channel headphone output driver is muted if bits D6–D0 are also 111 1111. 1: Right-channel analog volume control is routed to HPR output driver.
D6–D0	R/W	111 1111	Right-channel analog volume control gain (non-linear) for the HPR output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-145. Page 1 / Register 38 (0x26): Left Analog Volume to SPL

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Left-channel analog volume to left-channel class-D output driver is muted if bits D6–D0 are also 111 1111. 1: Left-channel analog volume control output is routed to left-channel class-D output driver.
D6–D0	R/W	111 1111	Left-channel analog volume control output gain (non-linear) for the left-channel class-D output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-146. Page 1 / Register 39 (0x27): Right Analog Volume to SPR

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Right-channel analog volume to right-channel class-D output driver is muted if bits D6–D0 are also 111 1111. 1: Right-channel analog volume control output is routed to right-channel class-D output driver.
D6–D0	R/W	111 1111	Right-channel analog volume control output gain (non-linear) for the right-channel class-D output driver, 0 dB to –78 dB. See Table 7-38.

Table 7-147. Page 1 / Register 40 (0x28): HPL Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D3	R/W	0000	0000: HPL driver PGA = 0 dB 0001: HPL driver PGA = 1 dB 0010: HPL driver PGA = 2 dB ... 1000: HPL driver PGA = 8 dB 1001: HPL driver PGA = 9 dB 1010–1111: Reserved. Do not write these sequences to these bits.
D2	R/W	0	0: HPL driver is muted. 1: HPL driver is not muted.
D1	R/W	1	Reserved
D0	R	0	0: Not all programmed gains to HPL have been applied yet. 1: All programmed gains to HPL have been applied.

Table 7-148. Page 1 / Register 41 (0x29): HPR Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	Reserved. Write only zero to this bit.
D6–D3	R/W	0000	0000: HPR driver PGA = 0 dB 0001: HPR driver PGA = 1 dB 0010: HPR driver PGA = 2 dB ... 1000: HPR driver PGA = 8 dB 1001: HPR driver PGA = 9 dB 1010–1111: Reserved. Do not write these sequences to these bits.
D2	R/W	0	0: HPR driver is muted. 1: HPR driver is not muted.
D1	R/W	1	Reserved. Write only '1' to this bit.
D0	R	0	0: Not all programmed gains to HPR have been applied yet. 1: All programmed gains to HPR have been applied.

Table 7-149. Page 1 / Register 42 (0x2A): SPL Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D3	R/W	00	00: Left-channel class-D driver output stage gain = 6 dB 01: Left-channel class-D driver output stage gain = 12 dB 10: Left-channel class-D driver output stage gain = 18 dB 11: Left-channel class-D driver output stage gain = 24 dB
D2	R/W	0	0: Left-channel class-D driver is muted. 1: Left-channel class-D driver is not muted.
D1	R/W	0	Reserved. Write only zero to this bit.
D0	R	0	0: Not all programmed gains to the Left-channel class-D driver have been applied yet. 1: All programmed gains to the Left-channel class-D driver have been applied.

Table 7-150. Page 1 / Register 43 (0x2B): SPR Driver

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D5	R/W	000	Reserved. Write only zeros to these bits.
D4–D3	R/W	00	00: Right-channel class-D driver output stage gain = 6 dB 01: Right-channel class-D driver output stage gain = 12 dB 10: Right-channel class-D driver output stage gain = 18 dB 11: Right-channel class-D driver output stage gain = 24 dB
D2	R/W	0	0: Right-channel class-D driver is muted. 1: Right-channel class-D driver is not muted.

Table 7-150. Page 1 / Register 43 (0x2B): SPR Driver (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D1	R/W	0	Reserved. Write only zero to this bit.
D0	R	0	0: Not all programmed gains to right-channel class-D driver have been applied yet. 1: All programmed gains to right-channel class-D driver have been applied.

Table 7-151. Page 1 / Register 44 (0x2C): HP Driver Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION		
D7–D5	R/W	000	Debounce time for the headset short-circuit detection		
			(1)	**MCLK/DIV (Page 3 / register 16) = 1-MHz Source**	**Internal Oscillator Source**
			000: Debounce time = 001: Debounce time = 010: Debounce time = 011: Debounce time = 100: Debounce time = 101: Debounce time = 110: Debounce time = 111: Debounce time =	0 µs 8 µs 16 µs 32 µs 64 µs 128 µs 256 µs 512 µs	0 µs 7.8 µs 15.6 µs 31.2 µs 62.4 µs 124.9 µs 250 µs 500 µs **Note**: These values are based on a nominal oscillator frequency of 8.2 MHz. The values scale to the actual oscillator frequency.
D4–D3	R/W	00	00: Default mode for the DAC 01: DAC performance increased by increasing the current 10: Reserved 11: DAC performance increased further by increasing the current again		
D2	R/W	0	0: HPL output driver is programmed as headphone driver. 1: HPL output driver is programmed as lineout driver.		
D1	R/W	0	0: HPR output driver is programmed as headphone driver. 1: HPR output driver is programmed as lineout driver.		
D0	R/W	0	Reserved. Write only zero to this bit.		

(1) The clock used for the debounce has a clock period = debounce duration / 8.

Table 7-152. Page 1 / Register 45 (0x2D): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Do not write to these registers.

Table 7-153. Page 1 / Register 46 (0x2E): MICBIAS

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: Device software power down is not enabled. 1: Device software power down is enabled.
D6–D4	R/W	000	Reserved. Write only zeros to these bits.
D3	R/W	0	0: Programmed MICBIAS is not powered up if headset detection is enabled but headset is not inserted. 1: Programmed MICBIAS is powered up even if headset is not inserted.
D2	R/W	0	Reserved. Write only zero to this bit.
D1–D0	R/W	00	00: MICBIAS output is powered down. 01: MICBIAS output is powered to 2 V. 10: MICBIAS output is powered to 2.5 V. 11: MICBIAS output is powered to AVDD.

Table 7-154. Page 1 / Register 48 (0x30): Delta-Sigma Mono ADC Channel Fine-Gain Input Selection for P-Terminal

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6 (1)	R/W	00	00: MIC1LP is not selected for the MIC PGA. 01: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: MIC1LP is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D5–D4	R/W	00	00: MIC1RP is not selected for the MIC PGA. 01: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ 10: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ 11: MIC1RP is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ
D3–D2	R/W	00	00: MIC1LM is not selected for the MIC PGA. 01: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ 10: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ 11: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ
D1–D0	R/W	00	Reserved. Write only zeros to these bits.

(1) Input impedance selection affects the microphone PGA gain. See Section 7.3.9.1 for details.

Table 7-155. Page 1 / Register 49 (0x31): ADC Input Selection for M-Terminal

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D6 (1)	R/W	00	00: CM is not selected for the MIC PGA. 01: CM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: CM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: CM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D5–D4		00	00: MIC1LM is not selected for the MIC PGA. 01: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 10 kΩ. 10: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 20 kΩ. 11: MIC1LM is selected for the MIC PGA with feed-forward resistance RIN = 40 kΩ.
D3–D0	R/W	0000	Reserved. Write only zeros to these bits.

(1) Input impedance selection affects the microphone PGA gain. See Section 7.3.9.1 for details.

Table 7-156. Page 1 / Register 50 (0x32): Input CM Settings

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	0	0: MIC1LP input is floating, if it is not used for the MIC PGA and analog bypass. 1: MIC1LP input is connected to CM internally, if it is not used for the MIC PGA and analog bypass.
D6	R/W	0	0: MIC1RP input is floating, if it is not used for the MIC PGA and analog bypass. 1: MIC1RP input is connected to CM internally, if it is not used for the MIC PGA and analog bypass.
D5	R/W	0	0: MIC1LM input is floating, if it is not used for the MIC PGA. 1: MIC1LM input is connected to CM internally, if it is not used for the MIC PGA.
D4–D1	R/W	00 00	Reserved. Write only zeros to these bits.
D0	R	0	0: Not all programmed analog gains to the ADC have been applied yet. 1: All programmed analog gains to the ADC have been applied.

Table 7-157. Page 1 / Register 51 (0x33) Through Page 1 / Register 127 (0x7F): Reserved

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	XXXX XXXX	Reserved. Write only the reset value to these bits.

7.4.2.3 Control Registers, Page 3: MCLK Divider for Programmable Delay Timer

Default values shown for this page only become valid 100 µs following a hardware or software reset.

Table 7-158. Page 3 / Register 0 (0x00): Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The only register used in page 3 is register 16. The remaining page-3 registers are reserved and must not be written to.

Table 7-159. Page 3 / Register 16 (0x10): Timer Clock MCLK Divider

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7	R/W	1	0: Internal oscillator is used for programmable delay timer. 1: External MCLK(1) is used for programmable delay timer.
D6–D0	R/W	000 0001	MCLK Divider to Generate 1-MHz Clock for the Programmable Delay Timer 000 0000: MCLK divider = 128 000 0001: MCLK divider = 1 000 0010: MCLK divider = 2 ... 111 1110: MCLK divider = 126 111 1111: MCLK divider = 127

(1) External clock is used only to control the delay programmed between the conversions and not used for doing the actual conversion. This feature is provided in case a more accurate delay is desired because the internal oscillator frequency varies from device to device.

7.4.2.4 Control Registers, Page 4: ADC Digital Filter Coefficients

Default values shown for this page only become valid 100 µs following a hardware or software reset.

Table 7-160. Page 4 / Register 0 (0x00): Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-4 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3110. Reserved registers must not be written to.

The filter coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-4 registers, excepting the previously described register 0.

Table 7-161. Page-4 Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1 (0x01)	XXXX XXXX	Reserved. Do not write to this register.
2 (0x02)	0000 0001	8 MSBs of N0 coefficient for AGC LPF (first-order IIR) used as averager to detect level

Table 7-161. Page-4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
3 (0x03)	0001 0111	8 LSBs of N0 coefficient for AGC LPF (first-order IIR) used as averager to detect level
4 (0x04)	0000 0001	8 MSBs of N1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
5 (0x05)	0001 0111	8 LSBs of N1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
6 (0x06)	0111 1101	8 MSBs of D1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
7 (0x07)	1101 0011	8 LSBs of D1 coefficient for AGC LPF (first-order IIR) used as averager to detect level
8 (0x08)	0111 1111	8 MSBs of N0 coefficient for ADC-programmable first-order IIR
9 (0x09)	1111 1111	8 LSBs of N0 coefficient for ADC-programmable first-order IIR
10 (0x0A)	0000 0000	8 MSBs of N1 coefficient for ADC-programmable first-order IIR
11 (0x0B)	0000 0000	8 LSBs of N1 coefficient for ADC-programmable first-order IIR
12 (0x0C)	0000 0000	8 MSBs of D1 coefficient for ADC-programmable first-order IIR
13 (0x0D)	0000 0000	8 LSBs of D1 coefficient for ADC-programmable first-order IIR
14 (0x0E)	0111 1111	Coefficient N0(15:8) for ADC biquad A or coefficient FIR0(15:8) for ADC FIR filter
15 (0x0F)	1111 1111	Coefficient N0(7:0) for ADC biquad A or coefficient FIR0(7:0) for ADC FIR filter
16 (0x10)	0000 0000	Coefficient N1(15:8) for ADC biquad A or coefficient FIR1(15:8) for ADC FIR filter
17 (0x11)	0000 0000	Coefficient N1(7:0) for ADC biquad A or coefficient FIR1(7:0) for ADC FIR filter
18 (0x12)	0000 0000	Coefficient N2(15:8) for ADC biquad A or coefficient FIR2(15:8) for ADC FIR filter
19 (0x13)	0000 0000	Coefficient N2(7:0) for ADC biquad A or coefficient FIR2(7:0) for ADC FIR filter
20 (0x14)	0000 0000	Coefficient D1(15:8) for ADC biquad A or coefficient FIR3(15:8) for ADC FIR filter
21 (0x15)	0000 0000	Coefficient D1(7:0) for ADC biquad A or coefficient FIR3(7:0) for ADC FIR filter
22 (0x16)	0000 0000	Coefficient D2(15:8) for ADC biquad A or coefficient FIR4(15:8) for ADC FIR filter
23 (0x17)	0000 0000	Coefficient D2(7:0) for ADC biquad A or coefficient FIR4(7:0) for ADC FIR filter
24 (0x18)	0111 1111	Coefficient N0(15:8) for ADC biquad B or coefficient FIR5(15:8) for ADC FIR filter
25 (0x19)	1111 1111	Coefficient N0(7:0) for ADC biquad B or coefficient FIR5(7:0) for ADC FIR filter
26 (0x1A)	0000 0000	Coefficient N1(15:8) for ADC biquad B or coefficient FIR6(15:8) for ADC FIR filter
27 (0x1B)	0000 0000	Coefficient N1(7:0) for ADC biquad B or coefficient FIR6(7:0) for ADC FIR filter
28 (0x1C)	0000 0000	Coefficient N2(15:8) for ADC biquad B or coefficient FIR7(15:8) for ADC FIR filter
29 (0x1D)	0000 0000	Coefficient N2(7:0) for ADC biquad B or coefficient FIR7(7:0) for ADC FIR filter
30 (0x1E)	0000 0000	Coefficient D1(15:8) for ADC biquad B or coefficient FIR8(15:8) for ADC FIR filter
31 (0x1F)	0000 0000	Coefficient D1(7:0) for ADC biquad B or coefficient FIR8(7:0) for ADC FIR filter
32 (0x20)	0000 0000	Coefficient D2(15:8) for ADC biquad B or coefficient FIR9(15:8) for ADC FIR filter
33 (0x21)	0000 0000	Coefficient D2(7:0) for ADC biquad B or coefficient FIR9(7:0) for ADC FIR filter
34 (0x22)	0111 1111	Coefficient N0(15:8) for ADC biquad C or coefficient FIR10(15:8) for ADC FIR filter
35 (0x23)	1111 1111	Coefficient N0(7:0) for ADC biquad C or coefficient FIR10(7:0) for ADC FIR filter
36 (0x24)	0000 0000	Coefficient N1(15:8) for ADC biquad C or coefficient FIR11(15:8) for ADC FIR filter
37 (0x25)	0000 0000	Coefficient N1(7:0) for ADC biquad C or coefficient FIR11(7:0) for ADC FIR filter
38 (0x26)	0000 0000	Coefficient N2(15:8) for ADC biquad C or coefficient FIR12(15:8) for ADC FIR filter
39 (0x27)	0000 0000	Coefficient N2(7:0) for ADC biquad C or coefficient FIR12(7:0) for ADC FIR filter
40 (0x28)	0000 0000	Coefficient D1(15:8) for ADC biquad C or coefficient FIR13(15:8) for ADC FIR filter
41 (0x29)	0000 0000	Coefficient D1(7:0) for ADC biquad C or coefficient FIR13(7:0) for ADC FIR filter
42 (0x2A)	0000 0000	Coefficient D2(15:8) for ADC biquad C or coefficient FIR14(15:8) for ADC FIR filter
43 (0x2B)	0000 0000	Coefficient D2(7:0) for ADC biquad C or coefficient FIR14(7:0) for ADC FIR filter
44 (0x2C)	0111 1111	Coefficient N0(15:8) for ADC biquad D or coefficient FIR15(15:8) for ADC FIR filter
45 (0x2D)	1111 1111	Coefficient N0(7:0) for ADC biquad D or coefficient FIR15(7:0) for ADC FIR filter
46 (0x2E)	0000 0000	Coefficient N1(15:8) for ADC biquad D or coefficient FIR16(15:8) for ADC FIR filter
47 (0x2F)	0000 0000	Coefficient N1(7:0) for ADC biquad D or coefficient FIR16(7:0) for ADC FIR filter
48 (0x30)	0000 0000	Coefficient N2(15:8) for ADC biquad D or coefficient FIR17(15:8) for ADC FIR filter
49 (0x31)	0000 0000	Coefficient N2(7:0) for ADC biquad D or coefficient FIR17(7:0) for ADC FIR filter

Table 7-161. Page-4 Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
50 (0x32)	0000 0000	Coefficient D1(15:8) for ADC biquad D or coefficient FIR18(15:8) for ADC FIR filter
51 (0x33)	0000 0000	Coefficient D1(7:0) for ADC biquad D or coefficient FIR18(7:0) for ADC FIR filter
52 (0x34)	0000 0000	Coefficient D2(15:8) for ADC biquad D or coefficient FIR19(15:8) for ADC FIR filter
53 (0x35)	0000 0000	Coefficient D2(7:0) for ADC biquad D or coefficient FIR19(7:0) for ADC FIR filter
54 (0x36)	0111 1111	Coefficient N0(15:8) for ADC biquad E or coefficient FIR20(15:8) for ADC FIR filter
55 (0x37)	1111 1111	Coefficient N0(7:0) for ADC biquad E or coefficient FIR20(7:0) for ADC FIR filter
56 (0x38)	0000 0000	Coefficient N1(15:8) for ADC biquad E or coefficient FIR21(15:8) for ADC FIR filter
57 (0x39)	0000 0000	Coefficient N1(7:0) for ADC biquad E or coefficient FIR21(7:0) for ADC FIR filter
58 (0x3A)	0000 0000	Coefficient N2(15:8) for ADC biquad E or coefficient FIR22(15:8) for ADC FIR filter
59 (0x3B)	0000 0000	Coefficient N2(7:0) for ADC biquad E or coefficient FIR22(7:0) for ADC FIR filter
60 (0x3C)	0000 0000	Coefficient D1(15:8) for ADC biquad E or coefficient FIR23(15:8) for ADC FIR filter
61 (0x3D)	0000 0000	Coefficient D1(7:0) for ADC biquad E or coefficient FIR23(7:0) for ADC FIR filter
62 (0x3E)	0000 0000	Coefficient D2(15:8) for ADC biquad E or coefficient FIR24(15:8) for ADC FIR filter
63 (0x3F)	0000 0000	Coefficient D2(7:0) for ADC biquad E or coefficient FIR24(7:0) for ADC FIR filter
64-127	0000 0000	Reserved. Write only reset values.

7.4.2.5 Control Registers, Page 8: DAC Digital Filter Coefficients

Default values shown for this page only become valid 100 µs following a hardware or software reset.

Table 7-162. Page 8 / Register 0: Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-8 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3110. Reserved registers must not be written to.

The filter coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-8 registers, excepting the previously described register 0.

Table 7-163. Page 8 / Register 1 (0x01) : DAC Coefficient Buffer Control

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D4	R/W	0000	Reserved. Write only the reset value.
D3	R	0	DAC PRB generated flag for toggling MSB of coefficient RAM address (only used in non-adaptive mode)
D2	R/W	0	DAC Adaptive Filtering Control 0: Adaptive filtering disabled in DAC Processing Blocks 1: Adaptive filtering enabled in DAC Processing Blocks
D1	R	0	DAC Adaptive Filter Buffer Control Flag 0: In adaptive filter mode, DAC Processing Blocks accesses DAC coefficient Buffer A and the external control interface accesses DAC coefficient Buffer B 1: In adaptive filter mode, DAC Processing Blocks accesses DAC coefficient Buffer B and the external control interface accesses DAC coefficient Buffer A

Table 7-163. Page 8 / Register 1 (0x01) : DAC Coefficient Buffer Control (continued)

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D0	R/W	0	DAC Adaptive Filter Buffer Switch Control 0: DAC coefficient buffers are not switched at the next frame boundary. 1: DAC coefficient buffers are switched at the next frame boundary, if adaptive filtering mode is enabled. This bit self-clears on switching.

Table 7-164. Page-8 DAC Buffer A Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
2 (0x02)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad A
3 (0x03)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad A
4 (0x04)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad A
5 (0x05)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad A
6 (0x06)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad A
7 (0x07)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad A
8 (0x08)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad A
9 (0x09)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad A
10 (0x0A)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad A
11 (0x0B)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad A
12 (0x0C)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad B
13 (0x0D)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad B
14 (0x0E)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad B
15 (0x0F)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad B
16 (0x10)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad B
17 (0x11)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad B
18 (0x12)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad B
19 (0x13)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad B
20 (0x14)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad B
21 (0x15)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad B
22 (0x16)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad C
23 (0x17)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad C
24 (0x18)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad C
25 (0x19)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad C
26 (0x1A)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad C
27 (0x1B)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad C
28 (0x1C)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad C

Table 7-164. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
29 (0x1D)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad C
30 (0x1E)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad C
31 (0x1F)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad C
32 (0x20)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad D
33 (0x21)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad D
34 (0x22)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad D
35 (0x23)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad D
36 (0x24)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad D
37 (0x25)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad D
38 (0x26)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad D
39 (0x27)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad D
40 (0x28)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad D
41 (0x29)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad D
42 (0x2A)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad E
43 (0x2B)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad E
44 (0x2C)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad E
45 (0x2D)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad E
46 (0x2E)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad E
47 (0x2F)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad E
48 (0x30)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad E
49 (0x31)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad E
50 (0x32)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad E
51 (0x33)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad E
52 (0x34)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad F
53 (0x35)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad F
54 (0x36)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad F
55 (0x37)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad F
56 (0x38)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad F
57 (0x39)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad F
58 (0x3A)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad F
59 (0x3B)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad F
60 (0x3C)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad F
61 (0x3D)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad F
62 (0x3E)	0000 0000	Reserved
63 (0x3F)	0000 0000	Reserved
64 (0x40)	0000 0000	8 MSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
65 (0x41)	0000 0000	8 LSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
66 (0x42)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad A
67 (0x43)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad A
68 (0x44)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad A
69 (0x45)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad A
70 (0x46)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad A
71 (0x47)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad A
72 (0x48)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad A
73 (0x49)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad A
74 (0x4A)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad A
75 (0x4B)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad A

Table 7-164. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
76 (0x4C)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad B
77 (0x4D)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad B
78 (0x4E)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad B
79 (0x4F)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad B
80 (0x50)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad B
81 (0x51)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad B
82 (0x52)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad B
83 (0x53)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad B
84 (0x54)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad B
85 (0x55)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad B
86 (0x56)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad C
87 (0x57)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad C
88 (0x58)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad C
89 (0x59)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad C
90 (0x5A)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad C
91 (0x5B)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad C
92 (0x5C)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad C
93 (0x5D)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad C
94 (0x5E)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad C
95 (0x5F)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad C
96 (0x60)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad D
97 (0x61)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad D
98 (0x62)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad D
99 (0x63)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad D
100 (0x64)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad D
101 (0x65)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad D
102 (0x66)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad D
103 (0x67)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad D
104 (0x68)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad D
105 (0x69)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad D
106 (0x6A)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad E
107 (0x6B)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad E
108 (0x6C)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad E
109 (0x6D)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad E
110 (0x6E)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad E
111 (0x6F)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad E
112 (0x70)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad E
113 (0x71)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad E
114 (0x72)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad E
115 (0x73)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad E
116 (0x74)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad F
117 (0x75)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad F
118 (0x76)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad F
119 (0x77)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad F
120 (0x78)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad F
121 (0x79)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad F
122 (0x7A)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad F

Table 7-164. Page-8 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
123 (0x7B)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad F
124 (0x7C)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad F
125 (0x7D)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad F
126 (0x7E)	0000 0000	Reserved
127 (0x7F)	0000 0000	Reserved

7.4.2.6 Control Registers, Page 9: DAC Digital Filter Coefficients

Default values shown for this page only become valid 100 µs following a hardware or software reset.

Table 7-165. Page 9 / Register 0 (0x00): Page Control Register

BIT	READ/ WRITE	RESET VALUE	DESCRIPTION
D7–D0	R/W	0000 0000	0000 0000: Page 0 selected 0000 0001: Page 1 selected ... 1111 1110: Page 254 selected 1111 1111: Page 255 selected

The remaining page-9 registers are either reserved registers or are used for setting coefficients for the various filters in the TLV320AIC3110. Reserved registers must not be written to.

The filter-coefficient registers are arranged in pairs, with two adjacent 8-bit registers containing the 16-bit coefficient for a single filter. The 16-bit integer contained in the MSB and LSB registers for a coefficient are interpreted as a 2s-complement integer, with possible values ranging from –32 768 to 32 767. When programming any coefficient value for a filter, the MSB register must always be written first, immediately followed by the LSB register. Even if only the MSB or LSB portion of the coefficient changes, both registers must be written in this sequence. is a list of the page-9 registers, excepting the previously described register 0.

Table 7-166. Page-9 DAC Buffer A Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	XXXX XXXX	Reserved. Do not write to this register.
2 (0x02)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable first-order IIR
3 (0x03)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable first-order IIR
4 (0x04)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable first-order IIR
5 (0x05)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable first-order IIR
6 (0x06)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable first-order IIR
7 (0x07)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable first-order IIR
8 (0x08)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable first-order IIR
9 (0x09)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable first-order IIR
10 (0x0A)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable first-order IIR
11 (0x0B)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable first-order IIR
12 (0x0C)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable first-order IIR
13 (0x0D)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable first-order IIR
14 (0x0E)	0111 1111	8 MSBs of n0 coefficient for DRC first-order high-pass filter
15 (0x0F)	1111 0111	8 LSBs of n0 coefficient for DRC first-order high-pass filter
16 (0x10)	1000 0000	8 MSBs of n1 coefficient for DRC first-order high-pass filter
17 (0x11)	0000 1001	8 LSBs of n1 coefficient for DRC first-order high-pass filter
18 (0x12)	0111 1111	8 MSBs of d1 coefficient for DRC first-order high-pass filter

Table 7-166. Page-9 DAC Buffer A Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
19 (0x13)	1110 1111	8 LSBs of d1 coefficient for DRC first-order high-pass filter
20 (0x14)	0000 0000	8 MSBs of n0 coefficient for DRC first-order low-pass filter
21 (0x15)	0001 0001	8 LSBs of n0 coefficient for DRC first-order low-pass filter
22 (0x16)	0000 0000	8 MSBs of n1 coefficient for DRC first-order low-pass filter
23 (0x17)	0001 0001	8 LSBs of n1 coefficient for DRC first-order low-pass filter
24 (0x18)	0111 1111	8 MSBs of d1 coefficient for DRC first-order low-pass filter
25 (0x19)	1101 1110	8 LSBs of d1 coefficient for DRC first-order low-pass filter
26-127	0000 0000	Reserved

7.4.2.7 Control Registers, Page 12: DAC Programmable Coefficients Buffer B (1:63)

Table 7-167. Page-12 DAC Buffer B Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	0000 0000	Reserved. Do not write to this register.
2 (0x02)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad A
3 (0x03)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad A
4 (0x04)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad A
5 (0x05)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad A
6 (0x06)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad A
7 (0x07)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad A
8 (0x08)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad A
9 (0x09)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad A
10 (0x0A)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad A
11 (0x0B)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad A
12 (0x0C)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad B
13 (0x0D)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad B
14 (0x0E)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad B
15 (0x0F)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad B
16 (0x10)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad B
17 (0x11)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad B
18 (0x12)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad B
19 (0x13)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad B
20 (0x14)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad B
21 (0x15)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad B
22 (0x16)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad C
23 (0x17)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad C
24 (0x18)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad C
25 (0x19)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad C
26 (0x1A)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad C
27 (0x1B)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad C
28 (0x1C)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad C
29 (0x1D)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad C
30 (0x1E)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad C
31 (0x1F)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad C
32 (0x20)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad D
33 (0x21)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad D

Table 7-167. Page-12 DAC Buffer B Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
34 (0x22)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad D
35 (0x23)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad D
36 (0x24)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad D
37 (0x25)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad D
38 (0x26)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad D
39 (0x27)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad D
40 (0x28)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad D
41 (0x29)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad D
42 (0x2A)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad E
43 (0x2B)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad E
44 (0x2C)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad E
45 (0x2D)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad E
46 (0x2E)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad E
47 (0x2F)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad E
48 (0x30)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad E
49 (0x31)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad E
50 (0x32)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad E
51 (0x33)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad E
52 (0x34)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable biquad F
53 (0x35)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable biquad F
54 (0x36)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable biquad F
55 (0x37)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable biquad F
56 (0x38)	0000 0000	8 MSBs of n2 coefficient for left DAC-programmable biquad F
57 (0x39)	0000 0000	8 LSBs of n2 coefficient for left DAC-programmable biquad F
58 (0x3A)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable biquad F
59 (0x3B)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable biquad F
60 (0x3C)	0000 0000	8 MSBs of d2 coefficient for left DAC-programmable biquad F
61 (0x3D)	0000 0000	8 LSBs of d2 coefficient for left DAC-programmable biquad F
62 (0x3E)	0000 0000	Reserved
63 (0x3F)	0000 0000	Reserved
64 (0x40)	0000 0000	8 MSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
65 (0x41)	0000 0000	8 LSBs 3D PGA Gain for PRB_P23, PRB_P24 and PRB_P25
66 (0x42)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad A
67 (0x43)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad A
68	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad A
69 (0x45)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad A
70 (0x46)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad A
71 (0x47)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad A
72 (0x48)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad A
73 (0x49)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad A
74 (0x4A)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad A
75 (0x4B)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad A
76 (0x4C)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad B
77 (0x4D)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad B
78 (0x4E)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad B
79 (0x4F)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad B
80 (0x50)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad B

Table 7-167. Page-12 DAC Buffer B Registers (continued)

REGISTER NUMBER	RESET VALUE	REGISTER NAME
81 (0x51)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad B
82 (0x52)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad B
83 (0x53)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad B
84 (0x54)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad B
85 (0x55)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad B
86 (0x56)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad C
87 (0x57)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad C
88 (0x58)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad C
89 (0x59)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad C
90 (0x5A)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad C
91 (0x5B)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad C
92 (0x5C)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad C
93 (0x5D)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad C
94 (0x5E)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad C
95 (0x5F)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad C
96 (0x60)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad D
97 (0x61)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad D
98 (0x62)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad D
99 (0x63)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad D
100 (0x64)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad D
101 (0x65)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad D
102 (0x66)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad D
103 (0x67)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad D
104 (0x68)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad D
105 (0x69)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad D
106 (0x6A)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad E
107 (0x6B)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad E
108 (0x6C)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad E
109 (0x6D)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad E
110 (0x6E)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad E
111 (0x6F)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad E
112 (0x70)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad E
113 (0x71)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad E
114 (0x72)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad E
115 (0x73)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad E
116 (0x74)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable biquad F
117 (0x75)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable biquad F
118 (0x76)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable biquad F
119 (0x77)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable biquad F
120 (0x78)	0000 0000	8 MSBs of n2 coefficient for right DAC-programmable biquad F
121 (0x79)	0000 0000	8 LSBs of n2 coefficient for right DAC-programmable biquad F
122 (0x7A)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable biquad F
123 (0x7B)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable biquad F
124 (0x7C)	0000 0000	8 MSBs of d2 coefficient for right DAC-programmable biquad F
125 (0x7D)	0000 0000	8 LSBs of d2 coefficient for right DAC-programmable biquad F
126	0000 0000	Reserved
127	0000 0000	Reserved

7.4.2.8 Control Registers, Page 13: DAC Programmable Coefficients RAM Buffer B (65:127)

Table 7-168. Page-13 DAC Buffer B Registers

REGISTER NUMBER	RESET VALUE	REGISTER NAME
1	0000 0000	Reserved. Do not write to this register.
2 (0x02)	0111 1111	8 MSBs of n0 coefficient for left DAC-programmable first-order IIR
3 (0x03)	1111 1111	8 LSBs of n0 coefficient for left DAC-programmable first-order IIR
4 (0x04)	0000 0000	8 MSBs of n1 coefficient for left DAC-programmable first-order IIR
5 (0x05)	0000 0000	8 LSBs of n1 coefficient for left DAC-programmable first-order IIR
6 (0x06)	0000 0000	8 MSBs of d1 coefficient for left DAC-programmable first-order IIR
7 (0x07)	0000 0000	8 LSBs of d1 coefficient for left DAC-programmable first-order IIR
8 (0x08)	0111 1111	8 MSBs of n0 coefficient for right DAC-programmable first-order IIR
9 (0x09)	1111 1111	8 LSBs of n0 coefficient for right DAC-programmable first-order IIR
10 (0x0A)	0000 0000	8 MSBs of n1 coefficient for right DAC-programmable first-order IIR
11 (0x0B)	0000 0000	8 LSBs of n1 coefficient for right DAC-programmable first-order IIR
12 (0x0C)	0000 0000	8 MSBs of d1 coefficient for right DAC-programmable first-order IIR
13 (0x0D)	0000 0000	8 LSBs of d1 coefficient for right DAC-programmable first-order IIR
14 (0x0E)	0111 1111	8 MSBs of n0 coefficient for DRC first-order high-pass filter
15 (0x0F)	1111 0111	8 LSBs of n0 coefficient for DRC first-order high-pass filter
16 (0x10)	1000 0000	8 MSBs of n1 coefficient for DRC first-order high-pass filter
17 (0x11)	0000 1001	8 LSBs of n1 coefficient for DRC first-order high-pass filter
18 (0x12)	0111 1111	8 MSBs of d1 coefficient for DRC first-order high-pass filter
19 (0x13)	1110 1111	8 LSBs of d1 coefficient for DRC first-order high-pass filter
20 (0x14)	0000 0000	8 MSBs of n0 coefficient for DRC first-order low-pass filter
21 (0x15)	0001 0001	8 LSBs of n0 coefficient for DRC first-order low-pass filter
22 (0x16)	0000 0000	8 MSBs of n1 coefficient for DRC first-order low-pass filter
23 (0x17)	0001 0001	8 LSBs of n1 coefficient for DRC first-order low-pass filter
24 (0x18)	0111 1111	8 MSBs of d1 coefficient for DRC first-order low-pass filter
25 (0x19)	1101 1110	8 LSBs of d1 coefficient for DRC first-order low-pass filter
26–127	0000 0000	Reserved

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

This typical connection highlights the required external components and system level connections for proper operation of the device in several popular use cases.

Each of these configurations can be realized using the Evaluation Modules (EVMs) for the device. These flexible modules allow full evaluation of the device in the most common modes of operation. Any design variation can be supported by TI through schematic and layout reviews. Visit http://e2e.ti.com for design assistance and join the audio amplifier discussion forum for additional information.

8.2 Typical Application

The following application shows the minimal requirements and connections for the TLV320AIC3110 usage. This application shows the usage of a microphone input (MIC1RP), line input (MIC1LP, MIC1LM), headphone output (HPLOUT, HPROUT) and speaker output (SPKP, SPKM). Additionally, a host processor is used for I^2C control and Data Interface.

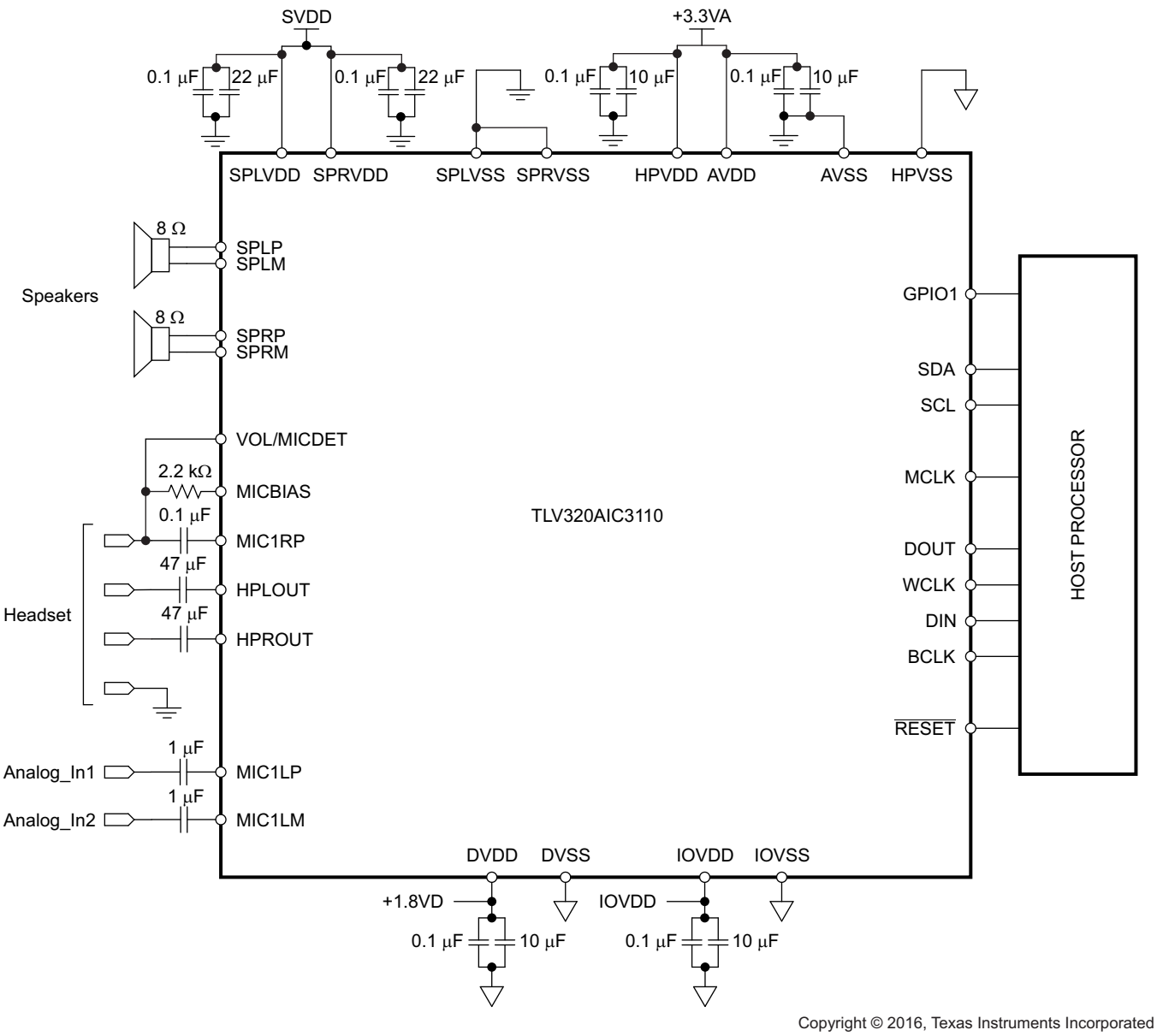


Figure 8-1. Typical Circuit Configuration

8.2.1 Design Requirements

For this design example, use the parameters listed in Table 8-1 as the input parameters.

Table 8-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
AVDD	3.3 V
DVDD	1.8 V
HPVDD	3.3 V
IOVDD	3.3 A
Maximum MICBIAS current	4 mA
SPKVDD	5 V
Power consumption (record)	9.24 mW (PRB_R5, 48 kHz, AOSR = 128)

Table 8-1. Design Parameters (continued)

DESIGN PARAMETER	EXAMPLE VALUE
Power consumption (playback)	25.62 mW (PRB_P1, 48 kHz, DOSR = 128, stereo headphones)

8.2.2 Detailed Design Procedure

Using Figure 8-1 as a guide, integrate the hardware into the system.

Following the recommended component placement, schematic layout and routing given in *Section 10*, integrate the device and its supporting components into the system PCB file.

Determining sample rate and master clock frequency is required since powering up the device as all internal timing is derived from the master clock. Refer to *Section 7.3.11* to get more information of how to configure correctly the required clocks for the device.

As the TLV320AIC3110 is designed for low-power applications, when powered up, the device has several features powered down. A correct routing of the TLV320AIC3110 signals is achieved by a correct setting of the device registers, powering up the required stages of the device and configuring the internal switches to follow a desired route. For more information of the device configuration and programming, refer to the TLV320AIC3110's technical documents on ti.com.

8.2.3 Application Curves

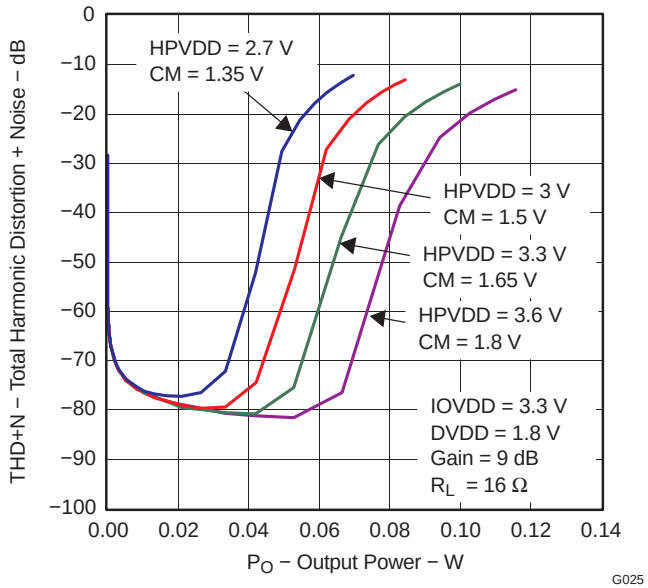


Figure 8-2. Headphone Output Power

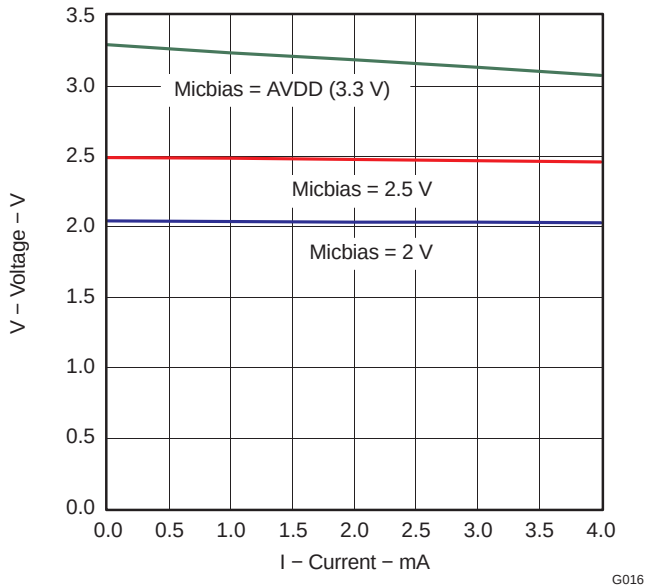


Figure 8-3. MICBIAS

9 Power Supply Recommendations

The TLV320AIC3110 has been designed to be extremely tolerant of power supply sequencing. However, in some rare cases, unexpected conditions and behaviors can be attributed to power supply sequencing.

It is important to consider that the digital activity must be separated from the analog and speaker activity. In order to separate the power supplies, the recommended power sequence is:

1. Speaker supplies
2. Digital supplies
3. Analog supplies

First, turn on the speaker supplies. Once they are stabilized, turn on the digital power supplies. Finally, once the digital power supplies are stabilized, the analog power supplies must be turned on.

Also, TI recommends to add decoupling capacitors close to the power supplies pins (see *Section 10* for details). These capacitors will ensure that the power pins will be stable. Additionally, undesired effects such pops will be avoided.

10 Layout

10.1 Layout Guidelines

PCB design is made considering the application and the review is specific for each system requirements. However, general considerations can optimize the system performance.

- The TLV320AIC3110 thermal pad must be connected to analog output driver ground using multiple VIAS to minimize impedance between the device and ground.
- Analog and digital grounds must be separated to prevent possible digital noise form affecting the analog performance of the board.
- The TLV320AIC3110 requires the decoupling capacitors to be placed as close as possible to the device power supply terminals.

10.2 Layout Example

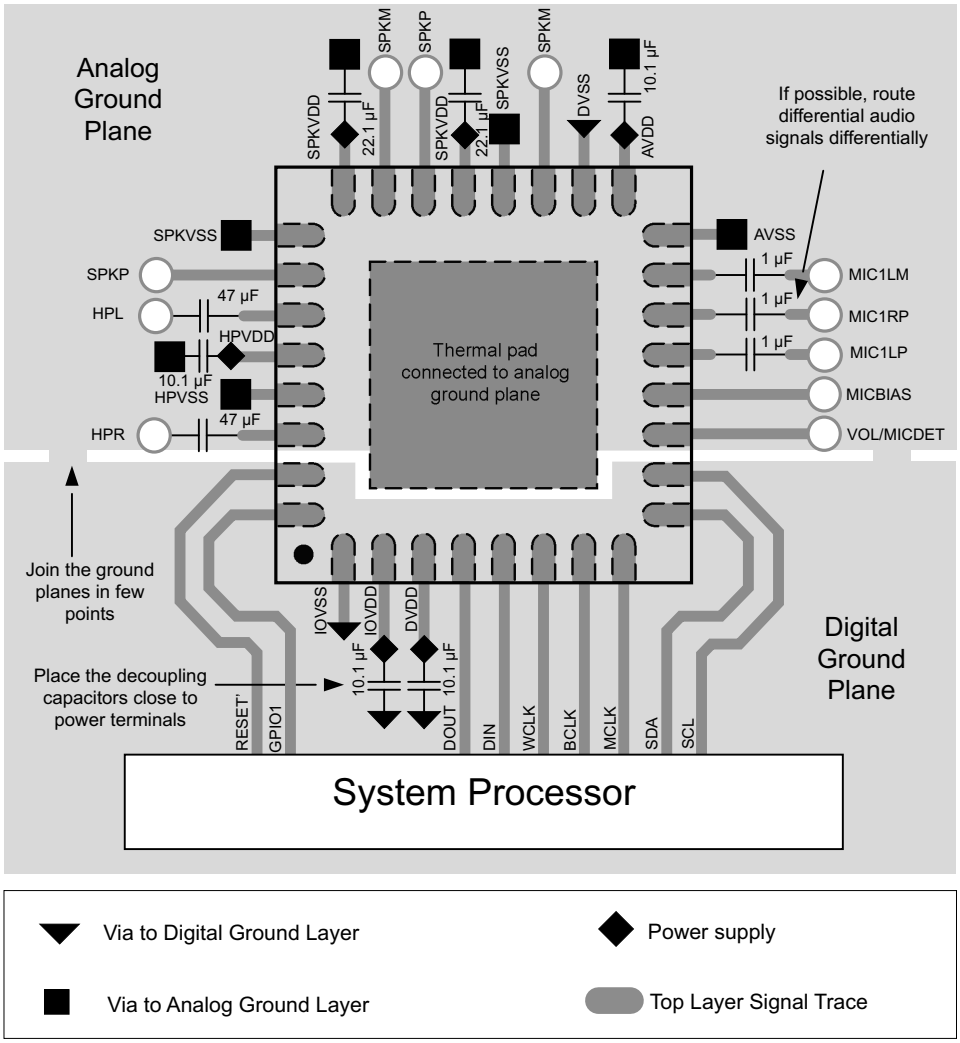


Figure 10-1. Example PCB Layout

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
MATLAB is a trademark of The MathWorks, Inc.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.4 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical Packaging and Orderable Information

12.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV320AIC3110IRHBR	ACTIVE	VQFN	RHB	32	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIC3110	Samples
TLV320AIC3110IRHBT	ACTIVE	VQFN	RHB	32	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	AIC3110	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

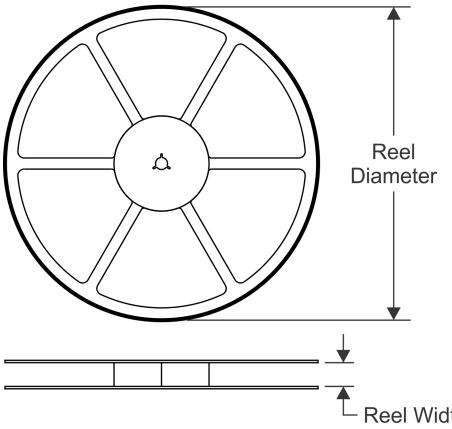
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

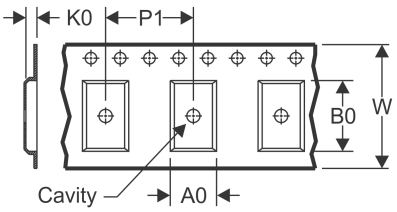
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

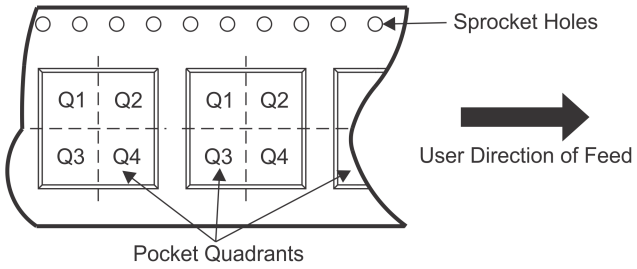


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

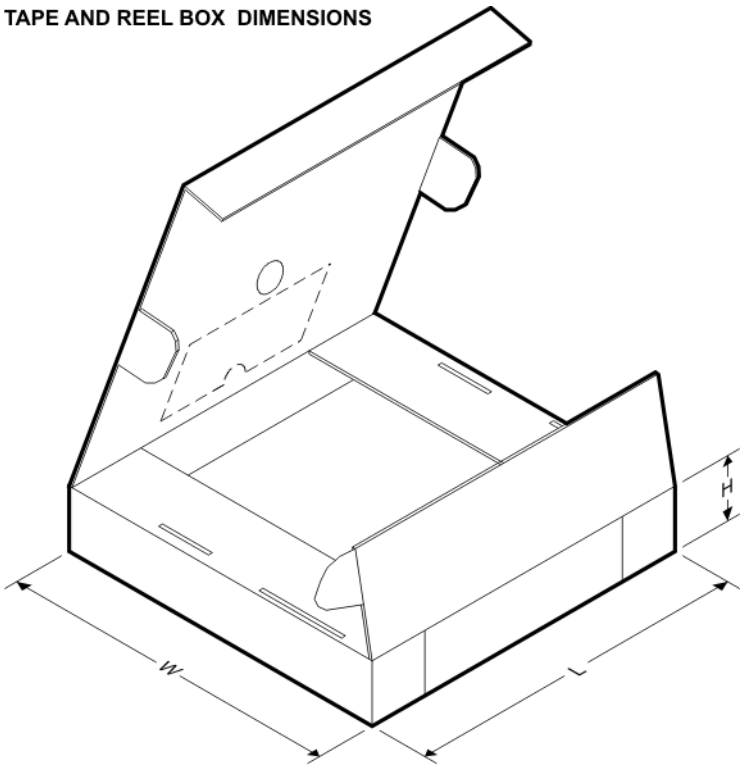
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV320AIC3110IRHBR	VQFN	RHB	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2
TLV320AIC3110IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.5	8.0	12.0	Q2
TLV320AIC3110IRHBT	VQFN	RHB	32	250	180.0	12.4	5.3	5.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV320AIC3110IRHBR	VQFN	RHB	32	3000	367.0	367.0	35.0
TLV320AIC3110IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0
TLV320AIC3110IRHBT	VQFN	RHB	32	250	210.0	185.0	35.0

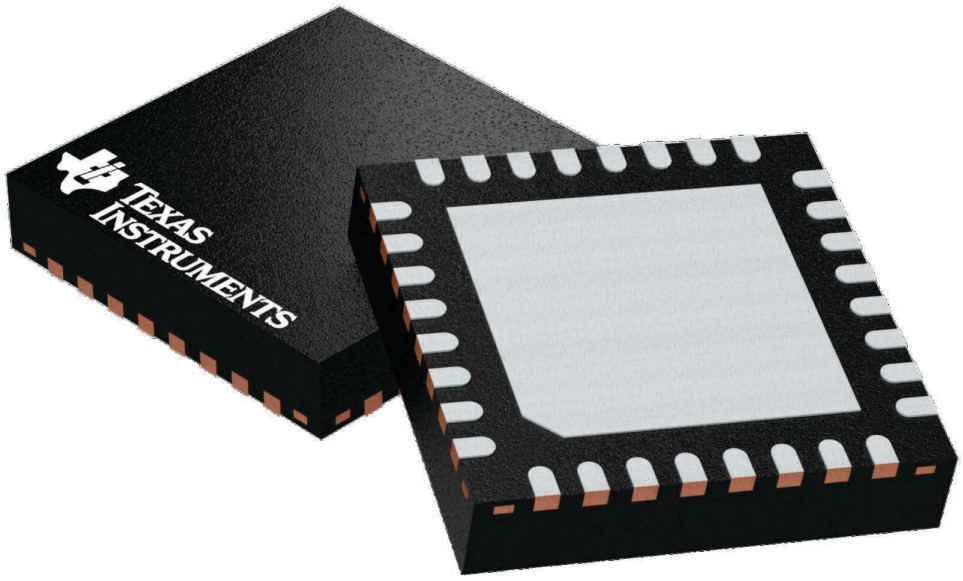
GENERIC PACKAGE VIEW

RHB 32

VQFN - 1 mm max height

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

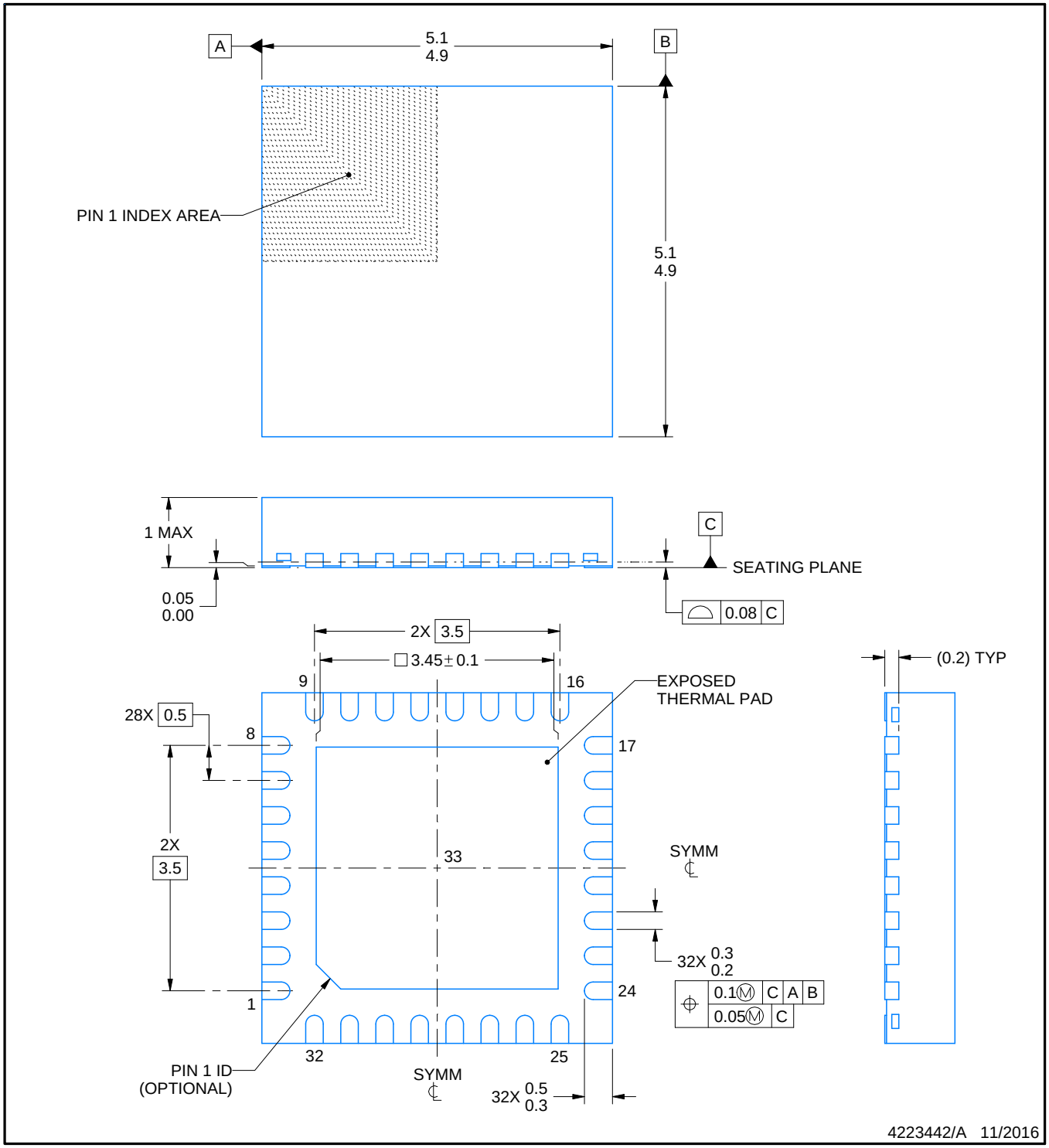
4224745/A

RHB0032E

PACKAGE OUTLINE

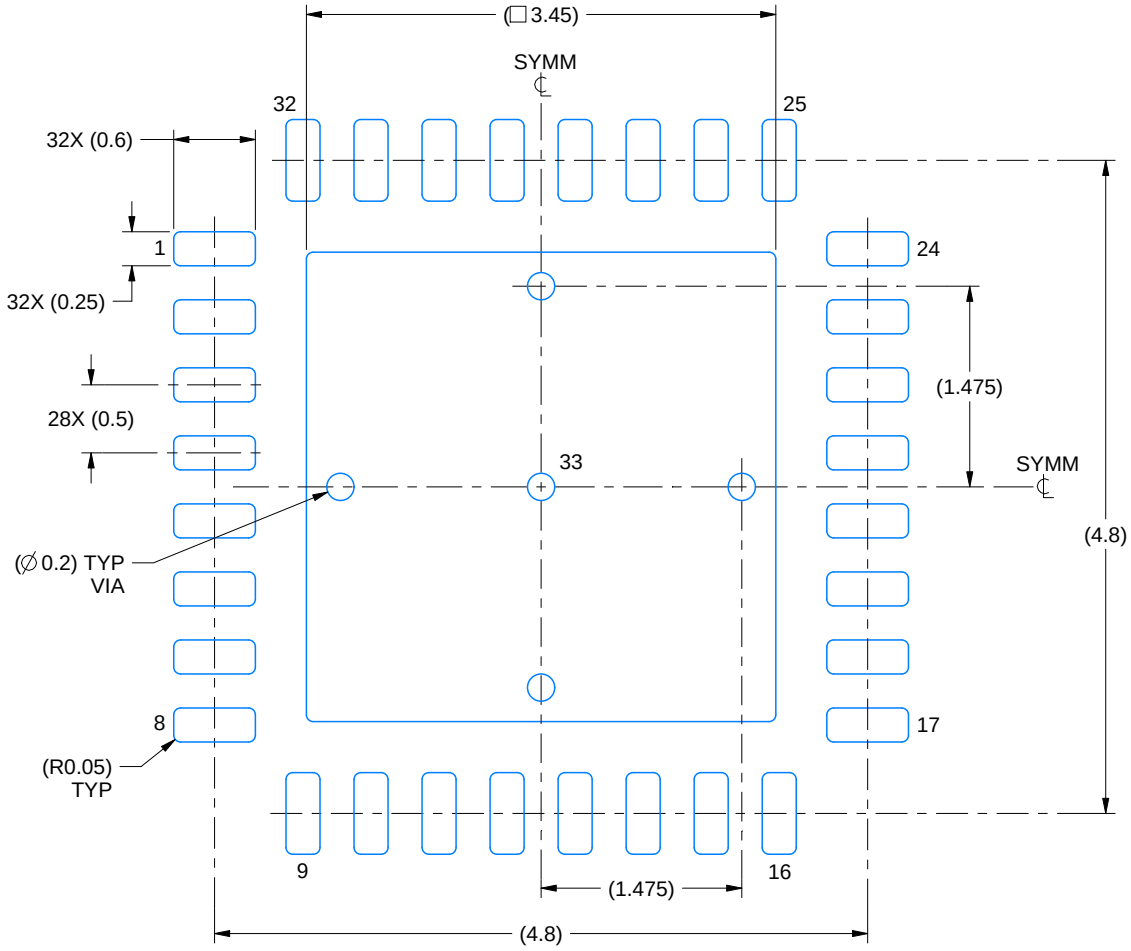
VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

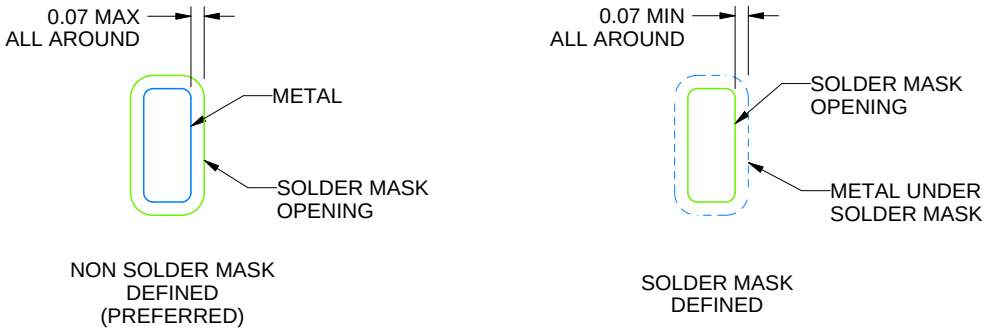


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:18X

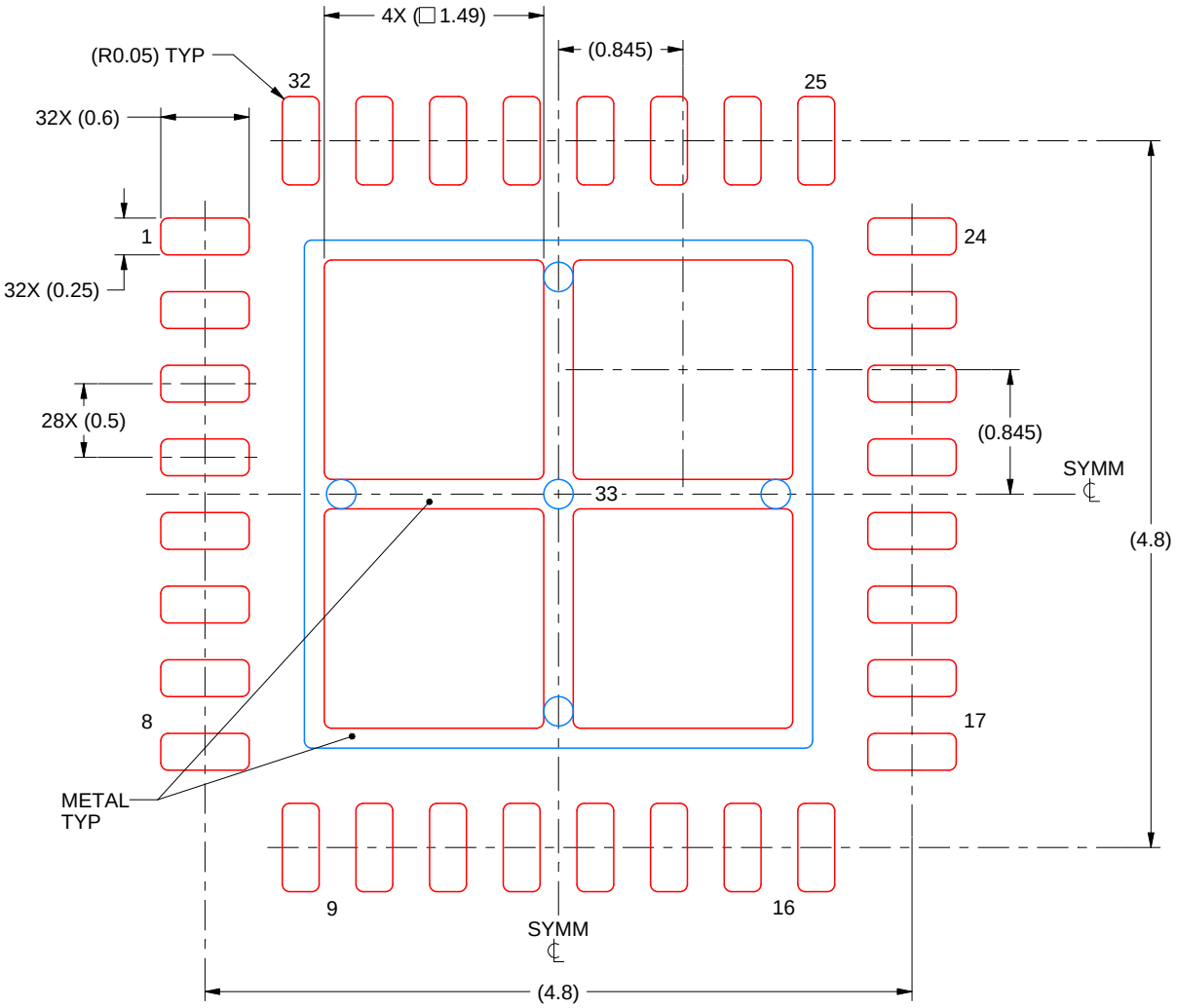


SOLDER MASK DETAILS

4223442/A 11/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4223442/A 11/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View TLV320AIC3110EVM-U on WIN SOURCE
- Texas Instruments Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management