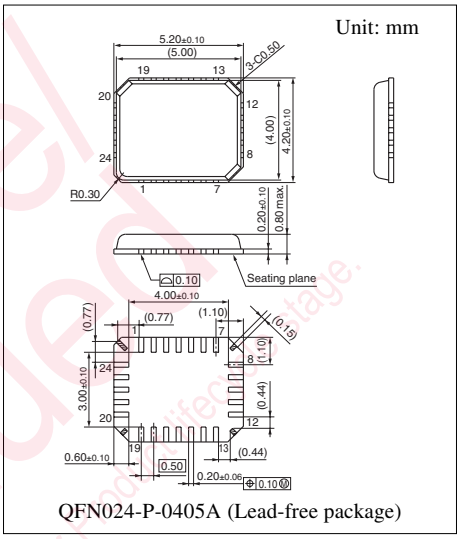
AN8049FHN

1.8-volt 3-channel step-up, step-down, and polarity inverting DC-DC converter control IC



QFN024-P-0405A (Lead-free package)

■ Overview

The AN8049FHN is a three-channel PWM DC-DC converter control IC that features low-voltage operation. This IC can form a power supply that provides two step-up outputs and one step-down or polarity inverted output with a minimal number of external components. Minimal operating supply voltage of this IC is as low as 1.8 V, so that it can operate from 2 dry-batteries.

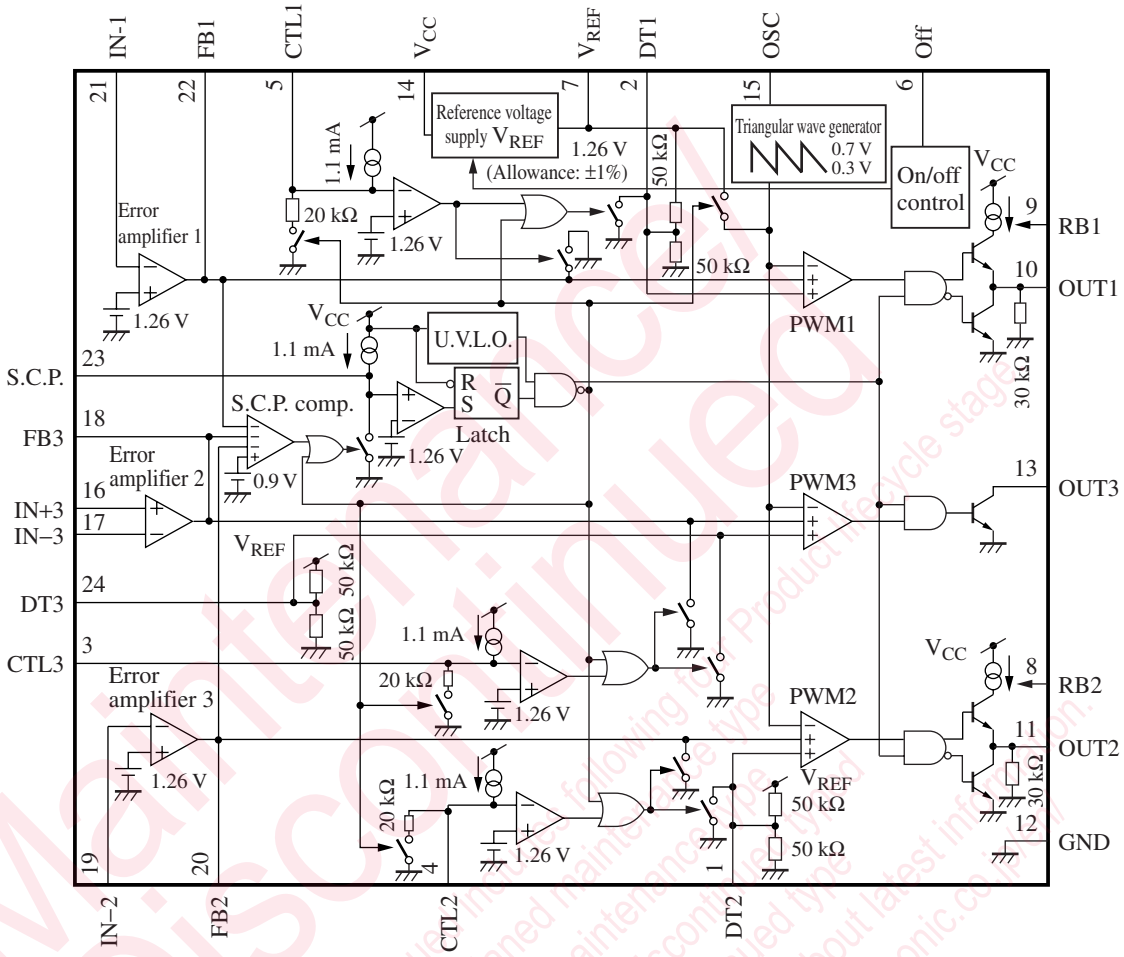
■ Features

- Wide operating supply voltage range: 1.8 V to 14 V
- High-precision reference voltage circuit
  - — V_{REF} pin voltage: ±1%
  - — Error amplifier: ±1.5%
- Ultrathin surface mounting package for miniaturized and thinner power supplies
- Supports control over a wide output frequency range: 20 kHz to 1 MHz
- On/off (sequence control) pins provided for each channel for easy sequence control setup
- The negative supply error amplifier supports 0-volt input.
  Common-mode input voltage range: − 0.1 V to V_{CC} −1.4 V
  This allows the number of external components to be reduced by two resistors.
- Fixed duty factor: 86%
  However, the duty can be adjusted to anywhere from 0% to 100% with an external resistor.
- Timer latch short-circuit protection circuit (charge current: 1.1 µA typical)
- Low input voltage malfunction prevention circuit (U.V.L.O.)
  (operation start voltage: 1.67 V typical)
- Standby function (active-high control input, standby mode current: 1 µA maximum)

■ Applications

- Electronic equipment that requires a power supply system

■ Block Diagram



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	DT2	13	OUT3
2	DT1	14	V_{CC}
3	CTL3	15	OSC
4	CTL2	16	IN+3
5	CTL1	17	IN−3
6	Off	18	FB3
7	V_{REF}	19	IN−2
8	RB2	20	FB2
9	RB1	21	IN−1
10	OUT1	22	FB1
11	OUT2	23	S.C.P.
12	GND	24	DT3

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	14.2	V
Off pin allowable application voltage	V_{OFF}	14.2	V
Error amplifier input allowable application voltage *2	V_{IN}	V_{CC}	V
OUT1 and OUT2 pin output source current	$I_{SO(OUT)}$	−50	mA
OUT3 pin output current	$I_{SI(OUT)}$	+50	mA
Power dissipation *1	P_D	111	mW
Operating temperature	T_{opr}	−30 to +85	°C
Storage temperature	T_{stg}	−55 to +150	°C

Note) ∗1: T_a = 85°C. For the independent IC without a heat sink.
∗2: When V_{CC} is less than 6 V, V_{IN-1} and V_{IN+2} must be V_{CC} .

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Off pin application voltage	V_{OFF}	0 to 14	V
OUT1 and OUT2 pin output source current	$I_{SO(OUT)}$	−40 (min.)	mA
OUT3 pin output current	$I_{SI(OUT)}$	40 (max.)	mA
Timing resistance	R_T	3 to 33	kW
Timing capacitance	C_T	100 to 1 000	pF
Oscillator frequency	f_{OUT}	20 to 1 000	kHz
Short-circuit protection time-constant setting capacitance	C_{SCP}	1 000 (min.)	pF
Output current setting resistance	R_B	750 to 15 000	Ω

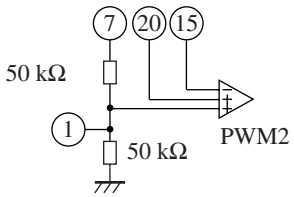
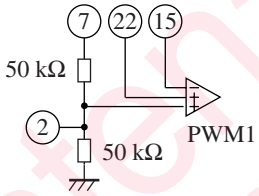
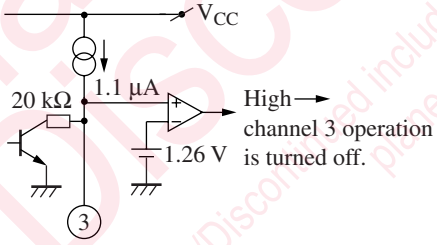
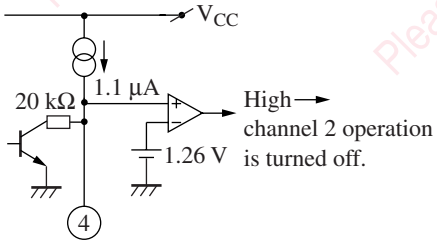
■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Reference voltage	V_{REF}	I_{REF} = – 0.1 mA	1.247	1.26	1.273	V
Line regulation with input fluctuation	Line	V_{CC} = 1.8 V to 14 V	—	2	20	mV
Load regulation	Load	I_{REF} = – 0.1 mA to –1 mA	–20	–3	—	mV
V_{REF} temperature characteristics	V_{RFEdT}	T_a = –30°C to +85°C	—	1	—	%
V_{REF} pin short-circuit current	I_{OC}		—	–10	—	mA
U.V.L.O. block						
Circuit operation start voltage	V_{UON}		1.59	1.67	1.75	V
Error amplifier 1 block						
Input threshold voltage 1	V_{TH1}		1.241	1.26	1.279	V
Input bias current 1	I_{B1}		—	0.1	0.2	µA
High-level output voltage 1	V_{EH1}		1.0	1.2	1.4	V
Low-level output voltage 1	V_{EL1}		—	—	0.2	
Output source current 1	$I_{SO(FB)1}$		–38	–31	–24	µA
Output sink current 1	$I_{SI(FB)1}$		0.5	—	—	mA
V_{TH} temperature characteristics 1	V_{THdT1}	T_a = –30°C to +85°C	—	1.5	—	%
Open-loop gain 1	A_{V1}		—	80	—	dB
Error amplifier 2 block						
Input threshold voltage 2	V_{TH2}		1.241	1.26	1.279	V
Input bias current 2	I_{B2}		—	0.1	0.2	µA
High-level output voltage 2	V_{EH2}		1.0	1.2	1.4	V
Low-level output voltage 2	V_{EL2}		—	—	0.2	
Output source current 2	$I_{SO(FB)2}$		–38	–31	–24	µA
Output sink current 2	$I_{SI(FB)2}$		0.5	—	—	mA
V_{TH} temperature characteristics 2	V_{THdT2}	T_a = –30°C to +85°C	—	1.5	—	%
Open-loop gain 2	A_{V2}		—	80	—	dB
Error amplifier 3 block						
Input offset voltage	V_{IO}		–6	—	6	mV
Common-mode input voltage range	V_{ICR}		– 0.1	—	V_{CC} – 1.4	V
Input bias current 3	I_{B3}		– 0.6	– 0.3	—	µA
High-level output voltage 3	V_{EH3}		1.0	1.2	1.4	V
Low-level output voltage 3	V_{EL3}		—	—	0.2	
Output source current 3	$I_{SO(FB)3}$		–38	–31	–24	µA
Output sink current 3	$I_{SI(FB)3}$		0.5	—	—	mA
Open-loop gain 3	A_{V3}		—	80	—	dB

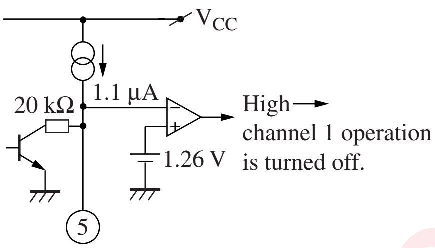
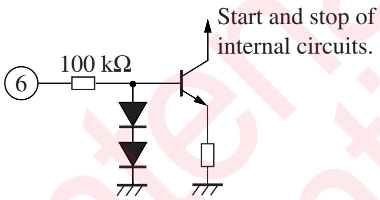
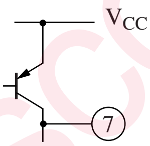
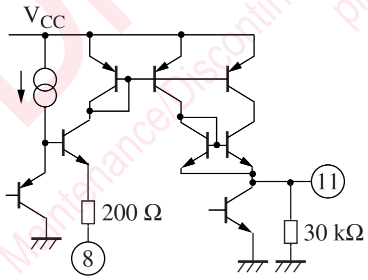
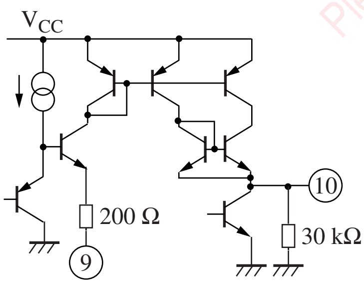
■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Oscillator block						
Oscillator frequency	f_{OUT}	R_T = 7.5 kΩ, C_T = 680 pF	170	190	210	kHz
Frequency supply voltage characteristics	f_{DV}	R_T = 7.5 kΩ, C_T = 680 pF	—	1	—	%
Frequency temperature characteristics	f_{DT}	R_T = 7.5 kΩ, C_T = 680 pF	—	3	—	%
Output 1 block						
Output duty factor 1	Du_1	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
High-level output voltage 1	V_{OH1}	I_O = −10 mA, R_B = 1 kΩ	V_{CC} − 1	—	—	V
Low-level output voltage 1	V_{OL1}	I_O = 10 mA, R_B = 1 kΩ	—	—	0.2	V
Output source current 1	$I_{SO(OUT)1}$	V_O = 0.7 V, R_B = 1 kΩ	−32	−27	−22	mA
Output sink current 1	$I_{SI(OUT)1}$	V_O = 0.7 V, R_B = 1 kΩ	40	—	—	mA
Pull-down resistor 1	R_{O1}		20	30	40	kΩ
Output 2 block						
Output duty factor 2	Du_2	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
High-level output voltage 2	V_{OH2}	I_O = −10 mA, R_B = 1 kΩ	V_{CC} − 1	—	—	V
Low-level output voltage 2	V_{OL2}	I_O = 10 mA, R_B = 1 kΩ	—	—	0.2	V
Output source current 2	$I_{SO(OUT)2}$	V_O = 0.7 V, R_B = 1 kΩ	−32	−27	−22	mA
Output sink current 2	$I_{SI(OUT)2}$	V_O = 0.7 V, R_B = 1 kΩ	40	—	—	mA
Pull-down resistor 2	R_{O2}		20	30	40	kΩ
Output 3 block						
Output duty factor 3	Du_3	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
Output saturation voltage	$V_{O(SAT)}$		—	—	0.2	V
Short-circuit protection circuit block						
Input standby voltage	V_{STBY}		—	—	0.1	V
Input threshold voltage	V_{THPC}		0.8	0.9	1.0	V
Input latch voltage	V_{IN}		—	—	0.1	V
Charge current	I_{CHG}	V_{SCP} = 0 V	−1.3	−1.0	−0.7	µA
Comparator threshold voltage	V_{THL}		—	1.26	—	V
On/off control block						
Input threshold voltage	$V_{ON(TH)}$		0.7	1.0	1.3	V
Off pin current	I_{OFF}	V_{OFF} = 5 V	—	35	—	µA
CTL block						
Input threshold voltage	V_{THCTL}		1.07	1.26	1.47	V
Charge current	I_{CTL}	V_{CTL} = 0 V	−1.3	−1.0	−0.7	µA
Whole device						
Average consumption current	$I_{CC(OFF)}$	R_B = 9.1 kΩ, duty = 50%	—	4.2	5.5	mA
Standby mode current	$I_{CC(SB)}$		—	—	1	µA

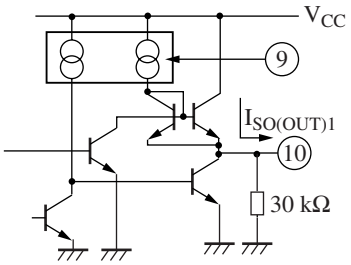
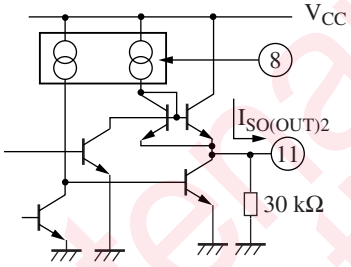
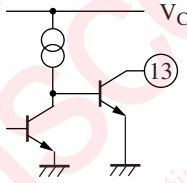
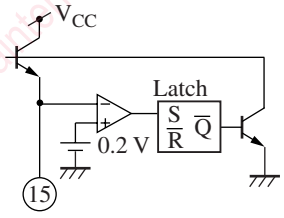
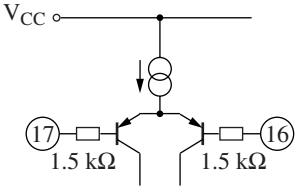
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		DT2: Sets the channel 2 soft start time. Set the time by connecting a capacitor between this pin and ground. Note that although the channel 2 maximum on duty is set internally to 86%, the maximum on duty can be set to a value of 86% or less by inserting a resistor between this pin and ground, and can be set to a value of 86% or more by inserting a resistor between this pin and the V_{REF} pin.	I
2		DT1: Sets the channel 1 soft start time. Set the time by connecting a capacitor between this pin and ground. Note that although the channel 1 maximum on duty is set internally to 86%, the maximum on duty can be set to a value of 86% or less by inserting a resistor between this pin and ground, and can be set to a value of 86% or more by inserting a resistor between this pin and the V_{REF} pin.	
3		CTL3: Controls the on/off state of channel 3. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. $t_{DLY3} = 1.26\ (V) \times C_{CTL3}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I
4		CTL2: Controls the on/off state of channel 2. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. $t_{DLY2} = 1.26\ (V) \times C_{CTL2}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I

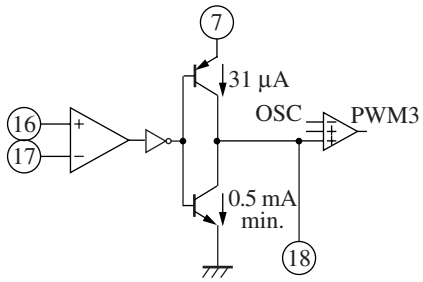
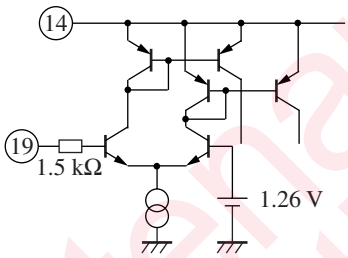
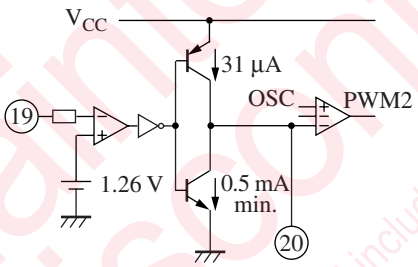
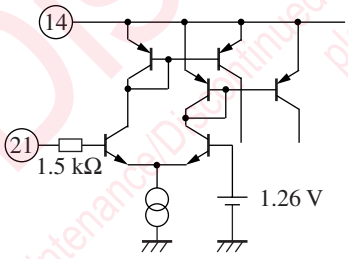
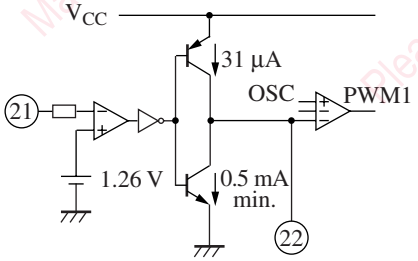
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
5		CTL1: Controls the on/off state of channel 1. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. $t_{DLY1} = 1.26\ (V) \times C_{CTL1}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I
6		Off: Controls the on/off state. When the input is high: normal operation ($V_{OFF} > 1.2$ V) When the input is low: standby mode ($V_{OFF} < 0.6$ V) In standby mode, the total current consumption is held to under 1 µA.	I
7		V_{REF}: Outputs the internal reference voltage. The reference voltage is 1.26 V (allowance: ±1%) when V_{CC} is 2.4 V and I_{REF} is – 0.1 mA. Insert a capacitor of at least 0.1 µF between V_{REF} and ground for phase compensation.	O
8		RB2: Connection for a resistor that sets the channel 2 output source current. Use a resistor in the range 750 Ω to 1.5 kΩ.	I
9		RB1: Connection for a resistor that sets the channel 1 output source current. Use a resistor in the range 750 Ω to 1.5 kΩ.	I

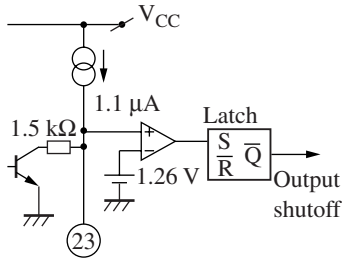
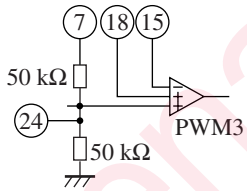
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
10		OUT1: Push-pull output. The absolute maximum rating for the output source current is −50 mA. Connecting the external resistor to RB1 terminal allows this circuit to provide an output source current with excellent line regulation and minimal sample-to-sample variations.	O
11		OUT2: Push-pull output. The absolute maximum rating for the output source current is −50 mA. Connecting the external resistor to RB2 terminal allows this circuit to provide an output source current with excellent line regulation and minimal sample-to-sample variations.	O
12		GND: Ground.	—
13		OUT3: Open-collector output. The absolute maximum rating for the output current is +50 mA.	O
14		V_{CC}: Power supply terminal. Provide the operating supply voltage in the range 1.8 V to 14 V.	—
15		OSC: Connection for the capacitor and resistor that determine the oscillator frequency. Use a capacitor in the range 100 pF to 1000 pF and a resistor in the range 3 kΩ to 33 kΩ. Use an oscillator frequency in the range 20 kHz to 1 MHz.	O
16		IN+3: Noninverting input to the error amplifier 3.	I
17		IN−3: Inverting input to the error amplifier 3.	I

■ Terminal Equivalent Circuit (continued)

Pin No.	Equivalent circuit	Description	I/O
18		FB3: Output from the error amplifier 3. This circuit can provide a source current of −31 µA or a sink current of 0.5 mA (minimum).	O
19		IN−2: Inverting input to the error amplifier 2.	I
20		FB2: Output from the error amplifier 2. This circuit can provide a source current of −31 µA or a sink current of 0.5 mA (minimum).	O
21		IN−1: Inverting input to the error amplifier 1.	I
22		FB1: Output from the error amplifier 1. This circuit can provide a source current of −31 µA or a sink current of 0.5 mA (minimum).	O

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
23		S.C.P.: Connection for the capacitor that sets the timer latch short-circuit protection circuit time constant. Use a capacitor with a value of 1 000 pF or higher. The charge current I_{CHG} is 1.1 µA typical.	O
24		DT3: Sets the channel 3 soft start time. Set the time by connecting a capacitor between this pin and ground. Note that although the channel 3 maximum on duty is set internally to 86%, the maximum on duty can be set to a value of 86% or less by inserting a resistor between this pin and ground, and can be set to a value of 86% or more by inserting a resistor between this pin and the V_{REF} pin.	I

■ Usage Notes

[1] Allowable power dissipation

Since the power dissipation (P) in this IC increases proportionally with the supply voltage, applications must be careful to operate so that the loss does not exceed the allowable power dissipation, P_D , for the package.

Reference formula:

$P = (V_{CC} - V_{BEQ1}) \times I_{SO(OUT)1} \times Du_1$ ← Power dissipation in the channel 1 output stage

$+ (V_{CC} - V_{BEQ2}) \times I_{SO(OUT)2} \times Du_2$ ← Power dissipation in the channel 2 output stage

$+ V_{O(SAT)3} \times I_{OUT3} \times Du_3$ ← Power dissipation in the channel 3 output stage

$+ V_{CC} \times I_{CC}$ ← Power dissipation between V_{CC} and ground

$< P_D$

V_{BEQ1} : The voltage between the base and emitter of the npn transistor Q1

$I_{SO(OUT)1}$: The OUT1 pin output source current
(When R_{RB1} is 1 kΩ, $I_{SO(OUT)1}$ will be 38 mA, maximum.)

Du_1 : The output 1 duty factor

V_{BEQ2} : The voltage between the base and emitter of the npn transistor Q2

$I_{SO(OUT)2}$: The OUT2 pin output source current
(When R_{RB2} is 1 kΩ, $I_{SO(OUT)2}$ will be 38 mA, maximum.)

Du_2 : The output 2 duty factor

$V_{O(SAT)3}$: The OUT3 pin saturation voltage (0.5 V maximum when OUT1 is 40 mA.)

I_{OUT3} : The OUT3 pin current (This will be $\{V_{CC} - V_{BEQ3} - V_{O(SAT)3}\}/R_{O3}$.)

Du_3 : The output 3 duty factor

I_{CC} : The V_{CC} pin current

■ Usage Notes (continued)

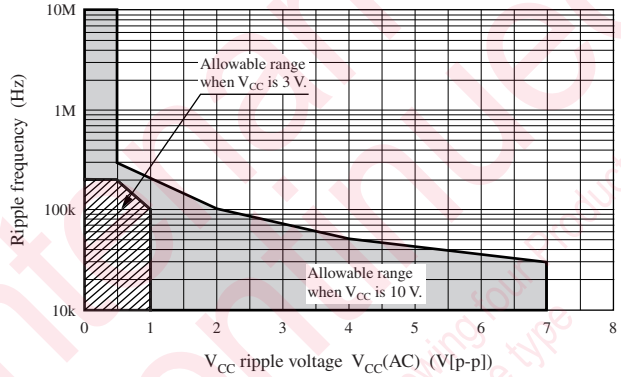
[2] Allowable V_{CC} ripple

V_{CC} ripple due to the switching transistor being turned on and off can cause this IC's U.V.L.O. circuit, which is biased by V_{CC} , to operate incorrectly, and can cause the S.C.P. capacitor charging operation to fail to start when the output is shorted.

The figure shows the allowable range for V_{CC} ripple. Applications should reduce V_{CC} ripple to be within this range, either by inserting a ripple filter in the V_{CC} line or by inserting a capacitor between the IC GND and V_{CC} pins and locating that capacitor as close to the IC as possible.

Note that the allowable range shown here is the result of testing the IC alone and that the allowable range may differ depending on the actual structure of the power supply circuit. Also note that this allowable range is a design target, and is not guaranteed by testing of all samples.

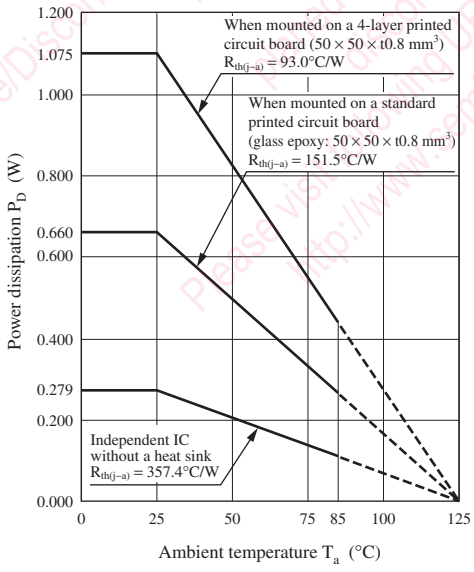
Allowable V_{CC} ripple



■ Application Notes

[1] P_D — T_a curves of QFN024-P-0405A

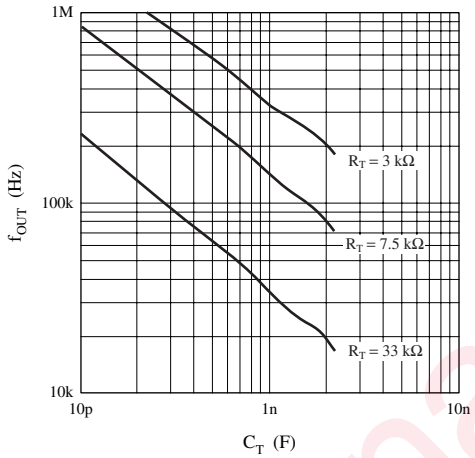
P_D — T_a



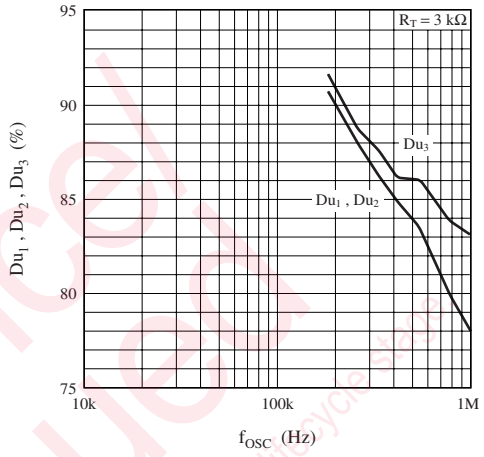
■ Application Notes (continued)

[2] Main characteristics

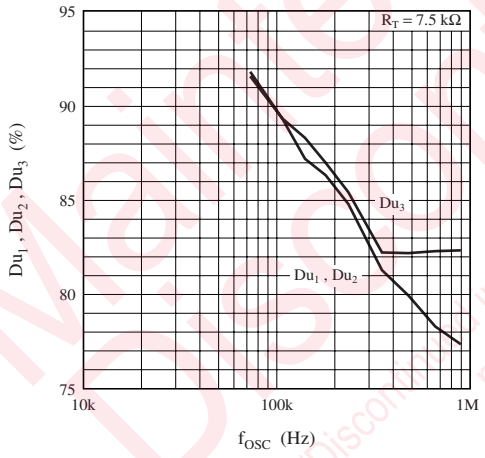
Timing capacitance — Oscillator frequency



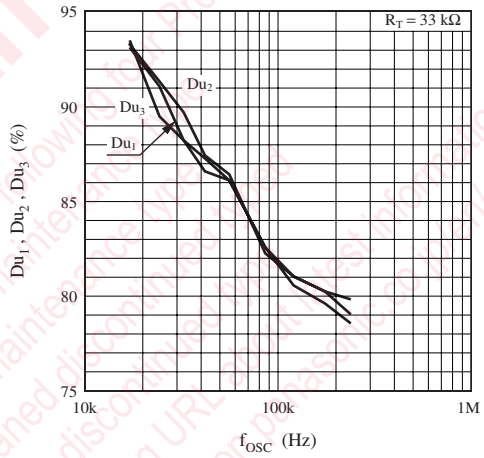
f_{OSC} — Maximum output duty



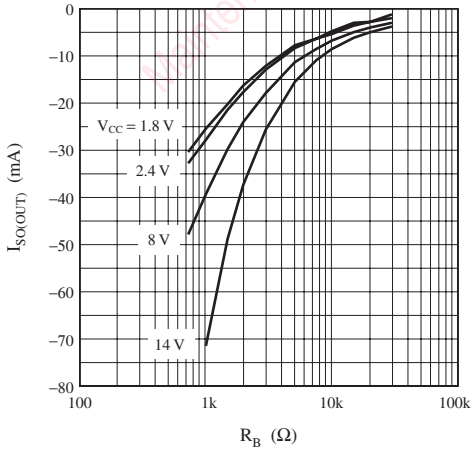
f_{OSC} — Maximum output duty



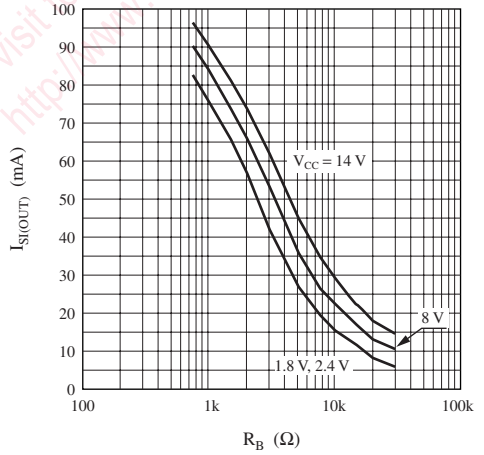
f_{OSC} — Maximum output duty



R_B — $I_{SO(OUT)}$

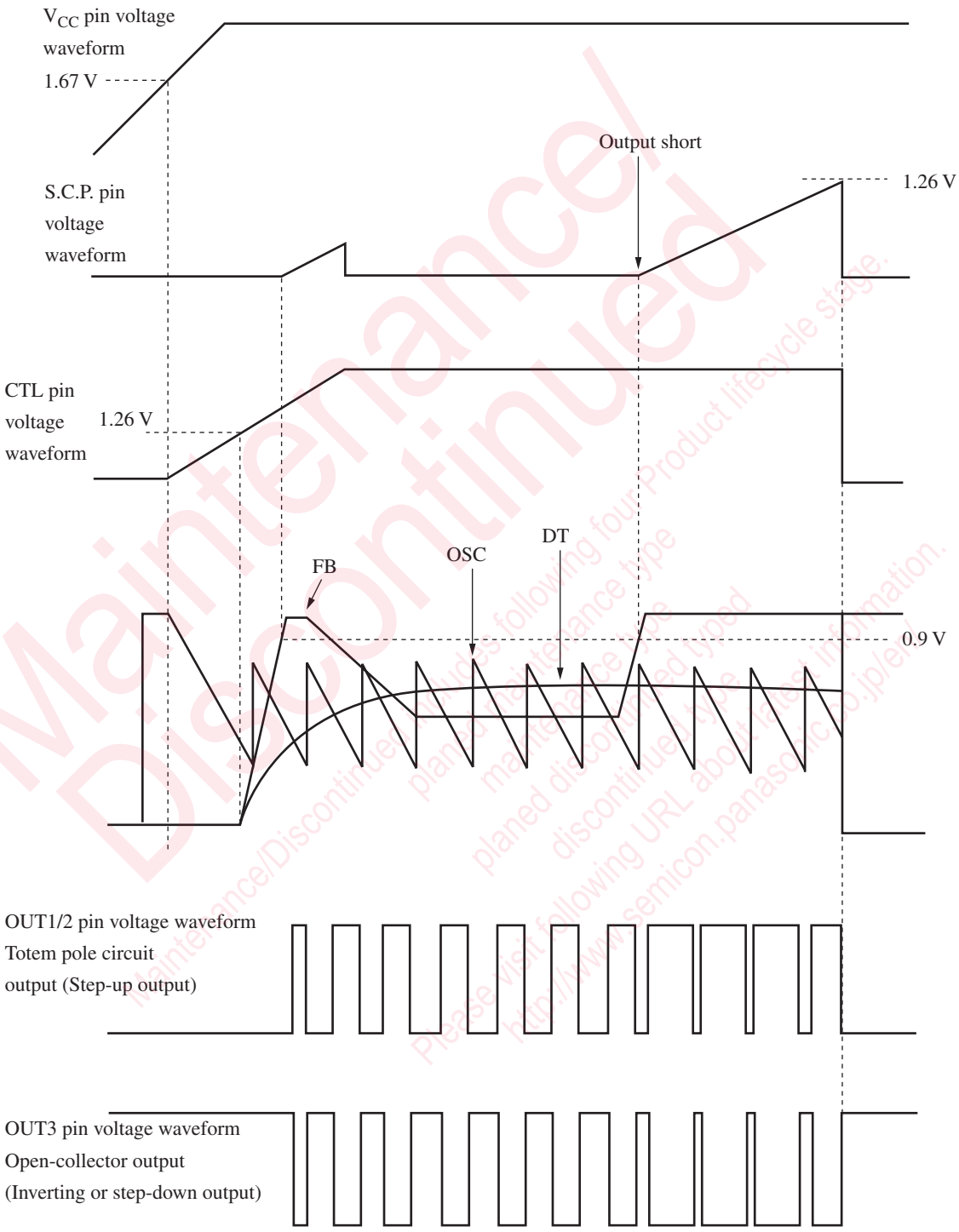


R_B — $I_{SI(OUT)}$



■ Application Notes (continued)

[3] Timing charts



■ Application Notes (continued)

[4] Function descriptions

1. Reference voltage block

This circuit is composed of a band gap circuit, and outputs a 1.26 V (typical) reference voltage that is temperature compensated to a precision of ±1%. This reference voltage is stabilized when the supply voltage is 1.8 V or higher. This reference voltage is used by error amplifiers 1 and 2.

2. Triangular wave generator

This circuit generates a triangular wave like a sawtooth with a peak of 0.7 V and a trough of 0.2 V using a capacitor C_T (for the time constant) and resistor R_T connected to the OSC pin (pin 15). The oscillator frequency can be set to an arbitrary value by selecting appropriate values for the external capacitor and resistor, C_T and R_T . This IC can use an oscillator frequency in the range 20 kHz to 1 MHz. The triangular wave signal is provided to the noninverting input of the PWM comparator in each channel internally to the IC. Use the formulas below for rough calculation of the oscillator frequency.

$$f_{OSC} \approx -\frac{1}{C_T \times R_T \times \ln \frac{V_{OSCL}}{V_{OSCH}}} \approx 0.8 \times \frac{1}{C_T \times R_T} \quad \text{(Hz)}$$

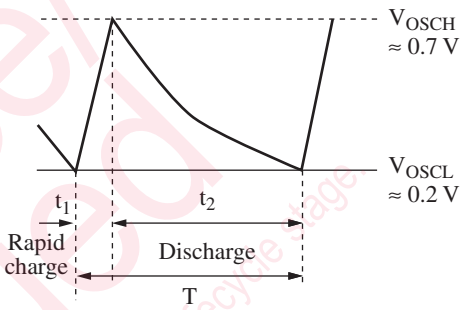


Figure 1. Triangular oscillator waveform

Note, however, that the above formulas do not take the rapid charge time, overshoot, and undershoot into account. See the experimentally determined graph of the oscillator frequency vs. timing capacitance value provided in the main characteristics section.

3. Error amplifier 1

This circuit is an npn-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage, and inputs that signal to a PWM comparator. The 1.26 V internal reference voltage is applied to the noninverting input. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB1 pin (pin 22) and the IN−1 pin (pin 21). The output voltage V_{OUT1} can be set using the circuit shown in the figure.

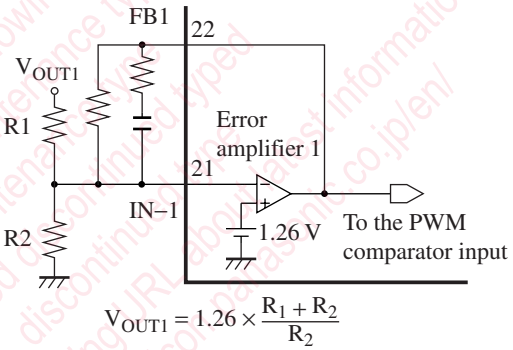


Figure 2. Connection method of error amplifier 1 (Step-up output)

4. Error amplifier 2

This circuit is an npn-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage, and inputs that signal to a PWM comparator. The 1.26 V internal reference voltage is applied to the noninverting input. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB2 pin (pin 20) and the IN−2 pin (pin 19). The output voltage V_{OUT2} can be set using the circuit shown in the figure.

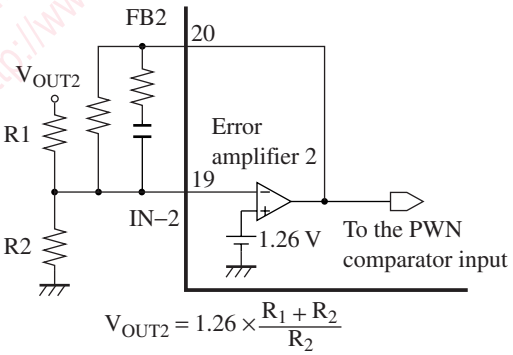


Figure 3. Connection method of error amplifier 2 (Step-up output)

■ Application Notes (continued)

[4] Function descriptions (continued)

5. Error amplifier 3

This circuit is a pnp-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage and inputs that signal to a PWM comparator. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB3 pin (pin 18) and the IN−3 pin (pin 17). The output voltage V_{OUT3} can be set using the circuit shown in the figure.

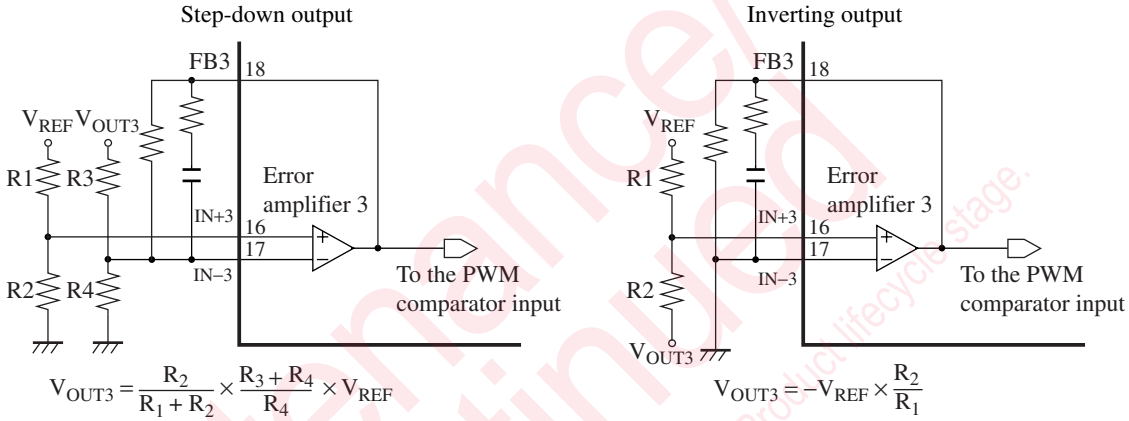


Figure 4. Connection method of error amplifier 3

6. Timer latch short-circuit protection circuit

This circuit protects the external main switching elements, flywheel diodes, choke coils, and other components against degradation or destruction if an excessive load or a short circuit of the power supply output continues for longer than a certain fixed period.

The timer latch short-circuit protection circuit detects the output of the error amplifiers. If the DC-DC converter output voltage drops and an FB pin (pins 18, 20, or 22) voltage exceeds 0.9 V, the S.C.P. comparator outputs a low level and the timer circuit starts. This starts charging the external protection circuit delay time capacitor.

If the error amplifier output does not return to the normal voltage range before that capacitor reaches 1.26 V, the latch circuit latches, the output drive transistors are turned off, and the dead-time is set to 100%.

7. Low input voltage malfunction prevention circuit (U.V.L.O.)

This circuit protects the system against degradation or destruction due to incorrect control operation when the power supply voltage falls during power on or power off.

The low input voltage malfunction prevention circuit detects the internal reference voltage that changes with the supply voltage level. While the supply voltage is rising, this circuit cuts off the output drive transistor until the reference voltage reaches 1.67 V. It also sets the dead-time to 100% and at the same time holds the S.C.P. pin (pin 23) and the DT pins (pins 1, 2, and 24) at 0 V, and the OSC pin (pin 15) at about 1.2 V.

8. PWM comparators

The PWM comparators control the on-period of the output pulse according to their input voltage.

The output transistors are turned on during periods when the OSC pin (pin 15) triangular wave is lower than both of the corresponding FB pin (pins 18, 20, or 22) and the corresponding DT pin (pins 1, 2, or 24).

The PWM 2 circuit turns the output transistor on during periods when OSC pin (pin 15) triangular wave is at a higher level than both of the FB2 pin (pin 20) and the DT2 pin (pin 1).

The maximum duty is set to 86% internally, but it can be set to a value lower than 86% by inserting a resistor between the corresponding DT pin and ground, and can be set to a value higher than 86% by inserting a resistor between the corresponding DT pin and the V_{REF} pin.

The IC's soft start function operates to gradually increase the width of the output pulse on-period during startup if a capacitor is inserted between the DT pin and ground.

■ Application Notes (continued)

[4] Function descriptions (continued)

9. Output 1 and output 2 blocks

These output circuits have a totem pole structure. A constant-current source output with good line regulation can be set up freely by connecting current setting resistors to the RB pins.

These circuits can provide a constant-current source output of up to 50 mA.

10. Output 3 block

This output circuit has an open collector structure.

An output current of up to 50 mA can be provided, and the output pin has a breakdown voltage of 15 V.

11. CTL block

The CTL block output circuit also has a totem pole structure. A constant-current source output with good line regulation can be set up freely by connecting current setting resistors to the RB2 pin.

The CTL block can provide a constant-current source output of up to 50 mA.

[5] Time constant setup for the timer latch short-circuit protection circuit

Figure 6 shows the structure of the timer latch short-circuit protection circuit. The short-circuit protection comparator continuously compares a 0.9 V reference voltage with the FB1, FB2, and FB3 error amplifier outputs.

When the DC-DC converter output load conditions are stable, the short-circuit protection comparator holds its average value since there are no fluctuations in the error amplifier outputs. At this time, the output transistor Q1 will be in the conducting state, and the S.C.P. pin will be held at 0 V.

If the output load conditions change rapidly and a high-level signal (0.9 V or higher) is input to the short-circuit protection comparator from the error amplifier output, the short-circuit protection comparator will output a low level and the output transistor Q1 will shut off. Then, the capacitor C_{SCP} connected to the S.C.P. pin will start to charge. When the external capacitor C_{SCP} is charged to about 1.26 V by the constant current of about 1.1 mA, the latch circuit will latch and the dead-time will be set to 100% with the output held fixed at the low level. Once the latch circuit has latched, the S.C.P. pin capacitor will be discharged to about 0 V, but the latch circuit will not reset unless either power is turned off or the power supply is restarted using on/off control.

$$1.26\ \text{V} = I_{CHG} \times \frac{t_{PE}}{C_{SCP}}$$

$$\therefore\ t_{PE}\ (\text{s}) = 1.15 \times C_{SCP}\ (\mu\text{F})$$

At power supply startup, the output appears to be in the shorted state, and the IC starts to charge the S.C.P. pin capacitor. Therefore, users must select an external capacitor that allows the DC-DC converter output voltage to rise before the latch circuit in the later stage latches. In particular, care is required if the soft start function is used, since that function makes the startup time longer.

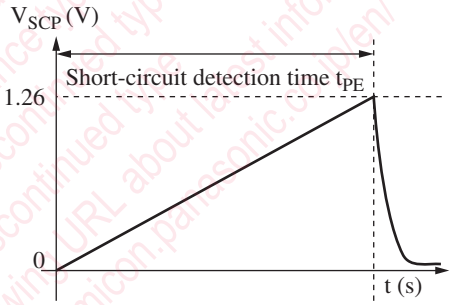


Figure 5. S.C.P. pin charging waveform

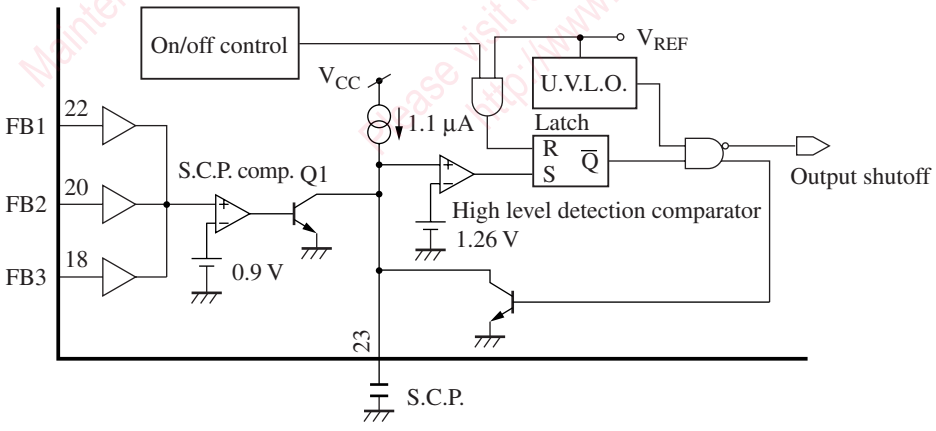


Figure 6. Short-circuit protection circuit

■ Application Notes (continued)

[6] Parallel synchronous operation of multiple ICs

Multiple instances of this IC can be operated in parallel. If the OSC pins (pin 15) and Off pins (pin 6) are connected to each other as shown in figure 7, the ICs will operate at the same frequency.

It is also possible to operate a one-channel control IC (e.g. the AN8016SH or AN8016NSH) and a two-channel control IC (e.g. the AN8017SA or AN8018SA) in this parallel synchronous mode. In this case, short the OSC and Off pins together.

Note that it is not possible to control the on/off states of each IC operating in this mode independently. It is only possible to turn all the ICs on or off at the same time remotely.

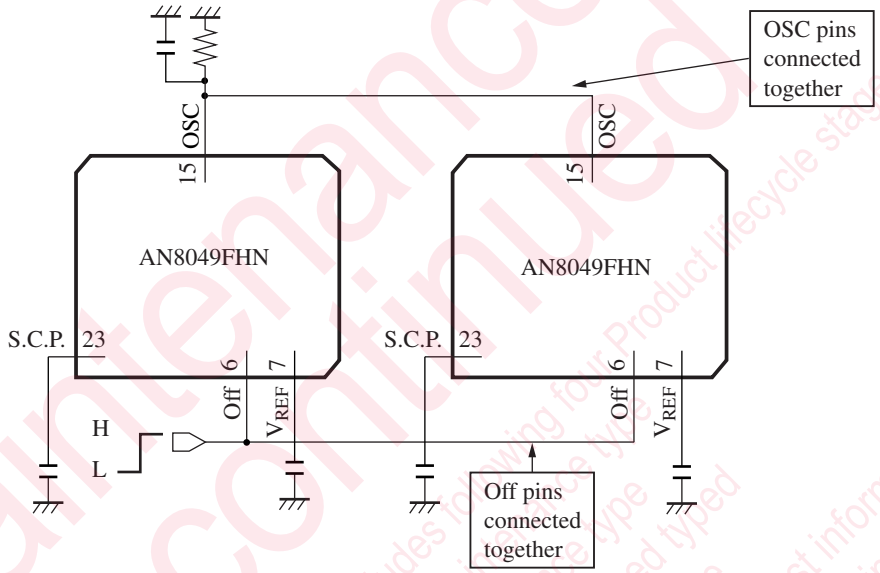


Figure 7. Slave operation circuit example

■ Application Notes (continued)

[7] Sequential operation

Delays can be provided in the startup times by inserting capacitors (C_{CTL}) between the CTL pins and ground.

Delay time: $t_{DLY} = 1.26\ (V) \times C_{CTL}\ (\mu F)/1.1\ (\mu A)$ (s)

Note that the individual channels can also be turned on or off independently by external signals. These external signals may have voltages in the range 0 V to V_{CC}.

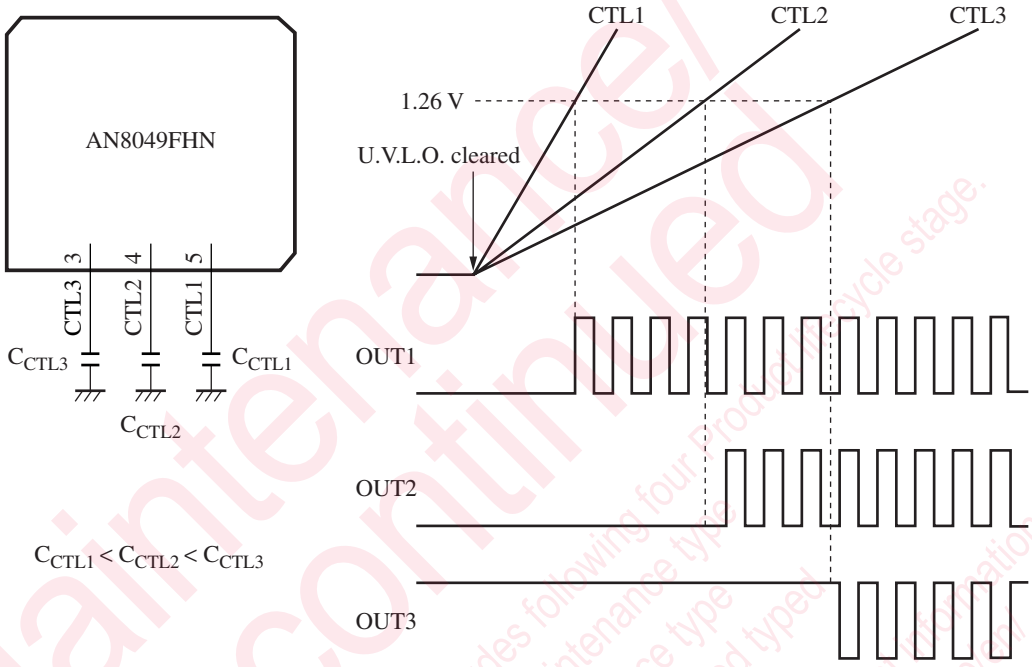


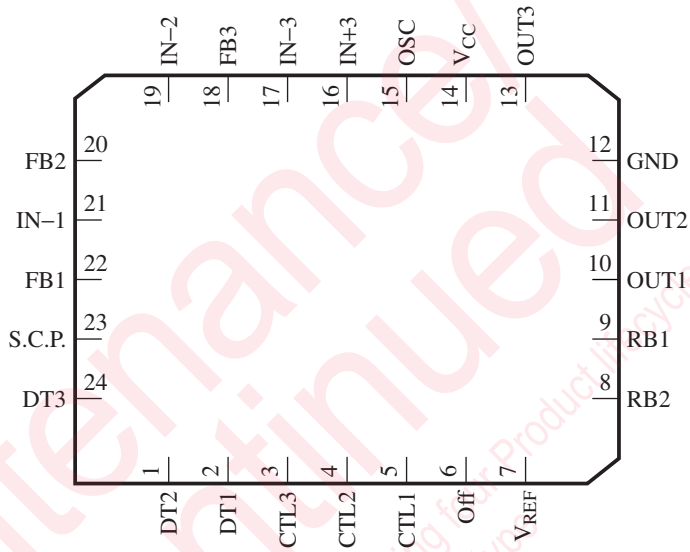
Figure 8. Sequential operation

■ Application Notes (continued)

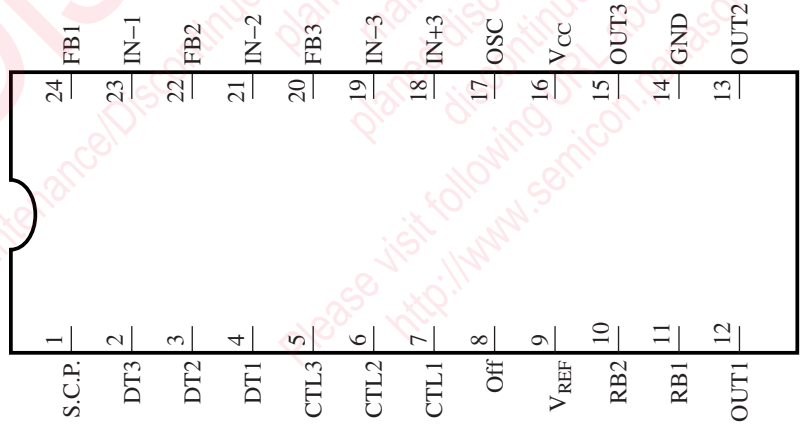
[8] Differences between this IC and the AN8049SH

The pin arrangements differ. The AN8049SH is an alternative package version of this IC.

AN8049FHN



AN8049SH

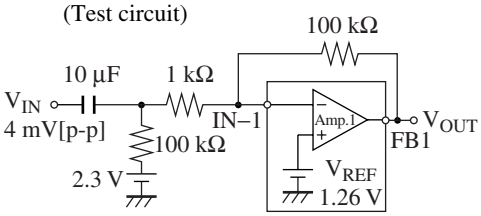


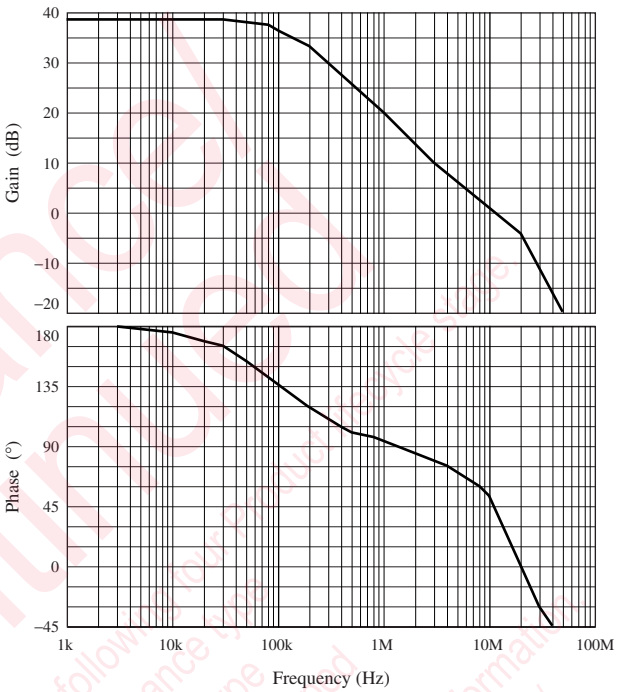
■ Application Notes (continued)

[9] Error amplifier frequency characteristics

1. Error amplifiers 1 and 2

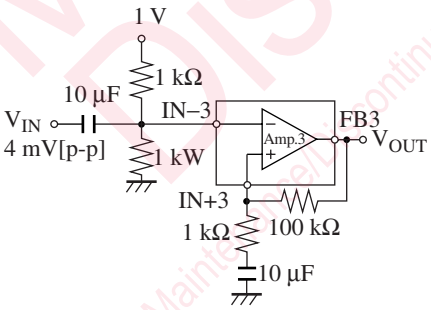
(Test circuit)

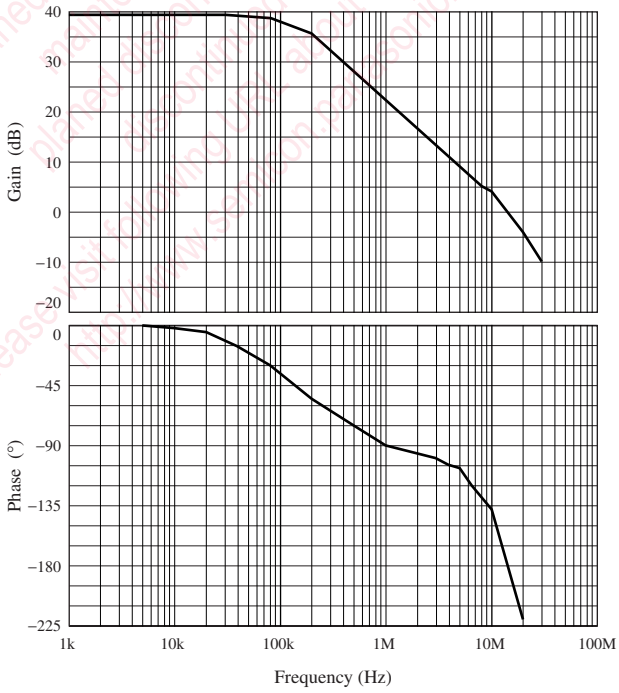




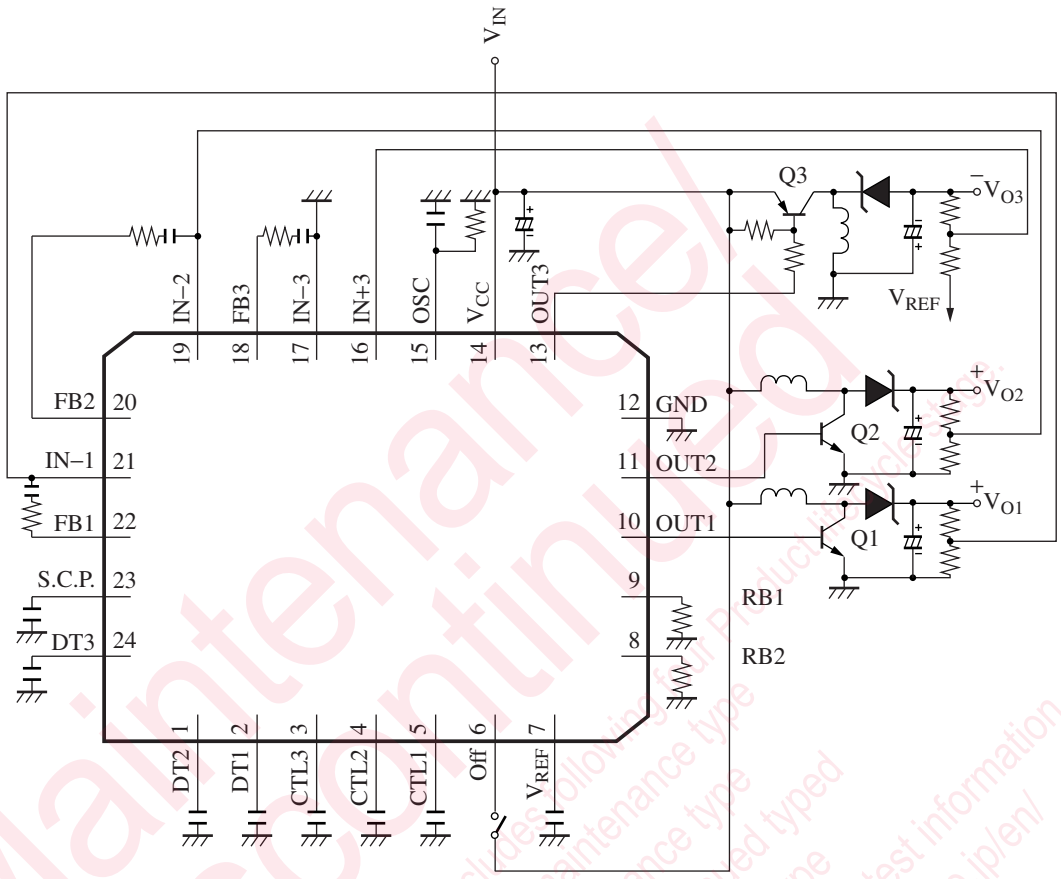
2. Error amplifier 3

(Test circuit)





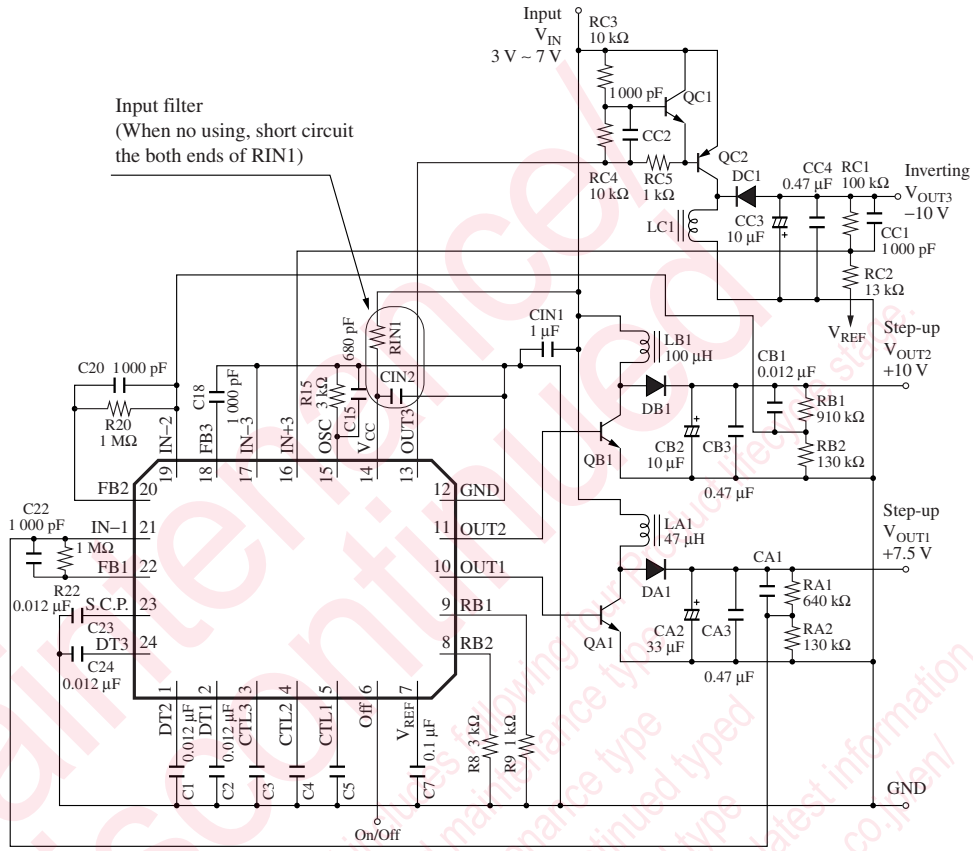
■ Application Circuit Example



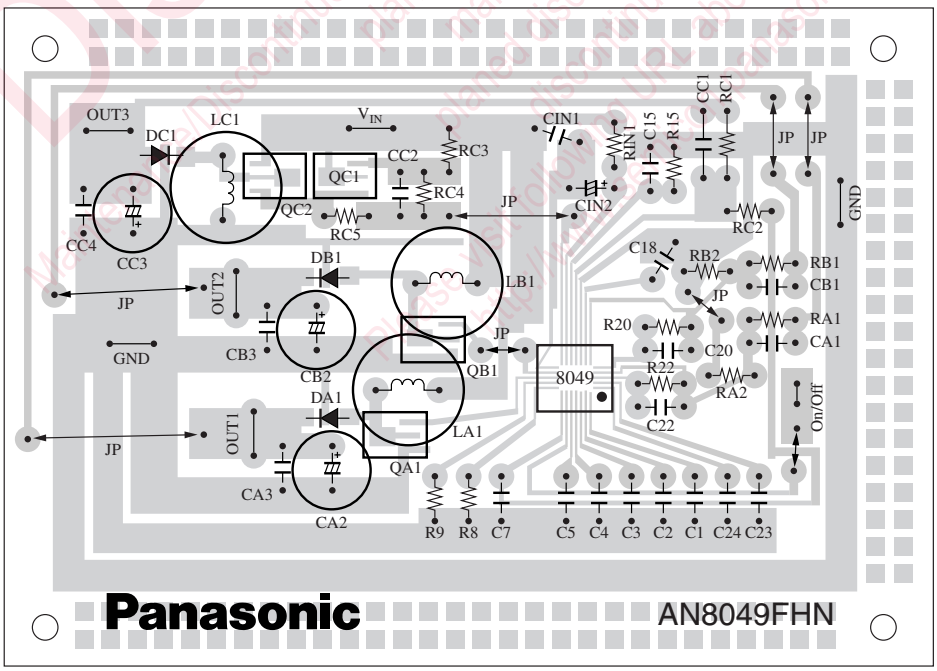
■ Evaluation Board

1. The element numbers of the board pair with the ones of the circuit.
2. "JP" of the board shows the jumper. Short circuit.

• Circuit



• Board



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