THE DATASHEET OF

AS3715-WL-00_EK_ST

AS3715

Dual Power Path PMIC

General Description

The AS3715 is a compact System PMU supporting two Li-Ion batteries and up to 14 power rails.

The device offers advanced power management functions. All necessary ICs and peripherals in a battery powered mobile device are supplied by the AS3715. It features 3 DCDC buck converters, one DCDC buck controller, a 5V HDMI booster, a HV backlight boost controller with 3 current sinks as well as 8 LDOs (2 low noise). The different regulated supply voltages are programmable via the serial control interface. 3-4MHz operation with 0.47uH coils is reducing cost and PCB space.

AS3715 contains a linear or switch mode Li-Ion battery charger with constant current and constant voltage operation. The maximum charging current is 1.5A. An internal battery switch and an optional external switch are separating the battery during charging or whenever an external power supply is present. In addition a second external battery path can be controlled. With these switches it is also possible to operate with no or deeply discharged batteries.

A dual USB input current limiter can be used to control the current taken form the USB supplies or charger inputs. Additional features are a 30V OV protection and JEITA compliant battery temperature supervision with selectable NTC beta values.

The single supply voltage may vary from 2.7V to 5.5V.

Ordering Information and Content Guide appear at end of datasheet.

Key Benefits and Features

Following the general description are key benefits and features for AS3715.

Figure 1:
Added Value of Using AS3715

Benefits	Features
Compact design due to small coils for IO and memory voltage generation	• DCDC step down regulators (3-4MHz) - Output (0.6V-3.3V; 2x1A, 1x2A)
High current generation with external power stages to minimize PMIC power dissipation	• DCDC step down controller - DVM (0.6V-1.5V; 1x5A)
Multiple independent voltage rails for general purpose IO supplies	• 8 universal LDOs - 6x universal IO range(0.8-3.3V; 0.3A) - 2x analog (1.2-3.3V; 0.25A)

Benefits	Features
Backlight boost controller for multiple display configurations or fixed voltage supplies	• Current mode boost controller with two current sinks. • Constant voltage operation and over-voltage protection • 3 programmable current sinks (max. 40mA) • Possible external PWM dimming input (DLS, CABC)
Self-contained Li-Ion battery charger with dual battery and USB path control.	• 1.5A max charging current • Dual battery control • Dual charger input with current limiters • Soft-, Trickle-, Constant Current and Constant Voltage operation (3.5 .. 4.44V) • Linear and switch mode charging • Charger timeout and JEITA temperature supervision • NTC beta selection
Save supervision in HW which works also without a processor.	• Supervisor with interrupt generation and selectable warning levels - Automatic battery monitoring - Automatic temperature monitoring - Power supply supervision for DCDC
Flexible multi-purpose IOs for general control tasks.	• General Purpose IOs - ADC input - Wake-up/stand-by input - PWM input/output - Low battery and power good status
Enables the processor to check the actual system state in detail.	• ADC with internal and external sources
Flexible and fast adaptation to different processors/applications.	• OTP programmable Boot and Power-down sequence
Power saving control according to the processor needs.	• Stand-by function with programmable sequence and voltages
Self-contained start-up and control dual battery and dual USB operation. Safety shutdown feature.	• Control Interface - I^2C control lines with watchdog - ONKEY with 4/8s emergency shut-down - POR with RESET I/O
Dedicated packages for specific applications. Optimization for PCB cost or size.	• Package - 81-ball WL-CSP 0.4mm pitch

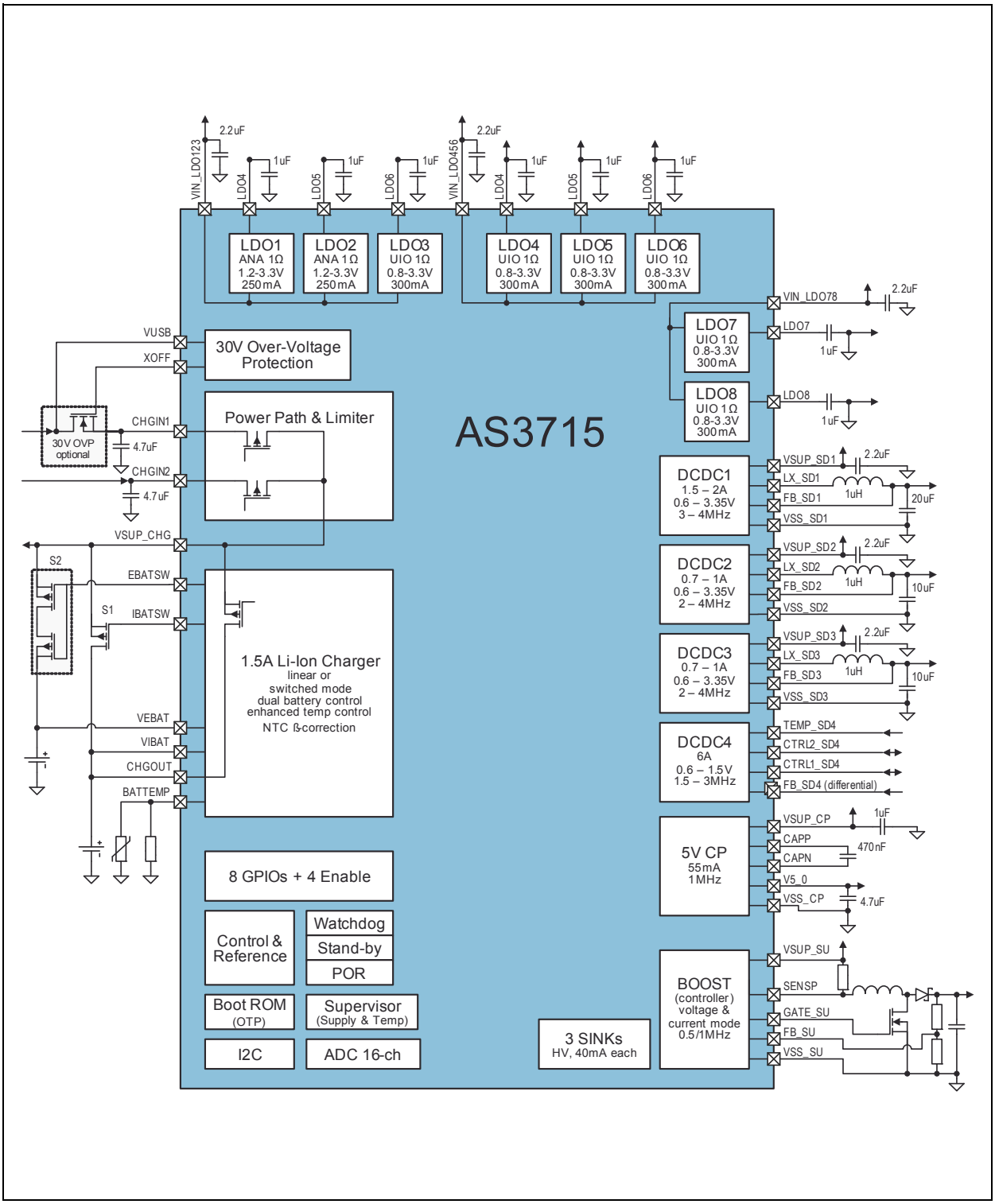
Applications

The device is suitable for digital still cameras, outdoor action cameras, digital movie cameras, general Li-Ion battery powered mobile devices.

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
Block Diagram for AS3715



Block Diagram: Shows the main function blocks of the AS3715.

Pin Assignments

Figure 3:
Pin Assignment

	1	2	3	4	5	6	7	8	9
A	VSS_SU	SENSEN_SU	LDO6	LDO5	LDO4	CHGIN1	VSUP_CHG	CHGIN2	CHGOUT
B	FB_SD4_N	GATE_SU	VIN_LDO456	GPIO8	EN2	CHGIN1	VSUP_CHG	CHGIN2	CHGOUT
C	CTRL1_SD4	TEMP_SD4	VSUP_SU	FB_SD4_P	FB_SU	EN1	IBATSW	XOFF	VSUP_SD3
D	CAPN	VSS_CP	VEBAT	CTRL2_SD4	SENSEP_SU	EN4	EBATSW	FB_SD3	LX_SD3
E	V5_0	CAPP	VSUP_CP	VIBAT	BATTEMP	VUSB	EN3	FB_SD2	VSS_SD3
F	V2_5	LDO3	CREF	GPIO7	GPIO6	SDA	VSS_ANA	VSSA	VSS_SD2
G	LDO2	VIN_LDO123	GPIO5	GPIO2	GPIO1	CURR3	FB_SD1	VSUP_SD2	LX_SD2
H	LDO1	GPIO3	SCL	ONKEY	VIN_LDO78	CURR2	LX_SD1	VSUP_SD1	VSUP_SD1
J	GPIO4	XRES	VSUP_GPIO	LDO7	LDO8	CURR1	LX_SD1	VSS_SD1	VSS_SD1

Pin Assignment: Shows the top view pin assignment of the AS3715

Figure 4:
Pin Description

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
F6	SDA	DI	SPI digital input in SPI mode; Data IO in I²C mode.	VSUP	Open
H3	SCL	DI	SPI clock input in SPI mode; SCK input in I²C mode.	VSUP	Open
H4	ONKEY	DI	Input pin to startup with pull-down	5.5V	Define level
J2	XRES	DIO	IO pin for reset during active state	VSUP	Define level
F1	V2_5	AO	Output voltage of low power LDO V2_5	2.6V	Mandatory
F3	CREF	AIO	Bypass capacitor for the internal voltage reference; connect 100nF	1.8V	Mandatory
J3	VSUP_GPIO	S	Supply pin for GPIOs (connect to other VSUP pins)	5.5V	Mandatory
F7	VSS_ANA	AIO	Analog sense GND input (connect to VSSA on PCB)	-	Mandatory
G5	GPIO1	DIO	General purpose input/output pin	VSUP	Open
G4	GPIO2	DIO	General purpose input/output pin	VSUP	Open
H2	GPIO3	DIO	General purpose input/output pin	VSUP	Open
J1	GPIO4	DIO	General purpose input/output pin	VSUP	Open
G3	GPIO5	DIO	General purpose input/output pin	VSUP	Open
F5	GPIO6	DIO	General purpose input/output pin / optional current sink	VSUP	Open
F4	GPIO7	DIO	General purpose input/output pin / optional current sink	VSUP	Open
B4	GPIO8	DI	General purpose input/output pin	VSUP	Open
C6	EN1	DI	Input pin to startup with pull-down	5.5V	Open
B5	EN2	DI	Input pin to startup with pull-down	5.5V	Open
E7	EN3	DI	Input pin to startup with pull-down	5.5V	Open
D6	EN4	DI	Input pin to startup with pull-down	5.5V	Open
G2	VIN_LDO123	S	Supply pad for LDOs	5.5V	Mandatory
B3	VIN_LDO456	S	Supply pad for LDOs	5.5V	Mandatory
H5	VIN_LDO78	S	Supply pad for LDOs	5.5V	Mandatory
H1	LDO1	AO	Output voltage of LDO - PMOS_1	3.3V	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
G1	LDO2	AO	Output voltage of LDO - PMOS_1	3.3V	Open
F2	LDO3	AO	Output voltage of LDO - PMOS_1	3.3V	Open
A5	LDO4	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
A4	LDO5	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
A3	LDO6	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
J4	LDO7	AO	Output voltage of LDO - PMOS_0.6	3.3V	Open
J5	LDO8	AO	Output voltage of LDO - PMOS_1	3.3V	Open
H9	VSUP_SD1	S	System supply voltage input of SD1 (connect to other VSUP pins)	5.5V	Mandatory
H8	VSUP_SD1	S	System supply voltage input of SD1 (connect to other VSUP pins)	5.5V	Mandatory
J7	LX_SD1	AIO	LX node of Stepdown1	VSUP	Open
H7	LX_SD1	AIO	LX node of Stepdown1	VSUP	Open
G7	FB_SD1	AI	Analog Feedback pin of SD1	3.6V	Open
J9	VSS_SD1	AIO	Power GND pin of Stepdown1	-	Mandatory
J8	VSS_SD1	AIO	Power GND pin of Stepdown1	-	Mandatory
G8	VSUP_SD2	S	System supply voltage input of SD2 (connect to other VSUP pins)	5.5V	Mandatory
G9	LX_SD2	AIO	LX node of Stepdown2	VSUP	Open
E8	FB_SD2	AI	Analog Feedback pin of SD2	3.6V	Open
F9	VSS_SD2	AIO	Power GND pin of Stepdown2	-	Mandatory
C9	VSUP_SD3	S	System supply voltage input of SD3 (connect to other VSUP pins)	5.5V	Mandatory
D9	LX_SD3	AIO	LX node of Stepdown3	VSUP	Open
D8	FB_SD3	AI	Analog Feedback pin of SD3	3.6V	Open
E9	VSS_SD3	AIO	Power GND pin of Stepdown3	-	Mandatory
C4	FB_SD4_P	AIO	Positive Feedback of SD1	3.6V	Open
B1	FB_SD4_N	AIO	Negative Feedback of SD1	3.6V	Open
C1	CTRL1_SD4	AIO	Bidirectional control pin of SD0, phase 1	VSUP	Open
D4	CTRL2_SD4	AIO	Bidirectional control pin of SD0, phase 2	VSUP	Open
C2	TEMP_SD4	AIO	Temperature control pin of power stage for SD1	VSUP	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
E3	VSUP_CP	S	System supply voltage input of CP (connect to other VSUP pins)	5.5V	Mandatory
E2	CAPP	AIO	Flying cap of charge pump	VSUP	Open
D1	CAPN	AIO	Flying cap of charge pump	VSUP	Open
E1	V5_0	AIO	Output voltage of charge pump	-	Open
D2	VSS_CP	AIO	Power GND pin of 5V charge pump	-	Mandatory
C3	VSUP_SU	S	System supply voltage input of SU (connect to other VSUP pins)	5.5V	Mandatory
D5	SENSEP_SU	AI	SU positive sense resistor input	VSUP	Open
A2	SENSEN_SU	AI	SU negative sense resistor input	VSUP	Open
C5	FB_SU	AI	Analog Feedback pin of SU	3.6V	Open
B2	GATE_SU	AO	SU ext. NMOS gate driver output	VSUP	Open
A1	VSS_SU	AIO	Power GND pin of SU	-	Mandatory
J6	CURR1	AIO	Current sink 1 terminal	30V	Open
H6	CURR2	AIO	Current sink 2 terminal	30V	Open
G6	CURR3	AIO	Current sink 3 terminal	30V	Open
D7	EBATSW	AO	External battery switch gate driver	VSUP	Open
C7	IBATSW	AO	Internal battery switch gate driver	VSUP	Open
C8	XOFF	AO	External OV NMOS gate driver	15V	Open
A6	CHGIN1	S	Charger adapter input (protected)	5.5V	Open
B6	CHGIN1	S	Charger adapter input (protected)	5.5V	Open
A8	CHGIN2	S	2nd Charger adapter input	5.5V	Open
B8	CHGIN2	S	2nd Charger adapter input	5.5V	Open
A7	VSUP_CHG	S IO	Current limiter output, Charger input	VSUP	Open
B7	VSUP_CHG	S IO	Current limiter output, Charger input	VSUP	Open
A9	CHG_OUT	AO	Charger output (liner, switched)	5.5V	Open
B9	CHG_OUT	AO	Charger output (liner, switched)	5.5V	Open
E6	VUSB	S	Charger adapter input (unprotected)	30V	Open
E4	VIBAT	S	Internal Li-Ion battery terminal	5.5V	Open
D3	VEBAT	S	External Li-Ion battery terminal	5.5V	Open

Pin #	Pin Name	I/O	Description	Max. Voltage	If not used
E5	BATTEMP	AIO	Li-Ion battery charger NTC input	3.6V	Open
F8	VSSA	AIO	Analog GND input	-	Mandatory

Pin Description: This table shows the pin description for the CSP package including information of the I/O type, protection and handling if the function block is not used.

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 5:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 30V pins	-0.5	32	V	Applicable for pins VUSB, CURR1/2/3
	Supply Voltage to Ground 15V pins	-0.5	17	V	Applicable for pins XOFF
	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins VSUP_SDx, VSUP_GPIO, VSUP_ANA, VIN_LDOx, LDOx, GPIOx, LX_SDx, GATE_SU, FB_SU, SENSEP/N XRES, SCL, SDA, ONKEY, ENx, VIBAT, VEBAT, E/IBATSW, CTRLx_SD4
	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pins V2_5, CREF, FB_SDx, TEMP_SD4, BATTEMP
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins VSSx, VSSA
	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70°C)					
P_T	Continuous power dissipation		1.2	W	P_T [(1)] for WL-CSP81 package (R_{THJA} ~ 45K/W)
Electrostatic Discharge					
	Electrostatic Discharge HBM		±1.5	kV	Norm: JEDEC JESD22-A114F

Symbol	Parameter	Min	Max	Units	Comments
Temperature Ranges and Storage Conditions					
T_A	Operating Temperature	-40	+85	°C	
R_{THJA}	Junction to Ambient Thermal Resistance			°C/W	R_{THJA} typ. 45K/W
T_J	Junction Temperature		+125	°C	
	Storage Temperature Range	-55	+125	°C	
T_{BODY}	Package Body Temperature		+260	°C	Norm IPC/JEDEC J-STD-020 (2)
	Humidity non-condensing	5	85	%	
	Moisture Sensitive Level	1			Represents an unlimited floor life time

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 6:
AS3715 Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VUSB	Charger HV input		0	5	30	V
CHGINx	Charger input		0	5	5.5	V
VIBAT, VEBAT	Battery Voltage		2.5	3.6	5.5	V
VSUPx	Supply Voltage		2.5	3.6	5.5	V
VINLDO123	Supply Voltage for LDO1, 2 & 3		2.7	3.6	5.5	V
VINLDO456	Supply Voltage for LDO4, 5 & 6		1.7	3.6	5.5	V
VINLDO78	Supply Voltage for LDO7 & 8		1.7	3.6	5.5	V
V2_5	Voltage on Pin V2_5		2.4	2.5	2.6	V
I_{low_power}	Low Power current	@ VSUPx = 4.2V		220		µA
I_{power_off}	Power-OFF current	All regulators OFF, V2_5 ON, supplied via VIBAT only		13		µA

Electrical Characteristics: VSUPx=+2.7V...+5.5V, TA =-40°C...+85°C. Typical values are at VSUPx=+3.6V, TA=+25°C, unless otherwise specified.

Typical Operating Characteristics

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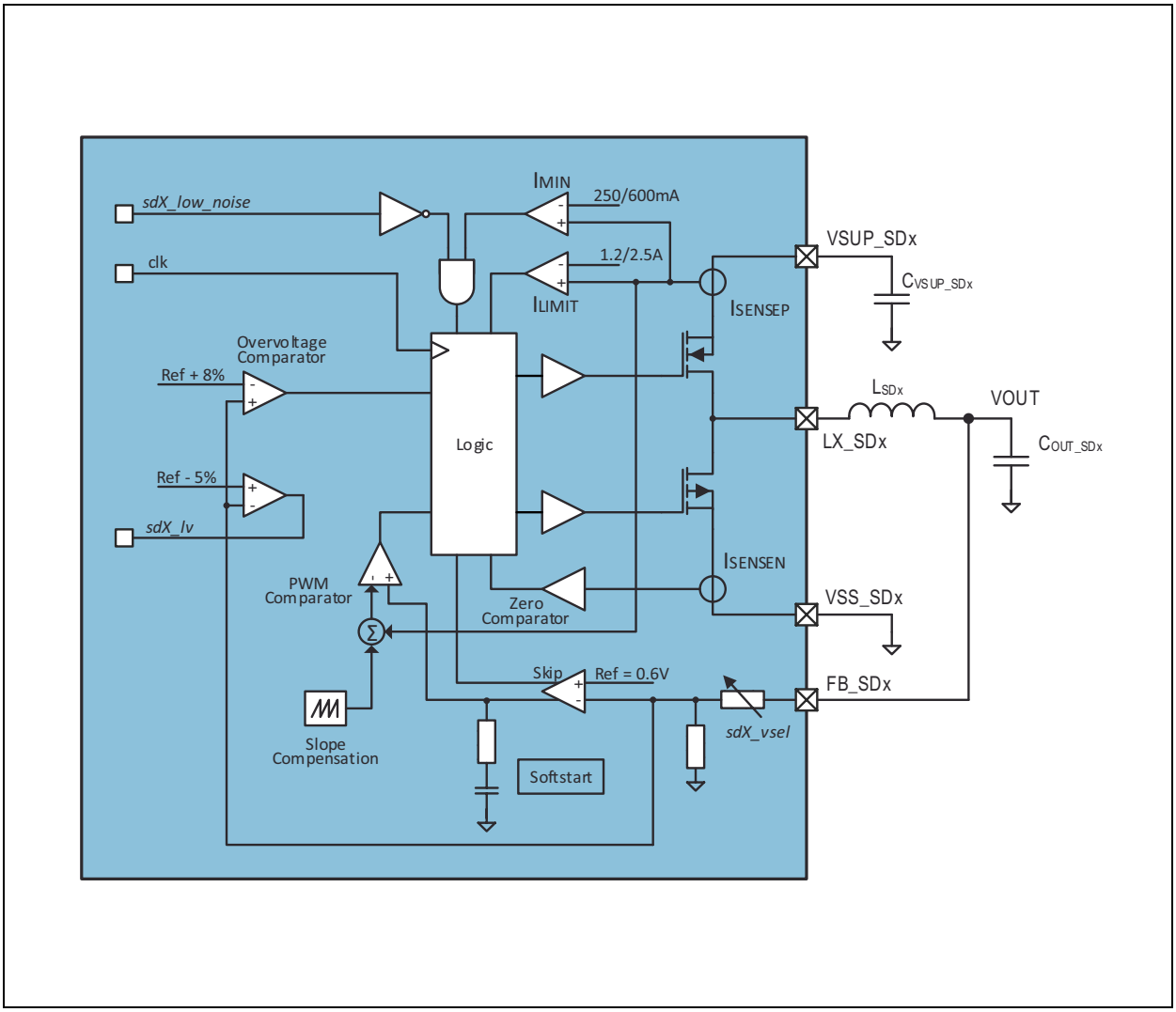
Detailed Description – Power Management Functions

DCDC Step-Down Converter

Description

The step-down converter is a high efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 2A (SD1), and 1A for (SD2, SD3), with an output capacitor of only 8-12µF. The implemented current limitation protects the DCDC and the coil during overload condition.

Figure 7:
Step Down DC/DC Converter Block Diagram



DCDC Step Down Converter Block Diagram: Shows the internal structure of the DCDC bucks.

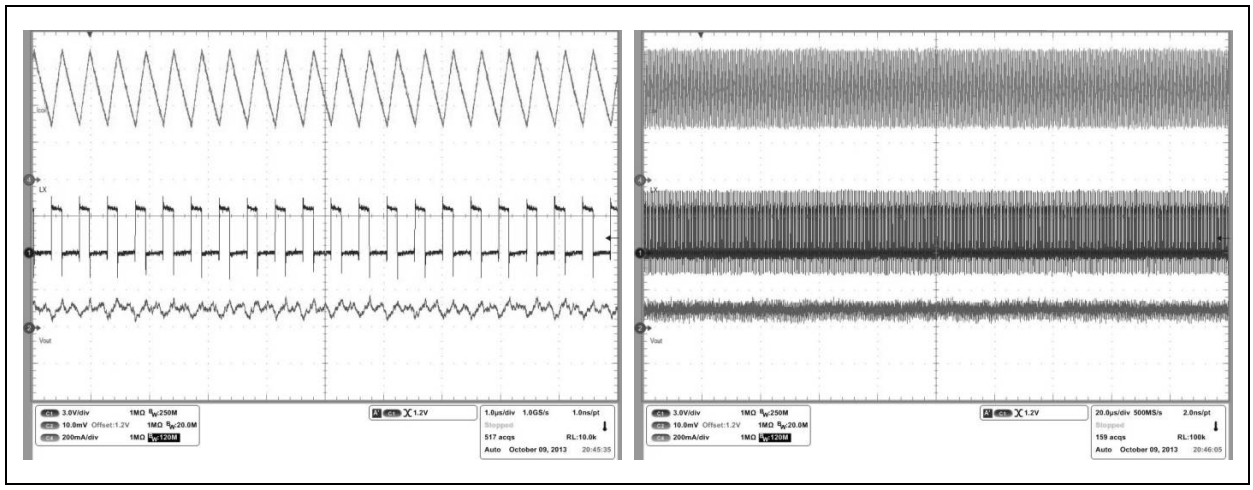
Mode Settings

Low Ripple, Low Noise Operation:

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode.

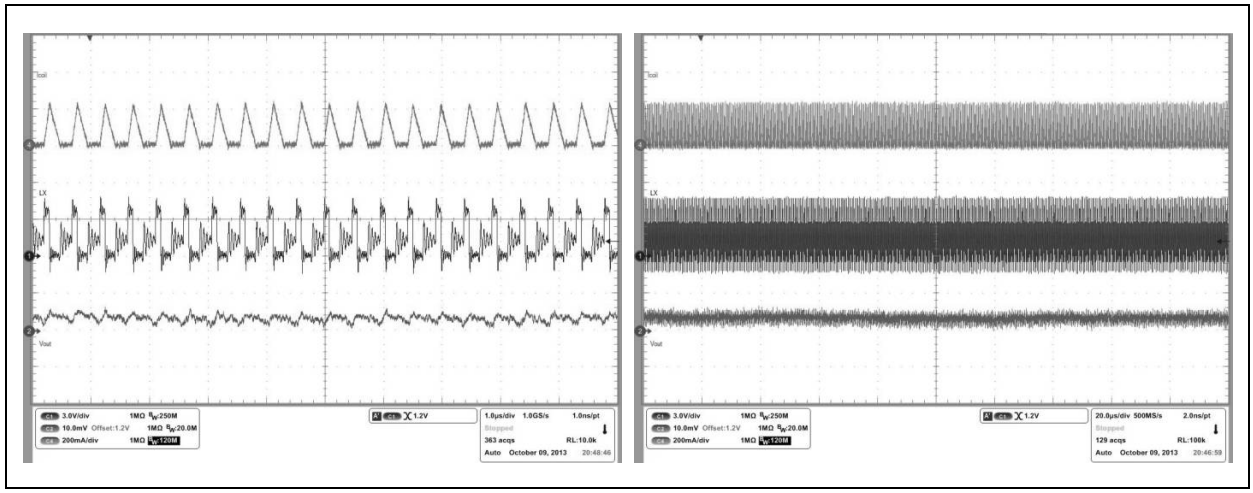
Figure 8:
DC/DC Buck Continuous Mode



DC/DC Buck Continuous Mode: Shows the DC/DC switching waveforms of for SD3 at about 500mA.

When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

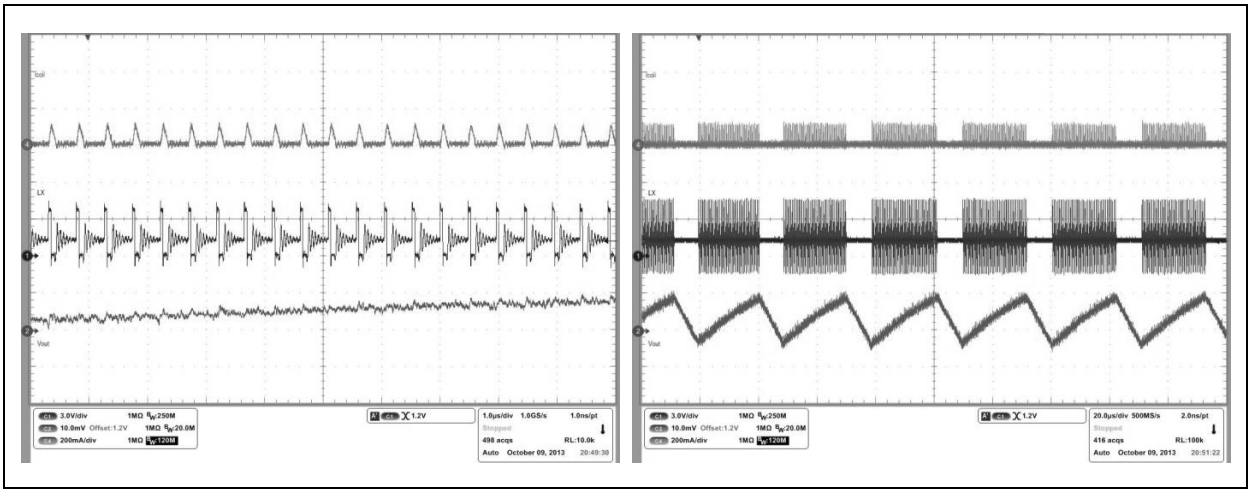
Figure 9:
DC/DC Buck Dis-continuous Mode



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD3 at about 60mA.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation and skip pulses during this time. The crossover point is about ~1% of the DCDC current limit.

Figure 10:
DC/DC Buck Dis-continuous & Low Power Mode



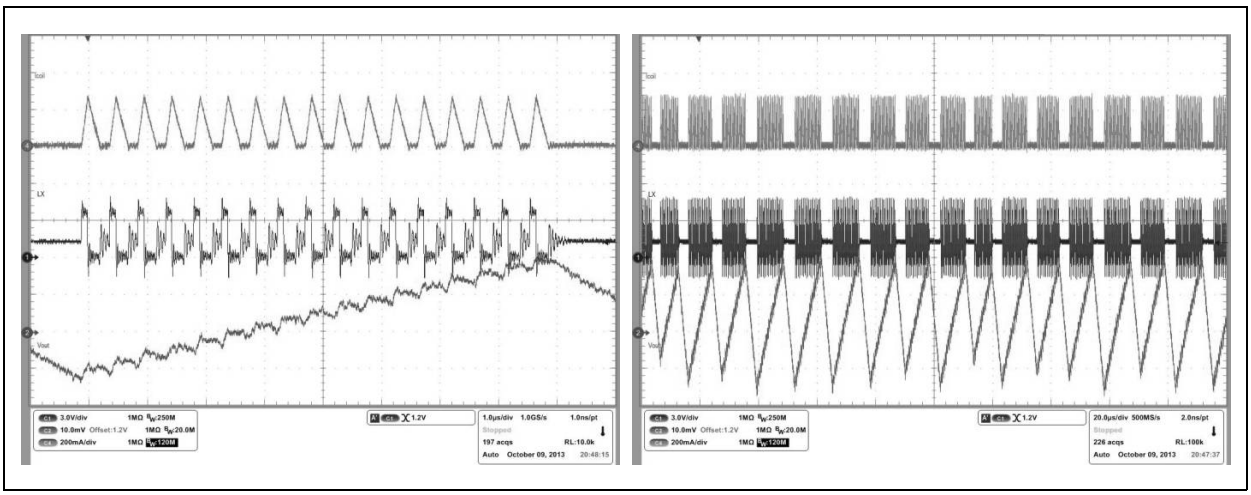
DC/DC Buck Dis-continuous & Low Power Mode: Shows the DC/DC switching waveforms of for SD3 at about 10mA.High efficiency operation (default setting).

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to higher output currents.

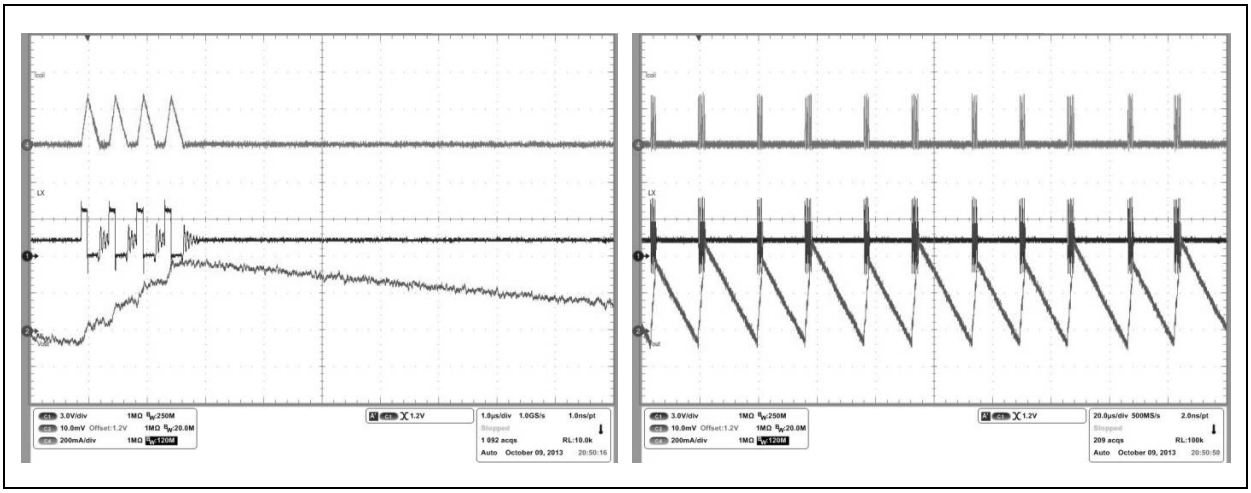
The crossover point to low power mode is already reached at reasonable high output currents (~10% of the DCDC current limit).

Figure 11:
DC/DC Buck Dis-continuous Mode & High Efficiency 1/2



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 60mA with the low_noise bit deactivated.

Figure 12:
DC/DC Buck Dis-continuous Mode & High Efficiency 2/2



DC/DC Buck Dis-continuous Mode: Shows the DC/DC switching waveforms of for SD5 at about 10mA with the low_noise bit deactivated.

It's possible to switch between these two modes during operation.

Power Save Operation (Automatically Controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down controllers, but only for one at a time. (see *dvm_time* and *sd_dvm_select* description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency for SD1 can be set to 3 or 4MHz. SD2 and SD3 have a 2, 3 or 4MHz mode. This mode is selected by setting *sdX_freq* and *sdX_fsel* to the appropriate values.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step-Down Converter Configuration Modes

The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd2_slave*, *sd3_slave* (the default is set by the Boot-OTP)

Parameter

Figure 13:
DC/DC Buck Converter Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.7		5.5	V
V_{OUT}	Regulated output voltage		0.6125		3.35	V
V_{OUT_tol}	Output voltage tolerance	min. 30mV	-3		+3	%
I_{LOAD_SD23}	Load current SD2, 3	VSD2, 3 <1.8V	0		1	A
		VSD2, 3 >1.8V	0		0.7	A
I_{LOAD_SD1}	Load current SD1	VSD1 <1.8V	0		2	A
		VSD1 >1.8V	0		1.2	A
I_{LIMIT}	Current limit	SD2, 3		1.2		A
		SD1		2.5		A
R_{PSW}	P-Switch ON resistance incl. bonds, substrate, etc	SD2, SD3; VSUP_SDx=3.0V		250	500	mΩ

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		SD1, VSUP_SDx=3.0V		120	200	mΩ
R_{NSW}	N-Switch ON resistance incl. bonds, substrate, etc	SD2, SD3; VSUP_SDx=3.0V		160	500	mΩ
		SD1; VSUP_SDx=3.0V		63	200	mΩ
f_{SW}	Switching frequency	sdX_frequ=1; sdX_fsel=1; fclk_int =4MHz		4		MHz
		sdX_frequ=0; sdX_fsel=1; fclk_int =4MHz		3		MHz
		sdX_frequ=0; sdX_fsel=0; fclk_int =4MHz (SD2/3 only)		2		MHz
ηeff	Efficiency	see figures below				%
I_{VDD}	Current consumption	Operating current without load		60		µA
R_{DISCHG}	Pull-down resistance	SD1 disabled		100		Ω
		SD2 or SD3 disabled		200		Ω

DC/DC Buck Converter Parameter: Shows the key electrical parameter of the internal DC/DC buck converters.

Figure 14:
DC/DC Buck Converter External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{OUT\_SD2;3}$	Output capacitor	Ceramic X5R or X7R	8			µF
	Output capacitor, sd2_fast=1 or sd3_fast=1	Ceramic X5R or X7R	18			µF
C_{OUT_SD1}	Output capacitor	Ceramic X5R or X7R	12			µF
	Output capacitor, sd1_fast=1	Ceramic X5R or X7R	27			µF
$C_{VSUP\_SD1;2;3}$	Input capacitor	Ceramic X5R or X7R		2.2		µF
$L_{SD1-SD3}$	Inductor	4/3MHz operation	0.5	1		µH
		4/3MHz; VOUT≤1.8V	0.3	0.47		µH

DC/DC Buck Converter External Components: Shows the external component parameter of the internal DC/DC buck converters.

Figure 15:
DC/DC Buck SD1 3.7V Efficiency vs. Iout

DC/DC Buck SD1 Efficiency: Shows efficiency of the internal SD1 buck converter @ 0.6V, 1.2V & 3.4V with VSUP=3.7V, 2.7MHz operation with TFM252010 1uH coils and T_A=+25°C .

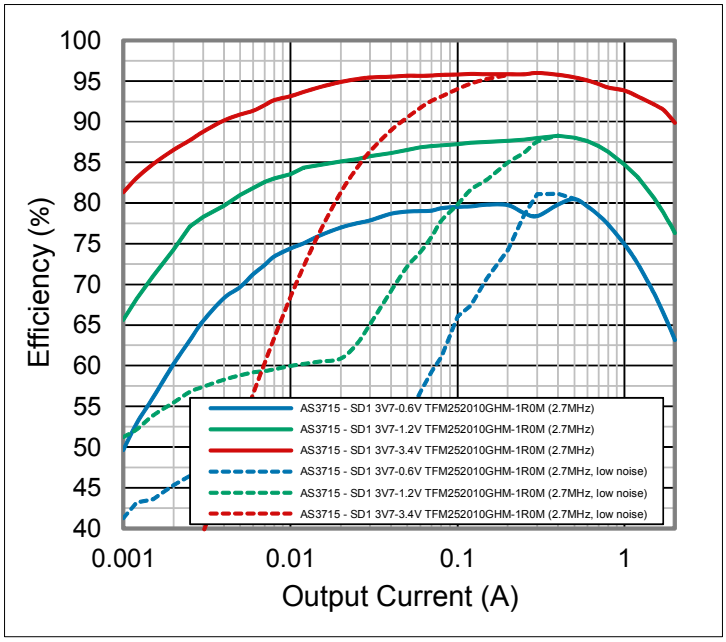
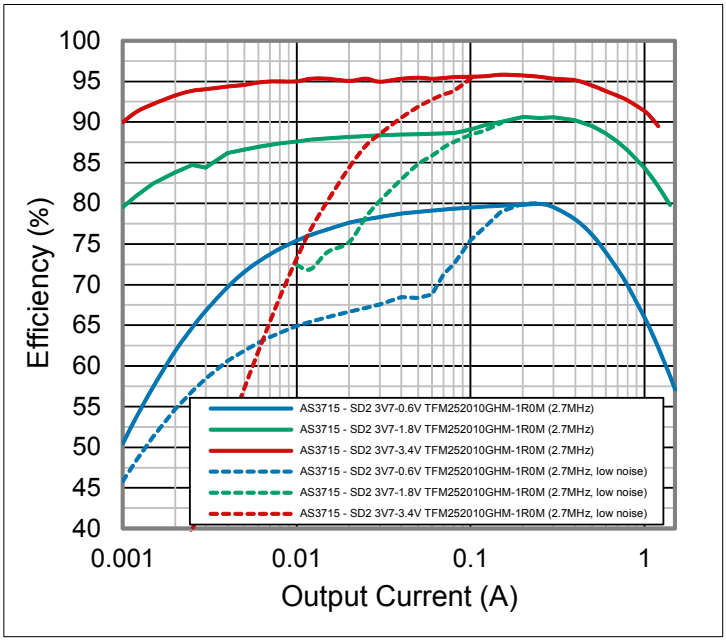


Figure 16:
DC/DC Buck SD2/3 3.7V Efficiency vs. Iout

DC/DC Buck SD2/3 Efficiency: Shows efficiency of the internal SD2/3 buck converter @ 0.6V, 1.8V & 3.4V with VSUP=3.7V, 2.7MHz operation with TFM252010 1uH coils and T_A=+25°C.

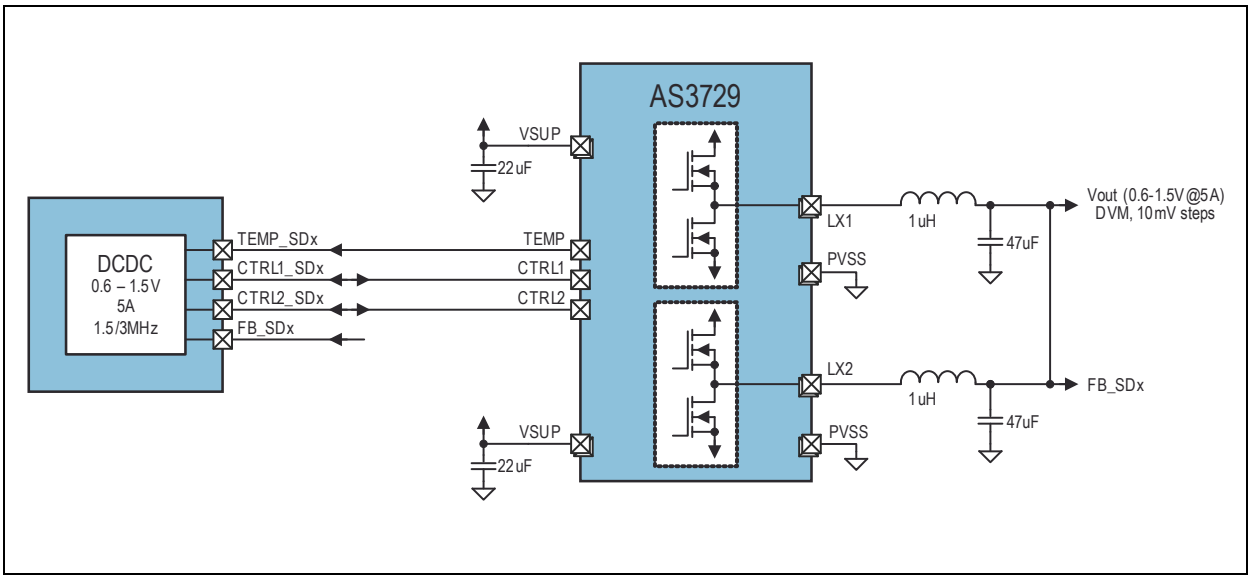


DCDC Step-Down Controller

Description

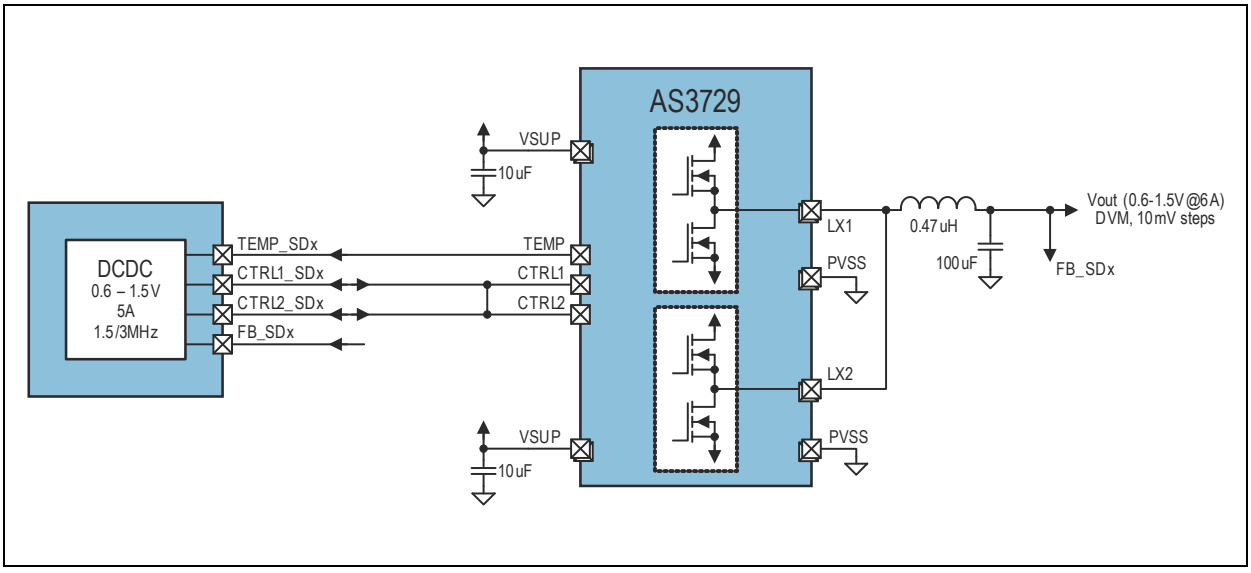
The Step-Down controller SD4 is a dual phase controller using an external power-stage incorporating 2 phases to achieve higher output currents. The maximum output current is 5A with having 2.5A per phase when using the AS3729 power stage. This allows the use of low profile coils without compromising on performance.

Figure 17:
SD4 DC/DC Buck Controller 5A Block Diagram



SD4 DC/DC Buck Controller: Shows basic connection of the SD4 controller to the external power stage (AS3729) for 5A output current.

Figure 18:
SD4 DC/DC Buck Controller 5A Combined Mode



SD4 DC/DC Buck Controller: Shows basic configuration of the SD4 controller to the external power stage (AS3729) for 5A output current using a single coil in combined mode.

Mode Settings

Low Ripple, Low Noise Operation:

Bit settings: *sdX_low_noise*=1

In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. As result, the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to tmin_on to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency, at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will enter low power mode operation. The crossover point is about ~1% of the DCDC current limit.

High efficiency Operation (Default Setting):

Bit settings: *sdX_low_noise*=0

In this mode there is a minimum coil current necessary before switching OFF the PMOS. As a result there are less pulses necessary at low output loads, and therefore the efficiency at low output load is increased. As drawback this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents (~10% of the DCDC current limit).

It's possible to switch between these two modes during operation.

Low Power Operation (sdX_low_power=1):

In this mode the controller is only running on a single phase (phase 1). Only one output stage of the external power stage is used to reduce the power consumption for e.g. a stand-by mode operation.

Power Save Operation (Automatically Controlled):

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/under-shoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

Force PWM Mode Operation:

Even in the case the load current gets so small that less than the minimum ON-time of the PMOS would be needed to keep the loop in regulation the regulator will still stay on the fixed switching frequency without entering low power mode. To guarantee a stable output voltage also negative coil currents are possible. This mode guarantees the lowest possible ripple and a fixed frequency over all load conditions for powering noise sensitive RF circuits, but is compromising on the efficiency. The mode is enabled by setting *sdX_force_pwm* =1.

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a bigger output capacitor to guarantee the stability of the regulator. The mode is enabled by setting *sdX_fast* =1.

100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down controllers, but only for one at a time. (see *dvm_time* and *sd_dvm_select* description)

Parameter

Figure 19:
DC/DC Buck Controller Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input voltage	Pin VSUP_SDx	2.5		5.5	V
V_{OUT}	Regulated output voltage		0.61		1.5	V
V_{OUT_tol}	Output voltage tolerance	min. 20mV	-2		+2	%
I_{VDD}	Current consumption	Dual phase without load		136		uA
f_{SW}	Switching frequency	fclk_int = 4MHz		2.7	3	MHz

DC/DC Buck Controller Parameter: Shows the key electrical parameter of the DC/DC buck controller.

Figure 20:
DC/DC Buck Controller External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
External Components 5A						
AS3729	# power stages		1			
C_{OUT_SD4}	Output capacitor	Ceramic X5R or X7R, high performance	40	47		µF
		Ceramic X5R or X7R, cost optimized	20	22		µF
C_{VSUP_SD4}	Input capacitor	Ceramic X5R or X7R	6	10		µF
L_{SD4}	Inductor	4A rated, 3MHz operation, low Ron	0.3	0.47		µH
External Components 8A (HV)						
AS3728	# power stages		1			
C_{OUT_SD4}	Output Capacitor	Ceramic X5R or X7R / 6.3V high performance	64	82		µF
		Ceramic X5R or X7R / 6.3V cost optimized	32	47		µF
C_{HVSUP_SD4}	HV Input Capacitor	Ceramic X5R or X7R / 25V	10	22		µF
C_{BOOT_SD4}	Boost Capacitor	Ceramic X5R or X7R / 6.3V		100		nF
C_{5VVSUP_SD4}	5V Supply Capacitor	Ceramic X5R or X7R / 6.3V		1		µF
L_{SDx_SD4}	Inductor	5A rated, 1MHz operation, low R_{ON}	0.5	1		µH

DC/DC Buck Controller External Components: Shows the external component parameter of the DC/DC buck controller.

Figure 21:
SD4 3.7V Eff vs. Iout Coil Comparison

DC/DC Buck SD4 Efficiency: Shows efficiency of the SD4 buck controller with AS3729 power stage for different coils @ 1.2V in dual phase and combined mode with VSUP=3.7V, 1.35MHz operation and T_A=+25°C.

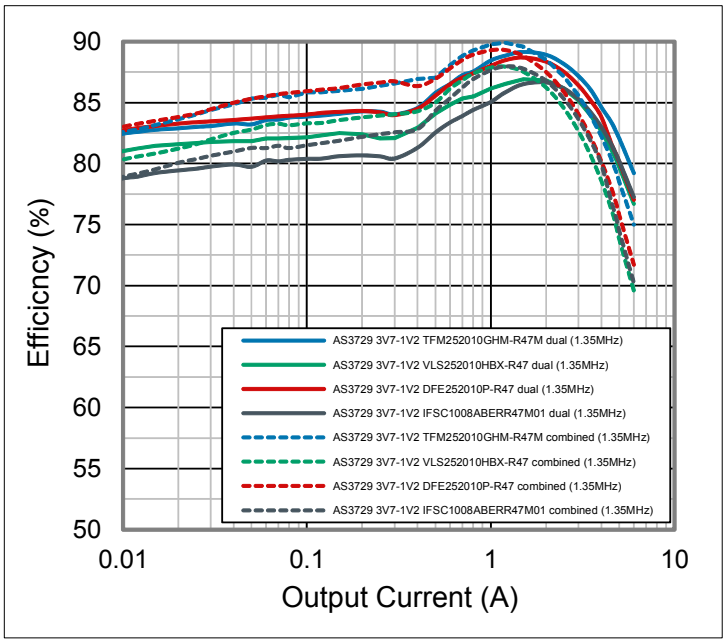
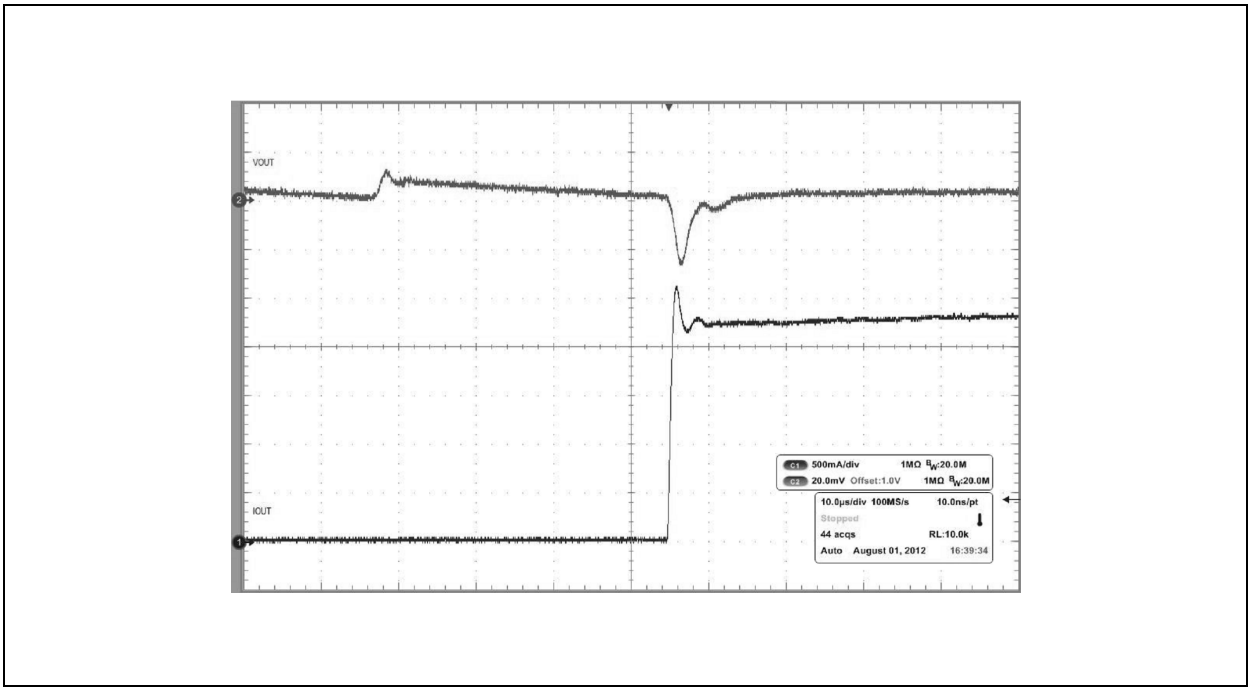
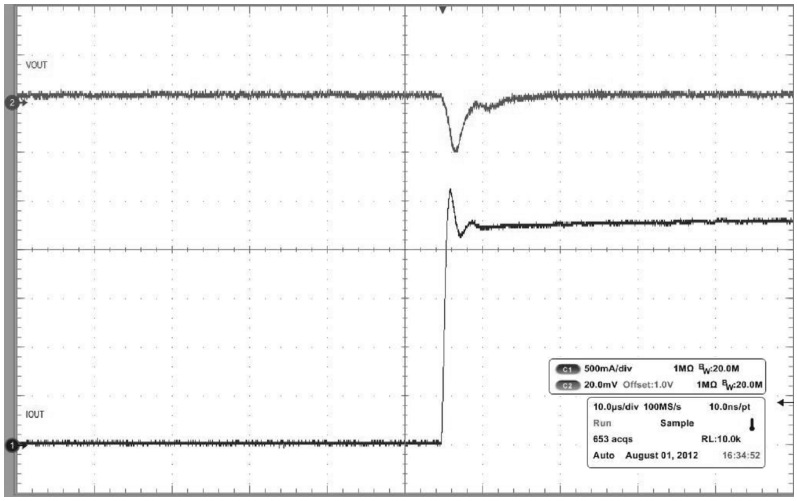


Figure 22:
DC/DC Buck SD4 Load Transient Fast Mode



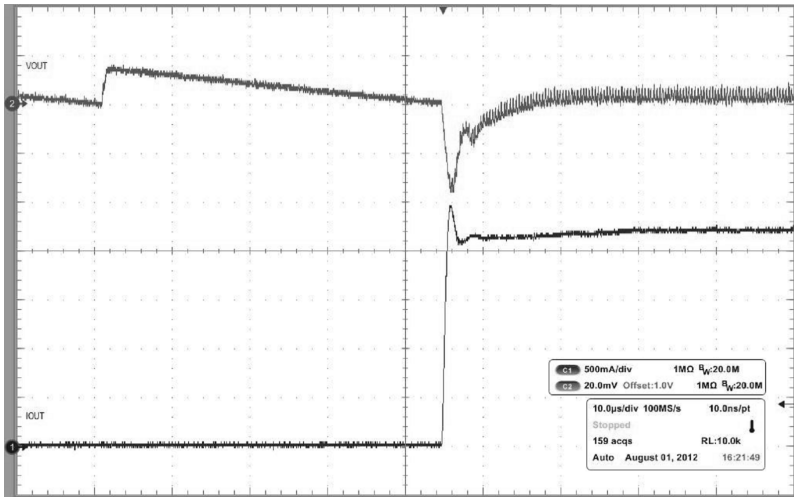
DC/DC Buck SD4 Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF and T_A=+25°C.

Figure 23:
DC/DC Buck SD4 Low Noise Load Transient Fast Mode



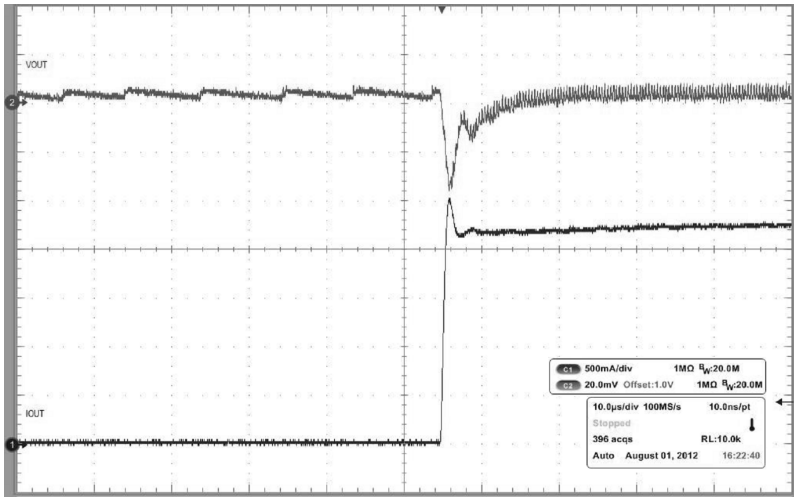
DC/DC Buck SD4 Low Noise Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=1, C_{OUT}=88uF, low_noise=1 and T_A=+25°C.

Figure 24:
DC/DC Buck SD4 Load Transient



DC/DC Buck SD4 Load Transient: Shows the response of the SD4 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=0, C_{OUT}=44uF and T_A=+25°C.

Figure 25:
DC/DC Buck SD4 Low Noise Load Transient



DC/DC Buck SD4 Low Noise Load Transient: Shows the response of the SD0 buck controller to a load transient from 0 to 2.3A @ 1.2V with VSUP=3.7V, 3MHz operation, fast=0, C_{OUT}=44uF, low_noise=1 and T_A=+25°C.

Analog LDO Regulators

Description

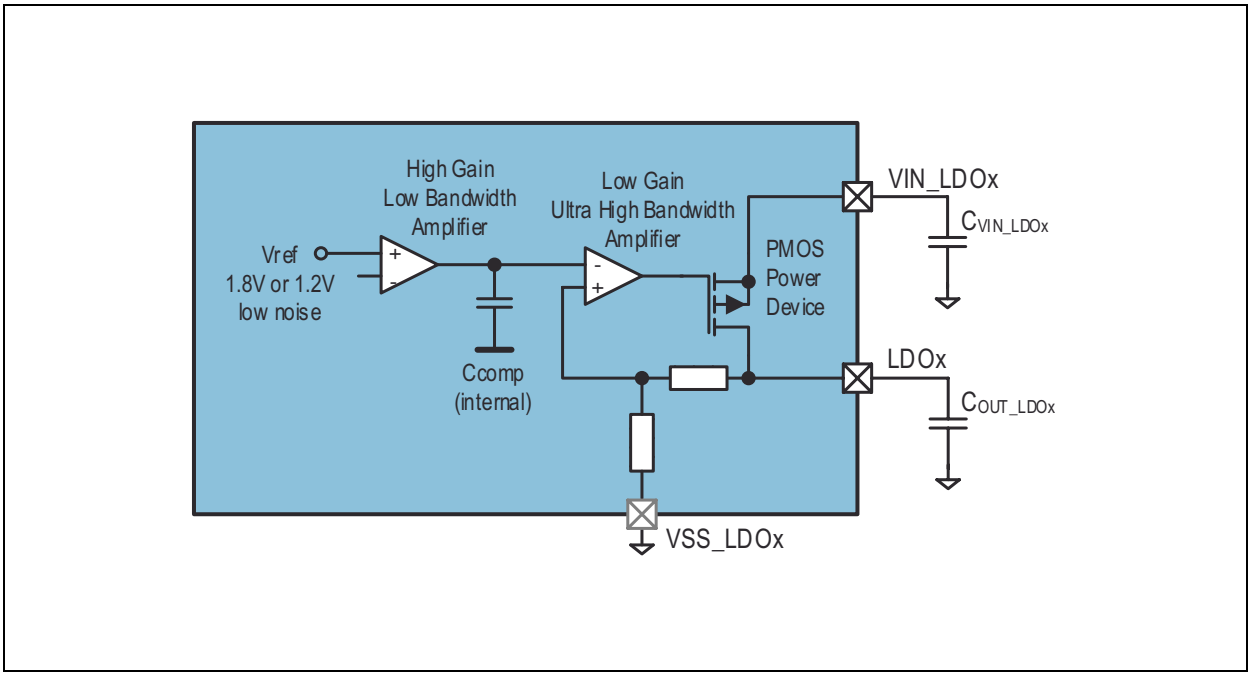
LDO1 and LDO2 are designed to supply sensitive analog circuits like LNA's, Transceivers, VCO's and other critical RF components of cellular radios. Another application is the supply of audio devices or as a reference for AD and DA converters. The design is optimized to deliver the best compromise between quiescent current and regulator performance for battery powered devices.

Stability is guaranteed with ceramic output capacitors of 1µF ±20% (X5R) or 2.2µF +100/-50% (Z5U). The low ESR of these caps ensures low output impedance at high frequencies. Regulation performance is excellent even under low dropout conditions, when the power transistor has to operate in linear mode. Power supply rejection is high enough to suppress the PA-ripple on the battery in TDMA systems at the output. The low noise performance allows direct connection of noise sensitive circuits without additional filtering networks. The low impedance of the power device enables the device to deliver up to IOUT current even at nearly discharged batteries without any decrease of performance.

The default guaranteed operating current during start-up is 150mA, but can be set to 250mA with *ldoX_ilimit* = 1.

To save power in low-power states where the full performance is not needed the bias current can be reduce by setting *reg_low_bias_mode* = 1.

Figure 26:
Analog IO LDO Block Diagram



Analog IO LDO Block Diagram: Shows the internal structure of the analog PMOS linear regulators.

Parameter

Figure 27:
Analog LDO Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{OUT\_LDO1;2}$	Output voltage	Iout<150mA; 10mV steps	1.2		3.3	V
V_{OUT_tol}	Output voltage tolerance	min. 40mV	-3		3	%
I_{OUT_L}	Output current (1)	ldoX_ilimit = 0 (150mA)	0		150	mA
I_{LIMIT_L}	Current limit (1)			300		mA
I_{OUT_H}	Output current (1)	ldoX_ilimit = 1 (250mA)	0		250	mA
I_{LIMIT_H}	Current limit (1)			500		mA
R_{ON}	ON resistance	LDO0-11		0.6		Ω
P_{SRR}	Power supply rejection ratio	f=1kHz	70			dB
		f=100kHz	40			
I_{OFF}	Shut down current				100	nA
I_{VDD}	Supply current	without load		50		µA
		without load, *reg_low_bias_mode* = 1		30		µA
t_{START}	Startup time	low current used during start-up			200	µs
$V_{LineReg}$	Line regulation	Static	-1		1	mV
		Transient; Slope: tr=15µs; delta 1V	-10		10	mV
$V_{LoadReg}$	Load regulation	Static	-1		1	mV
		Transient; Slope: tr=15µs; 1mA->300mA	-10		10	mV
R_{DISCHG}	Pull-down resistance	Regulator disabled		770		Ω

LDO Parameter: Shows the key electrical parameter of the linear regulators.

Note(s) and/or Footnote(s):

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested.

Figure 28:
LDO External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{OUT\_LDO1;2}$	Output capacitor	Ceramic X5R or X7R ldoX_limit = 0	1		5	µF
		Ceramic X5R or X7R *ldoX_limit* =1	2		5	µF
C_{VIN_LDO12}	Input capacitor	Ceramic X5R or X7R	2			µF

LDO External Components: Shows the external component parameter of the linear regulators.

Universal IO LDO Regulators

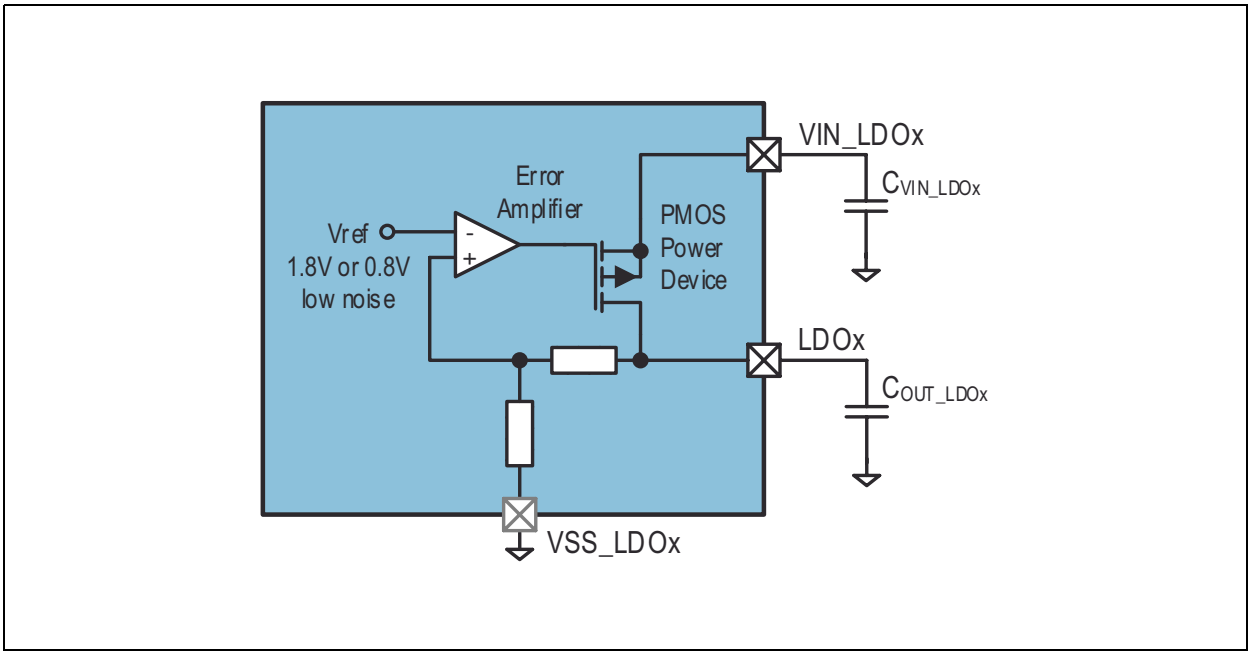
Description

6 universal IO range LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.8 to 3.3V) voltage range to be used for general purpose peripheral supply

Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

LDO7 & 8 offer in addition a load switch function, if the lowest possible drop-out without regulation is needed.

Figure 29:
Universal IO LDO Block Diagram



Universal IO LDO Block Diagram: Shows the internal structure of the universal IO PMOS linear regulators.

Parameter

Figure 30:
LDO Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OUT_LDO3-8}	Output voltage	Iout<150mA; 25mV steps	0.825		3.3	V
V_{OUT_tol}	Output voltage tolerance	min. 40mV	-3		3	%
I_{OUT_L}	Output current (1)	ldoX_ilimit = 0 (150mA)	0		150	mA
I_{LIMIT_L}	Current limit (1)			300		mA
I_{OUT_H}	Output current (1)	ldoX_ilimit = 1 (300mA)	0		300	mA
I_{LIMIT_H}	Current limit (1)			500		mA
R_{ON}	ON resistance	LDO3-8		0.6	1	Ω
P_{SRR}	Power supply rejection ratio	f=1kHz	60			dB
		f=100kHz	30			
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	without load		30	43	µA
t_{START}	Startup time	low current used during start-up			500	µs
$V_{LineReg}$	Line regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
$V_{LoadReg}$	Load regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA->300mA		30		mV
R_{DISCHG}	Pull-down resistance	Regulator disabled		730		Ω

LDO Parameter: Shows the key electrical parameter of the linear regulators.

Note(s) and/or Footnote(s):

1. Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

Figure 31:
LDO External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{OUT_LDO3-8}	Output capacitor	Ceramic X5R or X7R	0.7			µF
C_{VIN_LDO3-8}	Input capacitor	Ceramic X5R or X7R	1			µF

LDO External Components: Shows the external component parameter of the linear regulators.

Low Power LDO V2_5 Regulator

Description

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption, and still offering reasonable regulation characteristics. The regulator has three supply inputs selecting automatically the higher one. This gives the possibility to supply the chip core either with the VIBAT, VEBAT, VSUP or VUSBx depending on the conditions. Bulk switch comparators are used to avoid any parasitic current flow. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 0.7µF must be connected to the output.

Parameter

Figure 32:
Low Power LDO Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Supply voltage rage	see VIBAT, VEBAT, VSUP, VUSB1 or VUSB2				
R_{ON}	ON resistance	Guaranteed per design		50		Ω
I_{OFF}	Shut down current			100		nA
I_{VDD}	Supply current	Guaranteed per design, consider chip internal load for measurements.		3		µA
t_{START}	Startup time			200		µs
V_{OUT}	Output voltage		2.4	2.5	2.6	V
I_{OUT}	Output current	VSUP>3.0V in power_off mode			3	mA

Low Power LDO Parameter: Shows the key electrical parameter of the low power V2_5 linear regulator.

Figure 33:
Low Power LDO External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{V2_5}	Output capacitor	Ceramic X5R or X7R	0.7			µF

Low Power LDO External Components: Shows the external component parameter of the low power V2_5 linear regulator.

DCDC Step-up Converter

Description

The DC/DC Step Up converter is a high efficiency current mode PWM regulator, which provides an output voltage dependent on the maximum VDS voltage of the external transistor, and maximum load current selectable by the external shunt resistor. For Example:

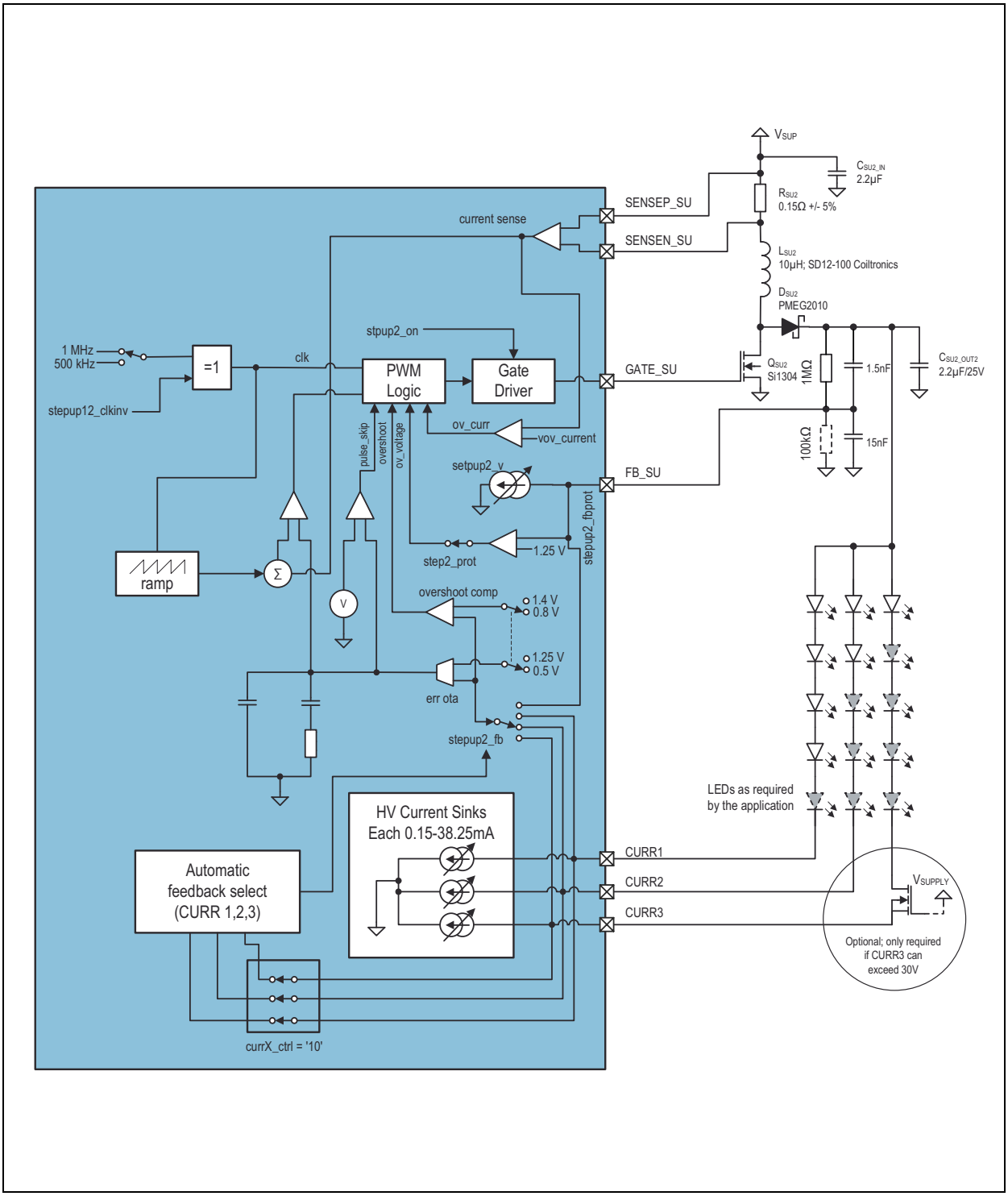
- 5V, 0.5-1A @ 1Mhz
- 25V, 50mA @ 1MHz
- 40V, 20mA @ 500kHz

A constant switching frequency results in a low noise on supply and output voltage.

Three feedback regulation modes are supported:

- Current feedback (all three current sinks can be selected)
- Current feedback with automatic feedback selection
- Voltage feedback

Figure 34:
DCDC Step-Up Converter



DCDC Step-Up Converter Block Diagram: Shows the internal structure of the DCDC boost controller including external components.

Feedback Selection

For the step up the following feedback selections are possible (selected by *setpup2_fb*): (see Figure 34)

Current Feedback

CURR1, CURR2 and CURR3 can be selected by *setpup2_fb* as a current feedback pin.

The step-up converter is regulated such that the required current at the feedback path can be supported. In this mode the output voltage will be limited by limiting the voltage on the selected feedback pin to 1.25V (select the external resistor network and *stepup2_v* to adjust this limitation voltage).

stepup2_prot_dis has to be set to 0, otherwise the protection is disabled.

Always choose the path with the higher voltage drop as feedback to guarantee adequate supply for the other, unregulated path.

Current Feedback with Automatic Feedback Selection

Same as above, but when *currX_ctrl* = 10b for the used current sinks, the chip automatically selects the highest string (CURR1, CURR2 or CURR3) as feedback input.

Voltage Feedback

The step-up converter output voltage is regulated by regulating the selected feedback pin voltage to 1.25V.

Calculating Resistors for Voltage Feedback or Over-Voltage Protection

Bit stepup_res should be set to 1 in voltage feedback mode using two resistors.

The output voltage is regulated to a constant value, given by:

(EQ1) $$V_{SU} = \frac{R_1 + R_2}{R_2} \times 1.25 + I_{FB} \times R_1$$

If R2 is not used, the output voltage is:

(EQ2) $$V_{SU} = 1.25 + I_{FB} \times R_1$$

V_{SU}: Step up regulator output voltage
R_1 Feedback resistor R1
R_2 Feedback resistor R2
I_{FB}: Tuning current on FB_SU pin: *stepup2_v* (0..31µA (1µA steps))

Figure 35:
SU Output Voltage or Protection Voltage

SU Output Voltage or Protection Voltage: Shows examples of possible output or protection voltages of the DCDC SU depending on external resistors and FB_SU current settings.

I_{FB} (*stepup2_v*)	V_{SU}	V_{SU}
µA	R_1=1MΩ, R_2 not used	R_1=500kΩ, R_2 = 64kΩ
0	-	11
1	-	11.5
2	-	12
3	-	12.5
4	-	13
5	6.25	13.5
6	7.25	14
7	8.25	14.5
8	9.25	15
9	10.25	15.5
10	11.25	16
11	12.25	16.5
12	13.25	17
13	14.25	17.5
14	15.25	18
15	16.25	18.5
16	17.25	19
17	18.25	19.5
18	19.25	20
19	20.25	20.5
20	21.25	21
21	22.25	21.5
…	…	…
30	31.25	26
31	32.25	26.5

Parameter

Figure 36:
DCDC SU Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{VDD}	Quiescent Current	Pulse skipping mode		140		µA
V_{FB}	Feedback voltage for external resistor divider	For constant voltage control	1.20	1.25	1.30	V
V_{CURR}	Feedback voltage for current sink regulation	CURR1, CURR2, CURR3		0.6		V
I_{DCDC_FB}	Additional tuning current at FB_SU	Adjustable by software in 1µA steps	0		31	µA
	Accuracy of feedback current	@ full scale	-7		7	%
V_{rsense_max}	Current limit voltage at Rsense	E.g.: 0.65A for 0.15Ω sense resistor		100		mV
R_{SW}	Switch resistance	ON-resistance of external switching transistor			1	Ω
I_{load}	Load current	At 25V output voltage	0		50	mA
f_{IN}	Switching frequency	Internal CLK frequency/4, default 1MHz		$f_{clk\_int}/4$		MHz
t_{MIN_ON}	Minimum ON time			130		ns
MDC	Maximum duty cycle	@ 1MHz		91		%

DCDC SU Parameter: Shows the key electrical parameter of the DCDC boost converter.

Figure 37:
DCDC SU External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{out}	Output capacitor	ceramic, ±20%		2.2		µF
L_{SU}	Inductor	Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency; Vout >8V		10		µH
		Use inductors with small $C_{parasitic}$ (<100pF) to get high efficiency; Vout <8V		4.7		µH
Q_{SU}	Transistor	$V_{GS(TH)}$ threshold voltage		1.3	1.5	V
		V_{DS} max drain to source voltage	V_{out_max} +20%			V
		$R_{DS(ON)}$ drain - source ON resistance		0.35		Ω
		Q_{GS} total gate charge @ V_{GS}=4.5V		3	5	nC
C_1 / C_2	Feedback capacitor ratio	Ratio should be smaller than the feedback resistor ratio (inverted) to avoid overshoots during start-up			R_2 / R_1	µF

DCDC SU External Components: Shows the external component parameter of the DCDC boost converter.

Current Sinks

Description

CURR1, 2 and 3 are high voltage (30V) current sinks, e.g. for series of white LEDs or general purpose usage to drive buzzer, vibrator, signal LEDs, etc.

Current sinks CURR1, 2 and 3 can be controlled individually. The step-up DCDC converter (SU) may supply them with voltages up to 30V. For an automatic feedback selection the used current sinks can be assigned to the SU booster.

If not used as a current sink, CURR3 can be used to output several status signals. In this mode the CURR3 output acts like an open-drain output and needs an external pull-up resistor for generating logic high levels.

Parameter

Figure 38:
Current Sink Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{CURR1,2,3}$	CURR1,2 & 3 current	For V(CURRx) > 0.5V resolution = 0.156mA	0		39.8	mA
$I_{DCDC\_protect}$	Current sink protection Current	Protection current if *stpup_on*=1 and *currx_current*=00h		2		µA
Δ	Absolute Accuracy	All Current sinks	-8		+8	%
$V_{CURR1,2,3}$	Voltage compliance	During normal operation	0.5		30	V

Current Sink Parameter: Shows the key electrical parameter of the HV current sinks.

Charge Pump

Description

- The Charge Pump uses the external flying capacitor to generate output voltages higher than the battery voltage. The output voltage is up to 2 times VSUP (without load), but is limited to $V_{CPOUTmax}$ all the time
- VSUP current = 2 times output current

Parameter

Figure 39:
Charge Pump Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CPOUT}	Output Current		0		60	mA
V_{CPOUT}	Output Voltage	VSUP = 3.4V min, I_{CPOUT}=55mA max	4.8		5.3	V
$V_{CPOUTmax}$	Output Voltage	Including output ripple			5.6	V
R_{CP}	Effective Charge Pump Output Resistance	VSUP = 3.0V		31		Ω
$I_{SHUTDOWN}$	Shutdown Current				0.1	µA

CP External Components: Shows the external component parameter of the 5V charge pump.

Figure 40:
CP External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{out}	Output capacitor	Ceramic, ±20%; capacitor between V5_0 and VSS_CP			4.7	µF
C_{FLY}	Flying capacitor	Ceramic, ±20%; capacitor between CAPP and CAPN		470		nF

CP External Components: Shows the external component parameter of the 5V charge pump.

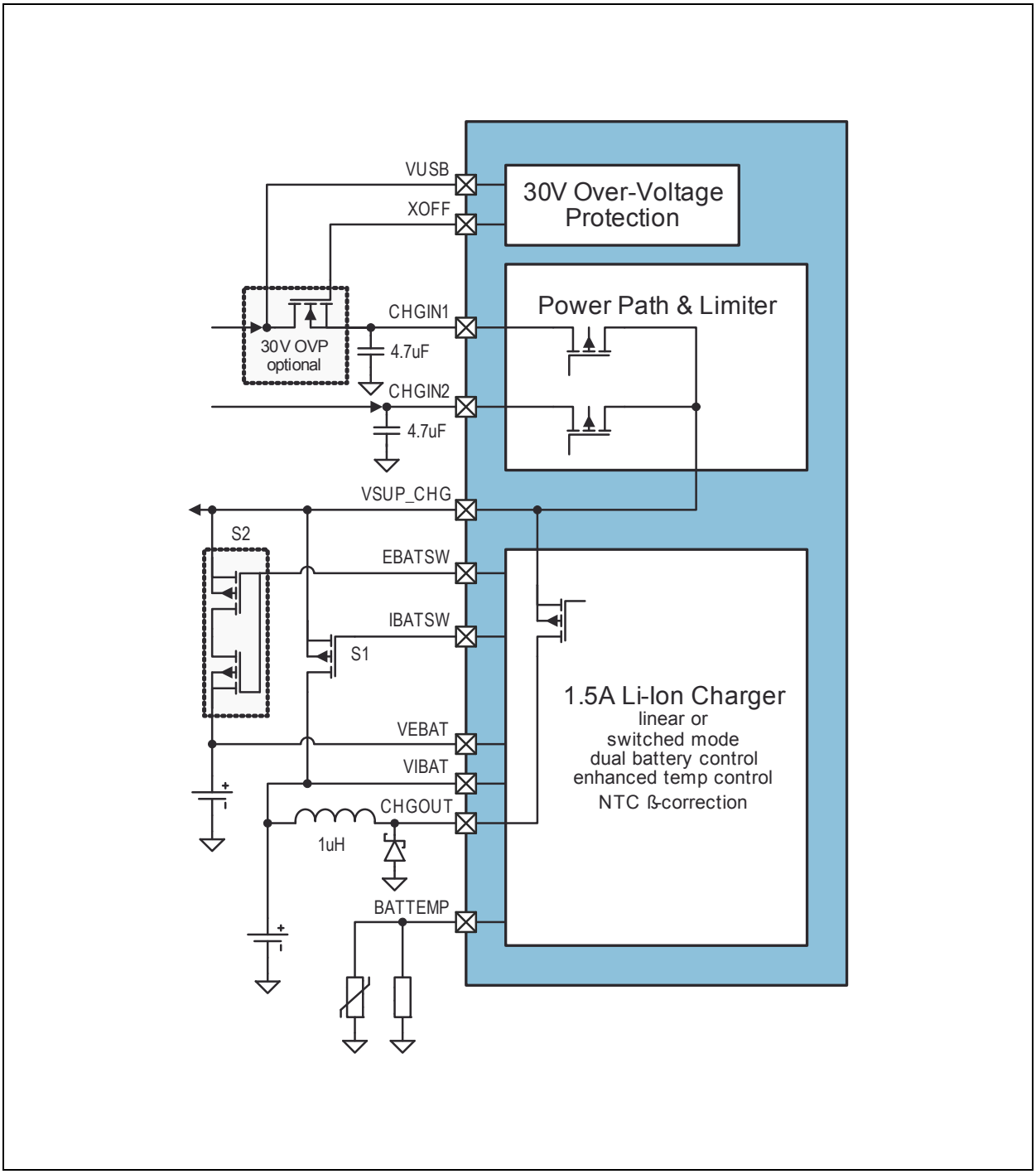
Charger

Description

The AS3715 device serves as a standalone battery charge controller supporting rechargeable Lithium Ion (LiIon) and Lithium Polymer batteries. Requiring only a few external components, a full-featured battery charger with a high degree of flexibility can easily be realized. The main features of the controller are:

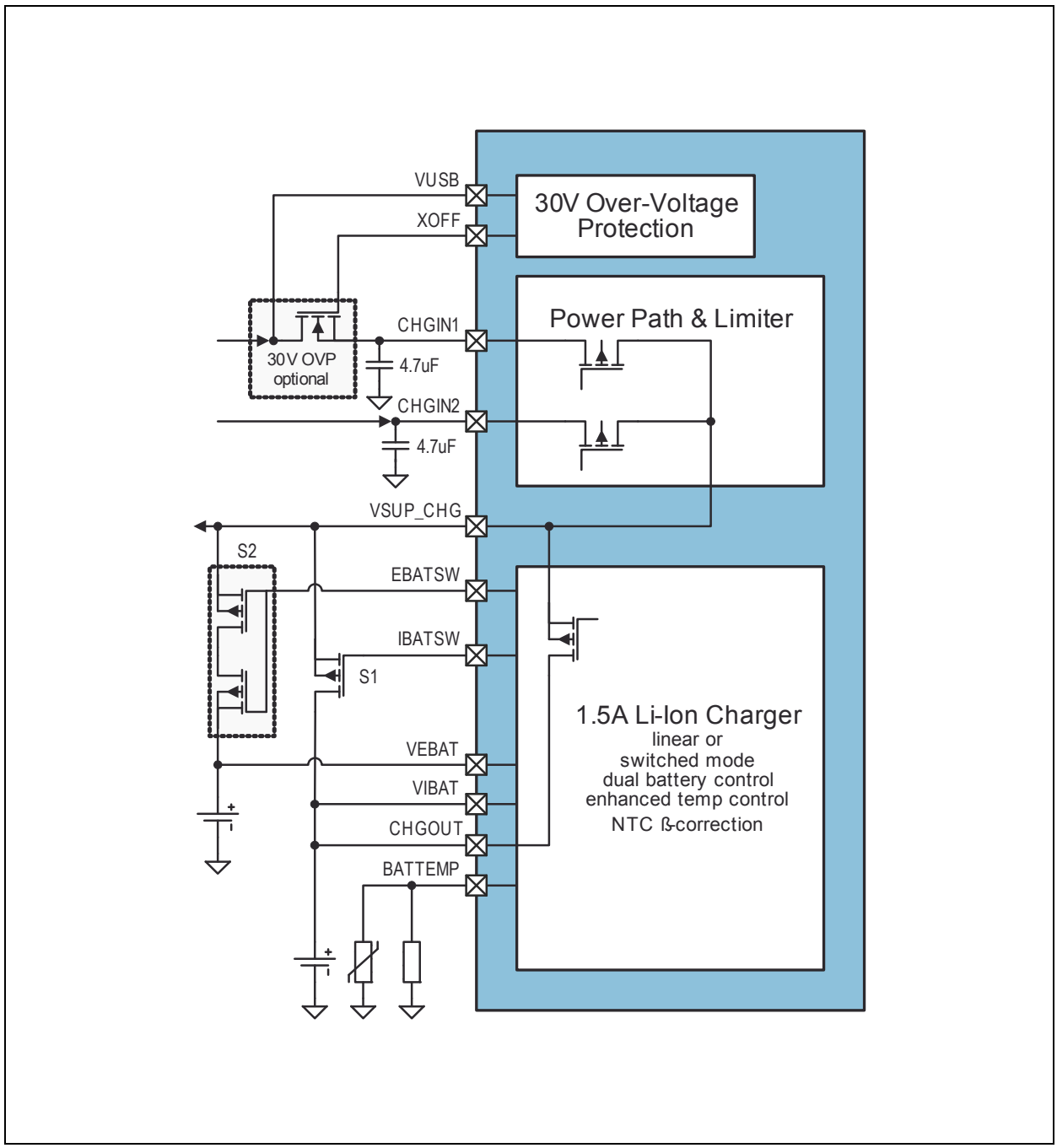
- Charge adapter detection
- PowerPath management & internal voltage regulator (V2_5), for dead battery startup
- Low current (soft) charging
- Low current (trickle) charging
- Constant current charging
- Constant voltage charging
- 30V Overvoltage protection for CHGIN1(optional)
- Battery presence indication
- Operation without battery
- Separate input current limitation for CHGIN1/2
- Input voltage drop regulation
- Programmable linear or switched mode operation
- Single power-path mode for reduced ON-resistance
- Bypass mode for high input current application (up to 6A)

Figure 41:
Charger Application Block Diagram, Switch Mode Charger



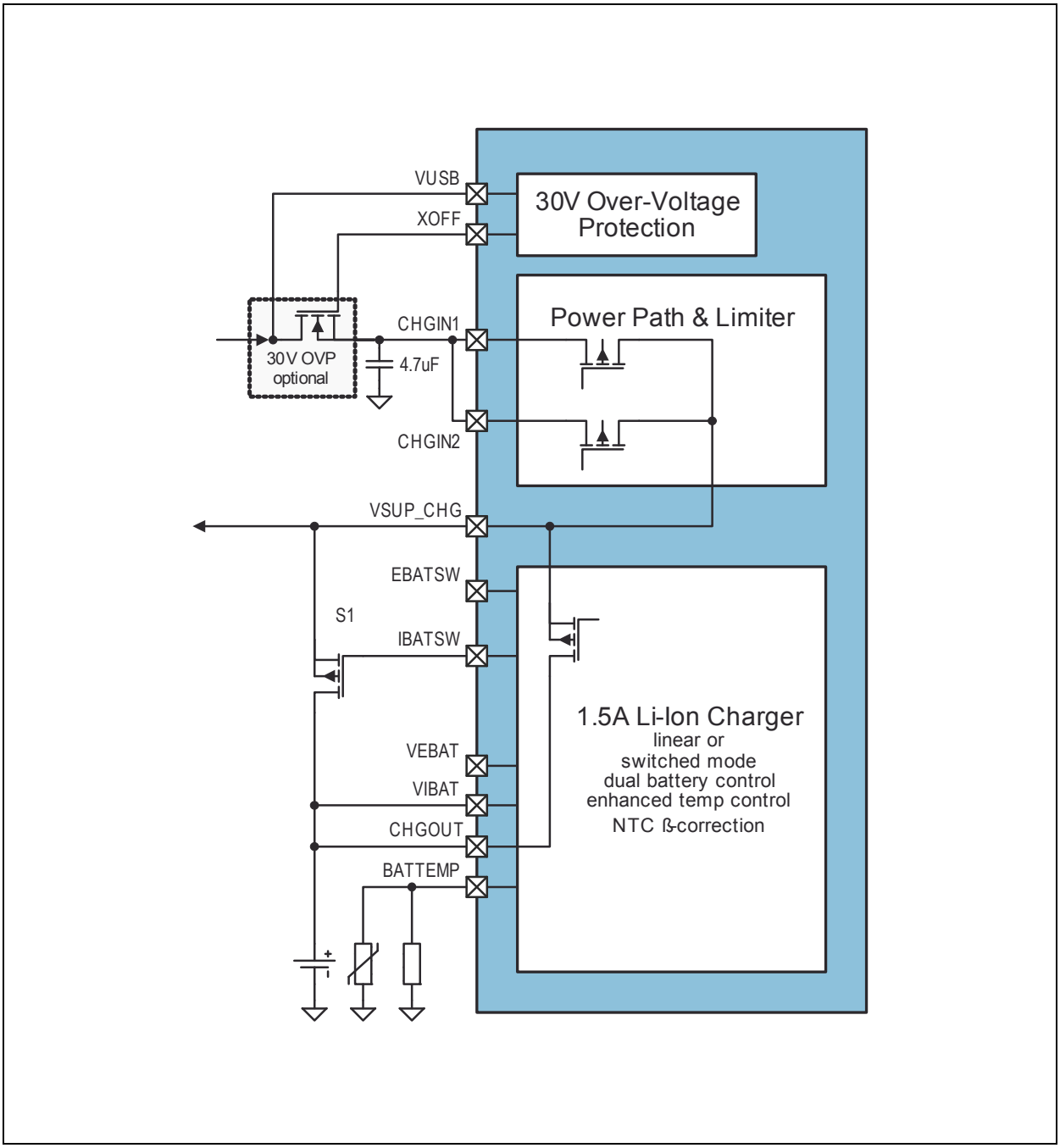
Switch Mode Charger Block Diagram: Shows the connections and external components for the charger operating in switch mode.

Figure 42:
Charger Application Block Diagram, Linear Mode Charger



Linear mode Charger Block Diagram: Shows the connections and external components for the charger operating in linear mode.

Figure 43:
Charger Application Block Diagram, Linear Mode Single Power-path and Battery



Linear mode Charger Block Diagram: Shows the connections and external components for the charger operating in linear mode with a single power-path and only one battery.

Charging Cycle Description

Charge Adapter Detection

The charge controller uses an integrated detection circuit to determine if an external charge adapter has been applied to the VUSB pin. If the adapter voltage exceeds the battery voltage at pin VBAT by V_{CHDET} the *ChDet* bit in the ChargerStatus register will be set. The detection circuit will reset the charge controller (bit *ChDet* is cleared) as soon as the voltage at the VUSB pin drops to only V_{CHMIN} above the battery voltage. In case the AS3715 device is reset the charge controller will also be reset, even if a charge adapter is applied to the VUSB pin.

Soft Charging

Soft charge mode is started when an external charge adapter has been detected, the *bat_charging_enable* is set and the battery voltage at pin VBAT is below the VSOFT threshold.

Low Current (Trickle) Charging

Trickle charge mode is started when an external charge adapter has been detected bat_charging_enable is set and the battery voltage at pin VBAT is below the $V_{TRICKLE}$ threshold and above V_{SOFT} threshold; bits *ChDet* and *Trickle* will be set in the ChargerStatus register. In this mode the charge current will be limited to *TrickleCurrent* (set in the ChargerCurrent register) to prevent undue stress in case of deeply discharged batteries. Once $V_{TRICKLE}$ has been exceeded, the charger will change over to constant current charging (*Trickle* is cleared).

Constant Current Charging

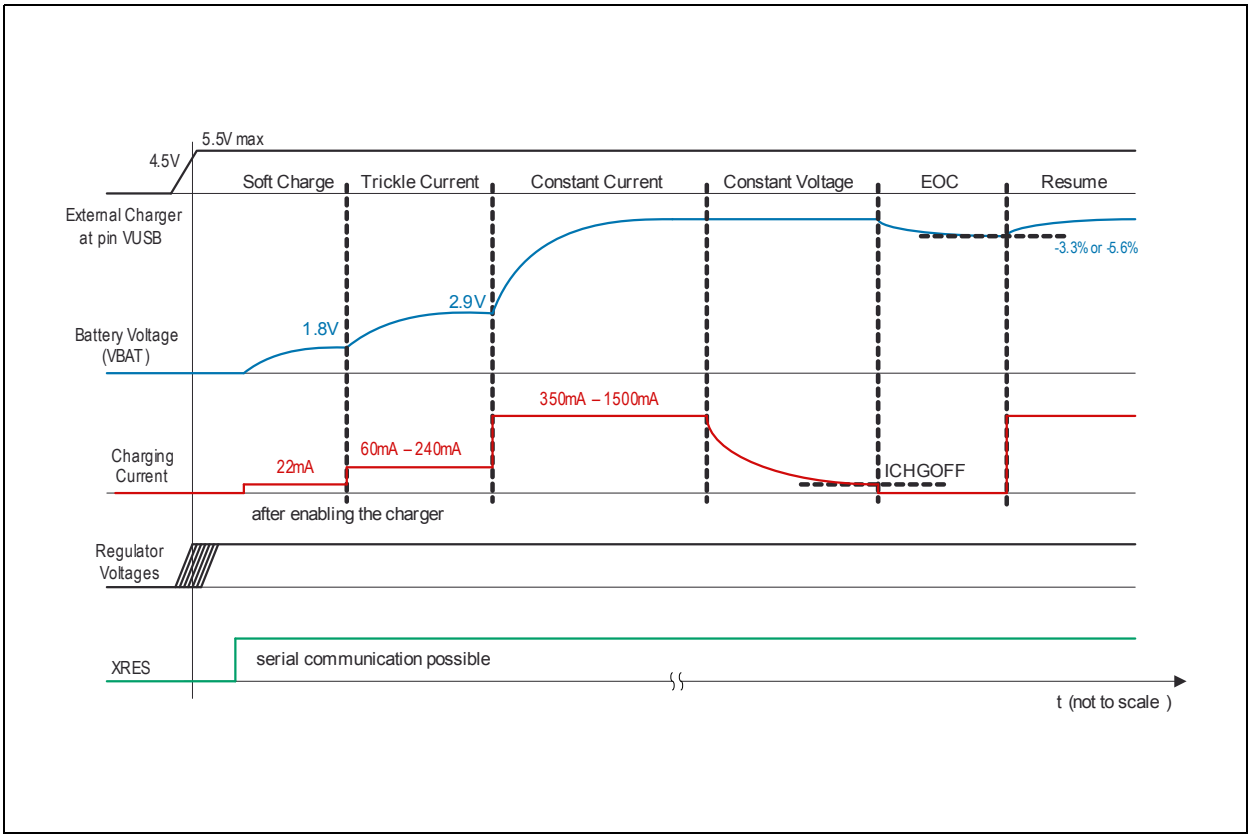
Constant current charging is initiated when *bat_charging_enable* is set and the battery voltage at pin VBAT is above the $V_{TRICKLE}$ and below V_{CHOFF}. The *CCM* bit is set when the charger has started, and the charge current will be limited to *ConstatntCurrent* by the battery charge controller. When the battery approaches full charge, its voltage will reach the charge termination threshold V_{CHOFF}. V_{CHOFF} depends on the *ChVoltEOC* bits settings. Top-off charge will be started (*CVM* will be set).

Constant Voltage Charging

Constant voltage charge mode is initiated and the *CVM* bit will be set when the V_{CHOFF} threshold has been reached.

The charge current is monitored during constant voltage charging. It will be decreasing from its initial value during constant current charging and eventually drop below the value set by *TrickleCurrent*. If the measured charge current is less than or equal to *TrickleCurrent*, the charging cycle is terminated and *EOC* is set.

Figure 44:
Charger States



Charger States Diagram: Shows a full charging cycle with the corresponding states.

Stop Charging Conditions

There are multiple safety features implemented that trigger a stop_charging condition:

These are the following:

- Battery temperature too high/low. If ntc_on=1 and voltage at pin NTC is below/above VBATTEMP threshold.
- Timeout timer expired (If *ch_timeout*>0 and charging time has been exceeded. (Can be reset by unplugging the charger, setting *bat_charging_enable*=0 or writing *charging_tmax*=0)
- VUSB over-voltage detected
- Die temp>140deg (ov_temp_140 set)
- All reset reasons

Battery Presence Indication

After EOC state is reached a timer for NOBAT detection is started. If there is no battery present, the VBAT voltage will drop to V_{RESUME}. Depending on the load on VBAT and the capacitor on VBAT this might take some milliseconds to 1 second. If the RESUME mode is enabled (bit *auto_resume*=1), the charger will restart charging (ConstantCurrent charging) after 100msec delay.

The 100msec dead time is necessary to get a battery oscillation frequency below 10Hz, if there is no battery present.

If the NOBAT detection timer is below 2 seconds after reaching *EOC* state, and this happens 2 times in serial, the *Nobat* bit in ChargerStatus register is set. If a battery is inserted the bit will be reset after the timer exceeds the 2 seconds.

Charger Overvoltage Protection

This blocks checks if the charger voltage VUSB is above VCHOVH. If the VUSB voltage is above VCHOVH , the pin XOFF is pulled to GND immediately, to protect the pin VCHG_IN, and the charger is set into OFF state. If the VUSB voltage is below VCHOVH the XOFF pin is charged up to VXOFF_REG with an integrated charge pump. If the pin exceeds VXOFF_MIN the bit is set and the charger is started.

NTC Supervision

This charger block also features a supply for an external NTC resistor to measure the battery temperature while charging. If the temperature is too high the charger will stop operation. If needed an interrupt can be generated based on this event. When the battery temperature drops the voltage on BATTEMP pin will rise above VBATTEMP_OFF and the charger will start charging again. This is forming a temperature hysteresis of about 3 to 5°C to avoid an oscillation of the charger.

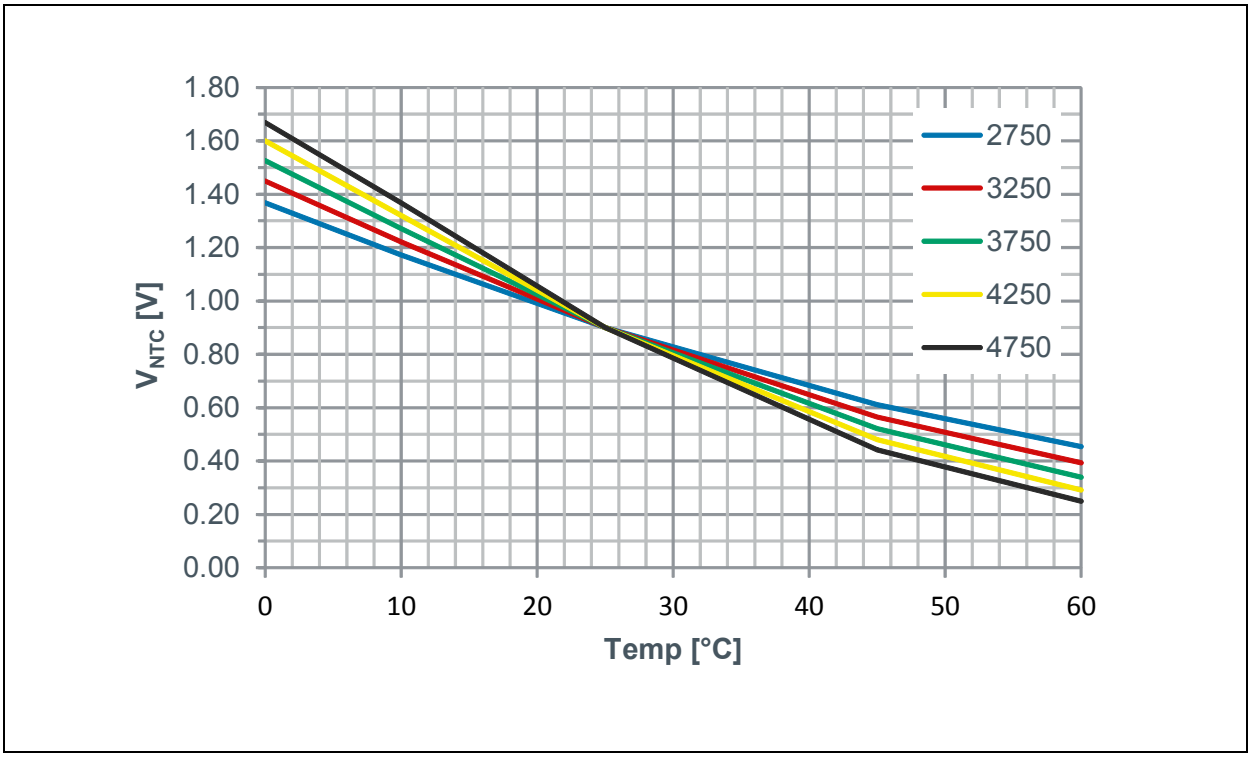
The type of NTC (*ntc_10k*:10k or 100k) can be selected via register settings. The battery temperature supervision via the NTC can be switched OFF (*ntc_on*= 0).

The supply for the NTC will be on when the *ntc_on* bit is set, no matter if a charger is detected or not.

NTC ß-Correction

To keep the voltage drop over the whole temperature range inside of the ADC input range a parallel resistor to the NTC is needed.

Figure 45:
NTC ß Influence



NTC ß Influence Diagram: Shows the voltage drop on the NTC over temperature for different ß using R_{NTC}=10kΩ, R_p=15kΩ and I_{NTC}=150uA.

The chip is supporting up to 4 temperature levels for supervision.

Figure 46:
NTC Supervision

		ß	2750	3250	3750	4250	4750	K
T1	e.g.: 0 C		1,37	1,45	1,53	1,60	1,67	V
T2	e.g.: 10 C		1,17	1,22	1,27	1,32	1,37	V
T3	e.g.: 45 C		0,61	0,57	0,52	0,48	0,44	V
T4	e.g.: 60 C		0,45	0,39	0,34	0,29	0,25	V

NTC Supervision: Example threshold voltages for different temperatures and ß using R_{NTC}=10kΩ, R_p=15kΩ and I_{NTC}=150uA.

The base values (T1min, T2min, T3min and T3min) for the comparator levels are marked in the table above. To adjust the comparator levels to the needed temperature levels dedicated adjust bits can be set (32-64 7mV steps).

(EQ3) Txlim_upper=Txmin + *Tx_adj* * 7mV

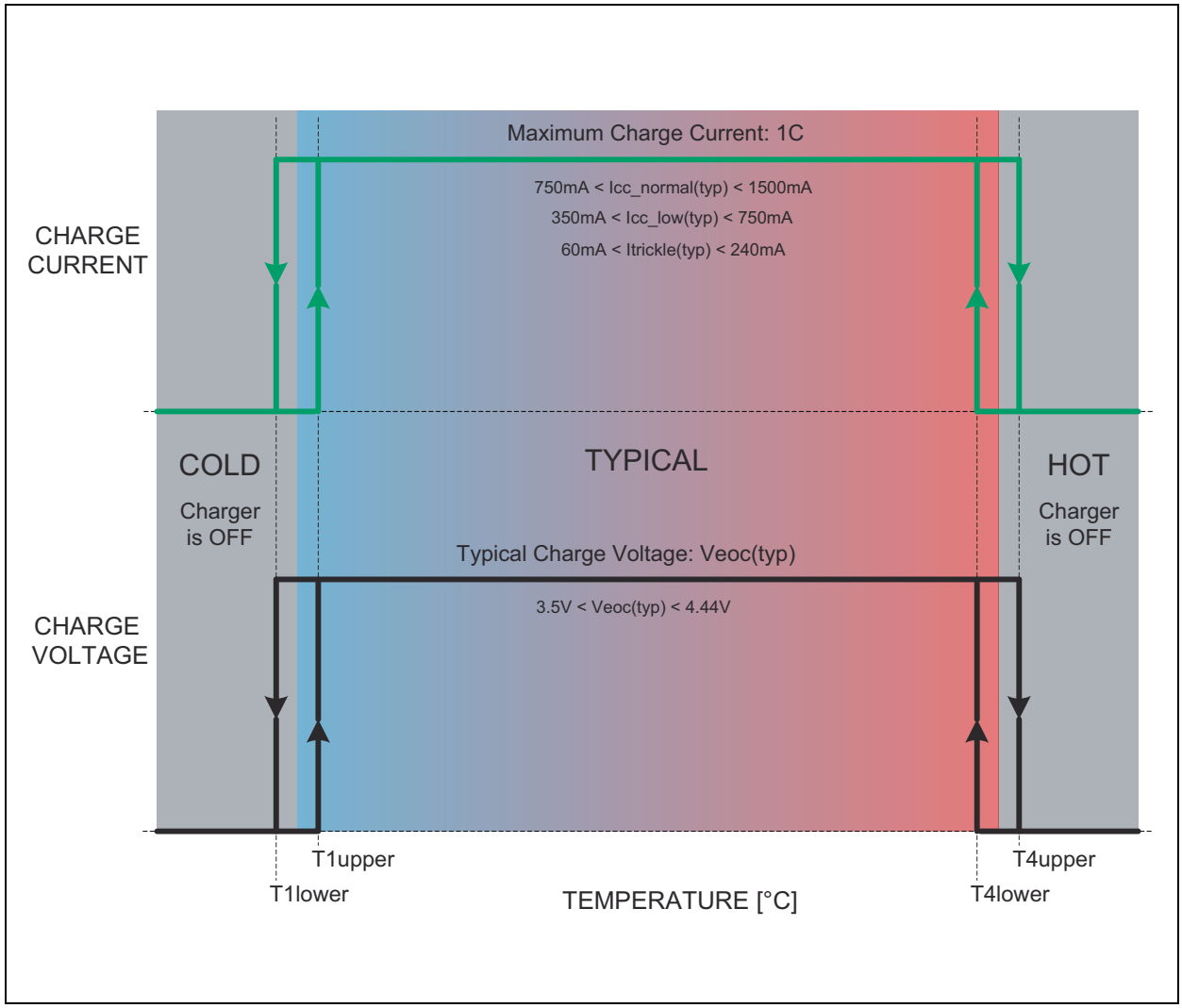
Also the hysteresis of the ON and OFF levels can be programmed (4bits with 16 7mV steps).

(EQ4) Txlim_lower=Txlim_upper + (*Tx_hyst* + 3) * 7mV

Charger MIN/MAX Temp Supervision

The simpler supervision mode is supervising T1 (0°C) and T4 (60°C)

Figure 47:
MIN/MAX Temp Supervision

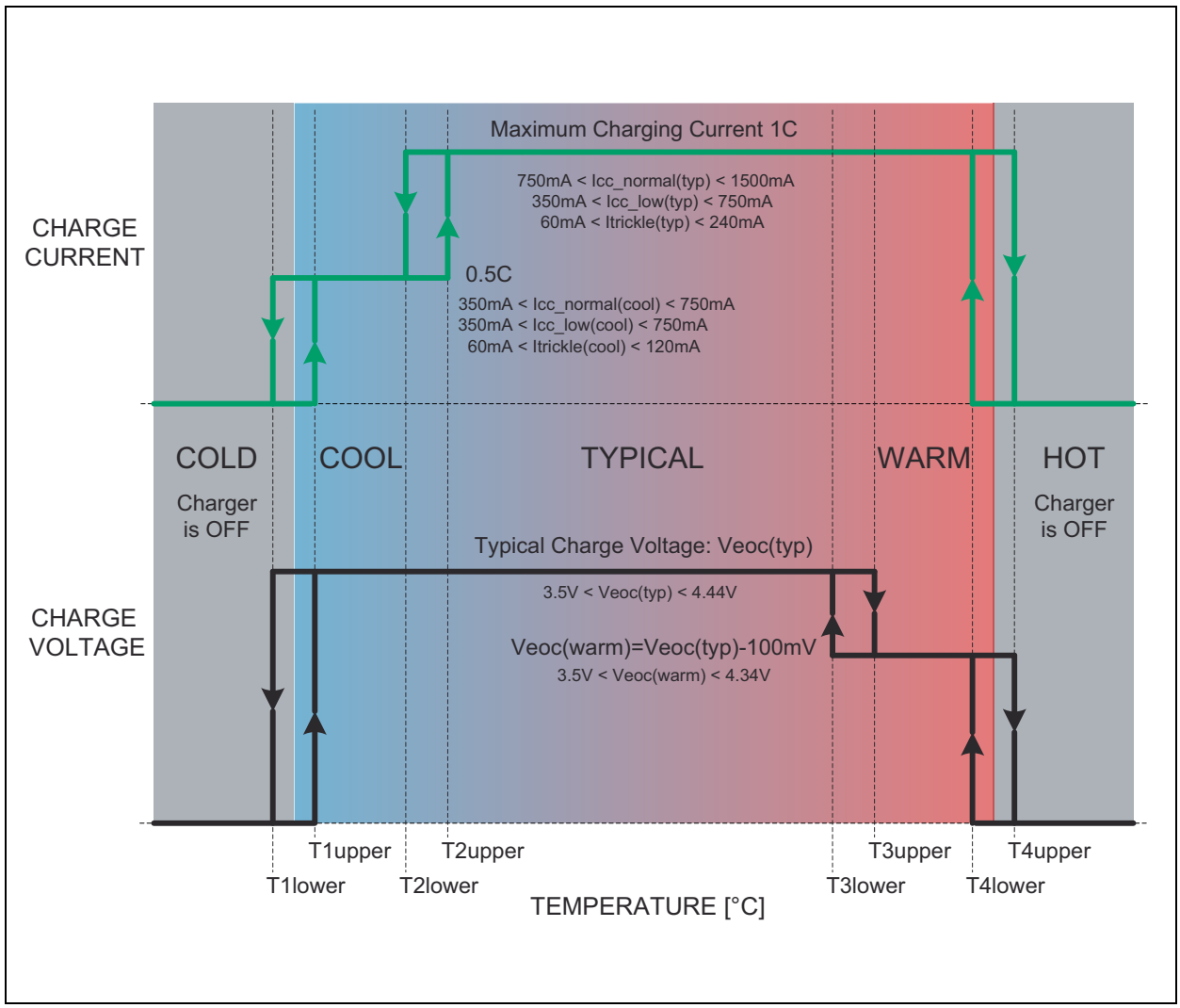


MIN/MAX Temp Supervision Diagram: Shows the voltage and current settings for the MIN/MAX temperature supervision.

Charger JEITA Temp Supervision

The more complex JEITA temperature supervision is monitoring T1 (0°C), T2 (10°C), T3 (45°C) and T4 (60°C) and adjusting charging current and voltage to it.

Figure 48:
JEITA Temp Supervision

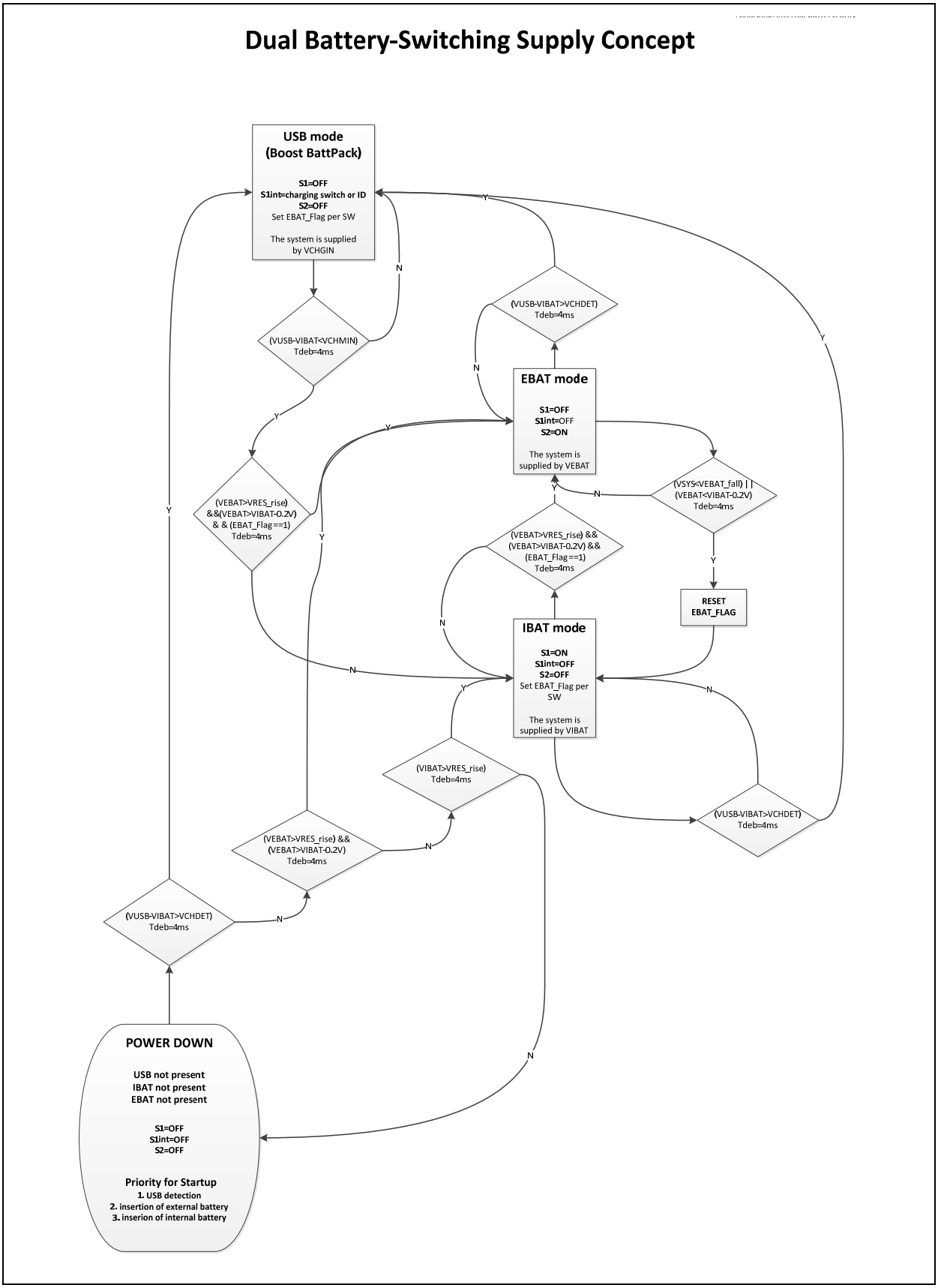


JEITA Temp Supervision Diagram: Shows the voltage and current settings for the JEITA temperature supervision.

Dual Battery Switching

The charger is only charging the battery connected to CHGOUT/VIBAT, but can handle to batteries and controls the external battery switches accordingly.

Figure 49:
Dual Battery Switching(Flowchart)

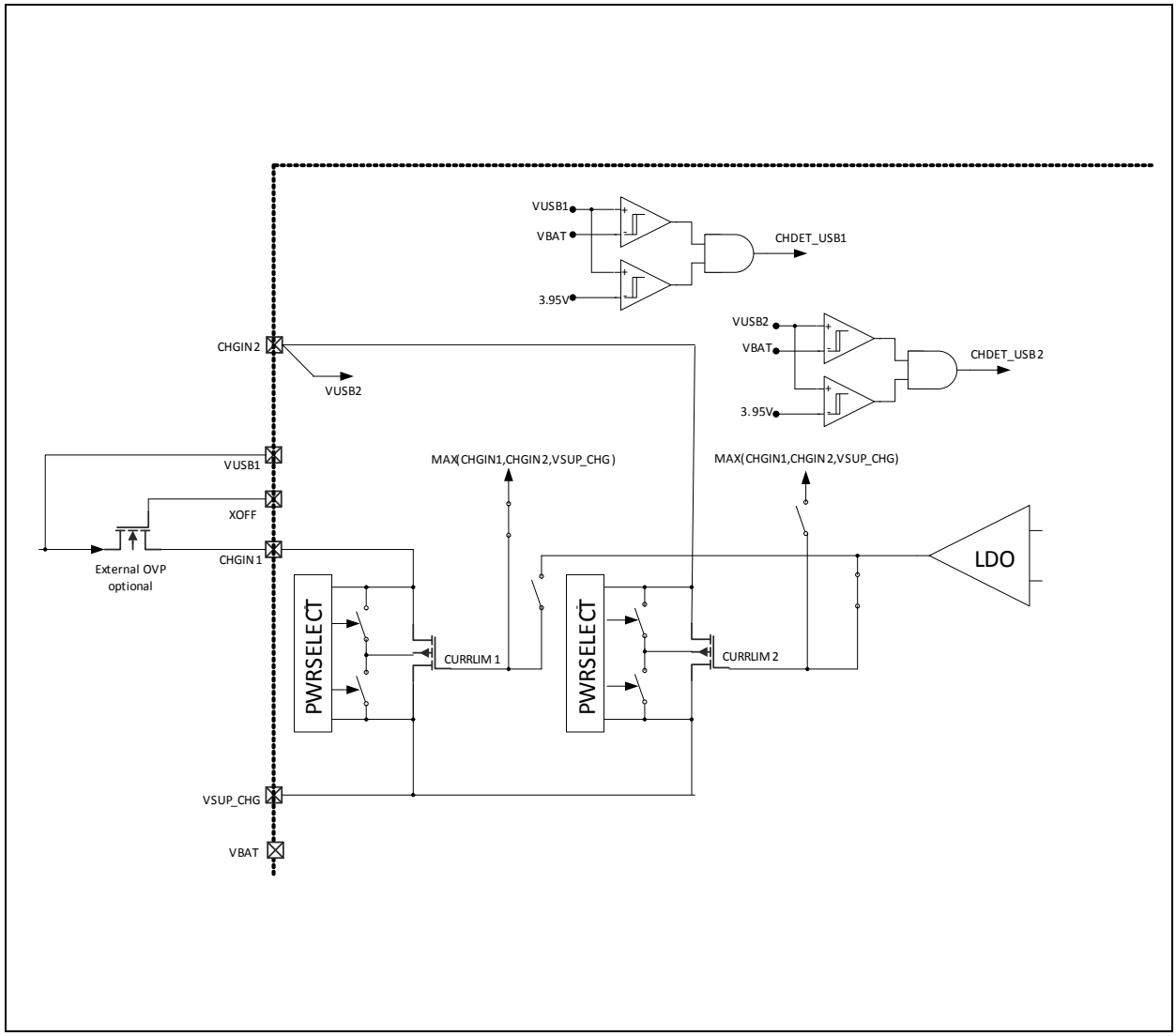


Dual Battery Switching Diagram: Shows the state diagram for controlling two batteries to the PMIC.

Dual Power Path

Two charger inputs can be used to hook up two different charger supplies. CHGIN1 as an optional protection function with an external NMOS using VUSB1 as sensing input.

Figure 50:
Dual Power Path Diagram



Dual Power Path Diagram: Shows the internal structure of the dual power path input.

Figure 51:
USB Input Selection

	VUSB2 > VBAT+VCHMIN and VUSB2 > 3.95V	VUSB2 < VBAT+VCHMIN or VUSB2 < 3.95V
en_usb2=0		
VUSB1 > VBAT+VCHMIN and VUSB1 > 3.95V	Device is powered from VUSB1	
VUSB1 < VBAT+VCHMIN or VUSB1 < 3.95V	No charge	No charge
en_usb2=1		
VUSB1 > VBAT+VCHMIN and VUSB1 > 3.95V	Device is powered from VUSB1	
VUSB1 < VBAT+VCHMIN or VUSB1 < 3.95V	Device is powered from VUSB2	No charge

Dual Power Path Diagram: Shows the priority of the charger input depending on *en_usb2* setting and the charger input voltages

Parameter

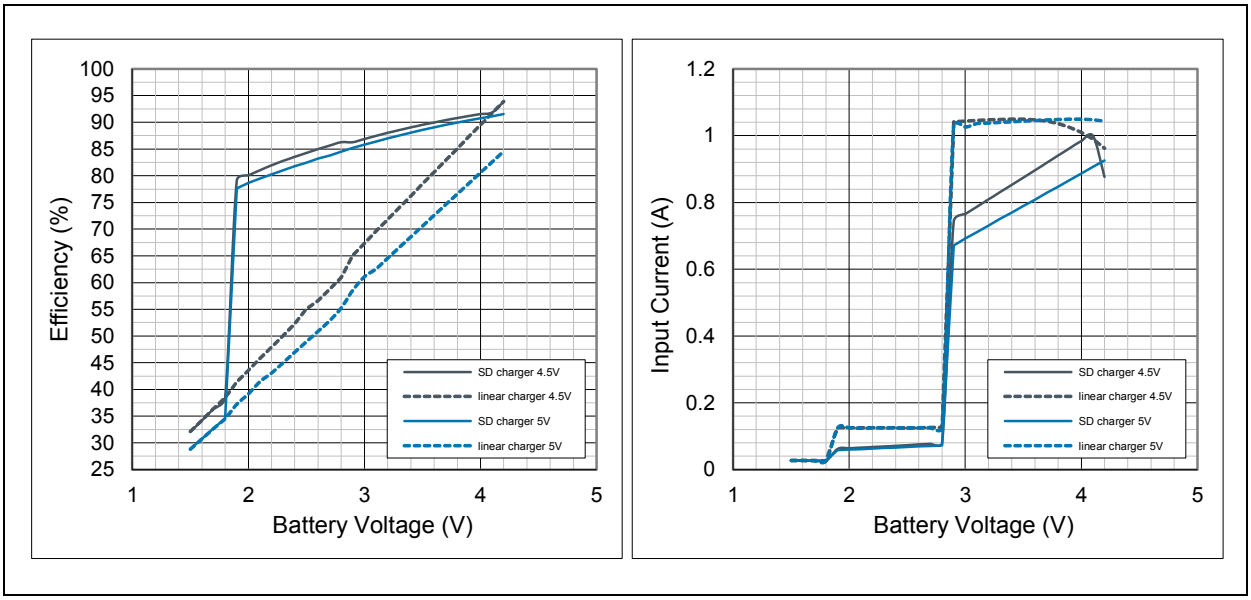
Figure 52:
Charger Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CHDET}	Charger Detection threshold	VUSB-VBAT Hysteresis is > 40mV	50	75	105	mV
V_{CHMIN}			0	20	35	mV
V_{SOFT}	Apply I_{SOFT} charging current below that VBAT voltage			1.8		V
I_{SOFT}	Charging current if VBAT is below V_{SOFT}			22		mA
$V_{TRICKLE}$	Trickle to CC current threshold	V_{BAT} rising		2.9		V
$I_{TRICKLE}$	Trickle/EOC current limit	Programmable in 60mA steps		60.. 240		mA
V_{CHOFF}	Charge termination threshold	Programmable in 20mV steps between 3.5 and 4.44V		3.5.. 4.44		V
		@ *ChVoltEOC*=35 (4.2V)	4.15	4.20	4.242	V
		@ *ChVoltEOC*= 47 (4.34V)	4.29	4.34	4.38	V

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{CC}	CC current limit	Programmable in 50mA steps		350.. 1500		mA
		Linear charging mode	-10		+10	%
I_{USB_limit}	USB input current limit	@ 470mA	-7%	470	+6%	mA
V_{RESUME}	Resume voltage limit to start charger	VBAT falling threshold relative to *ChVoltEOC* (depending on *ChVoltResume*)		-3.3 or -5.6		%
VSUP_min	VSUP level for charging current regulation (reduction), to avoid voltage drop on VSUP	Trickle current (or constant current in linear mode) will be regulated down, if VSUP drops below this level	-6%	3.9	3%	V
				4.2		
				4.5		
				4.7		
I_{REV_OFF}	Reverse current shut down	VSUP_CHG = 5V, VUSB open		5		µA
V_{Diode}	Ideal Diode start voltage			50		mV
R_{ON_BATSW}	Battery Switch ON-resistance			0.20		Ω
Temp Supervision						
$I_{BATTEMP}$	NTC Bias Current	100kΩ NTC 10kΩ NTC	-15%	15 150	+15 %	µA
XOFF Overvoltage Protection						
V_{CHOVH}	VUSB Overvoltage Detection	monitor voltage on VUSB, disable charging beyond this voltage (200mV hysteresis)		6.2	+3%	V
			-3%	6.0		
V_{XOFF_min}	Minimum XOFF voltage for charger startup			7.5		V
V_{XOFF_REG}	Regulation voltage for XOFF pin			10		V
I_{XOFF}	External pull down current on XOFF pin	Connect XOFF pin to MOSFET gates only			100	nA

Charger Parameter: Shows the key electrical parameter of the charger and power paths.

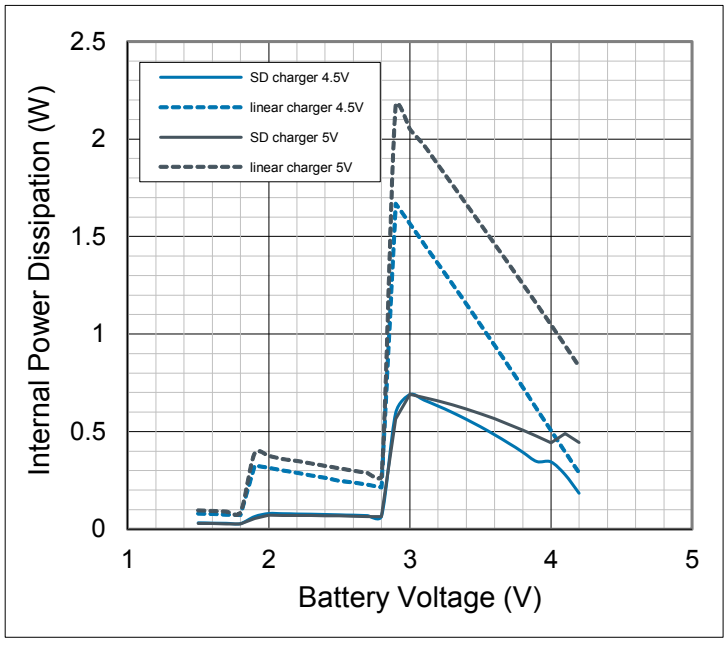
Figure 53:
Charger Efficiency and Input Current



Charger Efficiency and Input Current: Shows the efficiency of the charger in step-down and linear mode as well as the current from the charger input in both modes for 1A charging current.

Figure 54:
Charger Power Dissipation

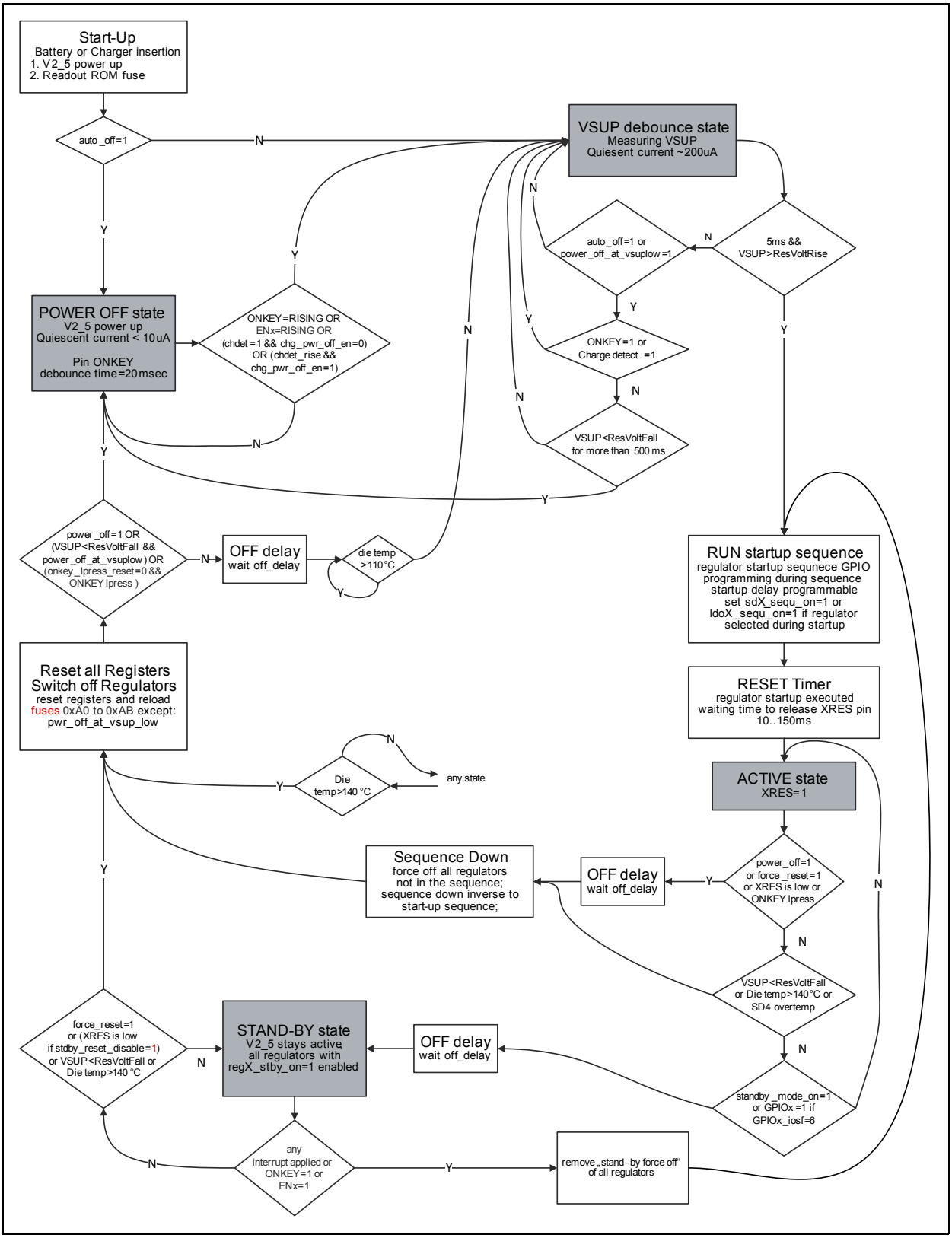
Charger Power Dissipation: Shows the power dissipation of the charger in step-down and linear mode for 1A charging current.



Detailed Description – System Functions

Start-up

Figure 55:
Start-up flow chart



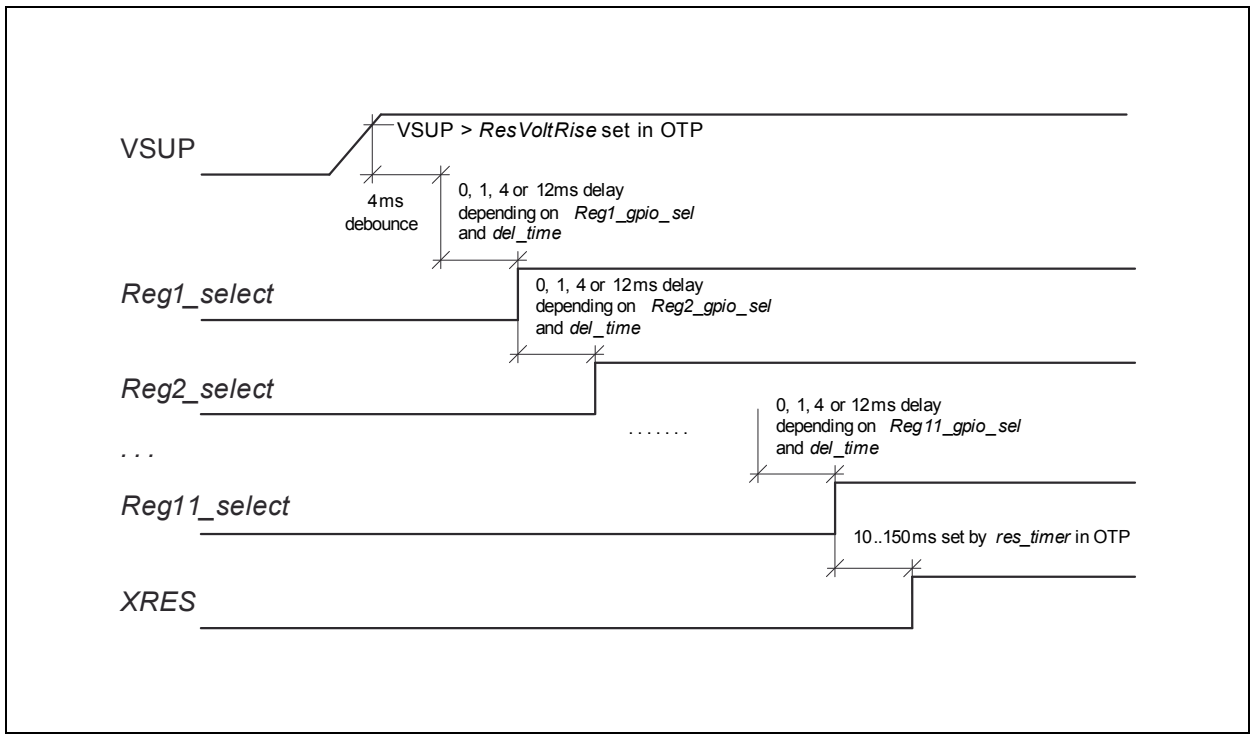
Start-up flow chart: Shows the main state transitions during start-up.

Normal Startup

The following gives a brief description on a start-up from scratch (battery insertion). More details can be found in the start-up flow charts.

- Powering up V2_5 (wait till it's above V_{POR})
- The external capacitor on CREF is charged to 1.8V.
- Check if VSUP is above ResVoltRise
- Configuration of Charger (DCDC or linear) and SDx slave modes is read from Boot-OTP
- Startup State machine reads out the internal Boot-OTP. The start-up sequence of Step-Down Converter, LDO's and GPIOs are controlled by the Boot-OTP.
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES)

Figure 56:
Regulator Power-up Sequence



Regulator Power-up Sequence: Shows timing relationships of the regulators and corresponding control signals during power-up.

Start-up Reasons

A Start-up can be activated from 4 different sources:

- VPOR has been reached (VUSB/VSUP/VBAT rising from scratch)
- ONKEY or ENx has been pulled high in power_off mode
- Reset cycle
- ResVoltRise was reached

Parameter

Figure 57:
ONKEY/ENx-input Start-up Conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$VUSB_{ON}$	Voltage in VUSB for system to start		4.2	5.0	30	V
V_{ON_IL}	ONKEY/ENx Low Level input voltage		–0.3		0.4	V
V_{ON_IH}	ONKEY/ENx High Level input		1.4		V_{VSUP_GPIO}	V
I_{ON_PD}	ONKEY/ENx Pull down current		5	12	20	µA

ONKEY-input Start-up Conditions: Shows the electrical parameter for the ONKEY input initiating the start-up.

Reset

Description

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added.

During each reset cycle the following states are controlled by the AS3715:

- Power-down sequence of the regulators
- Pin XRES is forced to GND
- All registers are set to their default values after power-ON, except the reset control- and status-registers.
- Normal startup with programmable power-ON sequence and regulator voltages (see Start-up)
- Reset is active until the programmable reset timer expires (set by register bits *res_timer<2:0>*)

Reset Reasons

Reset can be activated from 8 different sources:

- VPOR has been reached (VSUP/VBAT rising from scratch)
- VSUP low, ResVoltFall (2.5V) has been reached
- Software forced reset by force_reset
- ONKEY or ENx long press has been detected
- External triggered through the pin XRES
- Over-temperature T140 (die)
- Over-temperature T140 SD4 (sub die)
- Watchdog

Voltage Detection:

There are two types of voltage dependent resets: V_{POR} and $V_{RESRISE}$. V_{POR} monitors the voltage on V2_5 and $V_{RESRISE}$ monitors the voltage on VSUP. The linear regulator for V2_5 is always ON and uses the voltage VUSB/VBAT/VSUP as its source.

The pin XRES is only released if V2_5 is above V_{POR}, VSUP is above *ResVoltRise*.

$V_{RESFALL}$ is only accepted if the reset condition is longer than $V_{RESMASK}$. This guard time is used to avoid a complete reset of the system in case of short drops of VBAT.

Figure 58:
VSUP Supervision

SupResEn	power_off_at_vsuplow	auto_off	Behavior if VSUP<ResVoltFall
0	x	x	LowBat interrupt is generated
1	0	0	Reset cycle is initiated, PMIC will move to “VSUP debonce” state and start-up if VSUP>ResVoltRise
1	0	1	Reset cycle is initiated, PMIC will move to “VSUP debonce” state and try to start-up if VSUP>ResVoltRise, if not it will go to the “Power OFF” state
1	1	x	Reset cycle is initiated, PMIC will move to “Power OFF” state

VSUP Supervision: Describes the behavior of the PMIC when VSUP drops below ResVoltFall depending on OTP bit settings.

Power OFF:

To put the chip into ultralow power mode, write '1' into *power_off*. The chip stays in power OFF mode until it gets a wakeup signal from either the ON pin or from a charger insert. For more details see the start-up flowchart (Figure 55). The bit *power_off* is automatically cleared by this reset cycle. During power_off state all circuits are shut-off except the Low Power LDO (V2_5). Thus the current consumption of AS3715 is reduced to about 13µA (if only supplied via VIBAT). The digital part is supplied by V2_5, all other circuits are turned OFF in this mode, including references and oscillator. Except the reset control registers all other registers are set to their default value after power-ON.

Below table show the behavior of the PMIC in terms of USB pre-regulator and battery switch operation supplying VSUP when putting the PMIC into power_off state by setting *power_off*=1

Figure 59:
Pre-Regulator and Battery Switch Operation

#	Battery	USB present	chg_pwr_off_en	States of VSUP_CHG
1	don't care	YES	=1	PMIC enter power_off mode. Pre-regulator powered down, VSUP_CHG not powered
2	don't care	YES	=0	PMIC enter power_off mode and power ON again. VSUP_CHG powered by the pre-regulator
3a	IBAT attached	NO	don't care	PMIC enter power_off mode. VSUP_CHG connected to VIBAT via the internal battery switch
3b	EBAT attached	NO	don't care	PMIC enter power_off mode. VSUP_CHG not powered

Pre-Regulator and Battery Switch Operation: Shows the VSUP behavior under different supply conditions and settings when setting *power_off*=1.

Software Forced Reset

Writing '1' into the register bit *force_reset* immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External Triggered Reset:

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Over-temperature Reset:

The reset cycle can be started by over-temperature conditions. (see Supervisor)

Watchdog Reset:

If the watchdog is armed (register bit *wtdg_on* = 1 and *wtdg_res_on*= 1) and the timer expires it causes a reset. (see Watchdog).

Long ONKEY/ENx Press:

When applying a high level on the ONKEY or ENx input pins for 4s/8s (depending on *on_reset_delay*) a reset or power_off (depending on onkey_lpress_reset) is initiated. This is thought as a safety feature when the SW hangs up and no watchdog is used.

Figure 60:
ONKEY/ENx Longpress Behavior

onkey_lpress_reset	on_reset_delay	longpress behavior
0	0	power_off after 8s long press delay
0	1	power_off after 4s long press delay
1	0	reset_cycle after 8s long press delay
1	1	long press feature disabled

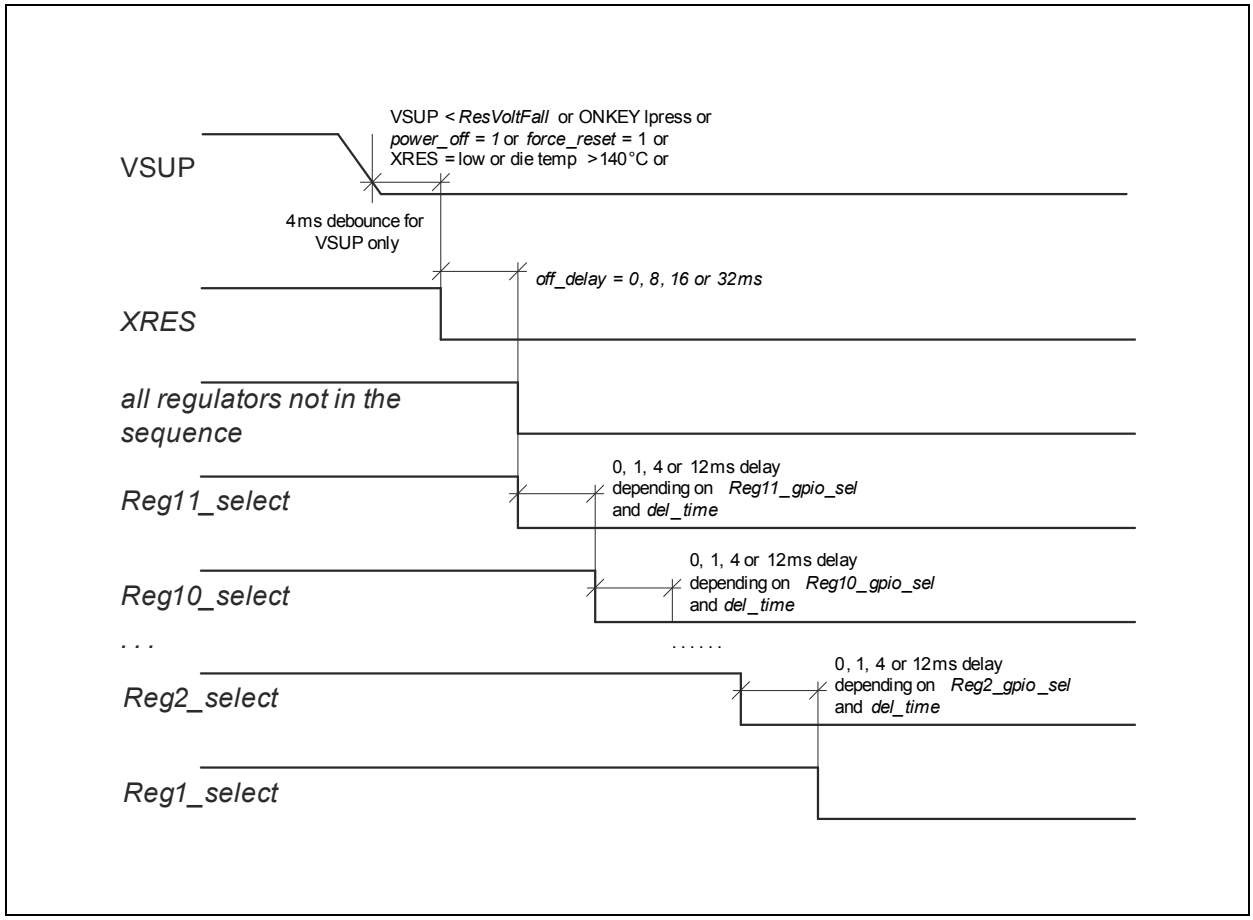
ONKEY/ENx Longpress Behavior: Shows the slectalbe options for behaving on a long press.

Reset and Power-OFF Sequence

The regulator power-down sequence is inverted to the power-up sequence programmed in the OTP. It can be slightly modified by setting or clearing the *sdX_sequ_on* and *ldoX_sequ_on* bits. The bit is set automatically for all the regulators defined in the OTP start-up sequence.

- Regulators which have the corresponding sequ_on bit cleared will be shut down before the power-down sequence starts.
- Regulators which have the bit set and are in the power-up sequence of the OTP will shut down in an inverted order.
- Regulators which have the bit set and are not part of the power-up sequence will shut down after the sequence has been completed.

Figure 61:
Regulator Power-down Sequence



Regulator Power-down Sequence: Shows timing relationships of the regulators and corresponding control signals during power-down.

Parameter

Figure 62:
Reset Levels

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{POR}	Overall power ON reset	Monitor voltage on V2_5; power ON reset for all internal functions	1.5	2.0	2.3	V
$V_{RESRISE}$	Reset level for VSUP rising	Monitor voltage on VSUP; rising level		ResVoltRise(1)		V
$V_{RESFALL}$	Reset level for VSUP falling	Monitor voltage on VSUP; falling level		2.7		V
		if SupResEn=1		ResVoltFall		V
$V_{RESMASK}$	Mask time for VRESFALL. Duration for VBAT<ResVoltFall or VSUP<vsup_min until a reset cycle is started (2)	FastResEn = 0		3		ms
		FastResEn = 1		4		us

Reset Levels: Shows the electrical parameter of the voltage supervisors controlling start-up and reset cycles.

Note(s) and/or Footnote(s):

1. It's recommended to set the ResVoltRise level 200mV above the ResVoltFall level to have a hysteresis.
2. XRES signal is de-bounced with the specified mask time for rising- and falling slope of V_{BAT}.

Figure 63:
XRES Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{XRES_IL}	XRES Low Level input voltage		-0.3		0.4	V
V_{XRES_IH}	XRES High Level input voltage		1.4		V_{VSUP_GPIO}	V

XRES Characteristics: Shows the electrical parameter for the XRES_IN and XRES_OUT.

Stand-by

Description

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or GPIO of the PMU. The interrupt has to be enabled and GPIO has to be configured before going to stand-by.

Figure 64:
Stand-by

State	Description
Enter via GPIO	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set the GPIO to input (*gpioX_mode* = 0) • Set the GPIO for stand-by control (*gpioX_iosf* = 6) • Set *regX_select and regX_voltage* if another voltage is needed during stand-by for up to 3 regulators • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Activate the selected GPIO (set to HIGH)
Enter via SW	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set *regX_select_stby* and *regX_voltage_stby* if another voltage is needing during stand-by for up to 7 regulators • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Set the delay for going into stand-by after the SW command *(off_delay*) • set *standby_mode* to 1
Stand-by	V2_5 chip supply is kept ON All other regulators are switched OFF dependent on the bits *sdX_stby_on* and *ldoX_stby_on* XRES_OUT goes active (can be disabled with *standby_reset_disable in the boot OTP*) and pwr_good goes inactive
Leave	The chip will come out of stand-by with • IRQ activation (use the GPIO restart interrupt (gpio_restart_int) to leave with the same GPIO you entered stand-by) • ONKEY/ENx = High Start-Up sequence is provided defined by the boot OTP

Stand-by: Shows different options to enter and leave the stand-by state.

Internal References

Description

The internal reference is power by the V2_5 always on LDO. It uses an external capacitor and resistor for filtering and current setting. In power_off mode the V2_5 stays alive but the reference will be disabled.

Low Power Mode

Use bit *low_power_on* to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3715 by 45uA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

For disabling the Low Power Mode *low_power_on* has to be cleared via the serial interface.

Parameter

Figure 65:
Reference Parameter

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{CEXT}	Reference Voltage	Low noise trimmed voltage reference – connected to Pad CREF; **do not load**	-1%	1.8	+1%	V
f_{CLK}	Accuracy of Internal reference clock	Adjustable by serial interface register clk_int	-12	f_{CLK}	+12	%

Reference Parameter: Shows the key electrical parameter of the on-chip reference.

Figure 66:
Reference External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{EXT}	External filter capacitor	Ceramic low-ESR capacitor between CREF and VSS	-10%	100	+10%	nF

Reference External Components: Shows the external component parameter of the on-chip reference.

GPIO Pins

Description

The device contains 8 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), ADC input (tri-state only for GPIO3,4,7 & 8), push-pull output (selectable lower or higher GPIO supply), or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

The polarity of the input and output signals can be inverted with the corresponding *gpioX_invert* bit, all further descriptions refer to normal (non-inverted) mode.

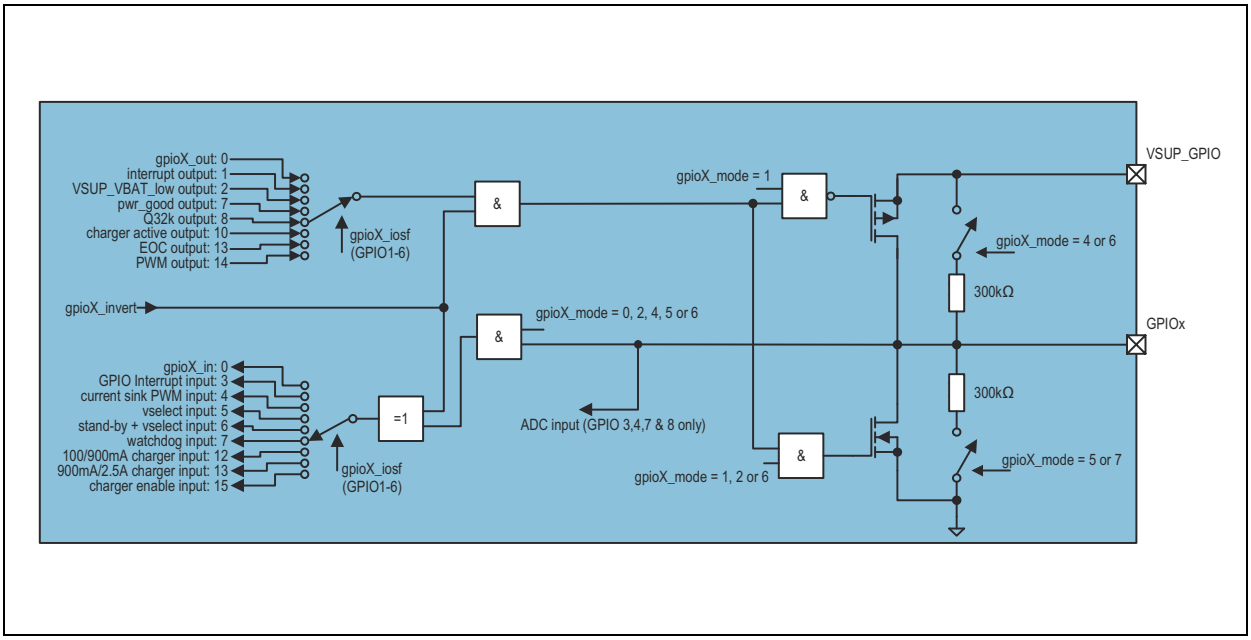
GPIO7 & 8 have no special IO functionality, they just provide gpioX_in/out function.

Figure 67:
GPIO Functions

Function	GPIO	1	2	3	4	5	6	7	8
Accessible via OTP during start-up		x	x	x	x				
Accessible during stand-by entry/leave		x	x	x	x				
Regulator ON/OFF control configurable in OTP				x					
Regulator ON/OFF control configurable after start-up		x	x	x					
IO special functions available		x	x	x	x	x	x		
ADC input function				x	x			x	x

GPIO Functions: Gives an overview which functions are available on which GPIOs.

Figure 68:
GPIO Block Diagram



GPIO Block Diagram: Shows the internal structure of the IO pads.

IO Functions

Normal IO operation:

If set to input, the logic level of the signal present at the GPIOx pin can be read from *gpioX_in*. If the output mode is chosen, *gpioX_out* specifies the logic level of the GPIOx pin.

This mode is also used for the ON/OFF control of the DCDC and LDOs. The selection which regulator is controlled by which GPIO, is done with the *gpio_ctrl_sdX or gpio_ctrl_ldoX* bits. The *gpioX_mode* should be set to input.

Interrupt Output

GPIOy pin logic state is derived from the interrupt signal INT. Whenever an interrupt is present, the GPIOx pin is pulled high. The *gpioX_mode* should be set to output.

VSUP_low Output

GPIOx pin will go high if VSUP falls below *ResVoltFall* and *SupResEn* = 0. The gpioX_mode should be set to output.

GPIO Interrupt Input

A falling or rising edge will set the *gpio_int* bit. The *gpioX_mode* should be set to input.

Current Sink PWM Input

The GPIO is used as PMW input for the current sink to control the current. 100% PWM mode will set the current to the value set by *currX_current*. The PWM control has to be enabled by currX_ctrl =11b for each current sink to be controlled. The *gpioX_mode* should be set to input.

Vselect Input

As long as the GPIOx pin is low the DCDC/LDOs operate with the normal register settings. If the GPIOx pin goes high the settings will change to the ones stored in *regX_voltage*.

The *gpioX_mode* should be set to input.

The regulator affected by this mode is selected by regX_select. While GPIO3 to GPIO6 always control all regulators selected by regX_select, GPIO1 and GPIO2 may be used to control two regulators separately:

Figure 69:
GPIO Vselect Modes

gpio1_iosf	gpio2_iosf	Vselect mode
≠ 5	≠ 5	No voltage select by GPIO for regulator
≠ 5	5	GPIO2 controls regulator selected by *reg1_select, reg2_select* and *reg3_select*
5	≠ 5	GPIO1 controls regulator selected by *reg1_select, reg2_select* and *reg3_select*
5	5	GPIO1 controls regulator selected by *reg1_select* GPIO2 controls regulator selected by *reg2_select & reg3_select*

Vselect Mode: Shows the different GPIO voltage control modes for regulators.

Stand-by and Vselect Input

This mode is very similar to the Vselect mode described in the previous paragraph. In addition to switch between 2 register settings of 3 regulators, the chip is set to stand-by mode when the GPIOx pin goes high and wakes up again when the pin is pulled low.

The *gpioX_mode* should be set to input.

While GPIO3 to GPIO6 always control all regulators selected by regX_select, GPIO1 and GPIO2 may be used to control two regulators separately:

Figure 70:
GPIO Stand-by and Vselect Modes

gpio1_iosf	gpio2_iosf	Vselect mode	Stand-by control
≠ 6	≠ 6	No voltage select by GPIO for regulator	No
≠ 6	6	GPIO2 controls regulator selected by *reg1_select, reg2_select* and *reg3_select*	Yes
6	≠ 6	GPIO1 controls regulator selected by *reg1_select, reg2_select* and *reg3_select*	Yes
6	6	GPIO1 controls regulator selected by *reg1_select* GPIO2 controls regulator selected by *reg2_select & reg3_select*	Yes

Stand-by and Vselect Mode: Shows the different GPIO voltage and stand-by control modes for regulators.

PWRGOOD Output

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators. The *gpioX_mode* should be set to output.

Q32k Output

When selected the GPIOx will provide the internal 32kHz oscillator frequency. The *gpioX_mode* should be set to output.

Watchdog Input

When pulling the GPIO high the watchdog will be triggered to avoid a reset cycle initiated by the watchdog. The *gpioX_mode* should be set to input.

SU1 OC Output

This output signal can be used to control an external disconnect transistor if SU1 detects an over current condition. The *gpioX_mode* should be set to output.

Charger Active Output

When selected, the GPIOx will go high if the charger is active. The *gpioX_mode* should be set to output.

EOC Output

When selected, the GPIOx will go high if the charger has reached the EOC state. The *gpioX_mode* should be set to output.

100/900mA Charger Input

With this function the charger input current limiter can be set to 100 or 900mA (low power or high power USB limit). The *gpioX_mode* should be set to input.

900mA/2.5A Charger Input

With this function the charger input current limiter can be set to 900mA or 2.5A (high power USB limit or full current enabled). The *gpioX_mode* should be set to input.

Charging Enable Input

When pulling the GPIO to high the charger is being enabled and vice versa. This is to enable the charger without I^2C communication. The *gpioX_mode* should be set to input.

PWM Output

The GPIO block includes an internal programmable PWM generator (can be connected to any of the GPIO outputs). Its timing is defined by *pwm_h_time*, *pwm_l_time* and *pwm_div*. The *gpioX_mode* should be set to output.

Parameter

Figure 71:
GPIO Pin Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{OL}	Low level output voltage	I_{OL}=+1mA; digital output	–0.3		+0.4	V
V_{OH}	High level output voltage	I_{OH}=–1mA; digital push-pull output	0.8 VSUP_GPIO		VSUP_GPIO	V
V_{IL}	Low level input voltage	Digital input	–0.3		0.4	V
V_{IH}	High level input voltage	Digital input	1.4		VSUP_GPIO	V
$I_{LEAKAGE}$	Leakage current	High impedance			10	µA
$R_{pull-up}$	Pull-up resistance	If enabled; VSUP_GPIO=3.6V		300		kΩ
$R_{pull-down}$	Pull-down resistance	If enabled; VSUP_GPIO=3.6V		300		kΩ

GPIO Pin Characteristics: Shows the key electrical parameter of the GPIO pins. VSUP=2.7 to 5.5V; Tamb = -20 to +70°C; unless otherwise mentioned.

Supervisor

All LDO's, the DCDC step ups and DCDC step downs have an integrated over-current protection.

An over-temperature protection of the chip is also integrated which can be switched ON with the serial interface signal *temp_pmc_on* (enabled by default; it is not recommended to disable the over-temperature protection).

Temperature Supervision (main die)

The chip has two signals for the serial interface: *ov_temp_110* and *ov_temp_140*. The flag *ov_temp_110* is automatically reset if the over-temperature condition is removed, whereas *ov_temp_140* has to be reset by the serial interface with the signal *rst_ov_temp_140*.

If the flag *ov_temp_140* is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T_{110} level (including hysteresis).

The flag *ov_temp_140* is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown:

Figure 72:
Temperature Supervision Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
T_{110}	ov_temp_110 rising threshold		95	110	125	°C
T_{140}	ov_temp_140 rising threshold		125	140	155	°C
T_{hyst}	ov_temp_110 and ov_temp_140 hysteresis			5		°C

Temperature Supervision Characteristic: Shows the key electrical parameter of the over-temperature supervision.

Temperature Supervision SD4 (sub die)

A similar supervision is installed for the power stage controlled by SD4. *temp_sd4_alarm* and *temp_sd4_shutdown* are indicating a >110°C or >140°C temperature condition of the sub die. For both events an interrupt can be triggered. With *mask_ovtemp*=0 reaching 140°C is initiating a reset cycle. If *mask_ovtemp*=1 only an interrupt is generated (if enabled)

Watchdog

Description

The purpose of the watchdog is to detect a deadlock of the software. If the watchdog is active, it must receive a continuous trigger signal within a programmable time window. If there is no signal anymore for a certain time period from a defined pad or special serial interface bit, it starts either a complete reset cycle or initiates the power OFF sequence.

The watchdog is highly configurable by the following register bits:

- The complete block can be switched ON by *wtdg_on = 1* and OFF by *wtdg_on* = 0.
- The watchdog time window is defined by the register *wtdg_timer* between 1s and 128s.
- The trigger signal can be either triggered by setting *wtdg_sw_sig* or using a HW signal on one of the GPIO pins *(gpioX_iosf*=9).
- If the watchdog expires, the system can start automatically a reset cycle if *wtdg_reset_on* = 1 and *wtdg_pweroff* = 0, or perform a power down if *wtdg_reset_on* = 1 and *wtdg_pweroff* = 1.
- If *wtdg_reset_on* = 0 and *wtdg_pweroff* = 0 only an interrupt is generated (if the interrupt is enabled)
- Whether the watchdog caused a reset can be seen in the *reset_reason*.

Interrupt Generation

Description

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt* 1…3 register are set by pulling high pin INT (INT has to be selected as GPIO output function). The output polarity can be changed to active low (XINT) by using the *gpioX_invert* bit of the selected GPIO. All the interrupt sources can be enabled in the Interrupt Mask 1…3 register. The Interrupt 1…3 registers are cleared automatically after the host controller has read them. To prevent the AS3715 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

10-Bit ADC

Description

This general purpose ADC can be used for measuring several voltages and currents to perform functions like battery monitor, temperature supervision, button press detection, etc.

Figure 73:
ADC Input Sources

#	Source	Range	LSB	Mode	Description
0	BATTEMP	1.8V	1.76mV	1:1	Check battery charging temperature
1	DIE temperature	1.8V	1.76mV	1:1	Tj = (0.866 * ADC10<9:0>) - 274
2	CHGIN2	5.5V	7.03mV	4:1	
3	CURR1	1.0V	1.76mV	1:1	
4	CURR2	1.0V	1.76mV	1:1	
5	CURR3	1.0V	1.76mV	1:1	
6	VUSB1	15V	26.4mV	15:1	Check USB charger HV input
7	CHGIN1	5.5V	7.03mV	4:1	Check USB charger LV input
8	VIBAT	5.5V	7.03mV	4:1	Check Li-Ion battery voltage
9	VSUP	5.5V	7.03mV	4:1	Check main system supply voltage
A	VEBAT	5.5V	7.03mV	4:1	Check 2nd Li-Ion battery voltage
B	GPIO3	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
C	GPIO4	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
D	GPIO7	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
E	GPIO8	1.8V / 5.5V	1.76 / 7.03mV	1:1 / 4:1	
F					Reserved

ADC Input Sources: Shows the various inputs with the corresponding resolution which can be measured by the internal ADC.

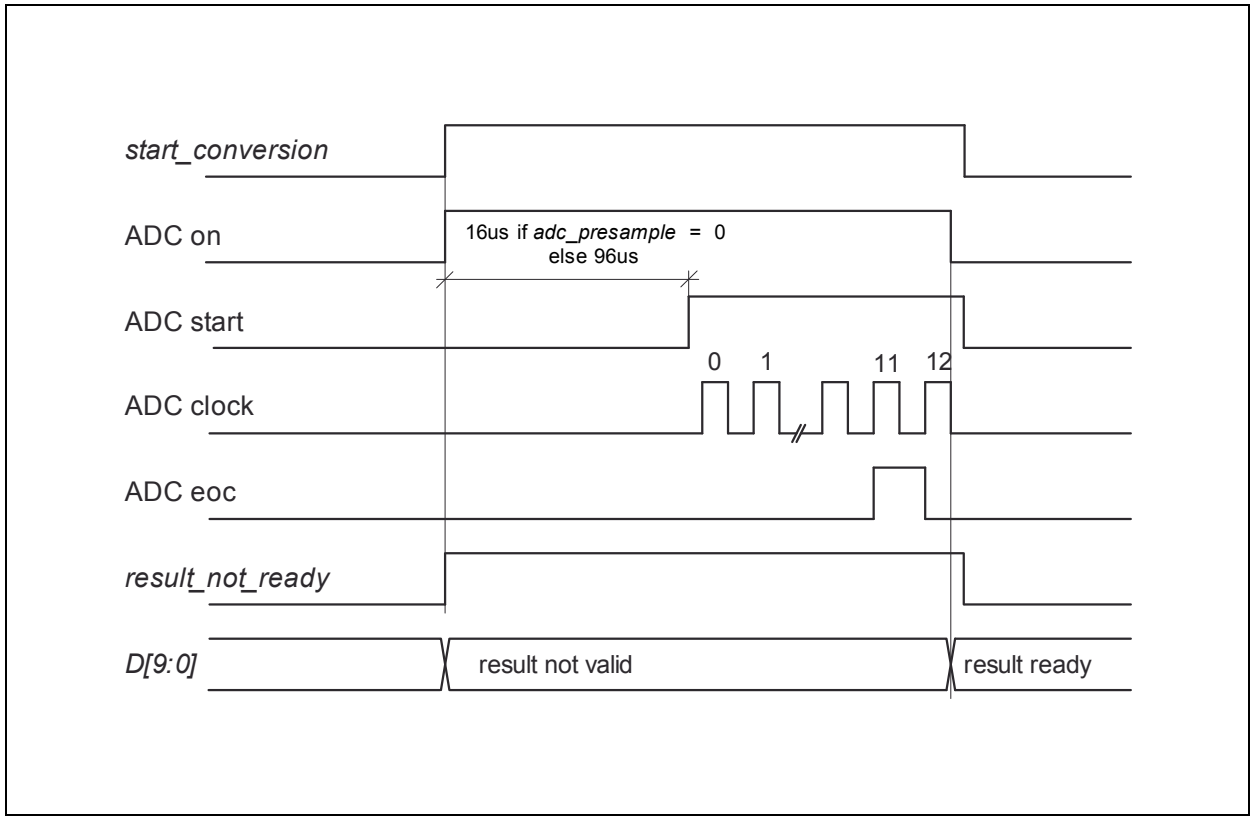
Parameter

Figure 74:
ADC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	Resolution		10			Bit
Vin	Input Voltage Range	For 1:1 mode	0		1.8	V
DNL	Differential Nonlinearity	1LSB 1.56mV for 1:1 (depending on selected channel)		± 0.25		LSB
INL	Integral Nonlinearity			± 0.5		LSB
Vos	Input Offset Voltage			2		LSB
Rin	Input Impedance	1:1	100			MΩ
		4:1		200		kΩ
Cin	Input Capacitance				9	pF
Idd	Power Supply Current	During conversion only		500		µA
Idd	Power Down Current			100		nA
Transient Parameters (25°C)						
Tc	Conversion Time			40		µs
fc	Clock Frequency	Internal CLK frequency/8		f_{clk_int} /8		kHz
ts	Settling time of S&H		1			µs

ADC Characteristic: Shows the key electrical parameter of the internal ADC.

Figure 75:
ADC Timing Diagram



ADC Timing Diagram: Shows timing of the control and data signals of the internal ADC.

Serial Control Interfaces

I²C Feature List

- Fast mode capability (max. SCL-frequency is 400kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I²C Protocol

Figure 76:
I²C Symbol Definition

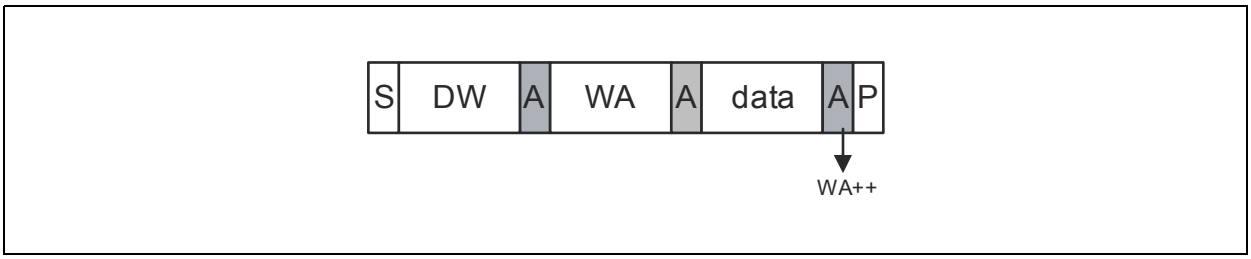
Symbol	Definition	RW	Note
S	Start condition after stop	R	1 bit
Sr	Repeated start	R	1 bit
DW	Device address for write	R	1000 0000b (80h)
DR	Device address for read	R	1000 0001b (81h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge

I²C Symbol Definition: Shows the symbols used in the following mode descriptions.

I²C Write Access

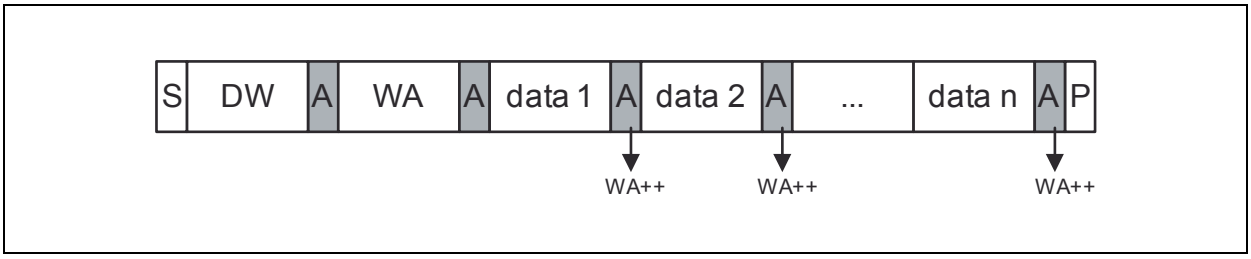
Byte Write and Page Write formats are used to write data to the slave.

Figure 77:
I²C Byte Write



I²C Byte Write: Shows the format of an I²C byte write access.

Figure 78:
I²C Page Write



I²C Page Write: Shows the format of an I²C page write access.

The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I²C Read access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 79:
I²C Random Read

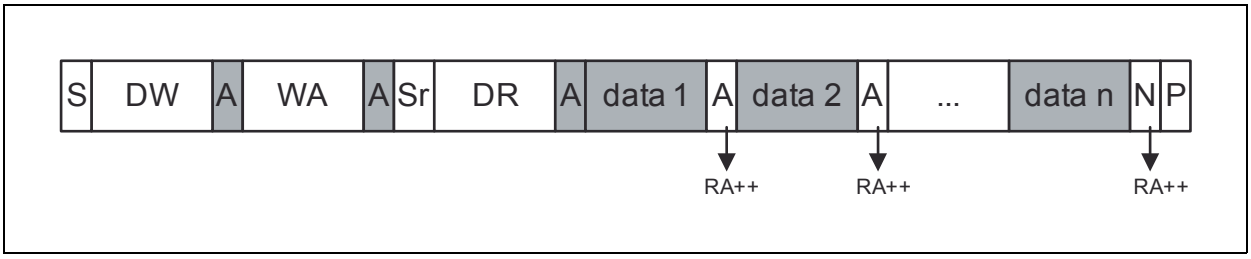
I²C Random Read: Shows the format of an I²C random read access.

Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

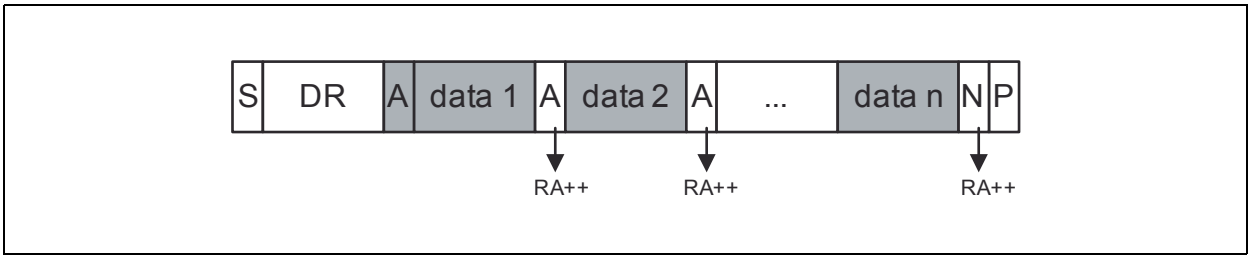
Figure 80:
I²C Sequential Read



I²C Sequential Read: Shows the format of an I²C sequential read access.

Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 81:
I²C Current Address Read



I²C Current Address Read: Shows the format of an I²C current address read access.

To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

I²C Parameter

Figure 82:
I²C Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IL}	SCL,SDA Low Level input voltage		-0.3		0.4	V
V_{IH}	SCL,SDA High Level input voltage		1.4		VSUP_GPIO	V
V_{OH}	High-Level Output Voltage	at -2.0mA	0.8x VSUP_GPIO_lv			V
V_{OL}	Low-Level Output Voltage	at 2.0mA			0.2x VSUP_GPIO_lv	V
C_{LOAD}	Capacitive Load				50	pF

I²C Characteristic: Shows the key electrical parameter of the I²C interface.

The AS3715 is compatible to the NXP two wire specification http://www.nxp.com/documents/user_manual/UM10204.pdf Version 4.0 Feb 2012 for standard mode and fast mode (no fast mode plus or high speed mode support).

Register Description

Register Overview

Figure 83:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
00h	SD1Voltage	sd1_frequ	sd1_vsel<6:0>				
01h	SD2Voltage	sd2_frequ	sd2_vsel<6:0>				
02h	SD3Voltage	sd3_frequ	sd3_vsel<6:0>				
03h	SD4Voltage	sd4_low_power	sd4_vsel<6:0>				
04h	LDO1Voltage	ldo1_on	ldo1_ilimit	-	ldo1		
05h	LDO2Voltage	ldo2_on	ldo2_ilimit	-	ldo2		
06h	LDO3Voltage	ldo3_ilimit	ldo3_vsel<6:0>				
07h	LDO4Voltage	ldo4_ilimit	ldo4_vsel<6:0>				
08h	LDO5Voltage	ldo5_ilimit	ldo5_vsel<6:0>				
09h	LDO6Voltage	ldo6_ilimit	ldo6_vsel<6:0>				
0ah	LDO7Voltage	ldo7_ilimit	ldo7_vsel<6:0>				
0bh	LDO8Voltage	ldo8_ilimit	ldo8_vsel<6:0>				
0ch	GPIO1control	gpio1_invert	gpio1_iosf<6:3>				
0dh	GPIO2control	gpio2_invert	gpio2_iosf<6:3>				
0eh	GPIO3control	gpio3_invert	gpio3_iosf<6:3>				
0fh	GPIO4control	gpio4_invert	gpio4_iosf<6:3>				

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
10h	SDcontrol	-		sd4_force_pwm	sd1_force_ pwm	sd4_enable	s
11h	LDOcontrol	-		ldo8_enable	ldo7_enable	ldo6_enable	l
20h	GPIOsignal_out	gpio8_out	gpio7_out	gpio6_out	gpio5_out	gpio4_out	
21h	GPIOsignal_in	gpio8_in	gpio7_in	gpio6_in	gpio5_in	gpio4_in	
22h	Reg1_Voltage	Reg1_voltage<7:0>					
23h	Reg2_Voltage	Reg2_voltage<7:0>					
24h	Reg_control	Reg_select2<7:4>					
25h	GPIOctrl_sd	gpio_ctrl_sd4<7:6>		gpio_ctrl_sd3<5:4>		gpio_ctrl_sd2<	
26h	GPIOctrl_ldo1	gpio_ctrl_ldo4<7:6>		gpio_ctrl_ldo3<5:4>		gpio_ctrl_ldo2<	
27h	GPIOctrl_ldo2	gpio_ctrl_ldo8<7:6>		gpio_ctrl_ldo7<5:4>		gpio_ctrl_ldo6<	
2bh	Reg3_Voltage	Reg3_voltage<7:0>					
2ch	Reg_control3	-					
2dh	SD4_control1	sd4_ilimit<7:6>		sd4_trim_gm<5:4>		sd4_lv_deb<3	
2eh	SD4_control2	temp_sd4_ shutdown	temp_sd4_alarm	sdmph_clk_div<5:4>		sd4_startslew<	
30h	SD_control1	sd4_low_noise	sd3_low_noise	sd2_low_noise	sd1_low_noise	sd4_fast	
31h	SD_control2	dvm_time_sd4<7:6>		dvm_time_sd1<5:4>		sd3_slave	
32h	Battery_voltage_m onitor	FastResEn	SupResEn	ResVoltFall<5:3>			
33h	Startup_Control	-					or

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
34h	ResetTimer	-	stby_reset_disable	auto_off	off_delay<4:3>		
35h	ReferenceControl	on_reset_delay	reg_low_bias_mode	clk_div2	standby_mode_on		c
36h	ResetControl	mask_ovtemp	reset_reason<6:3>				
37h	OvertemperatureControl					rst_ov_temp_140	ov
38h	WatchdogControl	-					
39h	Reg_standby_mod1	disable_regpd	-			sd4_stby_on	s
3ah	Reg_standby_mod2	ldo8_stby_on	ldo7_stby_on	ldo6_stby_on	ldo5_stby_on	ldo4_stby_on	ld
3bh	Reg_sequ_mod1	-				sd4_sequ_on	s
3ch	Reg_sequ_mod2	ldo8_sequ_on	ldo7_sequ_on	ldo6_sequ_on	ldo5_sequ_on	ldo4_sequ_on	ld
40h	curr_control	curr3_ctrl<7:4>				curr2_ctrl<3:	
41h	pwm_control_l	pwm_l_time<7:0>					
42h	pwm_control_h	pwm_h_time<7:0>					
43h	curr1_value	curr1_current<7:0>					
44h	curr2_value	curr2_current<7:0>					
45h	curr3_value	curr3_current<7:0>					
46h	Watchdog_min_timer	wtdg_min_timer<7:0>					
47h	Watchdog_max_timer	wtdg_max_timer<7:0>					

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
48h	WatchdogSoftwareSignal	pwm_div<7:6>		-			
51h	Stepup_control2	stepup2_v<7:3>					s
53h	Stepup_control4	-				stepup2_pwm_lowf	ste
54h	Stepup_control5	-				stepup2_pwm_mode	ste
55h	CPcontrol	-					
56h	ADC_BATTEMP	adc_battemp<7:0>					
60h	GPIO5control	gpio5_invert	gpio5_iosf<6:3>				
61h	GPIO6control	gpio6_invert	gpio6_iosf<6:3>				
63h	GPIO8_7control	gpio8_mode<7:5>			gpio8_invert	gpio	
67h	ENsignal_in	-				en4_in	
69h	SRAM	SRAM<7:0>					
70h	ADC_control	start_conversion	adc_presample	adc_slow	gpio_lv		
71h	ADC_MSB_result	result_not_ready	D9_3<6:0>				
72h	ADC_LSB_result	-					
73h	RegStatus	curr3_lv	curr2_lv	curr1_lv	-	sd4_lv	
74h	InterruptMask1	LowBat_int_m	ovtmp_int_m	onkey_int_m	chdet_int_m	eoc_int_m	res
75h	InterruptMask2	ebat_int_m	temp_sd4_shutdown_int_m	temp_sd4_alarm_int_m	bat_temp_m	sd4_lv_int_m	sd
76h	InterruptMask3	chdet2_int_m	en4_int_m	en3_int_m	en2_int_m	en1_int_m	gp

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
77h	InterruptStatus1	LowBat_int_i	ovtmp_int_i	onkey_int_i	chdet_int_i	eoc_int_i	re
78h	InterruptStatus2	ebat_int_i	temp_sd4_shutdown_int_i	temp_sd4_alarm_int_i	bat_temp_i	sd4_lv_int_i	s
79h	InterruptStatus3	chdet2_int_i	en4_int_i	en3_int_i	en2_int_i	en1_int_i	gp
7fh	ChargerControl0	-			usb12_feedthrough		
80h	ChargerControl1	cc_eoc_hcurr	Auto_Resume	bat_charging_enable	usb_current<		
81h	ChargerVoltageControl	vsup_min<7:6>		ChVoltEOC<5:0>			
82h	ChargerCurrentControl	eoc_current	cc_lowlimit	ConstantCurrent<5:2>			
83h	Chargerconfig	usb_combined	usb2_on	ChVoltResume	temp_sel<4:3>		
84h	NTCsupervision	-	ebat_enable			jeita_on	ze
85h	Chargersupervision	Charging_1Hz_clk	ovprot_dis	dcdc_chmode	charging_tmax		
86h	ChargerStatus1	Nobat	Battemp_hi	EOC	CVM	Trickle	
87h	ChargerStatus2	usb_prt_ready_deb	temp_cond<6:4>			batsw2_on	ba
88h	T1_adjust	-		T1_adj<5:0>			
89h	T2_adjust	-			T2		
8ah	T3_adjust	-			T3		
8bh	T4_adjust	-		T4_adj<5:0>			
8ch	T2_T1_hyst	T2_hyst<7:4>					

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
8dh	T4_T3_hyst	T4_hyst<7:4>					
8eh	LockRegister	-					cl
90h	ASIC_ID1	ID1<7:0>					
91h	ASIC_ID2	-					
a7h	Fuse7	del_time	unique_id	sequ_on	-		
a8h	Fuse8	sd3_slave	sd3_fsel	sd2_fsel	sd2_slave	sd4_fast	
a9h	Fuse9	auto_off	chg_pwr_off_en	res_timer<5:4>		Res	
aah	Fuse10	usb2_current<7:4>					
abh	Fuse11	power_off_at_ vsuplow	ovprot_dis	on_reset_delay	onkey_lpress_ reset	dcdc_chmode	
ach	Fuse12	Reg4_gpio_sel<7:6>		Reg3_gpio_sel<5:4>		Reg2_gpio_sel<	
adh	Fuse13	Reg2_select<7:4>					
aeh	Fuse14	reg1_V<7:0>					

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
afh	Fuse15	reg2_V<7:0>					
b0h	Fuse16	Reg4_select<7:4>					
b1h	Fuse17	reg3_V<7:0>					
b2h	Fuse18	reg4_V<7:0>					
b3h	Fuse19	Reg8_gpio_sel<7:6>		Reg7_gpio_sel<5:4>		Reg6_gpio_sel<	
b4h	Fuse20	Reg6_select<7:4>					
b5h	Fuse21	reg5_V<7:0>					
b6h	Fuse22	reg6_V<7:0>					
b7h	Fuse23	Reg8_select<7:4>					
b8h	Fuse24	reg7_V<7:0>					

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	
b9h	Fuse25	reg8_V<7:0>					
bah	Fuse26_uniqueID0	-		Reg11_gpio_sel<5:4>		Reg10_gpio_sel	
bbh	Fuse27_uniqueID1	Reg10_select<7:4>					
bch	Fuse28_uniqueID2	reg9_V<7:0>					
bdh	Fuse29_uniqueID3	reg10_V<7:0>					
beh	Fuse30_uniqueID4	ibattemp10k					
bfh	Fuse31_uniqueID5	reg11_V<7:0>					

Register Overview: Shows all the available registers.

Detailed Register Description

Figure 84:
SD1Voltage

Addr:00h		SD1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd1_frequ	0	RW	Selects between high and low frequency 0 : 3MHz 1 : 4MHz
6:0	sd1_vsel	b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD1=0.6V+sd1_vsel*12.5mV 41h-70h : V_SD1=1.4V+(sd1_vsel-40h)*25mV 71h-7Fh : V_SD1=2.6V+(sd1_vsel-70h)*50mV

Figure 85:
SD2Voltage

Addr:01h		SD2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd2_frequ	0	RW	Selects between high and low frequency dependent on sd2_fsel 0 : 2MHz if sd2_fsel=0, 3MHz if sd2_fsel=1 1 : 3MHz if sd2_fsel=0, 4MHz if sd2_fsel=1
6:0	sd2_vsel	b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD2=0.6V+sd2_vsel*12.5mV 41h-70h : V_SD2=1.4V+(sd2_vsel-40h)*25mV 71h-7Fh : V_SD2=2.6V+(sd2_vsel-70h)*50mV

Figure 86:
SD3Voltage

Addr:02h		SD3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd3_frequ	0	RW	Selects between high and low frequency dependent on sd3_fsel 0 : 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1 1 : 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1
6:0	sd3_vsel	b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. 00h : DC/DC powered down 01h-40h : V_SD3=0.6V+sd3_vsel*12.5mV 41h-70h : V_SD3=1.4V+(sd3_vsel-40h)*25mV 71h-7Fh : V_SD3=2.6V+(sd3_vsel-70h)*50mV

Figure 87:
SD4Voltage

Addr:03h		SD4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd4_low_power	0	RW	Controls low power mode for sd4 0 : Normal mode 1 : Low power mode. Reduced current capability only 1 phase enabled and reduced output current on that phase
6:0	sd4_vsel	b0000000	RW	The voltage select bits set the DC/DC output voltage level and power the DC/DC converter down. (0.6..1.5V) 00h : DC/DC powered down 01h-5Ah : V_SD4=0.6V+sd4_vsel*10mV 5Ah-7Fh : NA

Figure 88:
LDO1Voltage

Addr:04h		LDO1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo1_on	0	RW	Switch ON of LDO1 0 : LDO OFF 1 : LDO ON
6	ldo1_ilimit	0	RW	Sets limit of LDO1 0 : 150mA operating range 1 : 250mA operating range
4:0	ldo1_vsel	b00000	RW	The voltage select bits set the LDO output voltage 0h-0Fh : 1.2V + ldo1_vsel*50mV 10h-1Fh : 1.8V + (ldo1_vsel-16)*100mV

Figure 89:
LDO2Voltage

Addr:05h		LDO2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo2_on	0	RW	Switch ON of LDO2 0 : LDO OFF 1 : LDO ON
6	ldo2_ilimit	0	RW	Sets limit of LDO2 0 : 150mA operating range 1 : 250mA operating range
4:0	ldo2_vsel	b00000	RW	The voltage select bits set the LDO output voltage 0h-0Fh : 1.2V + ldo2_vsel*50mV 10h-1Fh : 1.8V + (ldo2_vsel-16)*100mV

Figure 90:
LDO3Voltage

Addr:06h		LDO3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo3_ilimit	0	RW	Sets limit of LDO3 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo3_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO3=0.8V+ldo3_vsel*25mV 25h-3fh : do not use 40h-7Fh : V_LDO3=1.725V+(ldo3_vsel-40h)*25mV

Figure 91:
LDO4Voltage

Addr:07h		LDO4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo4_ilimit	0	RW	Sets limit of LDO4 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo4_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO4=0.8V+ldo4_vsel*25mV 25h-3fh : do not use 40h-7Fh : V_LDO4=1.725V+(ldo4_vsel-40h)*25mV

Figure 92:
LDO5Voltage

Addr:08h		LDO5Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo5_ilimit	0	RW	Sets limit of LDO5 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo5_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO5=0.8V+ldo5_vsel*25mV 25h-3fh : do not use 40h-7Fh : V_LDO5=1.725V+(ldo5_vsel-40h)*25mV

Figure 93:
LDO6Voltage

Addr:09h		LDO6Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo6_ilimit	0	RW	Sets limit of LDO6 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo6_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO6=0.8V+ldo6_vsel*25mV 25h-3fh : do not use 40h-7Fh : V_LDO6=1.725V+(ldo6_vsel-40h)*25mV

Figure 94:
LDO7Voltage

Addr:0ah		LDO7Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo7_ilimit	0	RW	Sets limit of LDO7 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo7_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO7=0.8V+ldo7_vsel*25mV 25h-3fh : do not use 40h-7eh : V_LDO7=1.725V+(ldo7_vsel-40h)*25mV 7fh : V_LDO7=VIN_LDO78 (ldo7_sw_on=1)

Figure 95:
LDO8Voltage

Addr:0bh		LDO8Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo8_ilimit	0	RW	Sets limit of LDO8 0 : 150mA operating range 1 : 300mA operating range
6:0	ldo8_vsel	b0000000	RW	The voltage select bits set the LDO output voltage 0.825V...3.3V, 25mV steps 00h : LDO OFF 01h-24h : V_LDO8=0.8V+ldo8_vsel*25mV 25h-3fh : do not use 40h-7eh : V_LDO8=1.725V+(ldo8_vsel-40h)*25mV 7fh : V_LDO8=VIN_LDO78 (ldo8_sw_on=1)

Figure 96:
GPIO1control

Addr:0ch		GPIO1control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio1_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio1_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3, if GPIO2_iosf=5 then apply on RegSelect1 only) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/841mA charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio1_mode	b011	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 97:
GPIO2control

Addr:0dh		GPIO2control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio2_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio2_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3, if GPIO1_iosf=5 then apply on RegSelect2 and RegSelect3 only) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/841mA charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio2_mode	b011	RW_SM	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 98:
GPIO3control

Addr:0eh		GPIO3control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio3_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio3_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/841mA charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio3_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 99:
GPIO4control

Addr:0fh		GPIO4control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio4_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio4_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/84841 charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio4_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 100:
SDcontrol

Addr:10h		SDcontrol		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	sd4_force_pwm	b0	RW	Selects force PWM mode 0 : Normal mode 1 : Force PWM, inverted coil current possible to keep the fixed frequency
4	sd1_force_pwm	b0	RW	Selects force PWM mode 0 : Normal mode 1 : Force PWM, inverted coil current possible to keep the fixed frequency
3	sd4_enable	b1	RW	Global stepdown4 enable
2	sd3_enable	b1	RW	Global stepdown3 enable
1	sd2_enable	b1	RW	Global stepdown2 enable
0	sd1_enable	b1	RW	Global stepdown1 enable

Figure 101:
LDOcontrol

Addr:11h		LDOcontrol		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5	ldo8_enable	b1	RW	Global ldo8 enable
4	ldo7_enable	b1	RW	Global ldo7 enable
3	ldo6_enable	b1	RW	Global ldo6 enable
2	ldo5_enable	b1	RW	Global ldo5 enable
1	ldo4_enable	b1	RW	Global ldo4 enable
0	ldo3_enable	b1	RW	Global ldo3 enable

Figure 102:
GPIOsignal_out

Addr:20h		GPIOsignal_out		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio8_out	0	RW	This bit determines the output signal of the GPIO8 pin when selected as output source
6	gpio7_out	0	RW	This bit determines the output signal of the GPIO7 pin when selected as output source
5	gpio6_out	0	RW	This bit determines the output signal of the GPIO6 pin when selected as output source
4	gpio5_out	0	RW	This bit determines the output signal of the GPIO5 pin when selected as output source
3	gpio4_out	0	RW	This bit determines the output signal of the GPIO4 pin when selected as output source
2	gpio3_out	0	RW	This bit determines the output signal of the GPIO3 pin when selected as output source
1	gpio2_out	0	RW	This bit determines the output signal of the GPIO2 pin when selected as output source
0	gpio1_out	0	RW	This bit determines the output signal of the GPIO1 pin when selected as output source

Figure 103:
GPIOsignal_in

Addr:21h		GPIOsignal_in		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio8_in	0	RO	This bit reflects the logic level of the GPIO8 pin when configured as digital input pin
6	gpio7_in	0	RO	This bit reflects the logic level of the GPIO7 pin when configured as digital input pin
5	gpio6_in	0	RO	This bit reflects the logic level of the GPIO6 pin when configured as digital input pin
4	gpio5_in	0	RO	This bit reflects the logic level of the GPIO5 pin when configured as digital input pin
3	gpio4_in	0	RO	This bit reflects the logic level of the GPIO4 pin when configured as digital input pin
2	gpio3_in	0	RO	This bit reflects the logic level of the GPIO3 pin when configured as digital input pin
1	gpio2_in	0	RO	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin
0	gpio1_in	0	RO	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin

Figure 104:
Reg1_Voltage

Addr:22h		Reg1_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reg1_voltage	b00000000	RW	This register is mapped to the register address 0h+Reg1_select, if gioX_iosf=5 or 6 (Vselect input), and input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input 0 ..FFh : Selects voltage, ilimit, ON or frequ. Bits of LDO or DCDC

Figure 105:
Reg2_Voltage

Addr:23h		Reg2_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reg2_voltage	b00000000	RW	This register is mapped to the register address 0h+Reg1_select, if gioX_iosf=5 or 6 (Vselect input), and input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input 0 ..FFh : Selects voltage, ilimit, ON or frequ. Bits of LDO or DCDC

Figure 106:
Reg_control

Addr:24h		Reg_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reg_select2	b1111	RW	Selects regulator for mapping feature if reg_select2 ≥ 0Ch then feature disabled
3:0	Reg_select1	b1111	RW	Selects regulator for mapping feature if reg_select1 ≥ 0Ch then feature disabled

Figure 107:
GPIOctrl_sd

Addr:25h		GPIOctrl_sd		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_sd4	b00	RW_SM	Enable GPIO control of DCDC SD4. GPIO ctrl only enabled, if sd4_vsel>0 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
5:4	gpio_ctrl_sd3	b00	RW_SM	Enable GPIO control of DCDC SD3. GPIO ctrl only enabled, if sd3_vsel>0 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
3:2	gpio_ctrl_sd2	b00	RW_SM	Enable GPIO control of DCDC SD2. GPIO ctrl only enabled, if sd2_vsel>0 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
1:0	gpio_ctrl_sd1	b00	RW_SM	Enable GPIO control of DCDC SD1. GPIO ctrl only enabled, if sd1_vsel>0 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3

Figure 108:
GPIOctrl_ldo1

Addr:26h		GPIOctrl_ldo1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_ldo4	b00	RW_SM	Enable GPIO control of LDO4. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
5:4	gpio_ctrl_ldo3	b00	RW_SM	Enable GPIO control of LDO3. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
3:2	gpio_ctrl_ldo2	b00	RW_SM	Enable GPIO control of LDO2. GPIO ctrl only enabled, if LDO2_on=1 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
1:0	gpio_ctrl_ldo1	b00	RW_SM	Enable GPIO control of LDO1. GPIO ctrl only enabled, if LDO1_on=1 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3

Figure 109:
GPIOctrl_ldo2

Addr:27h		GPIOctrl_ldo2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_ldo8	b00	RW_SM	Enable GPIO control of LDO8. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
5:4	gpio_ctrl_ldo7	b00	RW_SM	Enable GPIO control of LDO7. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
3:2	gpio_ctrl_ldo6	b00	RW_SM	Enable GPIO control of LDO6. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3
1:0	gpio_ctrl_ldo5	b00	RW_SM	Enable GPIO control of LDO5. 0 : No GPIO control 1 : Controlled by GPIO1 2 : Controlled by GPIO2 3 : Controlled by GPIO3

Figure 110:
Reg3_Voltage

Addr:2Bh		Reg3_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	Reg3_voltage	b00000000	RW	This register is mapped to the register address 0h+Reg1_select, if gioX_iosf=5 or 6 (Vselect input), and input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input 0 ..FFh : Selects voltage, ilimit, ON or frequ. Bits of LDO or DCDC

Figure 111:
Reg_control3

Addr:2Ch		Reg_control3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3:0	Reg_select3	b1111	RW	

Figure 112:
SD4_control1

Addr:2Dh		SD4_control1		
Bit	Bit Name	Default	Access	Bit Description
7:6	sd4_ilimit	b00	RW	Selects overcurrent trip threshold of SD4 per phase 0 : 2.5A 1 : 3A 2 : 3.5A 3 : do not use
5:4	sd4_trim_gm	0	RW	Selects gm setting of OTA 0 : Fast setting 1 : Slow setting 2 : Medium setting 3 : Very slow setting
3:2	sd4_lv_deb	00	RW	Selects debounce time of sd1_lv signal 0 : No debouncing 1 : 1 us 2 : 4 us 3 : 20 us
1	sd4_combine	0	RW_SM	Selects phase mode (set during startup power_stage test) 0 : Normal mode 1 : Combine phase 1 and 2
0	sd4_phases	1b1	RW_SM	Selects number of phases for sd4 (set during startup power_stage test, can be changed after that) 0 : 1 phase used 1 : 2 phases used

Figure 113:
SD4_control2

Addr:2Eh		SD4_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	temp_sd4_shutdown	0	R	Indicates over temperature >140deg in subdie. Reset initated if mask_ovtemp=0
6	temp_sd4_alarm	0	R	Indicates over temperature >110deg in subdie
5:4	sdmph_clk_div	0	RW_SM	Divide clock of SD4 by 1, 2 or 4 0 : 2.7MHz 1 : 1.35MHz 2 : 0.675MHz 3 : 0.675MHz
3:2	sd4_startslew	0	RW	Sets the startup slew rate of SD4 0 : 2.5mV / us 1 : 5mV / us 2 : 10mV / us 3 : 20mV / us
1	sd4_nph_auto	0	R	Status of the actual number of phases used ,if phase switching enabled 0 : 1 phase 1 : 2 phases
0	sd4_phsw_on	0	RW	Switch ON automatic phase switching for sd4

Figure 114:
SD_control1

Addr:30h		SD_control1		
Bit	Bit Name	Default	Access	Bit Description
7	sd4_low_noise	0	RW	Enables low noise mode of SD4. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of >100mA applied in skip mode 1 : Low noise mode. Only minimum ON time applied in skip mode
6	sd3_low_noise	0	RW	Enables low noise mode of SD3. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of >100mA applied in skip mode 1 : Low noise mode. Only minimum ON time applied in skip mode
5	sd2_low_noise	0	RW	Enables low noise mode of SD2. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of >100mA applied in skip mode 1 : Low noise mode. Only minimum ON time applied in skip mode
4	sd1_low_noise	0	RW	Enables low noise mode of SD1. If enabled smaller current pulses and output ripple is activated 0 : Normal mode. Minimum current pulses of >100mA applied in skip mode 1 : Low noise mode. Only minimum ON time applied in skip mode
3	sd4_fast	0	RW_SM	Selects a faster regulation mode for SD4 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
2	sd3_fast	0	RW_SM	Selects a faster regulation mode for SD3 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
1	sd2_fast	0	RW_SM	Selects a faster regulation mode for SD2 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
0	sd1_fast	0	RW_SM	Selects a faster regulation mode for SD1 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required

Figure 115:
SD_control2

Addr:31h		SD_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	dvm_time_sd4	b00	RW	Time steps of DVM voltage change of SD4 If voltage of step Down is changed during operation (sdx_vsel) voltage is de/increased by single steps 10mV 0 : 0 usec, immediate change (no DVM) 1 : 1 usec time delay between steps 2 : 2 usec time delay between steps 3 : 8 usec time delay between steps
5:4	dvm_time_sd1	b00	RW	Time steps of DVM voltage change of SD1 If voltage of step Down is changed during operation (sdx_vsel) voltage is de/increased by single steps 12.5/25/50mV 0 : 0 usec, immediate change (no DVM) 1 : 4 usec time delay between steps 2 : 8 usec time delay between steps 3 : 16 usec time delay between steps
3	sd3_slave	0	RW_SM	Enables slave mode of SD3 0 : Normal mode of SD3 1 : SD3 is slave of SD2.
2	sd3_fsel	0	RW_SM	Selects between high and low frequency range 0 : 2 or 3MHz frequency (selctable by sd3_frequ) 1 : 3 or 4MHz frequency (selctable by sd3_frequ)
1	sd2_fsel	0	RW_SM	Selects between high and low frequency range 0 : 2 or 3MHz frequency (selctable by sd2_frequ) 1 : 3 or 4MHz frequency (selctable by sd2_frequ)
0	sd2_slave	0	RW_SM	Enables slave mode of SD2 0 : Normal mode of SD2 1 : SD2 is slave of SD1

Figure 116:
Battery_voltage_monitor

Addr:32h		Battery_voltage_monitor		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FastResEn	0	RW	0 : Vresetfall debounce time = 3msec 1 : Vresetfall debounce time = 4usec (tbd)
6	SupResEn	0	RW_SM	0 : A reset is generated if VSUP falls below 2.7V. (1) 1 : A reset is generated if VSUP falls below ResVoltFall
5:3	ResVoltFall	b000	RW_SM	This value determines the reset level ResVoltFall for falling VBAT. It is recommended to set this value at least 200mV lower than ResVoltRise 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V
2:0	ResVoltRise	b000	RO	This value determines the reset level ResVoltRise for rising VBAT. It is recommended to set this value at least 200mV higher than ResVoltFall 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V

Note(s) and/or Footnote(s):

1. If VSUP falls below ResVoltFall only an interrupt is generated (if enabled) and the uProcessor can shut down the system

Figure 117:
Startup_Control

Addr:33h		Startup_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	onkey_lpress_reset	0	RW_SM	Selects behavior for ONKEY/ENx longpress 0 : Change to power_off mode 1 : Reset cycle started if on_reset_delay=0; ONKEY/ENx longpress is disabled if on_reset_delay=1
1	chg_pwr_off_en	0	RO	Select charger detection in power OFF mode Read only (OTP setting) 0 : Exit of Power OFF mode, if charger is detected (level detection) 1 : Exit of Power OFF mode, if charger is attached or detached
0	power_off_at_vsuplow	0	RW_SM	Switch ON Power OFF mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0) 0 : If low battery is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltrise 1 : If low battery is detected, enter power OFF mode

Figure 118:
ResetTimer

Addr:34h		ResetTimer		
Bit	Bit Name	Default	Access	Bit Description
6	stby_reset_disable	0	RW	Disable Reset output signal (PIN XRES) in standby mode 0 : Normal mode, reset is active in standby mode 1 : No reset in standby mode and during exit of standby mode
5	auto_off	0	RO	Defines startup behavior at first battery insertion 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power OFF mode (Startup with ON key or charger insertion)
4:3	off_delay	b01	RW	Set Delay between I^2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command 0 : No delay 1 : 8 msec 2 : 16 msec 3 : 32 msec
1:0	res_timer	b00	RW_SM	Set RESTime, after the last regulator has started 0 : RESTIME=10ms 1 : RESTIME=50ms 2 : RESTIME=100ms 3 : RESTIME=150ms

Figure 119:
ReferenceControl

Addr:35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	on_reset_delay	0	RW_SM	Sets the ONKEY/ENx longpress delay time 0 : 8 sec 1 : 4 sec if onkey_lpress_reset=0; ONKEY/ENx longpress is disabled if onkey_lpress_reset=1
6	reg_low_bias_mode	0	RW_SM	
5	clk_div2	0	RW_SM	Divide internal clock oscillator by 2 to reduce quiescent current for low power operation 0 : Normal mode 1 : Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DCDC converters are divided by two. Reduced transient performance of DCDC converters.
4	standby_mode_on	0	RW_SM	Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by Reg_standby_mod. XRESET will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously ON.
3:1	clk_int	b000	RW_SM	Sets the internal CLK frequency fCLK used for fuel gauge, DCDCs, PWM, ...(1) 0 : 4 MHz (default) 1 : 3.8 MHz 2 : 3.6 MHz 3 : 3.4 MHz 4 : 3.2 MHz 5 : 3.0 MHz 6 : 2.8 MHz 7 : 2.6 MHz
0	low_power_on	0	RW_SM	Enable low power mode of internal reference. 0 : Standard mode 1 : Low power mode - all specification except noise parameters are still valid. Iq reduced by approx. 30uA

Note(s) and/or Footnote(s):

1. All frequencies, timings and delays in this datasheet are based on 4MHz clk_int.

Figure 120:
ResetControl

Addr:36h		ResetControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	mask_ovtemp	0	RW	Inhibit reset caused by over temperature of SD4 0 : Over temperature of SD4 causes reset 1 : Over temperature of SD4 causes interrupt only
6:3	reset_reason	b0000	RW_SM	Flags to indicate to the software the reason for the last reset 0 : VPOR has been reached (battery or charger insertion from scratch) 1 : ResVoltFall was reached (battery voltage drop below 2.75V) 2 : Software forced by force_reset 3 : Wakeup from power OFF by ON key 4 : Wakeup from power OFF by charger 5 : Reset caused by XRES pin 6 : Reset caused by overtemperature T140 7 : Reset caused by watchdog 8 : Reset caused by 8 seconds ON key press 9 : Reset caused by overtemperature T140 of subdie (SD4) 10 : Wakeup from standby mode by interrupt 11 : Wakeup from standby mode by ON key 12 : Wakeup from standby mode or power OFF by EN1 pin 13 : Wakeup from standby mode or power OFF by EN2 pin 14 : Wakeup from standby mode or power OFF by EN3 pin 15 : Wakeup from standby mode or power OFF by EN4 pin
2	on_input	0	R_PUSH1	Read:This flag represents the state of the ON pad directly Write: Setting to 1 resets the 4/8 sec. ON key reset timer
1	power_off	0	RW_SM	Setting to 1 starts a reset cycle, but waits after the Reg_off state for a rising edge on the pin ON or until the charger is detected
0	force_reset	0	RW	Setting to 1 starts a complete reset cycle

Figure 121:
OvertemperatureControl

Addr:37h		OvertemperatureControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	tco_140_a	0	RO	Only used for production test
6	tco_110_a	0	RO	Only used for production test
5:4	temp_test	b00	RW	
3	rst_ov_temp_140	0	RW_SMP	If the overtemperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterward 0 to rst_ov_temp_140
2	ov_temp_140	0	RO	Flag that the overtemperature threshold 2 (T140) has been reached - this flag is not reset by a overtemperature caused reset and has to be reset by rst_ov_temp_140
1	ov_temp_110	0	RO	Flag that the overtemperature threshold 1 (T110) has been reached
0	temp_pmc_on	1	RW	Switch ON/OFF of temperature supervision; default: ON - all other bits are only valid if set to 1 Leave at 1, do not disable

Figure 122:
WatchdogControl

Addr:38h		WatchdogControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	wtdg_res_on	0	RW	If the watchdog expires and wtdg_res_on = 1 a reset cycle will be started - see section Reset
0	wtdg_on	0	RW	Switches ON the complete watchdog 0 : Watchdog OFF 1 : Watchdog enabled

Figure 123:
Reg_standby_mod1

Addr:39h		Reg_standby_mod1		
Bit	Bit Name	Default	Access	Bit Description
7	disable_regpd	0	RW	This bit disables the pulldown of all regulators 0 : Normal operation approx. 1kOhm pulldown of all regulators 1 : Pulldown disabled >100kOhm of all regulators
3	sd4_stby_on	0	RW	Enable Step down 4 in standby mode
2	sd3_stby_on	0	RW	Enable Step down 3 in standby mode
1	sd2_stby_on	0	RW	Enable Step down 2 in standby mode
0	sd1_stby_on	0	RW	Enable Step down 1 in standby mode

Figure 124:
Reg_standby_mod2

Addr:3ah		Reg_standby_mod2		
Bit	Bit Name	Default	Access	Bit Description
7	ldo8_stby_on	0	RW	Enable LDO8 in standby mode
6	ldo7_stby_on	0	RW	Enable LDO7 in standby mode
5	ldo6_stby_on	0	RW	Enable LDO6 in standby mode
4	ldo5_stby_on	0	RW	Enable LDO5 in standby mode
3	ldo4_stby_on	0	RW	Enable LDO4 in standby mode
2	ldo3_stby_on	0	RW	Enable LDO3 in standby mode
1	ldo2_stby_on	0	RW	Enable LDO2 in standby mode
0	ldo1_stby_on	0	RW	Enable LDO1 in standby mode

Figure 125:
Reg_sequ_mod1

Addr:3bh		Reg_sequ_mod1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	sd4_sequ_on	0	RW_SM	Step down 4 controlled by sequencer for ramping down (reset or power_off)
2	sd3_sequ_on	0	RW_SM	Step down 3 controlled by sequencer for ramping down (reset or power_off)
1	sd2_sequ_on	0	RW_SM	Step down 2 controlled by sequencer for ramping down (reset or power_off)
0	sd1_sequ_on	0	RW_SM	Step down 1 controlled by sequencer for ramping down (reset or power_off)

Figure 126:
Reg_sequ_mod2

Addr:3ch		Reg_sequ_mod2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo8_sequ_on	0	RW_SM	LDO8 controlled by sequencer for ramping down (reset or power_off)
6	ldo7_sequ_on	0	RW_SM	LDO7 controlled by sequencer for ramping down (reset or power_off)
5	ldo6_sequ_on	0	RW_SM	LDO6 controlled by sequencer for ramping down (reset or power_off)
4	ldo5_sequ_on	0	RW_SM	LDO5 controlled by sequencer for ramping down (reset or power_off)
3	ldo4_sequ_on	0	RW_SM	LDO4 controlled by sequencer for ramping down (reset or power_off)
2	ldo3_sequ_on	0	RW_SM	LDO3 controlled by sequencer for ramping down (reset or power_off)
1	ldo2_sequ_on	0	RW_SM	LDO2 controlled by sequencer for ramping down (reset or power_off)
0	ldo1_sequ_on	0	RW_SM	LDO1 controlled by sequencer for ramping down (reset or power_off)

Figure 127:
curr_control

Addr:40h		curr_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	curr3_ctrl	b0000	RW	ON/OFF control of the pad CURR3 0 : Current sink is turned OFF 1 : Current sink is active 2 : Current sink is active and LED string connected to SU2. Required for automatic feedback selection. 3 : Controlled by internal PWM generator, or external, if gpioX_iosf=4 4 : XINT output 5 : VSUP_low output 6 : Charger active output 7 : EOC output 8 : Inverted signal of ON pin as output 9 : Signal of ON pin as output 10 : 32 kHz output (derived from oscillator) 11 : PWM output 12 : PWRGOOD output 13-15 : NA
3:2	curr2_ctrl	b00	RW	ON/OFF control of the pad CURR2 0 : Current sink is turned OFF 1 : Current sink is active 2 : Current sink is active and LED string connected to SU2. Required for automatic feedback selection. 3 : Controlled by internal PWM generator, or external, if gpioX_iosf=4
1:0	curr1_ctrl	b00	RW	ON/OFF control of the pad CURR1 0 : Current sink is turned OFF 1 : Current sink is active 2 : Current sink is active and LED string connected to SU2. Required for automatic feedback selection. 3 : Controlled by internal PWM generator, or external, if gpioX_iosf=4

Figure 128:
pwm_control_l

Addr:41h		pwm_control_l		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_l_time	b00000000	RW	This bit defines the low time of the PWM generator in 1Mhz units 0 : pwm_div * 1usec 1 : pwm_div * 2usec 2 : pwm_div * 3usec ... : ... 255 : pwm_div * 256usec

Figure 129:
pwm_control_h

Addr:42h		pwm_control_h		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	pwm_h_time	b00000000	RW	This bit defines the high time of the PWM generator in 1MHz units 0 : pwm_div * 1usec 1 : pwm_div * 2usec 2 : pwm_div * 3usec ... : ... 255 : pwm_div * 256usec

Figure 130:
curr1_value

Addr:43h		curr1_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr1_current	b00000000	RW	Defines the current into CURR1 if enabled by curr1_ctrl 0 : Power down (default state) 1 : 0.1563mA (LSB) ... : ... 255 : 39.84mA

Figure 131:
curr2_value

Addr:44h		curr2_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr2_current	b00000000	RW	Defines the current into CURR2 if enabled by curr2_ctrl 0 : Power down (default state) 1 : 0.1563mA (LSB) ... : ... 255 : 39.84mA

Figure 132:
curr3_value

Addr:45h		curr3_value		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	curr3_current	b00000000	RW	Defines the current into CURR3 if enabled by curr3_ctrl 0 : Power down (default state) 1 : 0.1563mA (LSB) ... : ... 255 : 39.84mA

Figure 133:
Watchdog_min_timer

Addr:46h		Watchdog_min_timer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	wtdg_min_timer	b00000000	RW	Defines the minimum watchdog trigger time (LSB=7.5ms, range: 0 - 1.9s)

Figure 134:
Watchdog_max_timer

Addr:47h		Watchdog_max_timer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	wtdg_max_timer	b11111111	RW	Defines the maximum watchdog trigger time (LSB=7.5ms, range: 7.5ms - 1.9s), do not set to (00)h

Figure 135:
WatchdogSoftwareSignal

Addr:48h		WatchdogSoftwareSignal		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	pwm_div	b00	RW	This bit defines the divider ratio of the prescaler for the PWM generator 0 : Divide by 1 1 : Divide by 2 2 : Divide by 4 3 : Divide by 16
0	wtdg_sw_sig	0	PUSH	Trigger input by the serial interface, if GPIO1..4_iosf<>9

Figure 136:
Stepup_control2

Addr:51h		Stepup_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:3	stepup2_v	b00000	RW	Defines the tuning current at FB_SU pin 0 : 0 uA 1 : 1 uA ... : ... 31 : 31 uA
2	stepup2_res	0	RW	Gain selection for SU2 0 : If DCDC is used with current feedback (CURR1,CURR2,CURR3) or if FB_SU is used with current feedback only (Only R1,C1 connected) 1 : If FB_SU is used with external resistor divider (2 resistors)
1	stepup2_freq	0	RW	Selects Stepup2 frequency 0 : 1 MHz 1 : 0.5 MHz
0	stepup2_on	0	RW	ON/OFF control of SU2 0 : OFF 1 : ON

Figure 137:
Stepup_control4

Addr:53h		Stepup_control4		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
3	stepup2_pwm_lowf	0	RW	Selects PWM operation of Stepup2 0 : High frequency operation PWM>20kHz.(1) 1 : Low frequency PWM operation: Stepup2_on and curr1..3_on (if PWM enabled) switched OFF during PWM low time
2	stepup2_prot_dis	0	RW	DCDC converter 2 overvoltage protection to prevent damage of external NFET, if CURR1, CURR2 or CURR3 feedback selected, and no LED string connected 0 : Switch OFF DCDC step up 2 if the voltage on FB_SU exceeds 1.25V 1 : Overvoltage protection disabled.
1:0	stepup2_fb	b00	RW_SM	Controls the feedback source 0 : FB_SU enabled (external resistor divider) 1 : CURR1 feedback enabled (feedback through white LEDs) 2 : CURR2 feedback enabled (feedback through white LEDs) 3 : CURR3 feedback enabled (feedback through white LEDs)

Note(s) and/or Footnote(s):

1. Step_up switched ON all the time. (current sinks are not switched OFF (currX_on=1 all the time), but currX_current masked to 00h during PWM low time.). During PWM OFF-time then feedback voltage is sampled.

Figure 138:
Stepup_control5

Addr:54h		Stepup_control5		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2	stepup2_clkinv	0	RW	Invert input clock of step up2 converter 0 : Use positive edge of internal clk 1 : Use negative edge of internal clk
3	stepup2_pwm_mode	0	RW	Enable PWM mode 0 : Normal operation 1 : PWM mode operation. Feedback is sampled during PWM offtime, if stepup2_lowf=0.

Figure 139:
CPcontrol

Addr:55h		CPcontrol		
Bit	Bit Name	Default	Access	Bit Description
1	cp_freq	0	RW	Clock frequency selection 0 : 1 MHz 1 : 500 kHz
0	cp_on	0	RW	0 : Set CP into 1:1 mode (OFFstate) 1 : Set CP into 1:2 mode

Figure 140:
ADC_BATTEMP

Addr:56h		ADC_BATTEMP		
Bit	Bit Name	Default	Access	Bit Description
7:0	adc_battemp	h00	RW_SM	ADC measures BATTEMP NTC every 256 ms (when ntc_on=1). Low-pass filtered (t=512ms).

Figure 141:
GPIO5control

Addr:60h		GPIO5control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio5_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio5_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/841mA charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio5_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 142:
GPIO6control

Addr:61h		GPIO6control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio6_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
6:3	gpio6_iosf	b0000	RW	Select the GPIO special function 0 : Normal I/O operation 1 : Interrupt output 2 : VSUP_low output 3 : GPIO interrupt input 4 : Current sink PWM input 5 : Vselect input, (apply on RegSelect1 and RegSelect2 and RegSelect3) 6 : standby + Vselect + GPIO restart interrupt input 7 : pwr_good output 8 : 32 kHz output (derived from oscillator) 9 : Watchdog input 10 : Charger active output 11 : EOC output 12 : 100/841mA charger input 13 : 841mA/2.5A charger input 14 : PWM output 15 : Charging_enable input
2:0	gpio6_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 143:
GPIO8_7control

Addr:63h		GPIO8_7control		
Bit	Bit Name	Default	Access	Bit Description
0	gpio7_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
3:1	gpio7_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown
4	gpio8_invert	0	RW	Invert GPIO input/output 0 : Normal mode 1 : Invert input or output
7:5	gpio8_mode	b011	RW	Selects the GPIO mode (I, I/O, Tri, Pulls) 0 : Input 1 : Output (push and pull) 2 : Output/Input (open drain, only NMOS is active) 3 : ADC input (Tristate) 4 : Input with pullup 5 : Input with pulldown 6 : Output/Input open drain (NMOS) with pullup, 7 : ADC input with pulldown

Figure 144:
ENsignal_in

Addr:67h		ENsignal_in		
Bit	Bit Name	Default	Access	Bit Description
0	en1_in	0	RO	This bit reflects the logic level of the EN1 pin
1	en2_in	0	RO	This bit reflects the logic level of the EN2 pin
2	en3_in	0	RO	This bit reflects the logic level of the EN3 pin
3	en4_in	0	RO	This bit reflects the logic level of the EN4 pin

Figure 145:
SRAM

Addr:69h		SRAM		
Bit	Bit Name	Default	Access	Bit Description
7:0	SRAM	8h00	RW	

Figure 146:
ADC_control

Addr:70h		ADC_control		
Bit	Bit Name	Default	Access	Bit Description
7	start_conversion	0	R_PUSH1	Starts one ADC conversion. ADC conversion time t_adc = t_presample + 13*t_adc_clk.
6	adc_presample	0	RW	Activation time of analog input multiplexor and S/H before ADC conversion. 0 : t_presample = 16 us 1 : t_presample = 96 us. Useful for high impedance signals.
5	adc_slow	0	RW	ADC sampling frequency. 0 : t_adc_clk = 4 us, f_adc_clk = 250 kHz (t_adc = t_presample + 52 us) 1 : t_adc_clk = 16 us, f_adc_clk = 62.5 kHz (t_adc = t_presample + 208 us)
4	gpio_lv	0	RW	0 : High voltage range of GPIO3/4/7/8 (4:1 divider active) 1 : Low voltage range of GPIO3/4/7/8 (1:1 divider, 1.8V max)
3:0	adc_select	b0000	RW	Selects an ADC channel 0 : BATTEMP NTC (1:1) 1 : Temperature sensor: DIE temperature [C] = adc_result * 0.866 - 274 (1:1) 2 : CHGIN2 (4:1, 5.5Vmax) 3 : CURR1 (1:1, 1Vmax) 4 : CURR2 (1:1, 1Vmax) 5 : CURR3 (1:1, 1Vmax) 6 : VUSB1(15:1, 15V max) 7 : CHGIN1 (4:1) 8 : VIBAT (4:1) 9 : VSUP (4:1) 10 : VEBAT (4:1) 11 : GPIO3 (4:1 or 1:1) 12 : GPIO4 (4:1 or 1:1) 13 : GPIO7 (4:1 or 1:1) 14 : GPIO8 (4:1 or 1:1) 15 : NA

Figure 147:
ADC_MSB_result

Addr:71h		ADC_MSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	result_not_ready	0	RO	Indicates end of conversion 0 : Result is ready 1 : Conversion is running
6:0	D9_3	b0000000	RW_SM	ADC result register Bit9..Bit3

Figure 148:
ADC_LSB_result

Addr:72h		ADC_LSB_result		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
2:0	D2_0	b000	RW_SM	ADC result register Bit2..Bit0

Figure 149:
RegStatus

Addr:73h		RegStatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	curr3_lv	0	RO	Bit is set when voltage of current sink CURR3 drops below low voltage threshold (1ms debounce time default)
6	curr2_lv	0	RO	Bit is set when voltage of current sink CURR2 drops below low voltage threshold (1ms debounce time default)
5	curr1_lv	0	RO	Bit is set when voltage of current sink CURR1 drops below low voltage threshold (1ms debounce time default)
3	sd4_lv	0	RO	Bit is set when voltage of step down4 drops below low voltage threshold (-5%) (1ms debounce time default)
2	sd3_lv	0	RO	Bit is set when voltage of step down3 drops below low voltage threshold (-5%) (1ms debounce time default)
1	sd2_lv	0	RO	Bit is set when voltage of step down2 drops below low voltage threshold (-5%) (1ms debounce time default)
0	sd1_lv	0	RO	Bit is set when voltage of step down1 drops below low voltage threshold (-5%) (1ms debounce time default)

Figure 150:
InterruptMask1

Addr:74h		InterruptMask1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_m	1	RW	Rising edge only
6	ovtmp_int_m	1	RW	Rising edge only
5	onkey_int_m	1	RW	Rising and falling edge
4	chdet1_int_m	1	RW	Rising and falling edge
3	eoc_int_m	1	RW	Rising and falling edge
2	resume_int_m	1	RW	Rising and falling edge
1	nobat_int_m	1	RW	Rising and falling edge
0	trickle_int_m	1	RW	Rising and falling edge

Figure 151:
InterruptMask2

Addr:75h		InterruptMask2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ebat_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
6	temp_sd4_shutdown_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
5	temp_sd4_alarm_int_m	1	RW	0 : Interrupt enabled 1 : Interrupt masked (disabled)
4	bat_temp_int_m	1	RW	Rising and falling edge of high and low temp
3	sd4_lv_int_m	1	RW	Rising edge only
2	sd3_lv_int_m	1	RW	Rising edge only
1	sd2_lv_int_m	1	RW	Rising edge only
0	sd1_lv_int_m	1	RW	Rising edge only

Figure 152:
InterruptMask3

Addr:76h		InterruptMask3		
Bit	Bit Name	Default	Access	Bit Description
1	gpio_int_m	1	RW	Rising and falling edge
2	gpio_restart_int_m	1	RW	Falling edge
3	en1_int_m	1	RW	Rising and falling edge
4	en2_int_m	1	RW	Rising and falling edge
5	en3_int_m	1	RW	Rising and falling edge
6	en4_int_m	1	RW	Rising and falling edge
7	chdet2_int_m	1	RW	Rising and falling edge

Figure 153:
InterruptStatus1

Addr:77h		InterruptStatus1		
Bit	Bit Name	Default	Access	Bit Description
7	LowBat_int_i	0	POP	Bit is set when VSUP drops below vres_fall
6	ovtmp_int_i	0	POP	Bit is set when 110deg is exceeded
5	onkey_int_i	0	POP	
4	chdet1_int_i	0	POP	
3	eoc_int_i	0	POP	
2	resume_int_i	0	POP	
1	nobat_int_i	0	POP	
0	trickle_int_i	0	POP	

Figure 154:
InterruptStatus2

Addr:78h		InterruptStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ebat_int_i	0	POP	Leaving and entering the No_charger_ebat-state
6	temp_sd4_shutdown_int_i	0	POP	Rising and falling edge
5	temp_sd4_alarm_int_i	0	POP	Rising and falling edge
4	bat_temp_int_i	0	POP	Rising and falling edge of high and low temp
3	sd4_lv_int_i	0	POP	
2	sd3_lv_int_i	0	POP	
1	sd2_lv_int_i	0	POP	
0	sd1_lv_int_i	0	POP	

Figure 155:
InterruptStatus3

Addr:79h		InterruptStatus3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1	gpio_int_i	0	POP	
2	gpio_restart_int_i	0	POP	
3	en1_int_i	0	POP	Rising and falling edge at pin EN1
4	en2_int_i	0	POP	Rising and falling edge at pin EN2
5	en3_int_i	0	POP	Rising and falling edge at pin EN3
6	en4_int_i	0	POP	Rising and falling edge at pin EN4
7	chdet2_int_i	0	POP	

Figure 156:
ChargerControl0

Addr:7fh		ChargerControl0		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4	usb12_feedthrough	0	RW	0 : Switch VSUP_CHG-CHGIN2 is OFF 1 : Switch VSUP_CHG-CHGIN2 is ON, charging with CHGIN2 is disabled
3:0	usb2_current	b0100	RW_SM	Sets the USB input current limit 0 : 94mA 1 : 187mA 2 : 280mA 3 : 374mA 4 : 463mA 5 : 623mA 6 : 727mA 7 : 841mA 8 : 998mA 9 : 1100mA 10 : 1395mA 11 : 1600mA 12 : 1740mA 13 : 1956mA 14 : 2230mA 15 : 2600mA

Figure 157:
ChargerControl1

Addr:80h		ChargerControl1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	cc_eoc_hcurr	1	RW	0 : Low current mode for eoc- and constant-current. The current is scaled by a factor of 2/5 of the nominal current value (eoc-current-range=24 - 96mA; constant-current range=300 - 600mA) 1 : High current mode for eoc- and constant-currrent. The nominal current values are used.(refer to Reg 82h).
6	Auto_Resume	1	RW	
5	bat_charging_enable	0	RW	0 : USB is supplying VSUP, but battery switch is open. USB charger regulates to Vsup_voltage 1 : Normal battery charger operation form usb charger
4:1	usb_current	b0100	RW_SM	Sets the USB input current limit, if not GPIO controlled 0 : 94mA (USB low current,also if gpiox_iosf=12 and gpiox=0) 1 : 187mA 2 : 280mA 3 : 374mA 4 : 463mA (USB high current,also if gpiox_iosf=12 and gpiox=1) 5 : 623mA 6 : 727mA 7 : 841mA 8 : 998mA 9 : 1100mA 10 : 1395mA 11 : 1600mA 12 : 1740mA 13 : 1956mA 14 : 2230mA 15 : 2600mA
0	usb_chgEn	1	RW	ON/OFF control of USB charger input

Figure 158:
ChargerVoltageControl

Addr:81h		ChargerVoltageControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	vsup_min	b01	RW	Regulate down battery charging current on that level of Vsup during trickle charging and constant current charging, to prevent voltage drop on vsup 0 : 3.9V 1 : 4.2V 2 : 4.50V 3 : 4.70V
5:0	ChVoltEOC	b100011	RW	Sets the end-of-charge voltage level VCHOFF. Voltage levels for jeita_warm and normal state 0 : 3.50/3.50V 1 : 3.52/3.52V ... : ... 4 : 3.58/3.58V 5 : 3.50/3.60V 6 : 3.52/3.62V ... : ... 35 : 4.10/4.20V ... : ... 47-63 : 4.34/4.44V

Figure 159:
ChargerCurrentControl

Addr:82h		ChargerCurrentControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	eoc_current	0	RW	Sets eoc_current 0 : eoc current = trickle current 1 : eoc current = trickle current / 2
6	cc_lowlimit	1	RW	Sets the range of the charging current limit in constant current mode. 0 : Normal mode Current = CCurrent 1 : Low current mode Current = CCurrent / 2
5:2	ConstantCurrent	b0000	RW	Sets the charging current limit in constant current mode. Current values for low current(jeita_cool or cc_lowlimit) and normal mode 0 : 350/750mA 1 : 400/800mA 2 : 400/850mA 3 : 450/900mA 4 : 450/950mA 5 : 500/1000mA 6 : 500/1050mA 7 : 550/1100mA 8 : 550/1150mA 9 : 600/1200mA 10 : 600/1250mA 11 : 650/1300mA 12 : 650/1350mA 13 : 700/1400mA 14 : 700/1450mA 15 : 750/1500mA
1:0	TrickleCurrent	b01	RW	Sets the charging current limit in trickle current mode. Current values for low current(jeita_cool) and normal mode 0 : 60/60mA 1 : 60/120mA 2 : 60/180mA 3 : 120/240mA

Figure 160:
Chargerconfig

Addr:83h		Chargerconfig		
Bit	Bit Name	Default	Access	Bit Description
7	usb_combined	0	RW	Enables the combined mode for USB1 with 2 PMOS in parallel for highest efficiency 0 : Combined mode for USB1 disabled 1 : Combined mode for USB1 enabled
6	usb2_on	1	RW	USB1/USB2 charger selection 0 : USB1 enabled; USB2 disabled 1 : USB1 enabled; USB2 enabled; with higher priority on USB1
5	ChVoltResume	0	RW	Sets the resume voltage level VCHRES. 0 : 0.9666*VCHOFF (120mV @ 4.2V) 1 : 0.9444*VCHOFF (233mV @ 4.2V)
4:3	temp_sel	b00	RW	Selects temperature regulation of charging current (die temp.) 0 : 110degC 1 : 90degC 2 : 120degC 3 : 130degC
2:0	vsup_voltage	b101	RW	Voltage regulation of VSUP of the input current limiter 0 : 4.4V 1 : 4.5V 2 : 4.6V 3 : 4.7V 4 : 4.8V 5 : 4.9V 6 : 5.0V 7 : 5.5V

Figure 161:
Chargerconfig2

Addr:84h		Chargerconfig2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
6	ebat_enable	1	RW_SM	0 : External battery is disabled 1 : External battery is enabled
3	jeita_on	0	RW	0 : JEITA temperature supervision is OFF 1 : JEITA temperature supervision is ON
2	zero_temp_on	0	RW	0 : 0degC battery temperature supervision OFF 1 : 0degC battery temperature supervision ON
1	ntc_10k	0	RW	Select NTC resistor type 0 : 100kOhm 1 : 10kOhm
0	ntc_on	0	RW	ON/OFF control of battery ntc supervision 0 : Enabled 1 : Disabled

Figure 162:
Chargersupervision

Addr:85h		Chargersupervision		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Charging_1Hz_clk	0	RW	Sets the mode for the charging output status (gpioX_iosf==10) 0 : Normal operation: charging=1, not charging=0 1 : 1Hz blinking operation: charging=1Hz, not charging=0
6	ovprot_dis	1	RW_SM	Disables external overvoltage protection, function of XOFF pin 0 : Overvoltage protection enabled 1 : Overvoltage protection disabled
5	dcdc_chmode	1	RW_SM	Enables dcdc charger mode 0 : Linear charger mode enabled 1 : Step down charger enabled
4	charging_tmax	1	R_PUSH0	0 : Read: no timeout reached, Write: reset charger timeout counter 1 : Charging timeout reached and charging stopped
3:0	ch_timeout	b0000	RW	Sets the charger timeout timer 0 : OFF 1 : 0.5 hour 2 : 1 hour 3 : 1.5 hour 4 : 2 hour 5 : 2.5 hour 6 : 3 hour 7 : 3.5 hour 8 : 4 hour 9 : 4.5 hour 10 : 5 hour 11 : 5.5 hour 12 : 6 hour 13 : 6.5 hour 14 : 7 hour 15 : 7.5 hour

Figure 163:
ChargerStatus1

Addr:86h		ChargerStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	Nobat	0	RO	Bit is set if no battery has been detected
6	ChDet2	0	RO	Bit is set when external charge adapter has been detected on pin VCHGIN2
5	EOC	0	RO	Bit is set if End of charge state has been reached
4	CVM	0	RO	Bit is set if charger is operating in constant voltage mode
3	Trickle	0	RO	Bit is set, if charger is operating in trickle current. Vbat<2.9V
2	Resume	0	RO	Bit is set if Battery voltage is below resume level
1	CCM	0	RO	Bit is set if charger is operating in constant current mode
0	ChDet1	0	RO	Bit is set when external charge adapter has been detected on pin VCHGIN1

Figure 164:
ChargerStatus2

Addr:87h		ChargerStatus2		
Bit	Bit Name	Default	Access	Bit Description
7	usb_prot_ready_deb	0	RO	Bit indicates, that the USB input voltage protection pin xoff is precharged to a voltage>7.5V xoff is pull to GND if an overvoltage on VUSB is detected
6:4	temp_cond	0	RO	Indicates temperature condition 0h : Battery is in typical condition 1h : Battery is in cold condition (0degC condition - bat low) 2h : Battery is in cool condition 3h : Battery is in warm condition 4h : Battery is in hot condition (60degC condition - bat high)
3	batsw2_on	0	RO	Bit indicates the status of the battery switch batsw2_on batsw2_mode 0 0 External Battery switch open 0 1 External Battery switch open with ideal diode, ref_ok=1 1 0 Charging mode 1 1 External Battery switch closed
2	batsw2_mode	0	RO	
1	batsw_on	0	RO	Bit indicates the status of the battery switch batsw_on batsw_mode 0 0 Internal Battery switch open 0 1 Internal Battery switch open with ideal diode, ref_ok=1 1 0 Charging mode 1 1 Internal Battery switch closed
0	batsw_mode	0	RO	

Figure 165:
T1_adjust

Addr:88h		T1_adjust		
Bit	Bit Name	Default	Access	Bit Description
5:0	T1_adj	d11	RW	The adjust bits set the trigger point T1lim_upper for the temperature comparator according the specified beta of the NTC-resistor 00h-3fh : T1lim_upper=T1min+T1_adj*7mV

Figure 166:
T2_adjust

Addr:89h		T2_adjust		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:0	T2_adj	d9	RW	The adjust bits set the trigger point T2lim_upper for the temperature comparator according the specified beta of the NTC-resistor 00h-1fh : T2lim_upper=T2min+T2_adj*7mV

Figure 167:
T3_adjust

Addr:8ah		T3_adjust		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
4:0	T3_adj	d27	RW	The adjust bits set the trigger point T3lim_upper for the temperature comparator according the specified beta of the NTC-resistor 00h-1fh : T3lim_upper=T3min+T3_adj*7mV

Figure 168:
T4_adjust

Addr:8bh		T4_adjust		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
5:0	T4_adj	d43	RW	The adjust bits set the trigger point T4lim_upper for the temperature comparator according the specified beta of the NTC-resistor 00h-3fh : T4lim_upper=T4min+T4_adj*7mV

Figure 169:
T2_T1_hyst

Addr:8ch		T2_T1_hyst		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	T2_hyst	d10	RW	The T2_hyst bits set the hysteresis for the temperature comparator 0h-fh : T2lim_lower=T2lim_upper+(T2_hyst+3)*7mV
3:0	T1_hyst	d13	RW	The T1_hyst bits set the hysteresis for the temperature comparator 0h-fh : T1lim_lower=T1lim_upper+(T1_hyst+3)*7mV

Figure 170:
T4_T3_hyst

Addr:8dh		T4_T3_hyst		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	T4_hyst	d8	RW	The T4_hyst bits set the hysteresis for the temperature comparator 0h-fh : T4lim_lower=T4lim_upper+(T4_hyst+3)*7mV
3:0	T3_hyst	d9	RW	The T3_hyst bits set the hysteresis for the temperature comparator 0h-fh : T3lim_lower=T3lim_upper+(T3_hyst+3)*7mV

Figure 171:
LockRegister

Addr:8eh		LockRegister		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
1:0	reg_lock	b00	RW	Enables lock of Regulator voltages Bits can only be set. Reset only with full reset cycle 0 : No lock 1 : Lock of voltage of LDOs (LDO1..8_vsel) (all bits) and voltage of StepDownBits(sd1..4_vsel) [5:6] only 2 : Lock voltage of StepDownbits 5:6 only (no LDOs) 3 : Lock voltage of StepDowns (all bits) and LDOs (all bits).
2	charger_lock	0	RW	Enables lock of the following charger registers: 81h,82h,83h, Chargervoltagecontrol, Chargercurrentcontrol, Chargerconfig Bits can only be set. Reset only with full reset cycle

Figure 172:
ASIC_ID1

Addr:90h		ASIC_ID1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	ID1	h8d	RO	

Figure 173:
ASIC_ID2

Addr:91h		ASIC_ID2		
Bit	Bit Name	Default	Access	Bit Description
3:0	revision	b0011	RO	For chips marked 2v2 (metal fuse!!!)

Figure 174:
SpareRegister1

Addr:9bh		SpareRegister1		
Bit	Bit Name	Default	Access	Bit Description
7:0	sparereg1	0	RW_SM	

Figure 175:
Fuse7

Addr:a7h		Fuse7		
Bit	Bit Name	Default	Access	Bit Description
7	del_time	b0	RW	Start sequence: Time to wait between turning ON RegX and RegX+1.(1) 0 : 1 or 4 ms 1 : 4 or 12 ms
6	unique_id	b0	RW	0 : Disable unique ID 1 : Enable unique ID: Fuse26..31 are used for UID and not for startup
5	sequ_on	b0	RW	Start sequence 0 : Regulators are OFF after startup 1 : Turn ON regulators (see Fuse12 .. Fuse31)
4:3	tksel	b00	RW	
2	sdmph_clk_div_0	b0	RW	
1:0	chg_eoc_v	b00	RW	

Note(s) and/or Footnote(s):

1. RegX_gpio_sel can shorten time or use GPIO1 or GPIO2 as timer.

Figure 176:
Fuse8

Addr:a8h		Fuse8		
Bit	Bit Name	Default	Access	Bit Description
7	sd3_slave	b0	RW	Enables slave mode of SD3 0 : Normal mode of SD3 1 : SD3 is slave of SD2.
6	sd3_fsel	b0	RW	Selects between high and low frequency range 0 : 2 or 3MHz frequency (selectable by sd3_frequ) 1 : 3 or 4MHz frequency (selectable by sd3_frequ)
5	sd2_fsel	b0	RW	Selects between high and low frequency range 0 : 2 or 3MHz frequency (selectable by sd2_frequ) 1 : 3 or 4MHz frequency (selectable by sd2_frequ)
4	sd2_slave	b0	RW	Enables slave mode of SD2 0 : Normal mode of SD2 1 : SD2 is slave of SD1.
3	sd4_fast	b0	RW	Selects a faster regulation mode for SD4 suitable for larger load changes. 0 : Normal mode, Cext=20uF 1 : Fast mode, Cext=40uF required
2	sd3_fast	b0	RW	Selects a faster regulation mode for SD3 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
1	sd2_fast	b0	RW	Selects a faster regulation mode for SD2 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required
0	sd1_fast	b0	RW	Selects a faster regulation mode for SD1 suitable for larger load changes. 0 : Normal mode, Cext=10uF 1 : Fast mode, Cext=22uF required

Figure 177:
Fuse9

Addr:a9h		Fuse9		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	auto_off	b0	RW	Defines startup behavior at first battery insertion 0 : Startup of chip if VBAT>ResVoltRise 1 : Enter power OFF mode (Startup with ON key or charger insertion)
6	chg_pwr_off_en	0	RW_SM	Enable power OFF mode, if charger is detected 0 : Exit of Power OFF mode, if charger is detected (level) 1 : Exit of Power OFF mode, if charger is attached or detached
5:4	res_timer	b00	RW	Set RESTime, after the last regulator has started 0 : RESTIME=10ms 1 : RESTIME=50ms 2 : RESTIME=100ms 3 : RESTIME=150ms
3:1	ResVoltRise	b000	RW	This value determines the reset level ResVoltRise for rising VBAT. ResVoltFall is set to ResVoltRise-2 by default 0 : 2.7V 1 : 2.9V 2 : 3.1V 3 : 3.2V 4 : 3.3V 5 : 3.4V 6 : 3.5V 7 : 3.6V
0	i2c_deva_bit1	b0	RW	

Figure 178:
Fuse10

Addr:aah		Fuse10		
Bit	Bit Name	Default	Access	Bit Description
7:4	usb2_current	b0000	RW	Sets the USB2 input current limit 0 : 94mA 1 : 187mA 2 : 280mA 3 : 374mA 4 : 463mA 5 : 623mA 6 : 727mA 7 : 841mA 8 : 998mA 9 : 1100mA 10 : 1395mA 11 : 1600mA 12 : 1740mA 13 : 1956mA 14 : 2230mA 15 : 2600mA
3:0	usb_current	b0000	RW	Sets the USB input current limit, if not GPIO controlled 0 : 94mA (USB low current,also if gpiox_iosf=12 and gpiox=0) 1 : 187mA 2 : 280mA 3 : 374mA 4 : 463mA (USB high current,also if gpiox_iosf=12 and gpiox=1) 5 : 623mA 6 : 727mA 7 : 841mA 8 : 998mA 9 : 1100mA 10 : 1395mA 11 : 1600mA 12 : 1740mA 13 : 1956mA 14 : 2230mA 15 : 2600mA

Figure 179:
Fuse11

Addr:abh		Fuse11		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	power_off_at_vsuplow	b0	RW	Switch ON Power OFF mode if low VSUP is detected during active or standby mode (Pin ON= low and bit auto_off=0) 0 : If low battery is detected, continuously monitor battery voltage and startup if battery voltage is above ResVoltrise 1 : If low battery is detected, enter power OFF mode
6	ovprot_dis	b0	RW	Enables external overvoltage protection, function of xoff 0 : Overvoltage protection disabled 1 : Overvoltage protection enabled
5	on_reset_delay	b0	RW	Sets the ONKEY/ENx longpress delay time 0 : 8 sec 1 : 4 sec if onkey_lpress_reset=0; ONKEY/ENx longpress is disabled if onkey_lpress_reset=1
4	onkey_lpress_reset	b0	RW	Selects behavior for ONKEY/ENx longpress 0 : Change to power_off mode 1 : Reset cycle started if on_reset_delay=0; ONKEY/ENx longpress is disabled if on_reset_delay=1
3	dcdc_chmode	b0	RW	Selects between linear and step down charger 0 : Linear charger enabled 1 : Step down charger enabled
2	SupResEn	b0	RW	0 : A reset is generated if VSUP falls below 2.7V.(1) 1 : A reset is generated if VSUP falls below ResVoltFall
1	gpio12_in_en	b0	RW	Enables input_pulldown for gpio1,gpio2 if this bit is set 0 : gpio1_mode and gpio2_mode are default (b011) 1 : gpio1_mode and gpio2_mode set to (b101) input with pulldown
0	dis_bypass	b0	RW	Used in charger FSM

Note(s) and/or Footnote(s):

1. If VSUP falls below ResVoltFall only an interrupt is generated (if enabled) and the uProcessor can shut down the system

Figure 180:
Fuse12

Addr:ach		Fuse12		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	Reg4_gpio_sel	b00	RW	See Reg1_gpio_sel
5:4	Reg3_gpio_sel	b00	RW	See Reg1_gpio_sel
3:2	Reg2_gpio_sel	b00	RW	See Reg1_gpio_sel
1:0	Reg1_gpio_sel	b00	RW	Waiting period before setting regulator[Reg1_select] = reg1_V. Power-down uses same timing (Wait time after turning OFF). 0 : No delay: Wait 0 ms. Then set Reg1 voltage. 1 : Delay: Wait 1 ms (del_time=1: 4 ms). Then set Reg1 voltage. 2 : Delay: Wait 4 ms (del_time=1: 12 ms). Then set Reg1 voltage. 3 : GPIO3 control: Wait 0 ms. Then set Reg1 voltage. Set gpio_ctrl_xxx=3 (Reg1 controlled by GPIO3)

Figure 181:
Fuse13

Addr:adh		Fuse13		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	Reg2_select	b0000	RW	
3:0	Reg1_select	b0000	RW	Selects Regulator address for startup sequence(Slot0) Address 00..0Fh selectable (fill up empty timeslots with the last regulator) 00h : SD1 .. : .. 03h : SD4 04h : LDO1 .. : .. 0Bh : LDO8 0Ch : GPIO1 .. : .. 0Fh : GPIO4

Figure 182:
Fuse14

Addr:aeh		Fuse14		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg1_V	b00000000	RW	

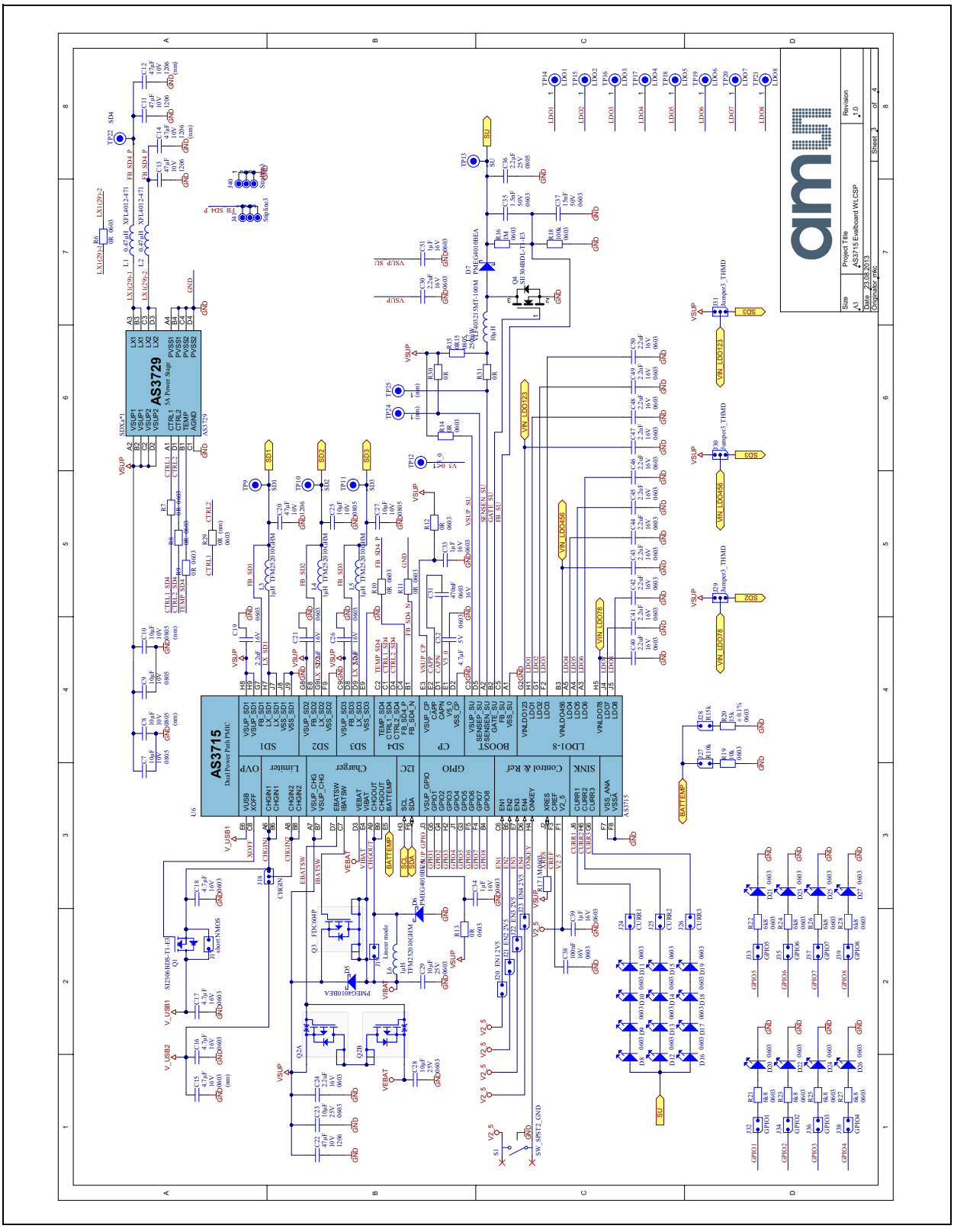
Figure 183:
Fuse30

Addr:beh		Fuse30		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	ibattemp10k	b0000	RW	BATTEMP NTC current for correction calculation Fh: 133.8uA Eh: 136.4uA Dh: 139.0uA Ch: 141.6uA Bh: 144.2uA Ah: 146.8uA 9h: 149.4uA 0h: 152.0uA 1h: 154.6uA 2h: 157.2uA 3h: 159.8uA 4h: 162.4uA 5h: 165.0uA 6h: 167.6uA 7h: 170.2uA 8h: n/a
3:0	Reg11_select	b0000	RW	

Application Information

Application Schematics

Figure 184:
Application Schematic



Application Schematic: Shows a basic connections and external components

PCB Routing Recommendations

Internal DCDC

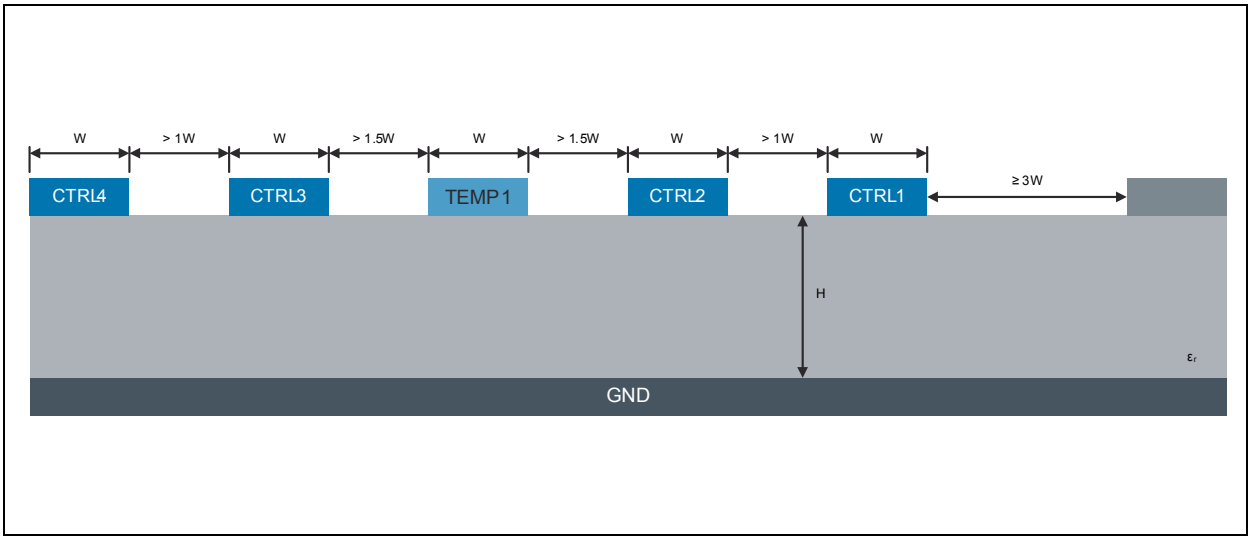
Attention should be paid to the routing of the VSUP, LX and GND traces of the DCDC converter.

- Keep the VSUP traces to the input capacitor as short as possible. Do not use vias for this connection.
- Make a common ground area for the input cap, output cap and PVSS terminal of the DCDC. Connect this ground area with vias to the system ground plane.
- Use short wide traces for LX node. If you need to set vias, use it on the LX trace and not on the capacitor connections.

Power Stage Connections

To avoid cross talk to other lines a minimum spacing of minimum 3W should be kept. For a proper DCDC operation it's recommended to avoid routing other clock traces being routed in parallel (also on other layers) to the control lines.

Figure 185:
PCB Control Line Routing

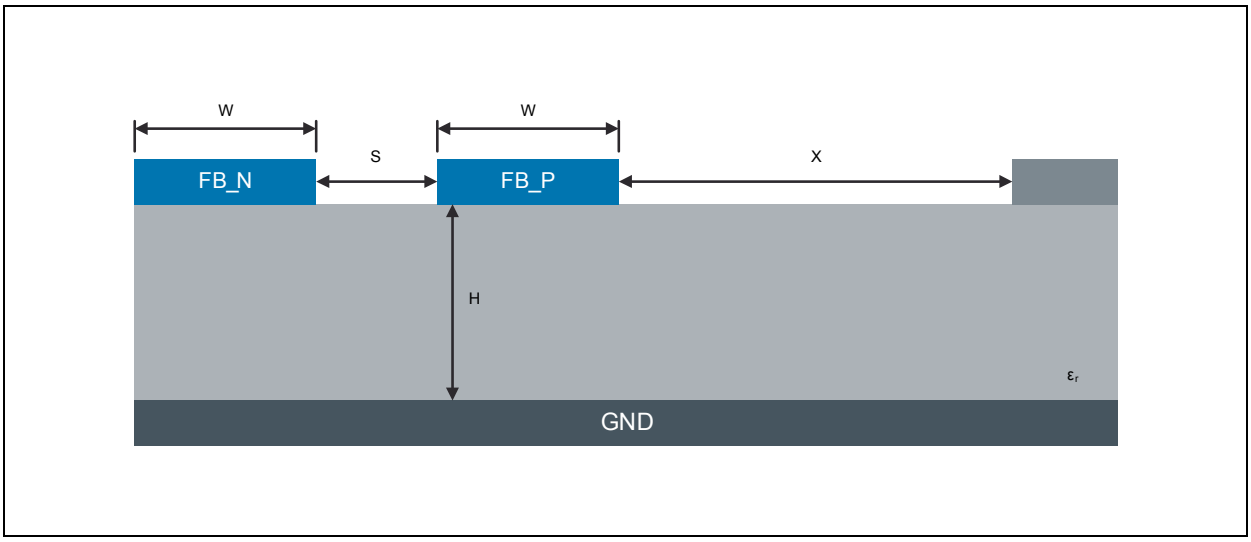


PCB Differential Feedback Routing: Shows an example PCB routing for the control lines of the multiphase controllers.

CTRL1&2, are not interfering with each other as they are running at 180° phase shift. They can be routed with a minimum spacing. The TEMP lines should be used as "guard traces" to other control line pairs (e.g. CTRL3&4 or CTRL 5&6 or CTRL 7&8) as well as to other sensitive or clock traces on the PCB. A minimum spacing of >1.5W should be used as spacing between TEMP and CTRL traces.

To minimize the cross talk of these clock lines, the width of the traces (W) should be the minimum acceptable width for manufacturing (e.g. 4mil).The differential feedback lines are less critical, nevertheless to ensure a good coupling between the differential lines and a low coupling to other traces and ground planes its recommended to have: S<W, S<H, X≥2W and 2S

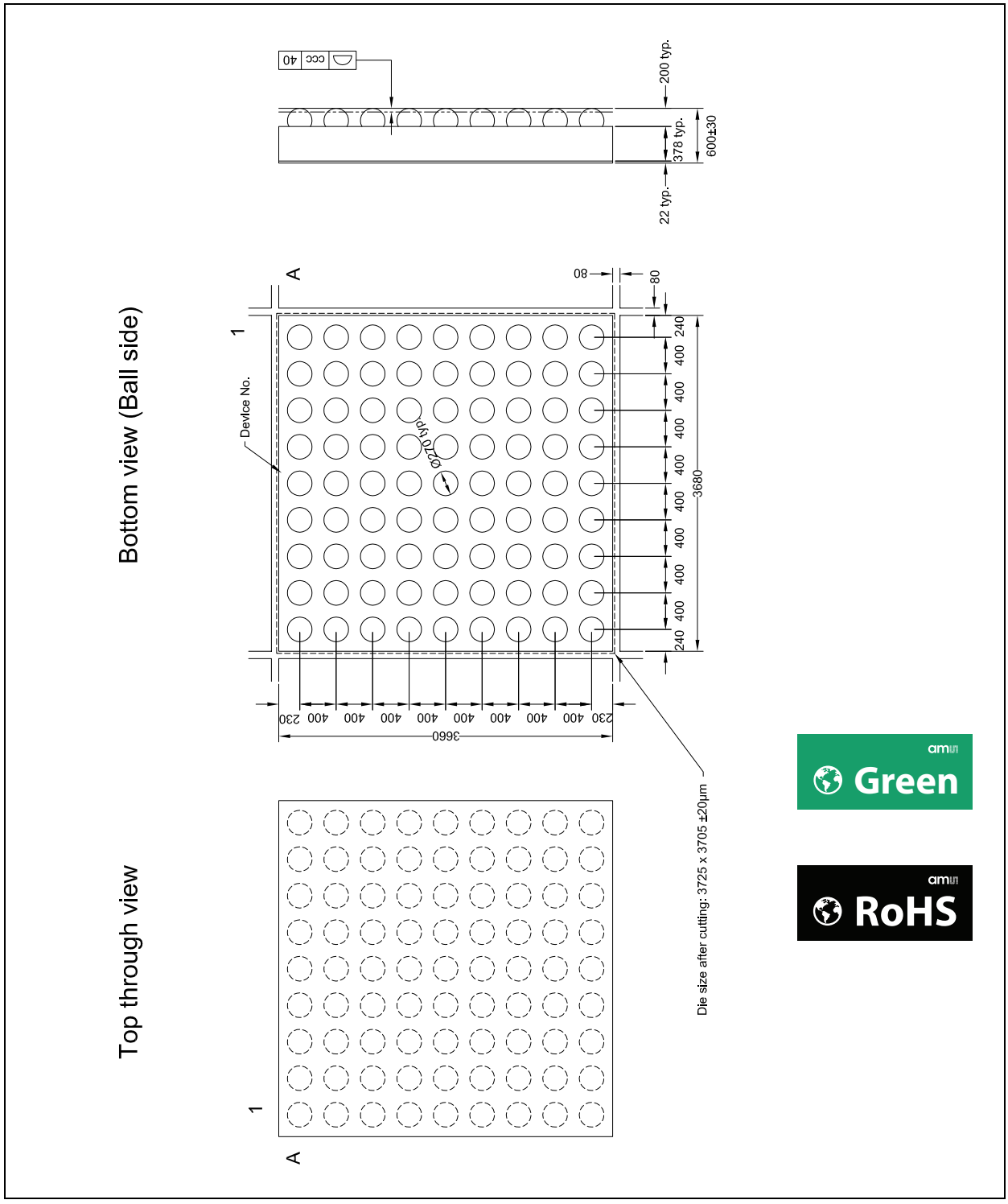
Figure 186:
PCB Differential Feedback Routing



PCB Differential Feedback Routing: Shows an example PCB routing for the differential feedback lines of the multiphase controllers.

Package Drawings & Markings

Figure 187:
Package Drawing (CSP)

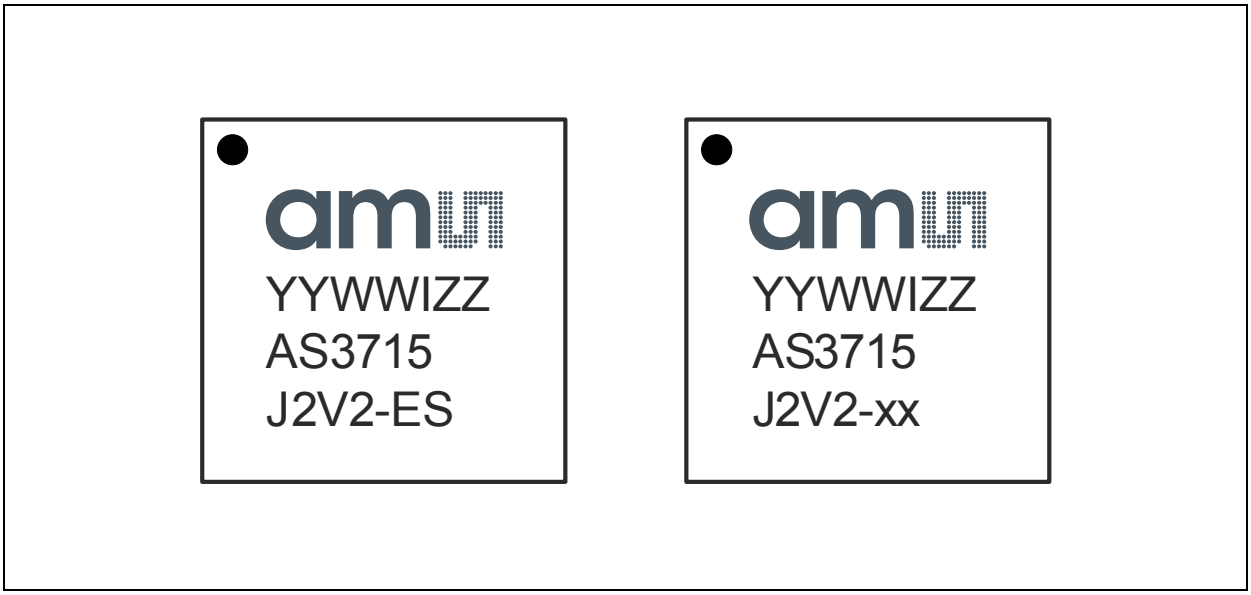


Package Drawings: Shows the outline dimensions of the CSP81 package

Note(s) and/or Footnote(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. All dimensions are in µm

Figure 188:
Marking



Marking: Shows the package marking for different product versions.

Figure 189:
Package Code

YY	WW	I	ZZ
Year	Manufacturing week	Plant identifier	Free choice

Package Code: Shows the coding of the package marking.

Figure 190:
Start-up Revision Code

xx	Sequence
ES	Engineering samples, no sequence programmed or sequence programmed on request
00	Standard programming (no sequence programmed)
xx	Other customer specified sequence programmed during production test

Start-up Revision Code: Shows the coding of the different startup sequences.

Ordering & Contact Information

Figure 191:
Ordering Information

Ordering Code	Marking	OTP programming	Delivery Form	Package
AS3715-BWLW-ES	J2V2-ES	Sequence programmable on request	WafflePack	81-pin WL-CSP 0.4mm pitch
AS3715-BWLT-xx	J2V2-xx	Other customer specified programming	Tape & Reel	81-pin WL-CSP 0.4mm pitch

Ordering Information: Shows the ordering information for the different product versions

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Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
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Revision Information

Changes from 0-02 (2014-Sep-09) to current revision 1-00 (2014-Sep-10)	Page (1)
Initial version for release	

Note(s) and/or Footnote(s):

1. Page numbers for the previous version may differ from page numbers in the current revision.

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