



**THE DATASHEET OF  
AT28C17-20JI**



## Features

- **Fast Read Access Time - 150 ns**
- **Fast Byte Write - 200  $\mu$ s or 1 ms**
- **Self-Timed Byte Write Cycle**
  - Internal Address and Data Latches
  - Internal Control Timer
  - Automatic Clear Before Write
- **Direct Microprocessor Control**
  - DATA POLLING
  - READY/BUSY Open Drain Output
- **Low Power**
  - 30 mA Active Current
  - 100  $\mu$ A CMOS Standby Current
- **High Reliability**
  - Endurance:  $10^4$  or  $10^5$  cycles
  - Data Retention: 10 years
- **5 V  $\pm$  10% Supply**
- **CMOS & TTL Compatible Inputs and Outputs**
- **JEDEC Approved Byte Wide Pinout**
- **Full Military, Commercial, and Industrial Temperature Ranges**

**16K (2K x 8)**  
**CMOS**  
**E<sup>2</sup>PROM**

## Description

The AT28C17 is a low-power, high-performance Electrically Erasable and Programmable Read Only Memory with easy to use features. The AT28C17 is a 16K memory organized as 2,048 words x 8 bits. The device is manufactured with Atmel's reliable nonvolatile CMOS technology.

The AT28C17 is accessed like a static RAM for the read or write cycles without the need of external components. During a byte write, the address and data are latched internally, freeing the microprocessor address and data bus for other operations. Following the initiation of a write cycle, the device will go to a busy state and automatically clear and write the latched data using an internal control timer. The device includes two methods for detecting the end of a write cycle, level detection of RDY/BUSY and DATA polling of I/O7. Once the end of a write cycle has been detected, a new access for a read or a write can begin.

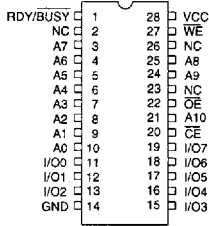
The CMOS technology offers fast access times of 150 ns at low power dissipation. When the chip is deselected the standby current is less than 100  $\mu$ A.

Atmel's 28C17 has additional features to ensure high quality and manufacturability. The device utilizes error correction internally for extended endurance and for improved data retention characteristics. An extra 32 bytes of E<sup>2</sup>PROM are available for device identification or tracking.

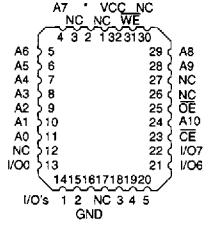
## Pin Configurations

Pin Name	Function
A0 - A10	Addresses
CE	Chip Enable
OE	Output Enable
WE	Write Enable
I/O0 - I/O7	Data Inputs/Outputs
RDY/BUSY	Ready/Busy Output
NC	No Connect

CERDIP, PDIP, SOIC  
 Top View



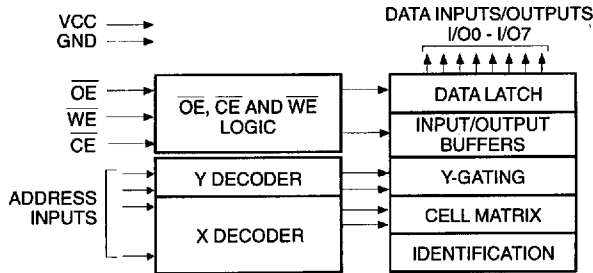
PLCC  
 Top View



\* = RDY/BUSY  
 Note: PLCC package pins 1 and 17 are DON'T CONNECT.



## Block Diagram



## Absolute Maximum Ratings\*

Temperature Under Bias.....	-55°C to +125°C
Storage Temperature.....	-65°C to +150°C
All Input Voltages (including N.C. Pins) with Respect to Ground .....	-0.6 V to +6.25 V
All Output Voltages with Respect to Ground .....	-0.6 V to $V_{CC} + 0.6 V$
Voltage on $\overline{OE}$ and A9 with Respect to Ground .....	-0.6 V to +13.5 V

\*NOTICE: Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## Device Operation

**READ:** The AT28C17 is accessed like a Static RAM. When  $\overline{CE}$  and  $\overline{OE}$  are low and  $\overline{WE}$  is high, the data stored at the memory location determined by the address pins is asserted on the outputs. The outputs are put in a high impedance state whenever  $\overline{CE}$  or  $\overline{OE}$  is high. This dual line control gives designers increased flexibility in preventing bus contention.

**BYTE WRITE:** Writing data into the AT28C17 is similar to writing into a Static RAM. A low pulse on the  $\overline{WE}$  or  $\overline{CE}$  input with  $\overline{OE}$  high and  $\overline{CE}$  or  $\overline{WE}$  low (respectively) initiates a byte write. The address location is latched on the last falling edge of  $\overline{WE}$  (or  $\overline{CE}$ ); the new data is latched on the first rising edge. Internally, the device performs a self-clear before write. Once a byte write has been started, it will automatically time itself to completion. Once a programming operation has been initiated and for the duration of twc, a read operation will effectively be a polling operation.

**FAST BYTE WRITE:** The AT28C17E offers a byte write time of 200  $\mu s$  maximum. This feature allows the entire device to be rewritten in 0.4 seconds.

**READY/ $\overline{BUSY}$ :** Pin 1 is an open drain READY/ $\overline{BUSY}$  output that can be used to detect the end of a write cycle. RDY/ $\overline{BUSY}$  is actively pulled low during the write cycle and is released at the completion of the write. The open drain connec-

tion allows for OR-tying of several devices to the same RDY/ $\overline{BUSY}$  line.

**DATA POLLING:** The AT28C17 provides  $\overline{DATA POLLING}$  to signal the completion of a write cycle. During a write cycle, an attempted read of the data being written results in the complement of that data for I/O7 (the other outputs are indeterminate). When the write cycle is finished, true data appears on all outputs.

**WRITE PROTECTION:** Inadvertent writes to the device are protected against in the following ways. (a)  $V_{CC}$  sense— if  $V_{CC}$  is below 3.8 V (typical) the write function is inhibited. (b)  $V_{CC}$  power on delay— once  $V_{CC}$  has reached 3.8 V the device will automatically time out 5 ms (typical) before allowing a byte write. (c) Write Inhibit— holding any one of  $\overline{OE}$  low,  $\overline{CE}$  high or  $\overline{WE}$  high inhibits byte write cycles.

**CHIP CLEAR:** The contents of the entire memory of the AT28C17 may be set to the high state by the CHIP CLEAR operation. By setting  $\overline{CE}$  low and  $\overline{OE}$  to 12 volts, the chip is cleared when a 10 msec low pulse is applied to  $\overline{WE}$ .

**DEVICE IDENTIFICATION:** An extra 32 bytes of E<sup>2</sup>PROM memory are available to the user for device identification. By raising A9 to  $12 \pm 0.5 V$  and using address locations 7E0H to 7FFH the additional bytes may be written to or read from in the same manner as the regular memory array.

## D.C. and A.C. Operating Range

		AT28C17-15	AT28C17-20	AT28C17-25
Operating Temperature (Case)	Com.	0°C - 70°C	0°C - 70°C	0°C - 70°C
	Ind.	-40°C - 85°C	-40°C - 85°C	-40°C - 85°C
	Mil.	-55°C - 125°C	-55°C - 125°C	-55°C - 125°C
V <sub>CC</sub> Power Supply		5 V ± 10%	5 V ± 10%	5V±10%

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## Operating Modes

Mode	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O
Read	V <sub>IL</sub>	V <sub>IL</sub>	V <sub>IH</sub>	D <sub>OUT</sub>
Write <sup>(2)</sup>	V <sub>IL</sub>	V <sub>IH</sub>	V <sub>IL</sub>	D <sub>IN</sub>
Standby/Write Inhibit	V <sub>IH</sub>	X <sup>(1)</sup>	X	High Z
Write Inhibit	X	X	V <sub>IH</sub>	
Write Inhibit	X	V <sub>IL</sub>	X	
Output Disable	X	V <sub>IH</sub>	X	High Z
Chip Erase	V <sub>IL</sub>	V <sub>H</sub> <sup>(3)</sup>	V <sub>IL</sub>	High Z

Notes: 1. X can be V<sub>IL</sub> or V<sub>IH</sub>.

2. Refer to A.C. Programming Waveforms.

3. V<sub>H</sub> = 12.0 V ± 0.5 V.

## D.C. Characteristics

Symbol	Parameter	Condition	Min	Max	Units
I <sub>LI</sub>	Input Load Current	V <sub>IN</sub> = 0 V to V <sub>CC</sub> + 1 V		10	μA
I <sub>LO</sub>	Output Leakage Current	V <sub>I/O</sub> = 0 V to V <sub>CC</sub>		10	μA
I <sub>SB1</sub>	V <sub>CC</sub> Standby Current CMOS	$\overline{CE} = V_{CC} - 0.3 \text{ V to } V_{CC} + 1.0 \text{ V}$		100	μA
I <sub>SB2</sub>	V <sub>CC</sub> Standby Current TTL	$\overline{CE} = 2.0 \text{ V to } V_{CC} + 1.0 \text{ V}$	Com.	2	mA
			Ind., Mil.	3	mA
I <sub>CC</sub>	V <sub>CC</sub> Active Current A.C.	f = 5 MHz; I <sub>OUT</sub> = 0 mA $\overline{CE} = V_{IL}$	Com.	30	mA
			Ind., Mil.	45	mA
V <sub>IL</sub>	Input Low Voltage			0.8	V
V <sub>IH</sub>	Input High Voltage		2.0		V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 2.1 mA = 4.0 for RDY/BUSY		.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -400 μA	2.4		V

## Pin Capacitance (f = 1 MHz, T = 25°C)<sup>(1)</sup>

	Typ	Max	Units	Conditions
C <sub>IN</sub>	4	6	pF	V <sub>IN</sub> = 0 V
C <sub>OUT</sub>	8	12	pF	V <sub>OUT</sub> = 0 V

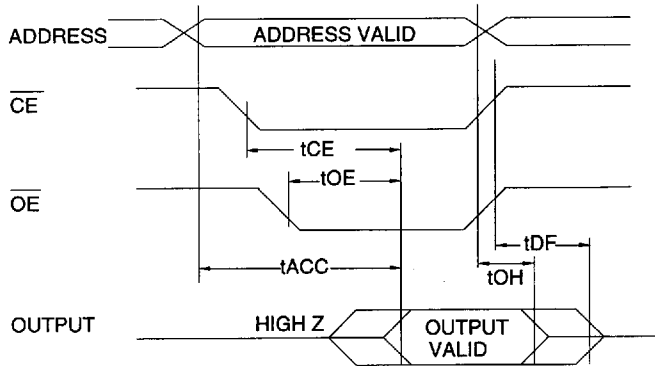
Note: 1. This parameter is characterized and is not 100% tested.



## A.C. Read Characteristics

Symbol	Parameter	AT28C17-15		AT28C17-20		AT28C17-25		Units
		Min	Max	Min	Max	Min	Max	
$t_{ACC}$	Address to Output Delay		150		200		250	ns
$t_{CE}^{(1)}$	$\overline{CE}$ to Output Delay		150		200		250	ns
$t_{OE}^{(2)}$	$\overline{OE}$ to Output Delay	10	70	10	80	10	100	ns
$t_{DF}^{(3,4)}$	$\overline{CE}$ or $\overline{OE}$ High to Output Float	0	50	0	55	0	60	ns
$t_{OH}$	Output Hold from $\overline{OE}$ , $\overline{CE}$ or Address, whichever occurred first	0		0		0		ns

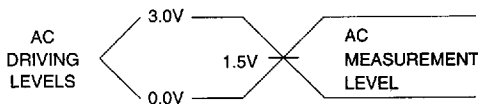
## A.C. Read Waveforms<sup>(1,2,3,4)</sup>



### Notes:

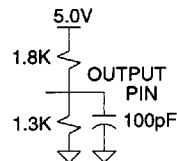
- $\overline{CE}$  may be delayed up to  $t_{ACC} - t_{CE}$  after the address transition without impact on  $t_{ACC}$ .
- $\overline{OE}$  may be delayed up to  $t_{CE} - t_{OE}$  after the falling edge of  $\overline{CE}$  without impact on  $t_{CE}$  or by  $t_{ACC} - t_{OE}$  after an address change without impact on  $t_{ACC}$ .
- $t_{DF}$  is specified from  $\overline{OE}$  or  $\overline{CE}$  whichever occurs first ( $C_L = 5$  pF).
- This parameter is characterized and is not 100% tested.

## Input Test Waveforms and Measurement Level



$t_R, t_F < 20$  ns

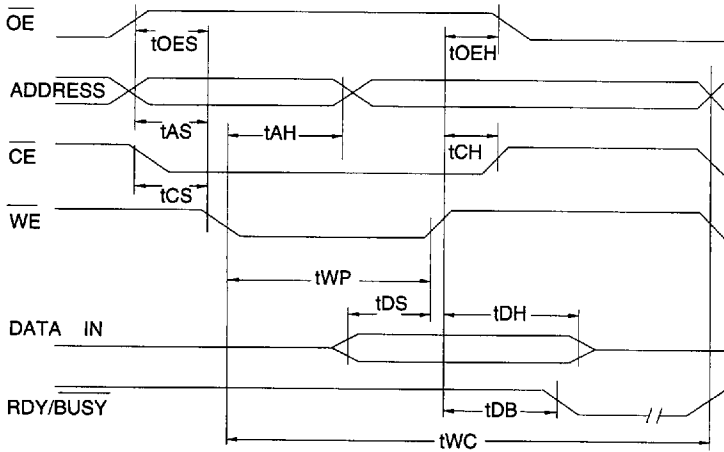
## Output Test Load



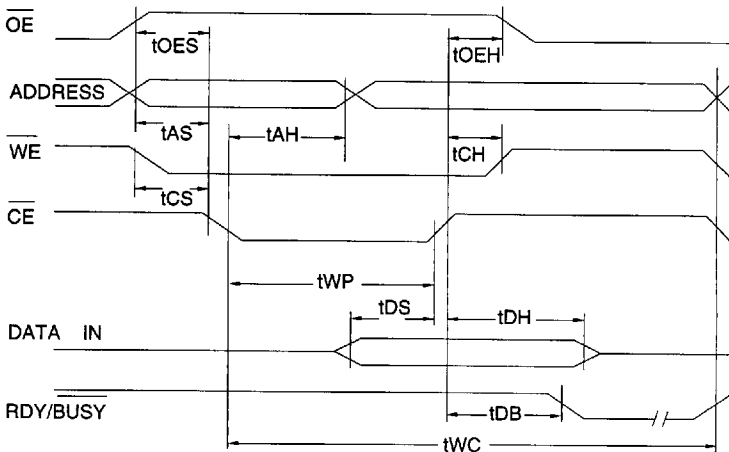
**A.C. Write Characteristics**

Symbol	Parameter	Min	Typ	Max	Units
tAS, tOES	Address, $\overline{OE}$ Set-up Time	10			ns
tAH	Address Hold Time	50			ns
tWP	Write Pulse Width ( $\overline{WE}$ or $\overline{CE}$ )	100		1000	ns
tDS	Data Set-up Time	50			ns
tDH, tOEH	Data, $\overline{OE}$ Hold Time	10			ns
tCS, tCH	$\overline{CE}$ to $\overline{WE}$ and $\overline{WE}$ to $\overline{CE}$ Set-up and Hold Time	0			ns
tDB	Time to Device Busy			50	ns
tWC	Write Cycle Time	AT28C17	0.5	1.0	ms
		AT28C17E	100	200	$\mu$ s

**A.C. Write Waveforms-  $\overline{WE}$  Controlled**



**A.C. Write Waveforms-  $\overline{CE}$  Controlled**

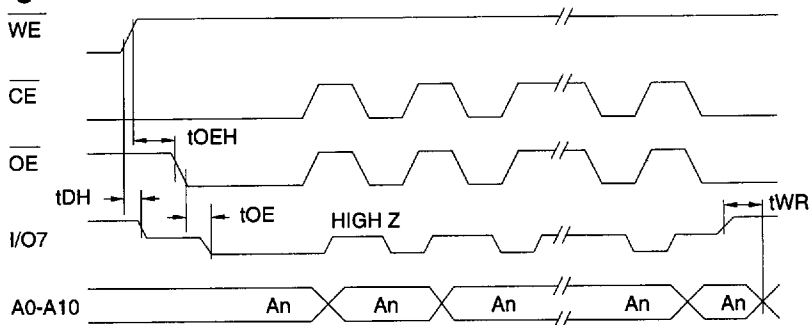


## Data Polling Characteristics <sup>(1)</sup>

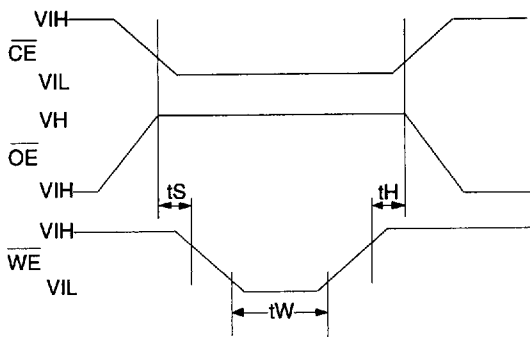
Symbol	Parameter	Min	Typ	Max	Units
t <sub>DH</sub>	Data Hold Time	10			ns
t <sub>OEH</sub>	$\overline{\text{OE}}$ Hold Time	10			ns
t <sub>OE</sub>	$\overline{\text{OE}}$ to Output Delay <sup>(2)</sup>				ns
t <sub>WR</sub>	Write Recovery Time	0			ns

Notes: 1. These parameters are characterized and not 100% tested.  
 2. See A.C. Read Characteristics.

## Data Polling Waveforms

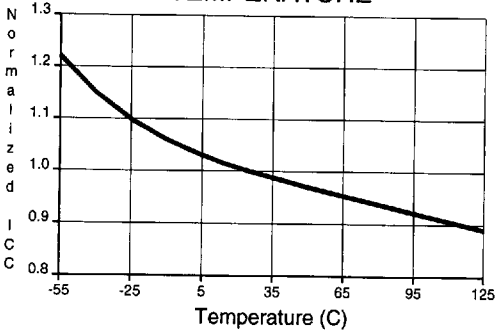


## Chip Erase Waveforms

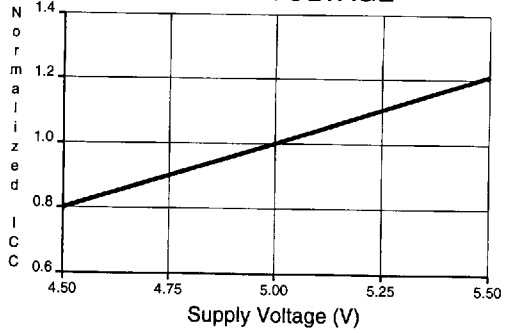


t<sub>S</sub> = t<sub>H</sub> = 1  $\mu$ sec (min.)  
 t<sub>W</sub> = 10 msec (min.)  
 V<sub>H</sub> = 12.0 V  $\pm$  0.5 V

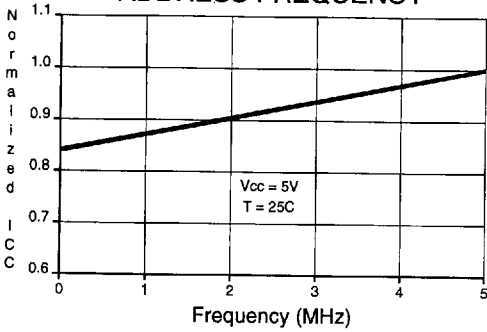
NORMALIZED SUPPLY CURRENT vs. TEMPERATURE



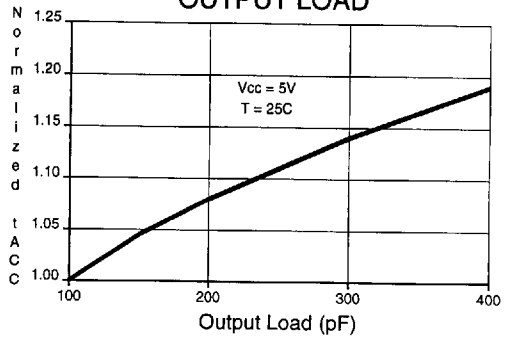
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



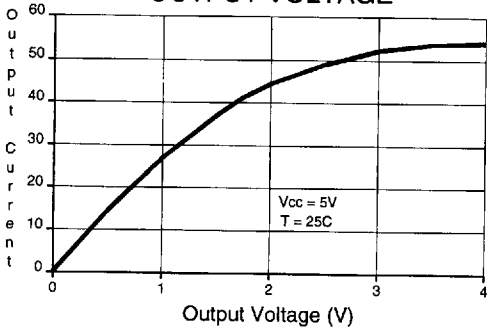
NORMALIZED SUPPLY CURRENT vs. ADDRESS FREQUENCY



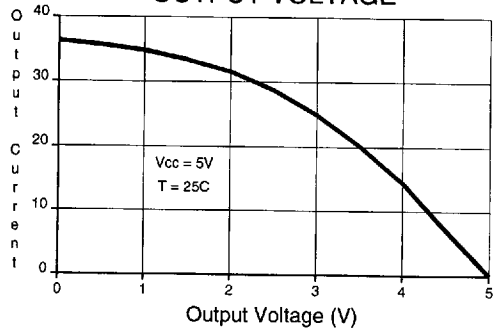
NORMALIZED ACCESS TIME vs. OUTPUT LOAD



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE





## Ordering Information<sup>(1)</sup>

t <sub>ACC</sub> (ns)	I <sub>CC</sub> (mA)		Ordering Code	Package	Operation Range
	Active	Standby			
150	30	0.1	AT28C17(E)-15DC	28D6	Commercial (0°C to 70°C)
			AT28C17(E)-15JC	32J	
			AT28C17(E)-15PC	28P6	
			AT28C17(E)-15SC	28S	
150	45	0.1	AT28C17(E)-15DI	28D6	Industrial (-40°C to 85°C)
			AT28C17(E)-15JI	32J	
			AT28C17(E)-15PI	28P6	
			AT28C17(E)-15SI	28S	
			AT28C17(E)-15DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
200	30	0.1	AT28C17(E)-20DC	28D6	Commercial (0°C to 70°C)
			AT28C17(E)-20JC	32J	
			AT28C17(E)-20PC	28P6	
			AT28C17(E)-20SC	28S	
200	45	0.1	AT28C17(E)-20DI	28D6	Industrial (-40°C to 85°C)
			AT28C17(E)-20JI	32J	
			AT28C17(E)-20PI	28P6	
			AT28C17(E)-20SI	28S	
			AT28C17(E)-20DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)
250	30	0.1	AT28C17(E)-25DC	28D6	Commercial (0°C to 70°C)
			AT28C17(E)-25JC	32J	
			AT28C17(E)-25PC	28P6	
			AT28C17(E)-25SC	28S	
			AT28C17-W	DIE	
250	45	0.1	AT28C17(E)-25DI	28D6	Industrial (-40°C to 85°C)
			AT28C17(E)-25JI	32J	
			AT28C17(E)-25PI	28P6	
			AT28C17(E)-25SI	28S	
			AT28C17(E)-25DM/883	28D6	Military/883C Class B, Fully Compliant (-55°C to 125°C)

Note: 1. See Valid Part Number table below.

**Valid Part Numbers**

The following table lists standard Atmel products that can be ordered.

Device Numbers	Speed	Package and Temperature Combinations
AT28C17	15	DC, JC, JI, PC, PI, SC, SI, DM/883
AT28C17E	15	DC, JC, JI, PC, PI, SC, SI, DM/883
AT28C17	20	DC, JC, JI, PC, PI, SC, SI, DM/883
AT28C17E	20	DC, JC, JI, PC, PI, SC, SI, DM/883
AT28C17	25	DC, JC, JI, PC, PI, SC, SI, DM/883
AT28C17E	25	DC, JC, JI, PC, PI, SC, SI, DM/883



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Package Type	
28D6	28 Lead, 0.600" Wide, Non-Windowed, Ceramic Dual Inline Package (Cerdip)
32J	32 Lead, Plastic J-Leaded Chip Carrier (PLCC)
28P6	28 Lead, 0.600" Wide, Plastic Dual Inline Package (PDIP)
28S	28 Lead, 0.300" Wide, Plastic Gull Wing, Small Outline (SOIC)
W	Die
Options	
Blank	Standard Device: Endurance = 10K Write Cycles; Write Time = 1 ms
E	High Endurance Option: Endurance = 100K Write Cycles; Write Time = 200 $\mu$ s









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