Power Supply IC Series for TFT-LCD Panels

4-channel System Power Supply + Gamma Buffer Amp IC

BD8150KVT

No.09035EBT03

●Description

The BD8150KVT is a system power supply IC that offers a 4-channel power supply with 10 gamma correction output channels and VCOM. The DC/DC block can be switched between step-up and step-down and supports both 5V and 12V input.

●Features

1) Multi-channel power supply with two DC/DC converter controller channels and two charge pump channels
2) 10channel gamma correction Buffer Amp output and 1channel VCOM
3) High reference voltage accuracy: ±1 %
4) Oscillating frequency: 1MHz
5) Built-in UVLO (Under Voltage Lockout) and output short-circuit protection circuits
6) Standby current of 0μA (Typ.)
7) Controllable start up sequence
8) TQFP64V package

●Applications

Power supply for LCD monitors and LCD TVs

●Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power supply voltage	Vcc	15	V
Regulator power supply voltage	REGVcc	15	V
Driver power supply voltage	PVcc	15	V
Junction temperature	Tjmax	125	°C
Power dissipation	Pd	1000*1	mW
Operating temperature range	Topr	−30 to 85	°C
Storage temperature range	Tstg	−55 to 150	°C

*1 Derated at 10mW/°C at Ta>25°C when mounted on a 70.0 mm × 70.0 mm × 1.6 mm glass epoxy board

●Operating Conditions (Ta=-30°C ~+85°C)

Parameter	Symbol	Limits		Unit
		Min.	Max.	
Power supply voltage	Vcc	2.7	13	V
Regulator power supply voltage	REGVcc	4.5	14	V
Driver power supply voltage	PVcc	2.7	13	V

●**Electrical Characteristics (Unless otherwise specified, Vcc = 5 V, REGVcc = 12V, Ta = 25°C)**

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[(1) DC/DC converter controller ERR AMP1, 2]						
Input bias current	Ib12	−3	−0.1	3	μA	INV = 0.5 V
Input offset voltage	Vos12	−10	0	10	mV	
Output source current	Iesc12	−2	−0.7	−0.2	mA	VFB = 1.25 V, INV = 0.5 V, NON = 2.5 V
Output sink current	Iesk12	0.1	0.3	1	mA	VFB = 1.25 V, INV = 1.5 V, NON = 0 V
Input voltage range	VNON12	−0.1	−	Vcc−1	V	
Max. output voltage	Voh12	1.8	2.1	2.4	V	IFB = −0.1 mA
Min. output voltage	Vol12	0.6	0.8	1.0	V	IFB = 0.1 mA
Feedback voltage	FB1	1.225	1.25	1.275	V	ERRAMP1 only
[(1) PWM and DRV]						
Output sink current	Ipsk12	70	130	200	mA	GD1, 2 = 5 V
Output source current	Ipsc12	−245	−160	−85	mA	GD1, 2 = 0 V
[(1) UD Selector]						
High-side threshold voltage	Vudh	Vcc × 0.7	Vcc	−	V	Step-down operation
Low-side threshold voltage	Vudl	−	0	Vcc × 0.3	V	Step-up operation
[(1) Detector 1, 2]						
High-side threshold voltage 1	Vdeh12	0.9	1.0	1.1	V	DET1, 2 L → H sweep up VINV
Low-side threshold voltage 1	Vdel12	0.6	0.7	0.8	V	DET1, 2 H → L sweep down VINV
High-side threshold voltage 2	Vdeh22	0.1	0.2	0.3	V	DET2 L→H,Inverting sweep down VNON
Low-side threshold voltage 2	Vdel22	0.4	0.5	0.6	V	DET2 H→L,Inverting sweep up VNON
DET1 max. output voltage	Vdh1	4.8	5.0	−	V	
DET1 min. output voltage	Vdl1	−	0	0.2	V	
DET2 max. output voltage	Vdh2	4.8	5.0	−	V	
DET2 min. output voltage	Vdl2	−	0	0.2	V	
[(1) Oscillator]						
Switching frequency	Fsw12	0.8	1.0	1.2	MHz	
Frequency variation	Fc12	−	10	−	%	Vcc = 3 V to 13 V
[(1) Soft start]						
Source current	Iscss	6	10	14	μA	
Sink current	Iskss	0.5	1	2	mA	CTL1, 2 = 0 V
[(1) Timer latch]						
Source current	Isctl	6	10	14	μA	SCP = 1.0 V
SCP threshold voltage	Vthscp	−	1.25	−	V	
[(1) DTC1]						
Input bias current	Vdtc1	−3	−0.1	3	μA	
High-side threshold voltage	VdtcH1	−	1.5	−	V	On Duty = 0%
Low-side threshold voltage	VdtcL1	−	1.0	−	V	On Duty = 100%
[(1) DTC2]						
Input bias current	Idtc2	−3	−0.1	3	μA	
High-side threshold voltage	IdtcH2	−	1.5	−	V	On Duty = 100%
Low-side threshold voltage	IdtcL2	−	1.0	−	V	On Duty = 0%
[(2) Charge pump driver ERR AMP3, 4]						
Feedback voltage	FB3	1.212	1.25	1.288	V	
	FB4	−	0	−	V	
Input bias current	Ib34	−3	−0.1	3	μA	Buffer
I/O voltage difference	ΔVd34	−	0.2	0.5	V	Io = −10 mA
Output current capacity	Io34	−	−130	−50	mA	VFB = 0 V

●**Electrical Characteristics (Unless otherwise specified, Vcc = 5 V, REGVcc = 12 V, Ta = 25°C)**

Parameter	Symbol	Limit			Unit	Conditions
		Min.	Typ.	Max.		
[(2) Driver]						
Switching frequency	Fsw34	200	250	300	kHz	
Frequency variation	Fc34	−	10	−	%	Vcc = 3V to 13V
[(2) Detector]						
High-side threshold voltage	Vdeh3	0.9	1.0	1.1	V	DET3 L → H, sweep up INV3
	Vdeh4	0.1	0.2	0.3	V	DET4 L → H, sweep down NON4
Low-side threshold voltage	Vdel3	0.6	0.7	0.8	V	DET3 H → L, sweep down NON3
	Vdel4	0.4	0.5	0.6	V	DET4 H → L, sweep up NON4
DET3 min. output voltage	Vdh3	4.8	5.0	−	V	
	Vdl3	−	0	0.2	V	
DET4 max. output voltage	Vdh4	4.8	5.0	−	V	
	Vdl4	−	0	0.2	V	
[(3) Low-dropout regulator]						
Feedback voltage	FBR	1.237	1.25	1.263	V	Buffer, Io = −10mA
Input bias current	Ibr	−3	−0.1	3	µA	Buffer
I/O voltage difference	ΔVdr	−	0.2	0.5	V	Io = −10mA
Output current capacity	Io	−	−130	−50	mA	VREG = 0V
Input stability	RegI	−	1	10	mV	REGVcc = 4.5V to 14V
Load stability	RegL	−	1	10	mV	Io = 1mA → 10mA
Ripple rejection ratio	RR	35	50	−	dB	f = 120Hz
[(4) Buffer Amp]						
Input offset voltage	Voso	−10	0	10	mV	
Input bias current	Ibo	−3	−0.1	3	µA	IN+ = 6V
Driver current	Ioo	20	50	−	mA	
Load stability	ΔVo	−	1	10	mV	Io = +1mA to −1mA
Slew rate	SRo	−	2	−	V/µs	
Max. output current	Voho	REGVcc −1.0	REGVcc −0.8	−	V	Io = −1mA, IN+ = REGVcc
Min. output current	Vohl	−	0.1	0.16	V	Io = 1mA, IN+ = 0V
[(5) Overall BG]						
BG output voltage	Vref	1.225	1.250	1.275	V	Io = −0.1mA
Input stability	ΔVi	−	5	20	mV	Vcc = 3V to 13V
Load stability	ΔVl	−	1	10	mV	Io = 0mA → 0.1mA
Output current capacity	Iovr	0.2	1	−	mA	BG = 0V
[VREF17]						
VREF17 output voltage	Vref17	1.666	1.700	1.734	V	Io = −0.1mA
Input stability	ΔVi17	−	5	20	mV	Vcc = 3V to 13V
Load stability	ΔVl17	−	1	10	mV	Io = 0mA → 0.1mA
Output current capacity	Iovr17	0.2	1	−	mA	VREF17 = 0V
[(5)CTL1 to CTL4]						
High-side threshold voltage	Vcth	Vcc×0.7	Vcc	−	V	Circuit active
Low-side threshold voltage	Vctl	−	0	Vcc×0.3	V	Circuit off
[(5) Under-voltage lockout protection]						
Threshold voltage	Vuvlo	2.327	2.45	2.573	V	
Hysteresis	Hys	−	0.1	−	V	
[(5)Total supply current]						
Standby current	Istb	−	0	10	µA	
Average consumption current	Icc	1.1	2	2.9	mA	
[(5)All ENABLE]						
Sink current	Ies	2	4	8	mA	ENABLE = 5V
[(5)PG]						
Source current	Igso	1.2	2.5	5	mA	CTL1 = CTL2 = 0V, PG = 2.5V
Sink current	Igsi	2	5	8	µA	CTL1 = 5V, PG = 2.5V

* This product is not designed for protection against radio active rays.

●Electrical Characteristics Curves (Unless otherwise specified, Ta = 25°C)

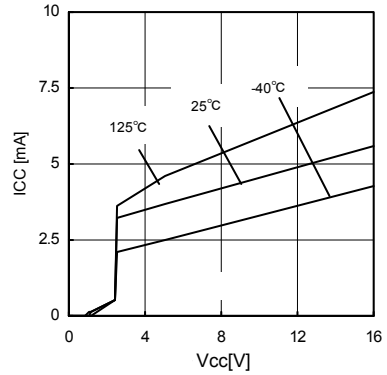


Fig. 1 Total Supply Current

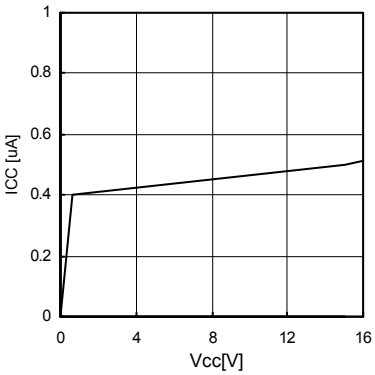


Fig. 2 Standby Current

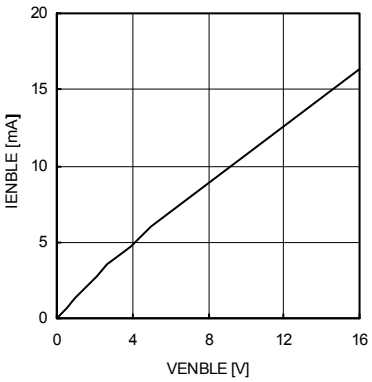


Fig. 3 ENB Pin Current

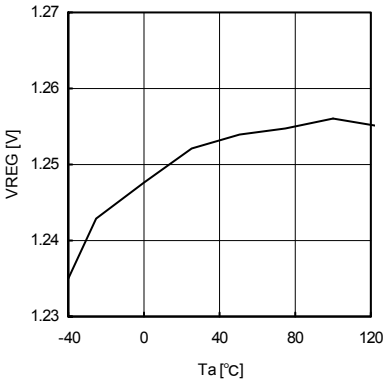


Fig. 4 VREG Voltage vs Temperature

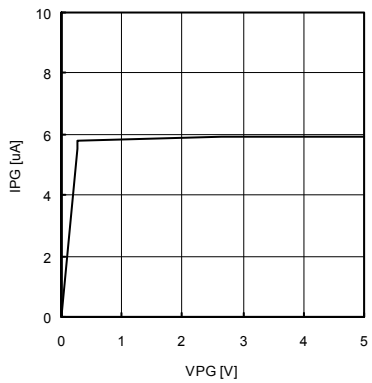


Fig. 5 PG Pin Sinking Current

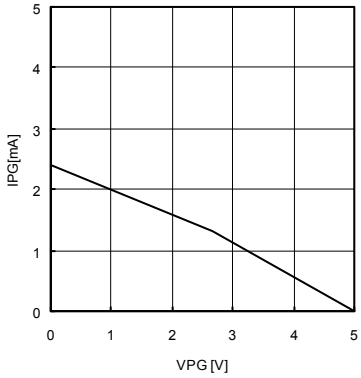


Fig. 6 PG Pin Source Current

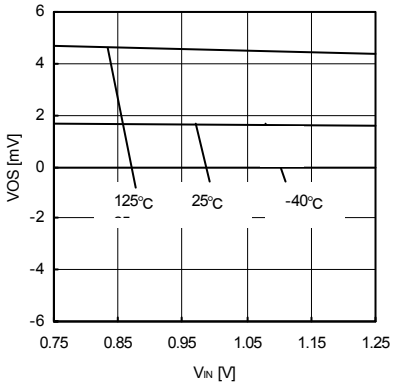


Fig. 7 Error Amp Offset Voltage

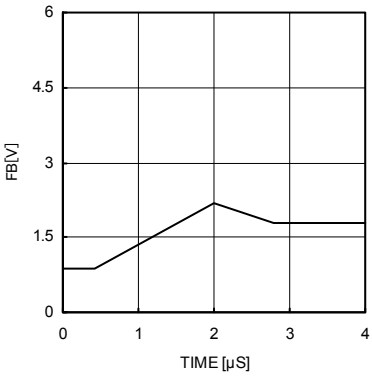


Fig. 8 Error Amp Slew Rate Waveform

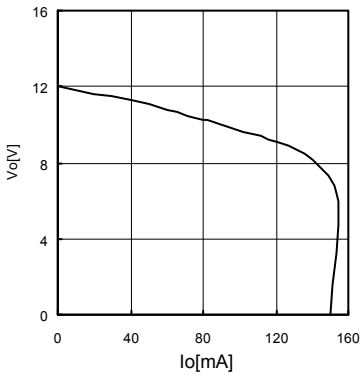


Fig. 9 Regulator Output Current Capacity

●Electrical Characteristics Curves (Unless otherwise specified, Ta = 25°C)

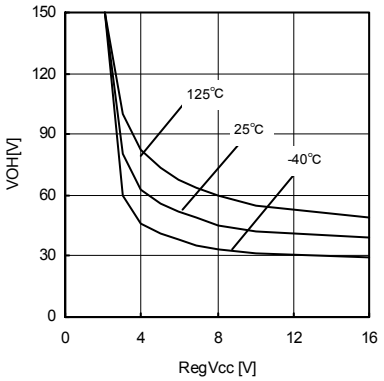


Fig. 10 Charge Pump
PMOS On Resistance

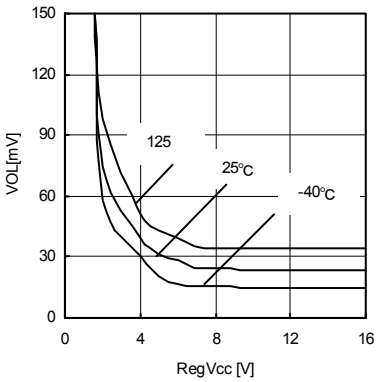


Fig. 11 Charge Pump
NMOS On Resistance

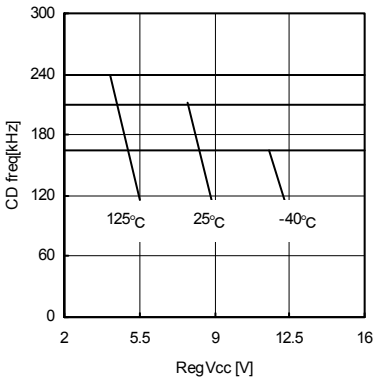


Fig. 12 Charge Pump
Switching Frequency

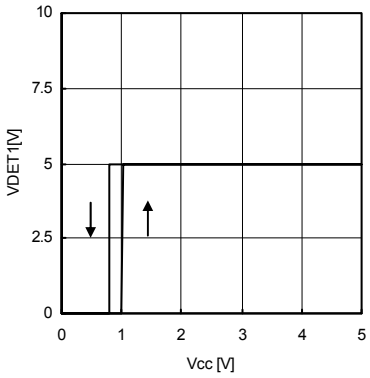


Fig. 13 Detectors 1 to 3
Threshold Voltage

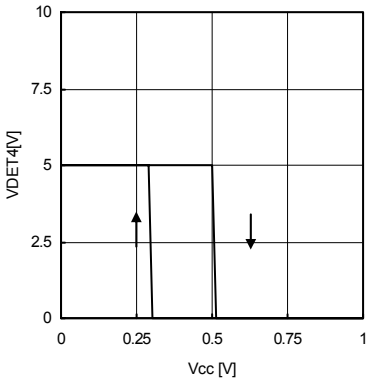


Fig. 14 Detector 4
Threshold Voltage

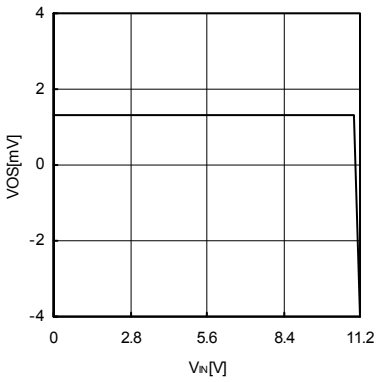


Fig. 15 Buffer Amp
Offset Voltage

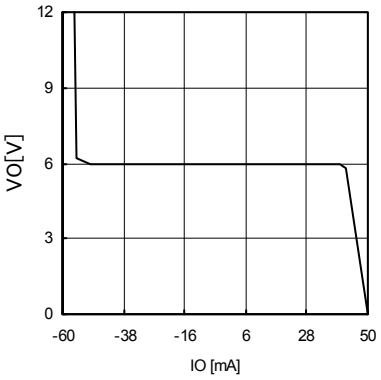


Fig. 16 Buffer Amp
Output current capacity

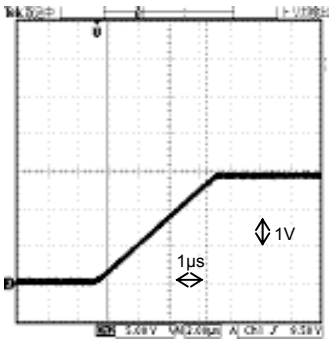


Fig. 17 Buffer Amp
Slew Rate Waveform

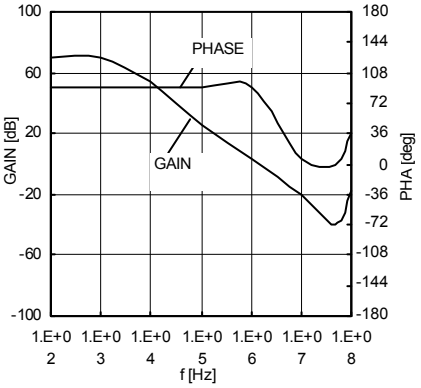
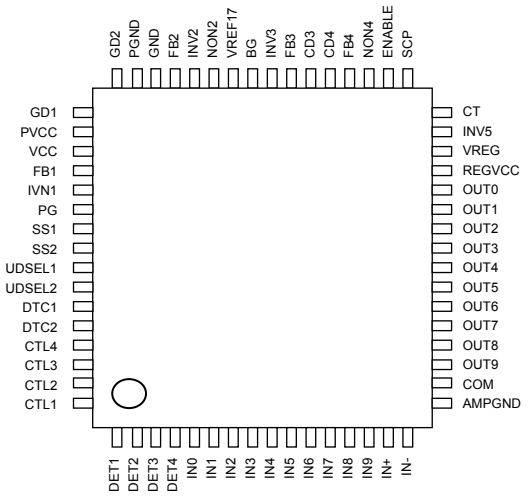


Fig.18 Buffer Amp
Open Loop

●Pinout Diagram



●Block Diagram

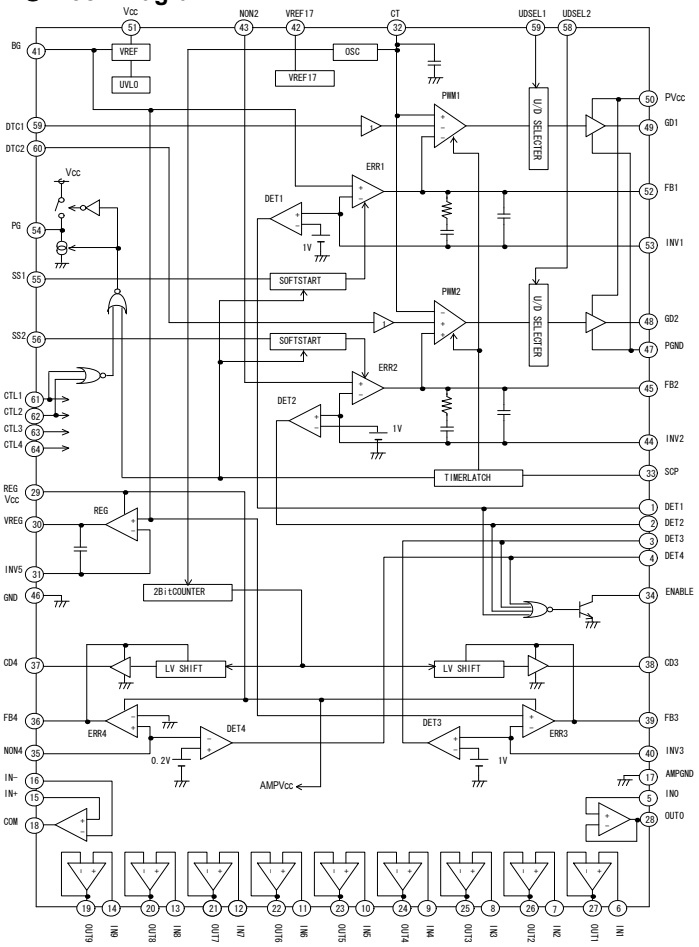


Fig. 19 BD8150KVT Pin Assignment Diagram and Block Diagram

●Pin Description

Pin No.	Pin Name	Function	Pin No.	Pin Name	Function
1	DET1	DC/DC detector output 1	33	SCP	Connect timer latch capacitor
2	DET2	DC/DC detector output 2	34	ENABLE	All channel output enable
3	DET3	Charge pump detector output 3	35	NON4	Charge pump feed back input 4
4	DET4	Charge pump detector output 4	36	FB4	Charge pump E/A output 4
5	IN0	Buffer amp 0 input	37	CD4	Charge pump driver output 4
6	IN1	Buffer amp 1 input	38	CD3	Charge pump driver output 3
7	IN2	Buffer amp 2 input	39	FB3	Charge pump E/A output 3
8	IN3	Buffer amp 3 input	40	INV3	Charge pump feed back input 3
9	IN4	Buffer amp 4 input	41	BG	Reference voltage monitor
10	IN5	Buffer amp 5 input	42	VREF17	1.7V Reference Voltage
11	IN6	Buffer amp 6 input	43	NON2	DC/DC E/A non inverting input 2
12	IN7	Buffer amp 7 input	44	INV2	DC/DC E/A inverting input 2
13	IN8	Buffer amp 8 input	45	FB2	DC/DC E/A output 2
14	IN9	Buffer amp 9 input	46	GND	Ground
15	IN+	Op-amp non inverting input	47	PGND	Power ground
16	IN-	Op-amp inverting input	48	GD2	DC/DC driver output 2
17	AMPGND	Buffer amp and op-amp ground	49	GD1	DC/DC driver output 1
18	COM	Op-amp output	50	PVCC	Power VCC supply
19	OUT9	Buffer amp 9 output	51	VCC	VCC supply
20	OUT8	Buffer amp 8 output	52	FB1	DC/DC E/A output 1
21	OUT7	Buffer amp 7 output	53	INV1	DC/DC E/A inverting input 1
22	OUT6	Buffer amp 6 output	54	PG	Pch FET switch driver output
23	OUT5	Buffer amp 5 output	55	SS1	Connect soft start capacitor 1
24	OUT4	Buffer amp 4 output	56	SS2	Connect soft start capacitor 2
25	OUT3	Buffer amp 3 output	57	UDSEL1	Step up/down select switch 1
26	OUT2	Buffer amp 2 output	58	UDSEL2	Step up/down select switch 2
27	OUT1	Buffer amp 1 output	59	DTC1	Dead time control voltage input1
28	OUT0	Buffer amp 0 output	60	DTC2	Dead time control voltage input2
29	REGVCC	Charge pump, Regulator, op-amp and buffer amp power supply	61	CTL4	Charge pump control switch 4
30	VREG	Regulator output	62	CTL3	Charge pump control switch 3
31	INV5	Regulator negative feed back input	63	CTL2	DC/DC control switch 2
32	CT	Ramp wave monitor	64	CTL1	DC/DC control switch 1

●Block Description

- VREF
  This block outputs a highly accurate reference voltage of 2.5V and has a current capacity of over 1mA. ON/OFF control is possible using the CTL pin.
- ERRAMP
  This is an error amp that amplifies and outputs the NON and INV voltage differential. The output pulse duty is determined by the output FB voltage. When FB is 1.95V or more it is switched OFF, and when 1.45V or less the output NPN Tr is switched ON.
- OSC
  This block determines the RT and CT switching frequency. The triangular waveform is determined by RT and CT.
- Timer latch
  This is a protection circuit that detects output short-circuits (when the error amp output is 1V or less). Once activated, the timer begins charging the SCP terminal capacitance at 7μA. When the SCP voltage is 1.8V or more, the latch is applied and shutdown begins. Recovery can be accomplished by turning on Vcc and CTL.
- PWM/driver
  This is a PWM comparator that determines the duty by comparing the error amp output and the oscillator triangular waveform in order to determine the maximum duty ratio for the DTC. It is turned to OFF when the DTC voltage is 1.95V and turned ON at 1.45V. Use the VREF resistance division to set the DTC voltage.
- UVLO
  This is a protective circuit that shuts down the system when the input voltage becomes 2.5V in order to prevent IC malfunction. A 0.1V hysteresis exists and reset is implemented once the voltage is at least 2.6V.
- Soft start
  Soft start is activated during startup in order to prevent DC/DC converter inrush current. The delay time depends on the pin capacitance. The circuit is set to LOW when a protective circuit is triggered. When reset, soft start will once again operate at startup.
- DET
  This is a comparator that detects whether each output voltage is output as set. When output as set, High is output to pins DET1 to DET4. When all of the DET pins are High, the ENABLE pin is set to High.
- U/D selector
  This selector switches between the step-up DC/DC and step-down DC/DC. Step-down operation is performed for high input, and step-up operation is performed for low input.
- VREF17
  A 1.7V reference voltage is output. This is used for the DTC setting. Perform resistance division from this voltage and set the DTC voltage.
- REG
  This is the regulator output for the gamma correction setting. Providing gamma correction resistance division under this regulator makes it possible to obtain a stable gamma correction voltage.
- 2-bit counter
  A charge pump switching frequency is generated from the DC/DC converter frequency. This becomes 1/4 of the DC/DC converter frequency.
- DRV block (DC/DC converter)
  This is a driver block that outputs the pulse between Vcc and GND. This directly drives the P-channel FET or N-channel FET. For step-up, connect the N-channel FET, for step-down, connect the P-channel FET.
- DRV (charge pump)
  This driver block outputs the pulse between FB and GND. Feedback control is applied to the FB voltage to stabilize the charge pump. The FB voltage only increases to the Reg Vcc voltage, so the Reg Vcc voltage is the maximum switching amplitude.
- Buffer Amp
  This IC has a built-in 10channel buffer amp for gamma correction voltage generation. Using this amp allows generation of a gamma correction voltage that is input to the source driver.
- VCOM
  A 1-channel differential input operation amp is built-in for VCOM. Using an external bipolar Tr buffer makes it possible to generate a VCOM voltage.

●Timing Chart

•Basic Operation

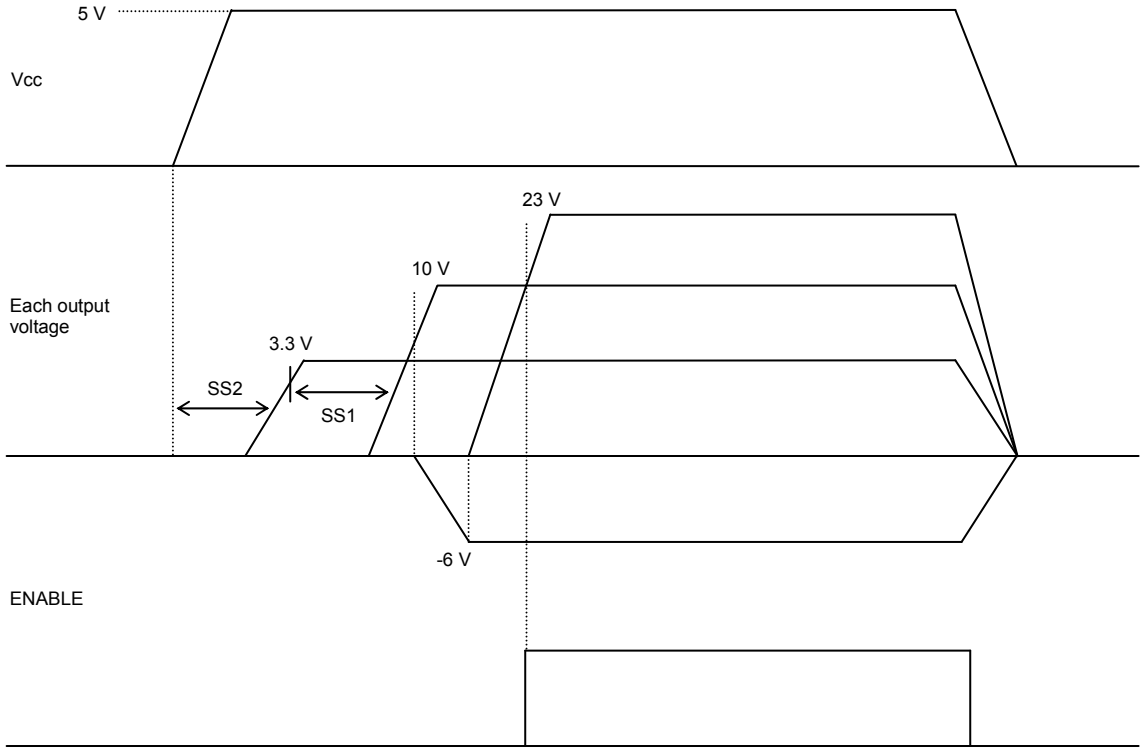


Fig. 20 Basic Operation

●When short protection is triggered

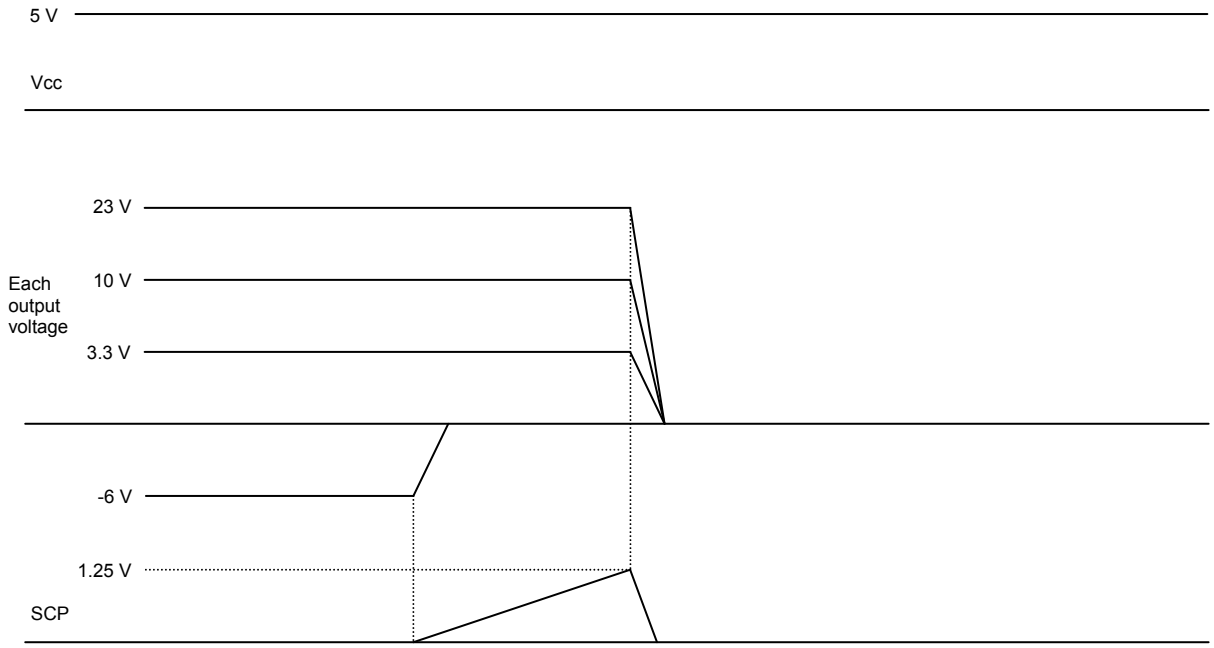


Fig. 21 During Short Protection Operation

●Selecting Application Components

1 DC/DC converter block design

1-1 Operating mode determination

The step-down, step-up, and inverting switching regulators are comprised of UDSEL (Pins 58, 59), error amp input NON (Pin 43), and INV pins (Pins 44, 53). NON1 is internally connected to BG.

Operating mode	UDSEL	NON	INV
Step-down	VCC	BG	FEEDBACK
Step-up	GND	BG	FEEDBACK
Inverting	VCC	FEEDBACK	GND

1-2 Setting the oscillating frequency

Applying capacitance to the CT pin (Pin 32) allows the oscillating frequency to be set. Refer to Fig.22 when setting the capacitance. When nothing is applied, the frequency is set to 1 MHz (Typ.).

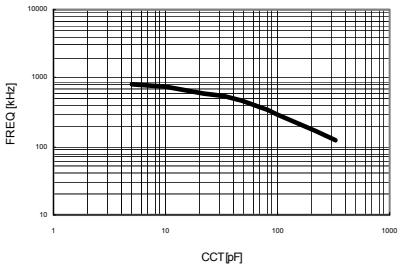


Fig. 22 CT Capacitance vs Oscillating Frequency

1-3 L and C selection

Select the output L and C so that the output ripple voltage is within specifications. Select L so that the sum of the ripple current and load current (input current for step-up and inversion) does not exceed the rated current of the coil. And select C so that the output ripple voltage including the switching noise does not exceed breakdown voltage.

Coil current $\Delta IL = (V_{CC} - VO) \times VO / (L \times f \times V_{CC})$ [A] (step-down)

$\Delta IL = V_{CC} \times (VO - V_{CC}) / (L \times f \times VO)$ [A] (Step-up)

$\Delta IL = V_{CC} \times VO / (L \times f \times (VO - V_{CC}))$ [A] (Inversion)

Output ripple voltage $\Delta VPP = \Delta IL \times RESR + (\Delta IL \times VO) / (2 \times C \times f \times V_{CC})$ [V] (step-down)

$\Delta VPP = (\Delta IL + IO) \times RESR + (\Delta IL \times VO) / (2 \times C \times f \times V_{CC})$ [V] (Step-up, Inversion)

Where, RESR = Internal resistance component in output C.

1-4 Switching MOSFET selection

There is no problem if the absolute maximum rating exceeds the rated current of L and the breakdown voltage + rectification diode VF for C, but select a low gate capacitance (inrush charge amount) to achieve high-speed switching.

1-5 Rectification diode selection

Select a Schottky barrier diode having a current capacity above the rated current of L and an inverse breakdown voltage above the breakdown voltage of C and that, in particular, has a low forward direction voltage VF.

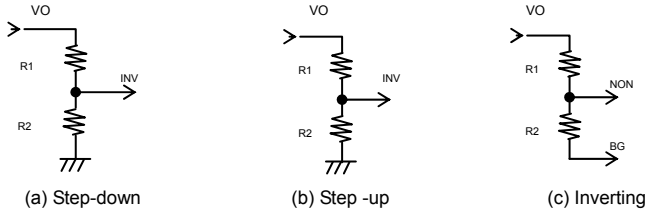
1-6 Feedback resistance value setting

Use the following equation to set the feedback resistance value to achieve stability at the specified output voltage.

Output voltage $VO = (R1 + R2) \times BG / R2$ [V] (step-down)

$VO = (R1 + R2) \times BG / R2$ [V] (Step-up)

$VO = -(R1 \times BG) / R2$ [V] (Inversion)



(a) Step-down (b) Step -up (c) Inverting

Fig. 23 Feedback Resistance Setting

The INV and NON pins are easily affected by noise, so use as short a pattern layout as possible and make sure that there is no overlap of the switching lines.

1-7 Setting soft start time

Applying capacitance to the SS pins (pins 55, 56) allows the soft start time to be set. Refer to Fig. 24 in order to select the appropriate capacitance. The soft start time will vary depending on the application, such as frequency, coil, and capacitance, so always verify operation under actual conditions.

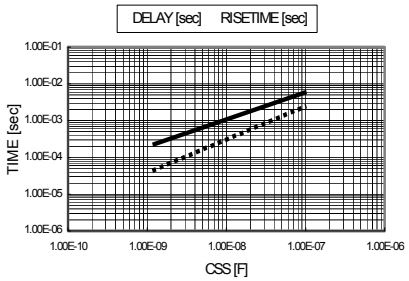


Fig. 24 Soft Start Time for SS Capacitance

1-8 Load switch MOSFET selection and corresponding soft start (step-up channels only)

Switching does not exist in the circuits from VCC to VO for normal step-up applications, so the coil or rectification diode could be damaged by an output short. To prevent this, insert a PMOSFET load switch between the VCC and coil. Select a PMOSFET with breakdown voltage between the gate sources and between the drain sources higher than VCC. Furthermore, if soft start is to be applied to the load switch, insert a capacitor between the gate sources. Refer to Fig. 26 when selecting the soft start time. Please note that the soft start time depends on the PMOSFET gate capacitance.

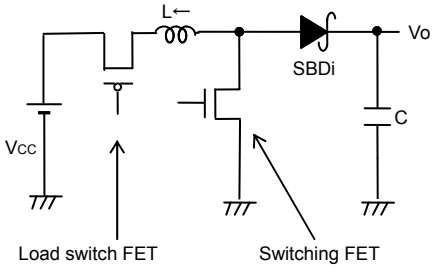


Fig. 25 Load Switch Circuit Diagram

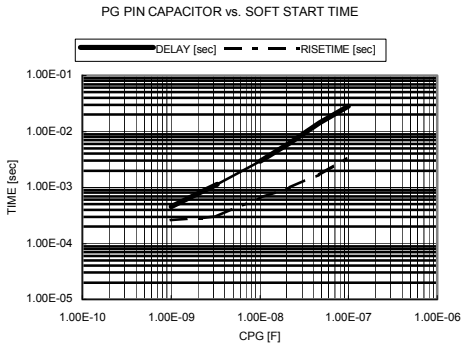


Fig. 26 Soft Start Time for PG Capacitance

1-9 RC filter setting for phase compensation

Phase compensation is required for stabilization in DC/DC converter applications. A built-in phase compensation circuit makes this possible.

1) When using internal phase compensation, observe the following requirements in designs.

(1) Internally set the switching frequency (1MHz Typ.).

(2) $1 / (2\pi\sqrt{LC}) = 10 - 30$ kHz

(3) $1 / (2\pi R1C1) = 10 - 100$ kHz

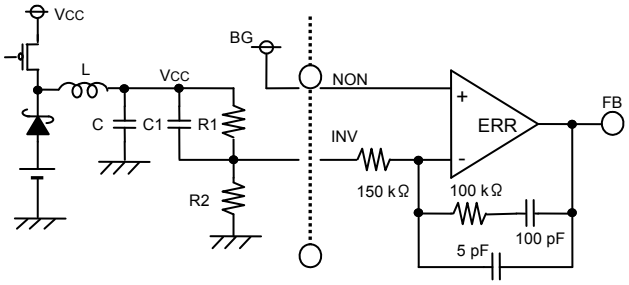


Fig. 27 Internal Phase Compensation

2) Using external phase compensation

When changing the oscillating frequency and L or C values, insert an RC filter circuit between INV and FB.

(1) $(1/2\pi\sqrt{LC}) \times 0.5 < 1 / (2\pi R1C1) < (1/2\pi\sqrt{LC}) \times 2$

(2) $(1/2\pi\sqrt{LC}) \times 0.5 < 1 / (2\pi R4C2) < (1/2\pi\sqrt{LC}) \times 2$

(3) R3 > R4

(4) $(1/2\pi R4C2) \times 5 < 1 / (2\pi R3C3) < fsw / 2$

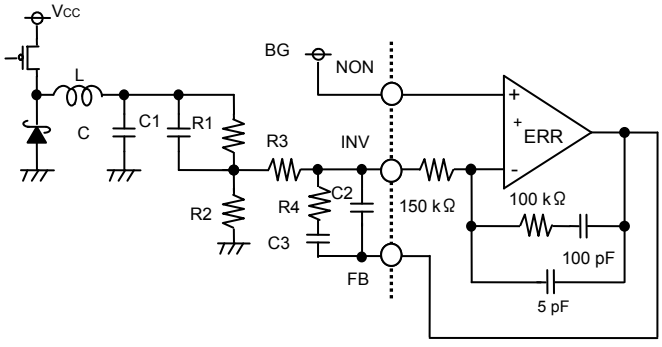


Fig. 28 External Phase Compensation

1-10 When only one channel is used for the DC/DC converter

This IC has built-in detector circuits for detection of output voltage startup. The ENABLE signal changes to High when all detectors are on, meaning the ENABLE signal (Pin 34) will not switch to High if channels not used by the DC/DC converter are set to OFF. If there exist channels that are not used, set them as follows so that the ENABLE signal will be switched to High.

(1) Make the CTL (Pins 63, 64) HIGH (VCC).

(2) Detection is performed on the feedback side, so the INV and NON of unused channels should be shorted.

(3) Connect the SS pin to GND.

1-11 Output short protection circuit

This IC has a built-in timer latch type output short protection function to prevent damage from overcurrent from the output MOSFET. Adding capacitance to the SCP pin (Pin 33) allows the delay time to be set until protection can be provided.

In the event of an output short, a rated current (7μA, Typ.) flows to the SCP capacitor. When the threshold voltage (1.25V, Typ.) is attained, a latch is applied and the IC is shut down. The shutdown is canceled by CTL or turning the power on again. Refer to Fig. 29 in order to determine the capacitance that will set the delay time.

The output power transistor damage time varies depending on the application, so perform evaluations using the actual product under operating conditions. Furthermore, if not using short protection, short the SCP pin to GND.

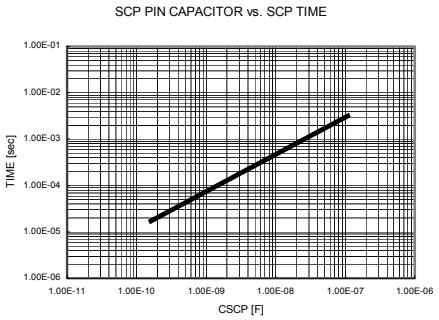


Fig. 29 SCP Capacitance vs Short Protection Delay Time

2 Charge pump design

2-1 Basic circuit operation

The charge pump circuit stores a charge in a flying capacitor and then supplies the charge to a post-circuit. There are double charge pumps, triple charge pumps, etc. In this example, the charge pump error amp output voltage FB (Pins 36, 39) is added to the step-up side voltage, so a circuit equation that stabilizes the set voltage is used.

For the high-side (VO3) charge pump, the output voltage VO3 is set by feedback resistors R5 and R6.

$VO3 = BG \times (R5 + R6) / R6$ [V]

Further, the maximum output voltage (no load) of VO3 is found using the following equation.

$VO3MAX = 2 \times VO1 + FB3 - 3VF$ [V]

Where, VF is the diode's forward voltage. For VO3MAX, set the numerical V amount higher than VO3. (See Fig. 30.)

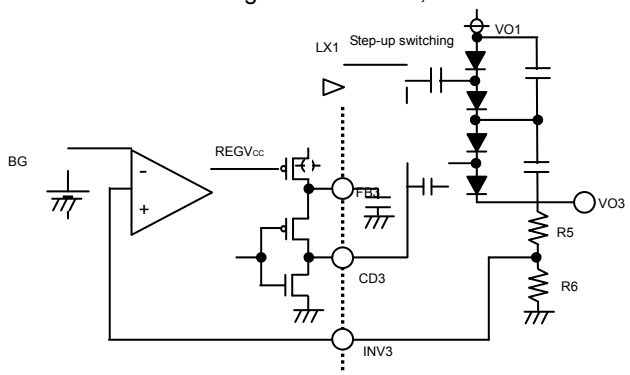


Fig. 30 High-side Charge Pump Circuit Diagram

For the low-side (VO4) charge pump, the output voltage (VO4) setting and maximum output voltage (VO4MAX) is found using the following equation.

$VO4 = -(R7 / R8) \times BG$ [V]

$VO4MAX = -FB4 + 2 \times VF$ [V]

Where, VF is the diode's forward voltage

For VO4MAX, set the numerical V amount higher than VO4.

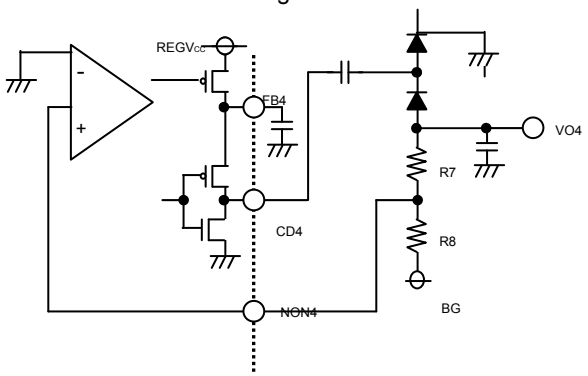


Fig. 31 Low-side Charge Pump Circuit Diagram

2-2 Flying capacitor setting

For the flying capacitor, select a breakdown voltage that is sufficiently high compared to the switching voltage.

2-3 Output capacitance setting

Use an output capacitance with a breakdown voltage that is sufficiently high compared to the output voltage. In addition, for the output capacitance CO, refer to the following equation and set it within the output ripple voltage ΔVPP range.

$\Delta VPP = IO / (2 \times CO \times fSW)$ [V]

Where, the fSW is the charge pump switching frequency and has a period 4 times that of the DC/DC.

2-4 Diode selection

The charge pump switching voltage is applied in reverse to the diode. For this reason, select a sufficiently high reverse breakdown voltage. For the current capacity, use one with a rating of at least 5 times the load.

2-5 Error amp output voltage FB capacitance selection

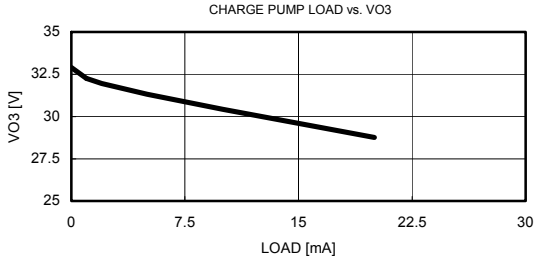


Fig. 32 High-side Charge Pump Load vs Maximum Voltage

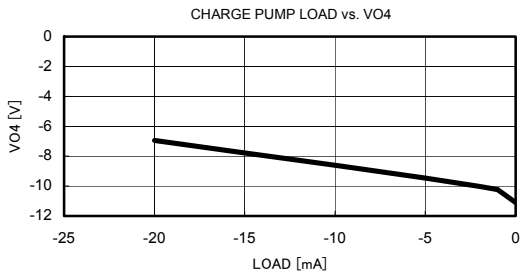


Fig. 33 Low-side Charge Pump Load vs Maximum

3 Regulator Block Design

3-1 Basic operation

The voltage at the very top of the gamma correction voltage range is set using an internal low-saturation regulator. The output voltage VREG (pin 30) is set using the resistance division R9 and R10.

VREG = BG × (R9 + R10) / R10 [V]

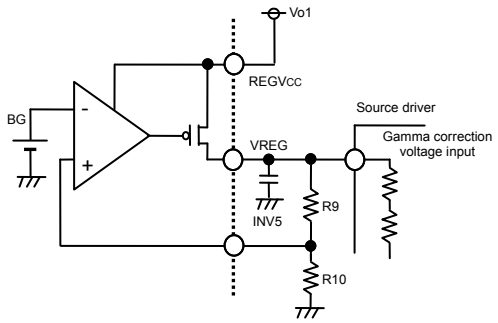


Fig. 34 Gamma Correction Voltage Regulator Circuit Diagram

Note that a 0.5V potential difference is required between REGVCC and VREG for the regulator power supply. The reference voltage BG accuracy is ±1%.

3-2 VREG output capacitance selection

A capacitor for preventing oscillation is required at the VREG (Pin 30) output. Select one 1μF or larger with a sufficiently high breakdown voltage.

4 Gamma correction voltage block design

4-1 Gamma correction voltage setting resistance value selection

A 10channel Buffer Amp is incorporated. The input voltage set by resistance division allows output of a gamma correction voltage with greater current capacity. The configuration in the figure below can output gamma correction voltage with high accuracy.

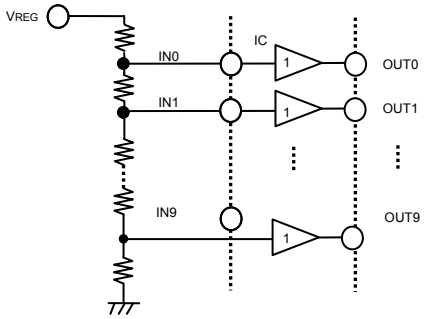


Fig. 35 Gamma Correction Voltage Generation Block Circuit Diagram

4-2 Back plate bias common voltage setting

This IC incorporates a 1channel operation Buffer in addition to the 10channel Buffer Amp. This Op Amp, along with discrete Transistor, can be used to set the back plate bias common voltage.

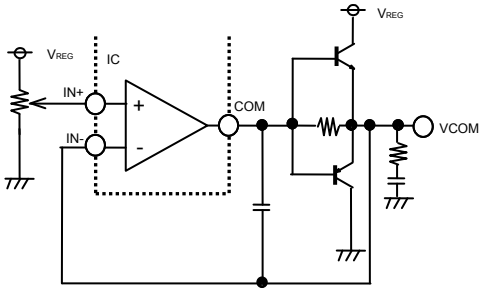


Fig. 36 Common Voltage Setting Circuit Diagram

●Application Circuit Diagram

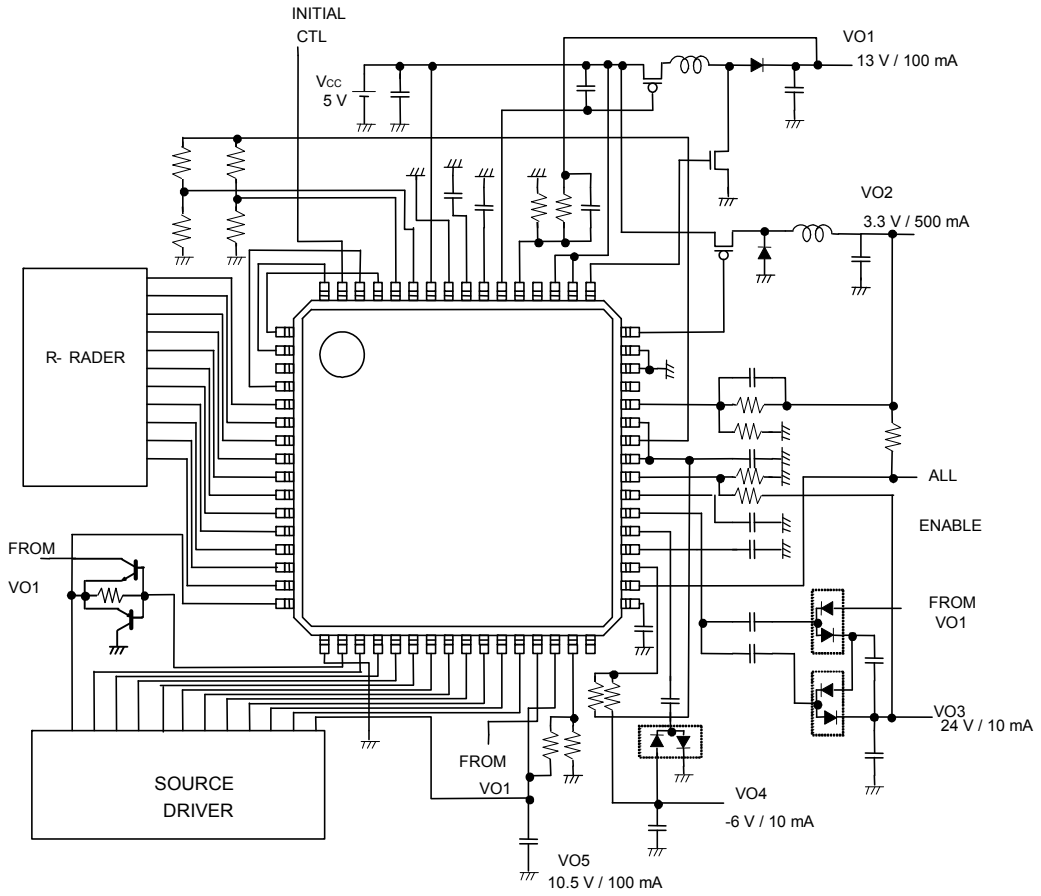


Fig. 37 BD8150KVT Application Circuit Diagram

●Startup sequence

The startup sequence of each output terminal can be set using the detection (DET1 to DET4) and control pins (CTL1 to CTL4). The detection pins switch from L to H when the feedback side INV voltage of each block reaches 80% of the reference side. For this reason, the startup sequence can be set by connecting a detection pin to the control pin to be started up next.

The detection pins have a hysteresis width with a standard value of 0.3 V. However, if a ripple exceeding this is applied to the INV pin, chattering will occur. After all outputs have begun, if even one turns off, all outputs will stop.

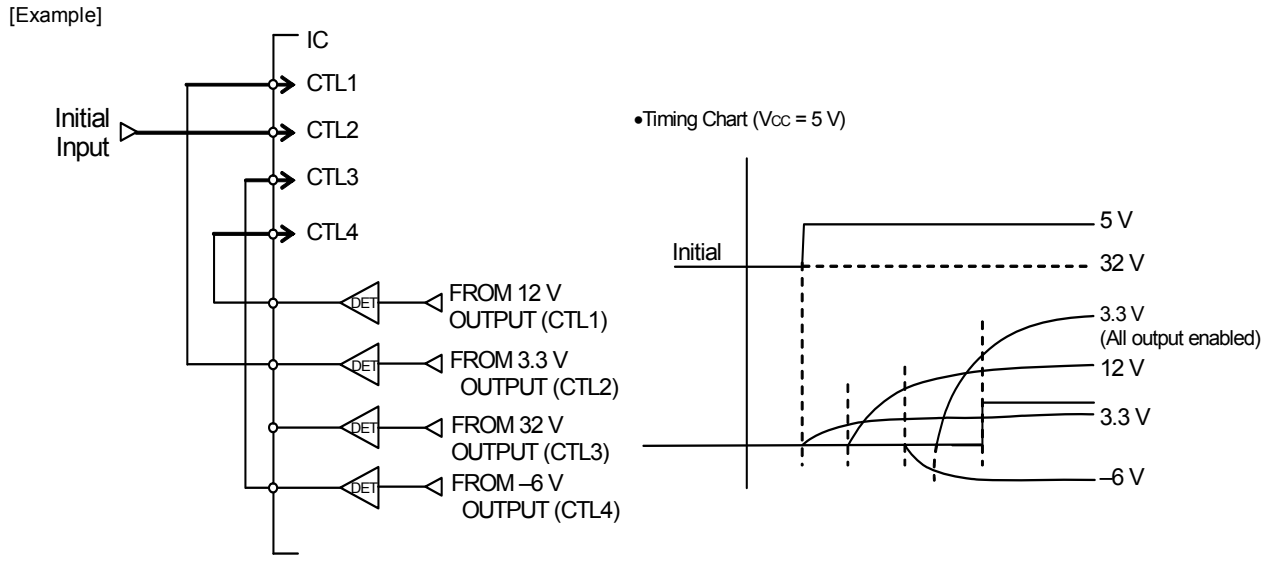


Fig. 38 Timing Chart

●I/O Equivalent Circuit Diagrams

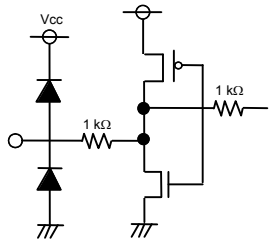
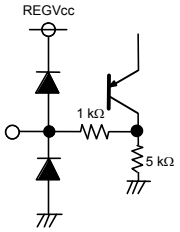
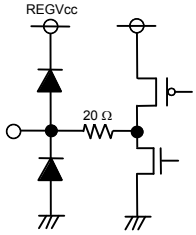
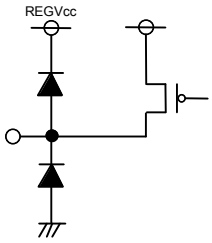
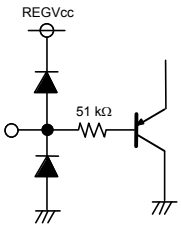
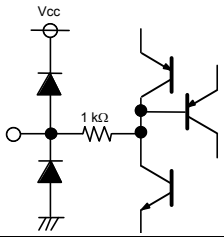
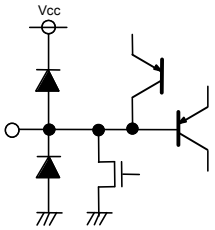
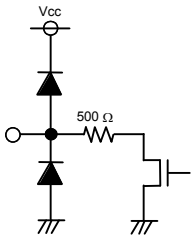
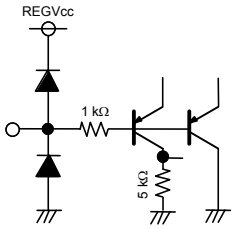
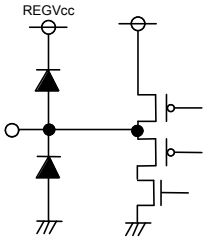
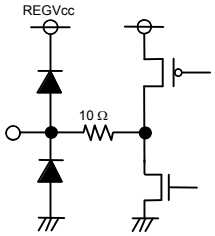
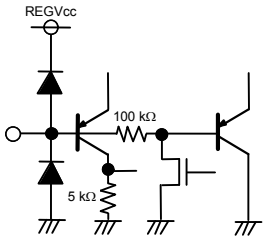
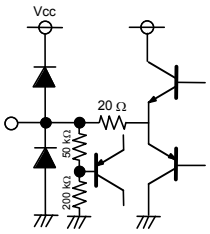
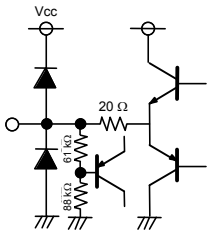
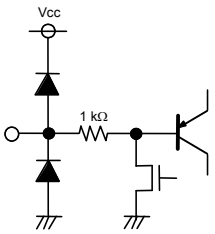
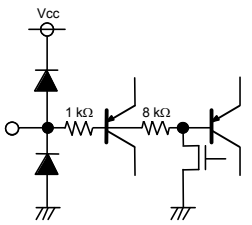
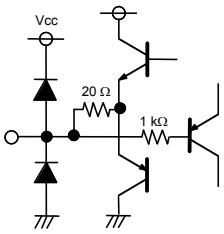
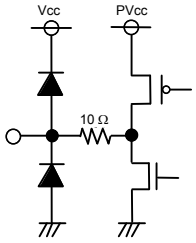
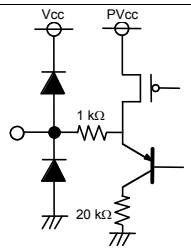
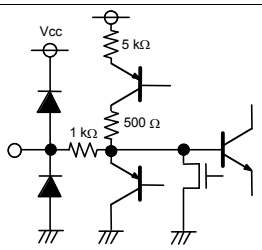
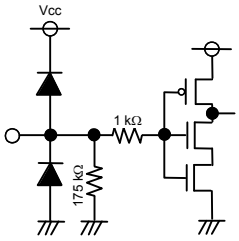
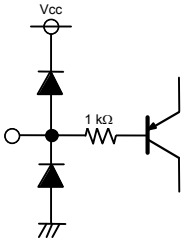
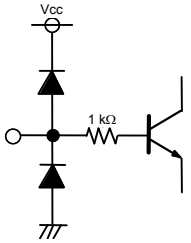
1. DET1 2. DET2 3. DET3 4. DET4	5. IN0 6. IN1 7. IN2 8. IN3 9. IN4 10. IN5 11. IN6 12. IN7 13. IN8 14. IN9 15 .IN+ 16. IN-	18. COM 19. OUT9 20. OUT8 21. OUT7 22. OUT6 23. OUT5 24. OUT4 25. OUT3 26. OUT2 27. OUT1 28. OUT0	30.VREG
			
31. INV5	32. CT	33. SCP	34. ENABLE
			
35. NON4	36. FB4 39. FB3	37. CD4 38. CD3	40. INV3
			
41. BG	42. VREF17	43. NON	44. INV2 53. INV1
			
45. FB2 52. FB1	48. GD2 49. GD1	54. PG	55. SS2 56. SS2
			
57. UDSEL 58. UDSEL 61. CTL4 62. CTL3 63. CTL2 64. CTL1	59. DTC1	60. DTC2	
			

Fig. 39 I/O Equivalent Circuit Diagram

●Notes for use

1. Absolute maximum ratings
   An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

2. Connecting the power supply connector backward
   Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Power supply lines
   Design PCB layout pattern to provide low impedance GND and supply lines. To obtain a low noise ground and supply line, separate the ground section and supply lines of the digital and analog blocks. Furthermore, for all power supply terminals to ICs, connect a capacitor between the power supply and the GND terminal. When applying electrolytic capacitors in the circuit, not that capacitance characteristic values are reduced at low temperatures.

4. GND voltage
   The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design
   Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors
   Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field
   Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. Testing on application boards
   When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

9. Regarding input pin of the IC
   This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:
   When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
   When GND > Pin B, the P-N junction operates as a parasitic transistor.
   Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.

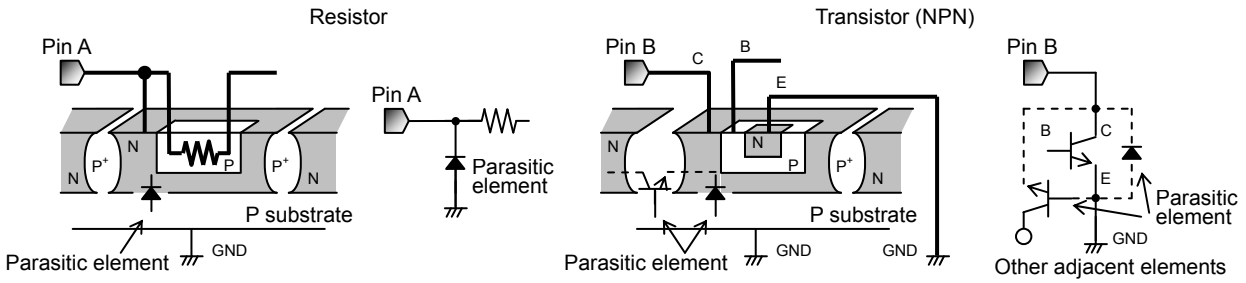
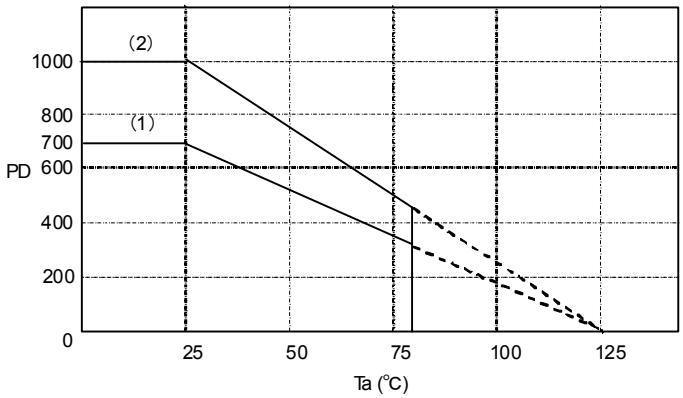


Fig.40 Example of IC structure

10. Ground Wiring Pattern
    When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

●Thermal Dissipation Curve



(1) IC without heat sink
(2) When mounted on a glass epoxy board
(70 mm × 70 mm × 1.6 mm)

Fig.41

●Ordering part number

B	D	8	1	5	0	K	V	T	-	E	2

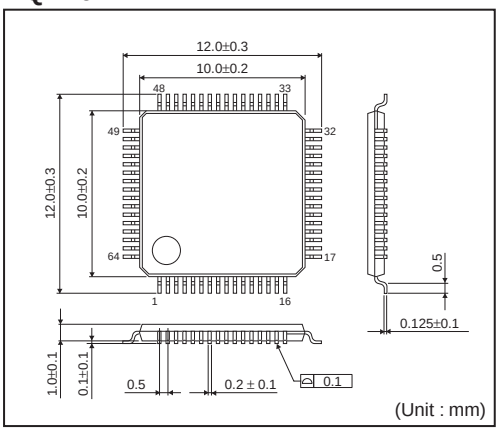
Part No. (BD)

Part No. (8150)

Package
KVT: TQFP64V

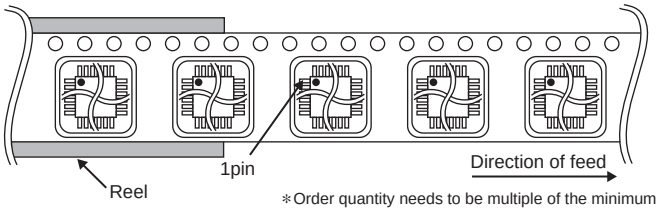
Packaging and forming specification
E2: Embossed tape and reel

TQFP64V



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	1000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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