



**THE DATASHEET OF  
BLC9G20LS-470AVTZ**



# BLC9G20LS-470AVT

Power LDMOS transistor

Rev. 3 — 24 November 2017

AMMPLÉON

Product data sheet

## 1. Product profile

### 1.1 General description

470 W LDMOS packaged asymmetric Doherty power transistor for base station applications at frequencies from 1805 MHz to 1990 MHz.

**Table 1. Typical performance**

Typical RF performance at  $T_{case} = 25\text{ °C}$  in an asymmetrical Doherty production test circuit.  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 500\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}$ , unless otherwise specified.

Test signal	f	$V_{DS}$	$P_{L(AV)}$	$G_p$	$\eta_D$	ACPR
	(MHz)	(V)	(W)	(dB)	(%)	(dBc)
1-carrier W-CDMA	1805 to 1880	28	80	16	49	-35 <a href="#">[1]</a>

[1] Test signal: 3GPP test model 1; 64 DPCH; PAR = 7.2 dB at 0.01% probability on CCDF per carrier.

### 1.2 Features and benefits

- Excellent ruggedness
- High efficiency
- Low thermal resistance providing excellent thermal stability
- Designed for broadband operation (1805 MHz to 1990 MHz)
- Asymmetric design to achieve optimum efficiency across the band
- Lower output capacitance for improved performance in Doherty applications
- Designed for low memory effects providing excellent digital pre-distortion capability
- Internally matched for ease of use
- Integrated ESD protection
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- RF power amplifiers for base stations and multi carrier applications in the 1805 MHz to 1990 MHz frequency range

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain2 (peak)		<p>aaa-014884</p>
2	drain1 (main)		
3	gate1 (main)		
4	gate2 (peak)		
5	source <a href="#">[1]</a>		
6	video decoupling (peak)		
7	video decoupling (main)		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLC9G20LS-470AVT	-	air cavity plastic earless flanged package; 6 leads	SOT1258-1

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	65	V
$V_{GS(amp)main}$	main amplifier gate-source voltage		-5	+13	V
$V_{GS(amp)peak}$	peak amplifier gate-source voltage		-5	+13	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

## 5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA (main)};$ $V_{GS(amp)peak} = 0.5\text{ V}; T_{case} = 80\text{ °C}$		
		$P_L = 49\text{ dBm}$	0.26	K/W
		$P_L = 51\text{ dBm}$	0.20	K/W

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Main device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 1.44\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 144\text{ mA}$	1.5	2	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 30\text{ V}; I_D = 864\text{ mA}$	1.8	2.1	2.35	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	31.5	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 5.04\text{ A}$	-	10.2	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 5.04\text{ A}$	-	99	165	$\text{m}\Omega$
<b>Peak device</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.6\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 260\text{ mA}$	1.5	2	2.5	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 30\text{ V}; I_D = 1560\text{ mA}$	1.4	1.85	2.25	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 32\text{ V}$	-	-	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	49	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$g_{fs}$	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 9.1\text{ A}$	-	17.3	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 9.1\text{ A}$	-	51	85	$\text{m}\Omega$

**Table 7. RF characteristics**

Test signal: 1-carrier W-CDMA; PAR = 7.2 dB at 0.01 % probability on the CCDF; 3GPP test model 1; 1 to 64 DPCH; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_{L(AV)} = 80\text{ W}$	14.5	15.7	-	dB
$RL_{in}$	input return loss	$P_{L(AV)} = 80\text{ W}$	-	-10	-6	dB
$\eta_D$	drain efficiency	$P_{L(AV)} = 80\text{ W}$	42.5	47.5	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 80\text{ W}$	-	-33	-28	dBc

**Table 8. RF characteristics**

Test signal: pulsed CW;  $t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ %}$ ; RF performance at  $V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}; T_{case} = 25\text{ °C}$ ; unless otherwise specified; in an asymmetrical Doherty production test circuit at frequencies from 1805 MHz to 1880 MHz.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$P_{L(M)}$	peak output power		380	425	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLC9G20LS-470AVT is capable of withstanding a load mismatch corresponding to a VSWR = 10 : 1 through all phases under the following conditions:  $V_{DS} = 28\text{ V}$ ;  $I_{Dq} = 400\text{ mA}$  (main);  $V_{GS(amp)peak} = 0.5\text{ V}$ ;  $P_L = 250\text{ W}$  (CW);  $f = 1805\text{ MHz}$ .

### 7.2 Impedance information

**Table 9. Typical impedance of main device**

Measured load-pull data of main device;  $I_{Dq} = 400\text{ mA}$  (main);  $V_{DS} = 28\text{ V}$ .

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
1805	1.03 – j4.87	1.22 – j3.6	206.0	60.0	15.16
1843	2.10 – j4.50	1.22 – j3.6	200.0	60.0	14.93
1880	1.58 – j5.07	1.22 – j3.6	200.4	60.3	15.34
<b>Maximum drain efficiency load</b>					
1805	1.03 – j4.87	2.31 – j2.74	142.5	68.12	17.44
1843	2.10 – j4.50	2.08 – j2.55	137.0	68.24	17.06
1880	1.58 – j5.07	1.90 – j2.76	146.0	67.8	17.30

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

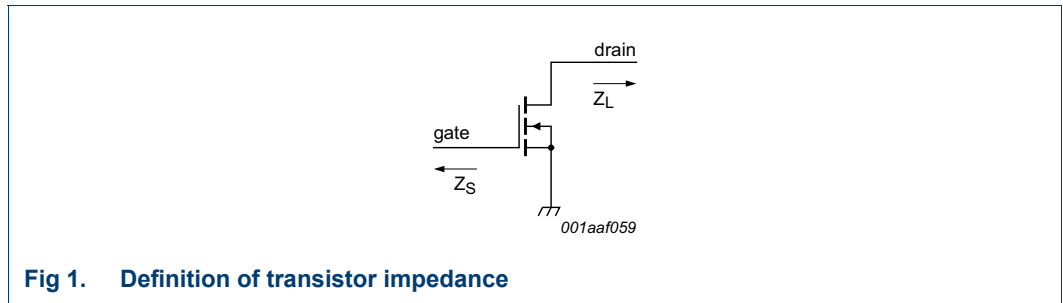
**Table 10. Typical impedance of peak device**

Measured load-pull data of peak device;  $I_{Dq} = 1300\text{ mA}$  (peak);  $V_{DS} = 28\text{ V}$ .

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (W)	η <sub>D</sub> [2] (%)	G <sub>p</sub> [2] (dB)
<b>Maximum power load</b>					
1805	1.06 – j5.55	2.0 – j3.8	322.8	56.90	15.60
1843	1.89 – j5.55	2.0 – j3.8	315.5	56.18	15.16
1880	1.86 – j6.21	2.2 – j4.1	313.3	55.30	15.74
<b>Maximum drain efficiency load</b>					
1805	1.06 – j5.55	2.76 – j2.70	267.9	64.5	17.23
1843	1.89 – j5.55	2.68 – j2.24	234.4	63.5	17.04
1880	1.86 – j6.21	2.68 – j2.24	230.7	63.5	17.79

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.



### 7.3 Recommended impedances for Doherty design

**Table 11. Typical impedance of main device at 1 : 1 load**

Measured load-pull data of main device;  $I_{Dq} = 400 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ .

f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (dBm)	η <sub>D</sub> [3] (%)	G <sub>p</sub> [3] (dB)
1805	1.03 – j4.87	1.83 – j3.50	52.6	46.5	19.1
1843	2.10 – j4.50	1.67 – j3.30	52.7	47.0	19.2
1880	1.58 – j5.07	1.50 – j3.12	52.8	48.1	19.4

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P<sub>L(AV)</sub> = 49 dBm.

**Table 12. Typical impedance of main device at 1 : 2.5 load**

Measured load-pull data of main device;  $I_{Dq} = 400 \text{ mA (main)}$ ;  $V_{DS} = 28 \text{ V}$ .

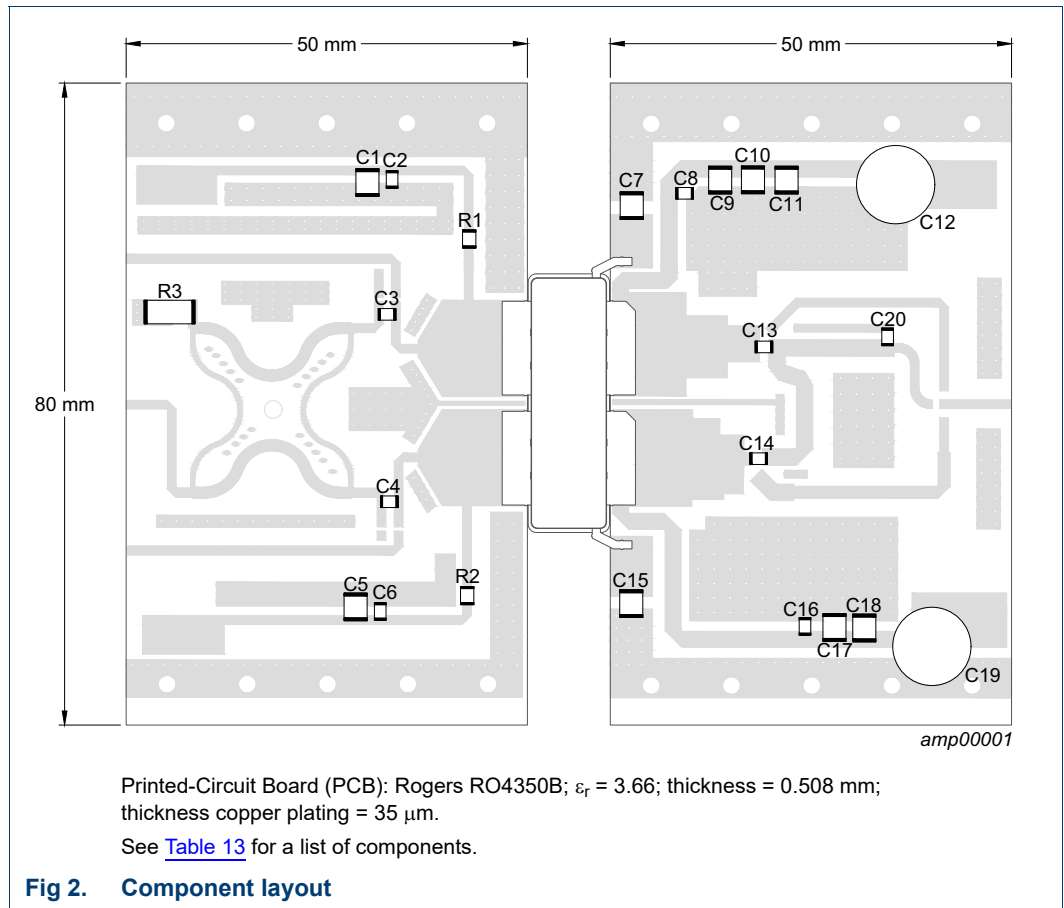
f (MHz)	Z <sub>S</sub> [1] (Ω)	Z <sub>L</sub> [1] (Ω)	P <sub>L</sub> [2] (dBm)	η <sub>D</sub> [3] (%)	G <sub>p</sub> [3] (dB)
1805	1.03 – j4.87	2.56 – j1.80	50.48	63.6	21.2
1843	2.10 – j4.50	2.84 – j1.96	50.46	64.0	21.4
1880	1.58 – j5.07	3.14 – j2.12	50.40	64.0	21.5

[1] Z<sub>S</sub> and Z<sub>L</sub> defined in [Figure 1](#).

[2] at 3 dB gain compression.

[3] at P<sub>L(AV)</sub> = 49 dBm.

7.4 Test circuit



**Table 13. List of components**  
See [Figure 2](#) for component layout.

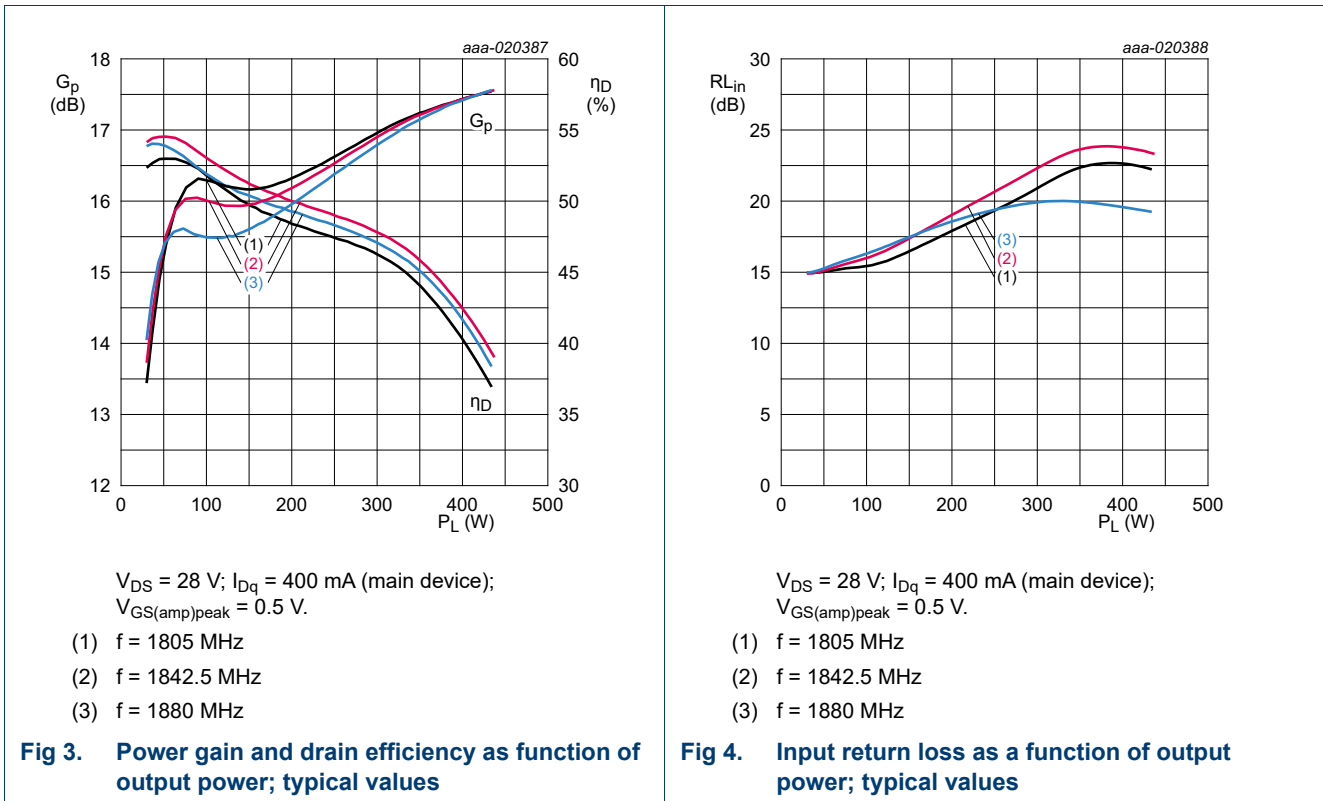
Component	Description	Value	Remarks
C1, C5, C7, C9, C10, C11, C15, C17, C18	multilayer ceramic chip capacitor	10 $\mu\text{F}$ , 50 V	[1]
C2, C3, C4, C6, C8, C16	multilayer ceramic chip capacitor	36 pF	[2]
C12, C19	electrolytic capacitor	1000 $\mu\text{F}$ , 63 V	
C13	multilayer ceramic chip capacitor	10 pF	[2]
C14	multilayer ceramic chip capacitor	27 pF	[2]
C20	multilayer ceramic chip capacitor	0.1 pF	[2]
R1, R2	resistor	5.1 $\Omega$	SMD 0805
R3	resistor	50 $\Omega$	SMD 0805

[1] Murata or capacitor of same quality

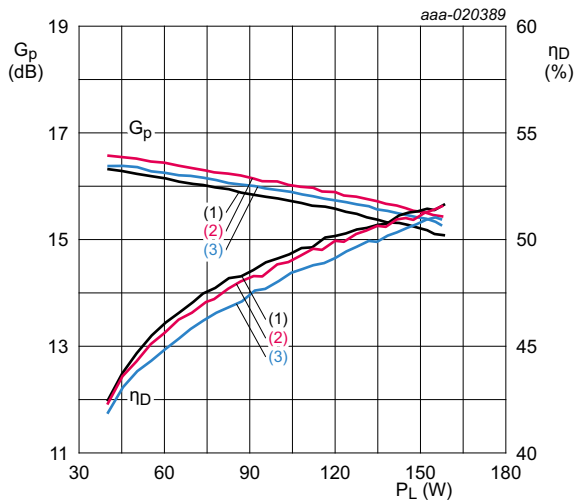
[2] American Technical Ceramics type 600F or capacitor of same quality

7.5 Graphical data

7.5.1 Pulsed CW

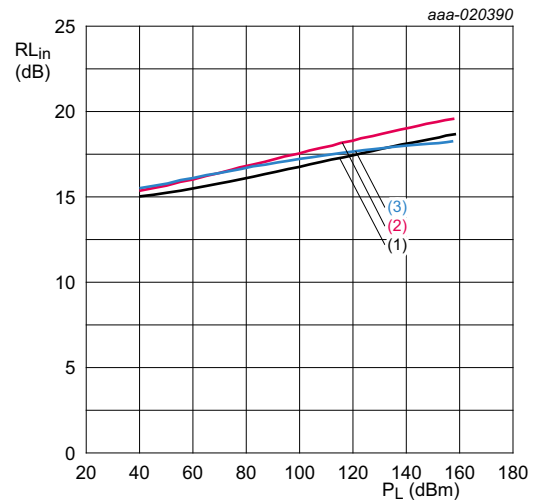


7.5.2 1-Carrier W-CDMA



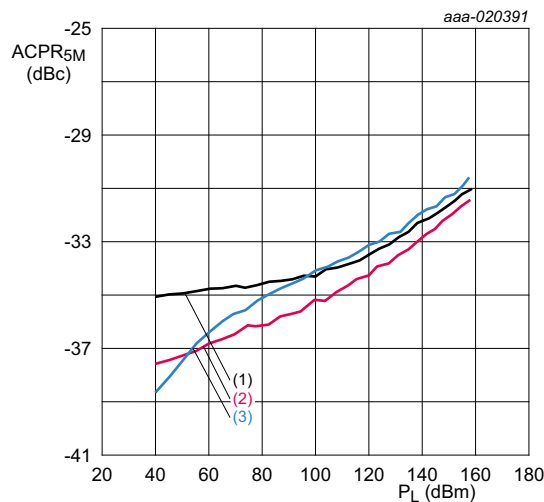
$V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA (main device)}; V_{GS(amp)peak} = 0.5\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

**Fig 5. Power gain and drain efficiency as function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA (main device)}; V_{GS(amp)peak} = 0.5\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

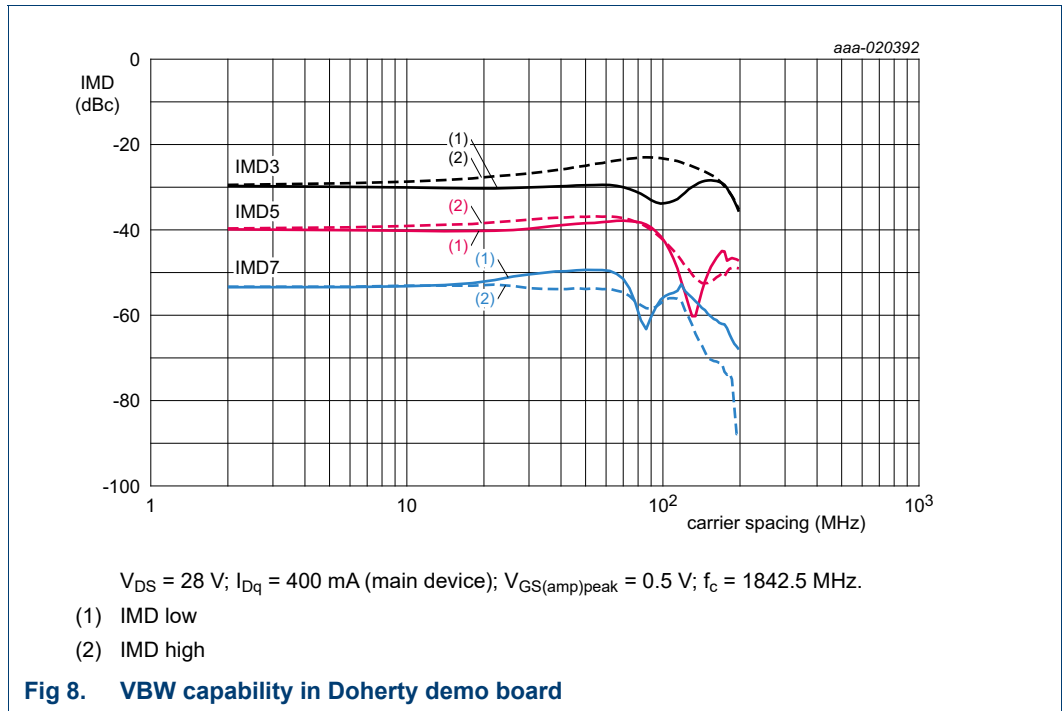
**Fig 6. Input return loss as a function of output power; typical values**



$V_{DS} = 28\text{ V}; I_{Dq} = 400\text{ mA (main device)}; V_{GS(amp)peak} = 0.5\text{ V}.$   
 (1)  $f = 1805\text{ MHz}$   
 (2)  $f = 1842.5\text{ MHz}$   
 (3)  $f = 1880\text{ MHz}$

**Fig 7. Adjacent channel power ratio (5 MHz) as a function of output power; typical values**

7.5.3 2-Tone VBW



### 8. Package outline

Air cavity plastic earless flanged package; 6 leads

SOT1258-1

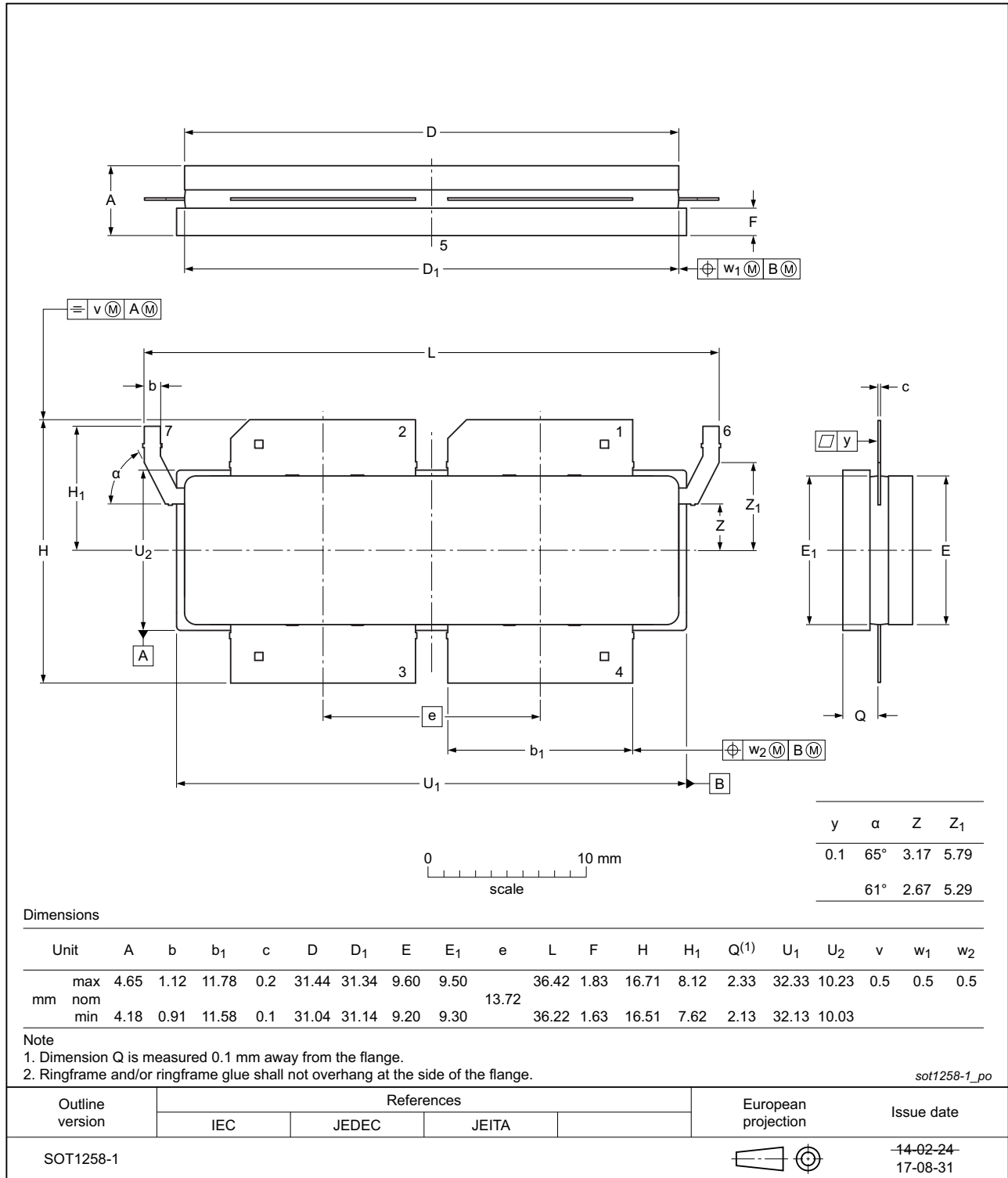


Fig 9. Package outline SOT1258-1

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

**Table 14. ESD sensitivity**

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A <a href="#">[1]</a>
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 <a href="#">[2]</a>

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V, but fails after exposure to an ESD pulse of 750 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V, but fails after exposure to an ESD pulse of 4000 V.

## 10. Abbreviations

**Table 15. Abbreviations**

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DPCH	Dedicated Physical CHannel
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
VBW	Video BandWidth
W-CDMA	Wideband Code Division Multiple Access

## 11. Revision history

**Table 16. Revision history**

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLC9G20LS-470AVT v.3	20171124	Product data sheet	-	BLC9G20LS-470AVT v.2
Modifications:	<ul style="list-style-type: none"> <li>• <a href="#">Table 2 on page 2</a>: changed simplified version drawing SOT1258-3 to SOT1258-1</li> <li>• <a href="#">Table 3 on page 2</a>: changed version SOT1258-3 to SOT1258-1</li> <li>• <a href="#">Figure 2 on page 6</a>: updated figure</li> <li>• <a href="#">Figure 9 on page 10</a>: changed package outline drawing SOT1258-3 to SOT1258-1</li> </ul>			
BLC9G20LS-470AVT v.2	20161202	Product data sheet	-	BLC9G20LS-470AVT v.1
BLC9G20LS-470AVT v.1	20160224	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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Date of release: 24 November 2017  
 Document identifier: BLC9G20LS-470AVT

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