



**THE DATASHEET OF  
BLF178P,112**



## 1. Product profile

### 1.1 General description

A 1200 W LDMOS power transistor for broadcast applications and industrial applications in the HF to 110 MHz band.

Table 1. Application information

Test signal	f (MHz)	V <sub>DS</sub> (V)	P <sub>L</sub> (W)	G <sub>p</sub> (dB)	η <sub>D</sub> (%)
CW	108	50	1000	26	75
pulsed RF	108	50	1200	28.5	75

### 1.2 Features and benefits

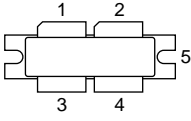
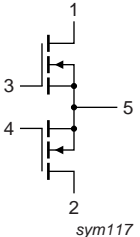
- Typical pulsed performance at frequency of 108 MHz, a supply voltage of 50 V and an I<sub>Dq</sub> of 40 mA, a t<sub>p</sub> of 100 μs with δ of 20 %:
  - ◆ Output power = 1200 W
  - ◆ Power gain = 28.5 dB
  - ◆ Efficiency = 75 %
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (10 MHz to 110 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Industrial, scientific and medical applications
- FM transmitter applications

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF178P	-	flanged balanced LDMOST ceramic package; 2 mounting holes; 4 leads	SOT539A

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

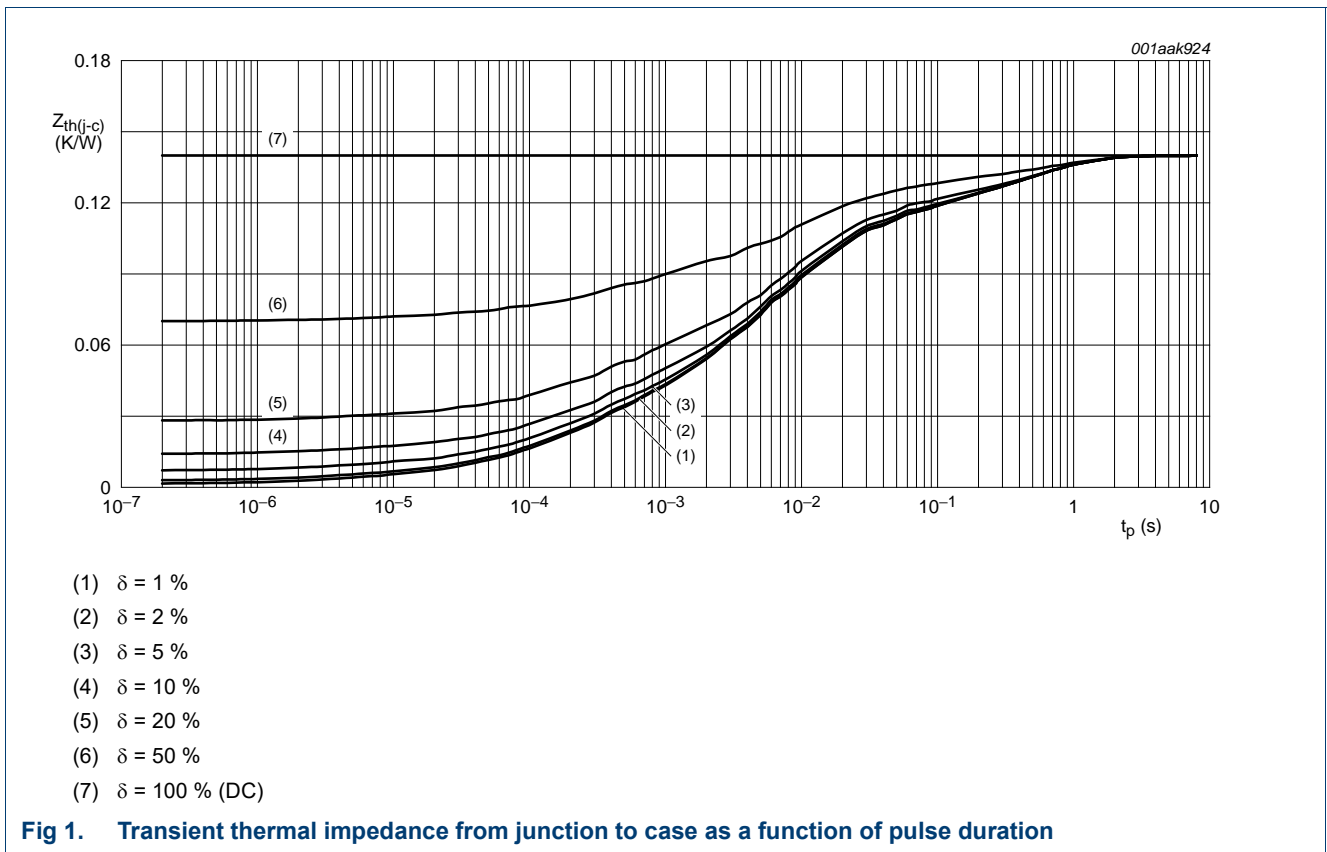
Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	110	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$I_D$	drain current		-	88	A
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature		-	225	°C

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 150\text{ }^\circ\text{C}$	[1][2] 0.14	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ }^\circ\text{C}; t_p = 100\text{ }\mu\text{s}; \delta = 20\text{ }\%$	[3] 0.04	K/W

- [1]  $T_j$  is the junction temperature.
- [2]  $R_{th(j-c)}$  is measured under RF conditions.
- [3] See [Figure 1](#).



## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

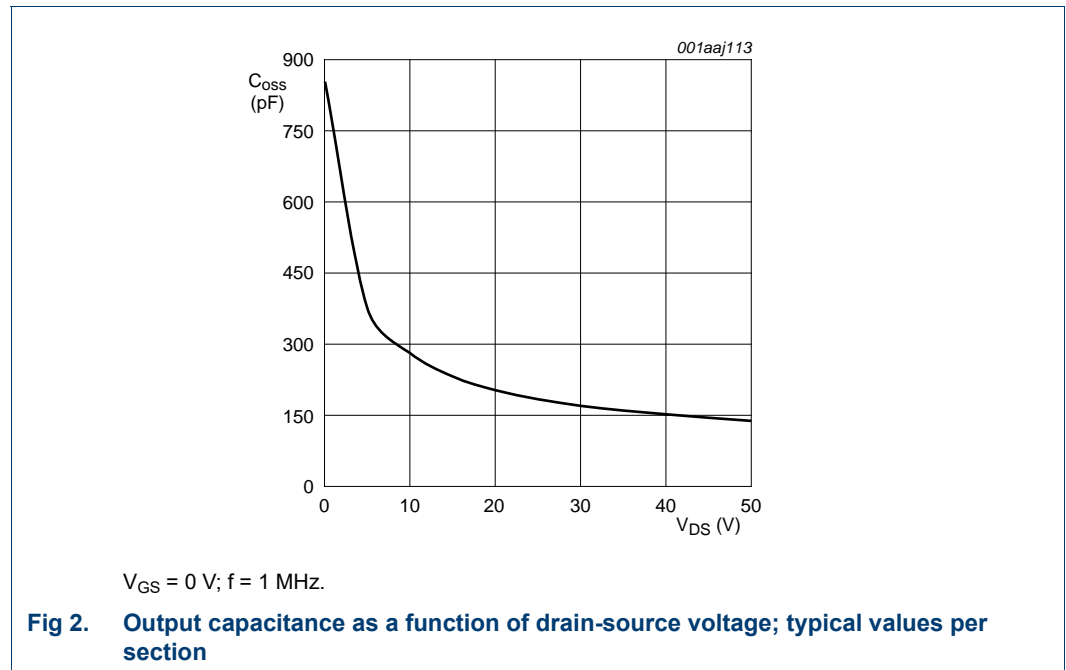
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.5\text{ mA}$	110	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 500\text{ mA}$	1.25	1.7	2.25	V
$V_{GSq}$	gate-source quiescent voltage	$V_{DS} = 50\text{ V}; I_D = 20\text{ mA}$	0.8	1.3	1.8	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	2.8	$\mu\text{A}$

**Table 6. DC characteristics ...continued**  
 $T_j = 25\text{ }^\circ\text{C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $V_{DS} = 10\text{ V}$	58	71	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 11\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}$ ; $I_D = 16.66\text{ A}$	-	0.07	-	$\Omega$
$C_{rs}$	feedback capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	3	-	pF
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	403	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 50\text{ V}$ ; $f = 1\text{ MHz}$	-	138	-	pF

**Table 7. RF characteristics**  
 Test signal: pulsed RF;  $t_p = 100\text{ }\mu\text{s}$ ;  $\delta = 20\%$ ;  $f = 108\text{ MHz}$ ; RF performance at  $V_{DS} = 50\text{ V}$ ;  
 $I_{DQ} = 40\text{ mA}$ ;  $T_{case} = 25\text{ }^\circ\text{C}$ ; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$G_p$	power gain	$P_L = 1200\text{ W}$	27	28.5	31	dB
$RL_{in}$	input return loss	$P_L = 1200\text{ W}$	-	-16	-12	dB
$\eta_D$	drain efficiency	$P_L = 1200\text{ W}$	71	75	-	%



### 6.1 Ruggedness in class-AB operation

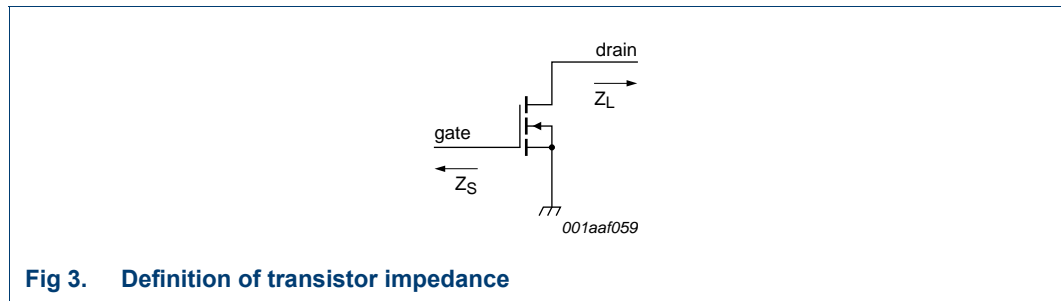
The BLF178P is capable of withstanding a load mismatch corresponding to  $VSWR = 13 : 1$  through all phases under the following conditions:  $V_{DS} = 50\text{ V}$ ;  
 $I_{DQ} = 40\text{ mA}$ ;  $P_L = 1200\text{ W}$  pulsed;  $f = 108\text{ MHz}$ .

## 7. Test information

### 7.1 Impedance information

**Table 8. Typical impedance**  
Simulated  $Z_S$  and  $Z_L$  test circuit impedances.

f	$Z_S$	$Z_L$
MHz	$\Omega$	$\Omega$
108	$3.91 - j3.56$	$3.59 - j1.73$

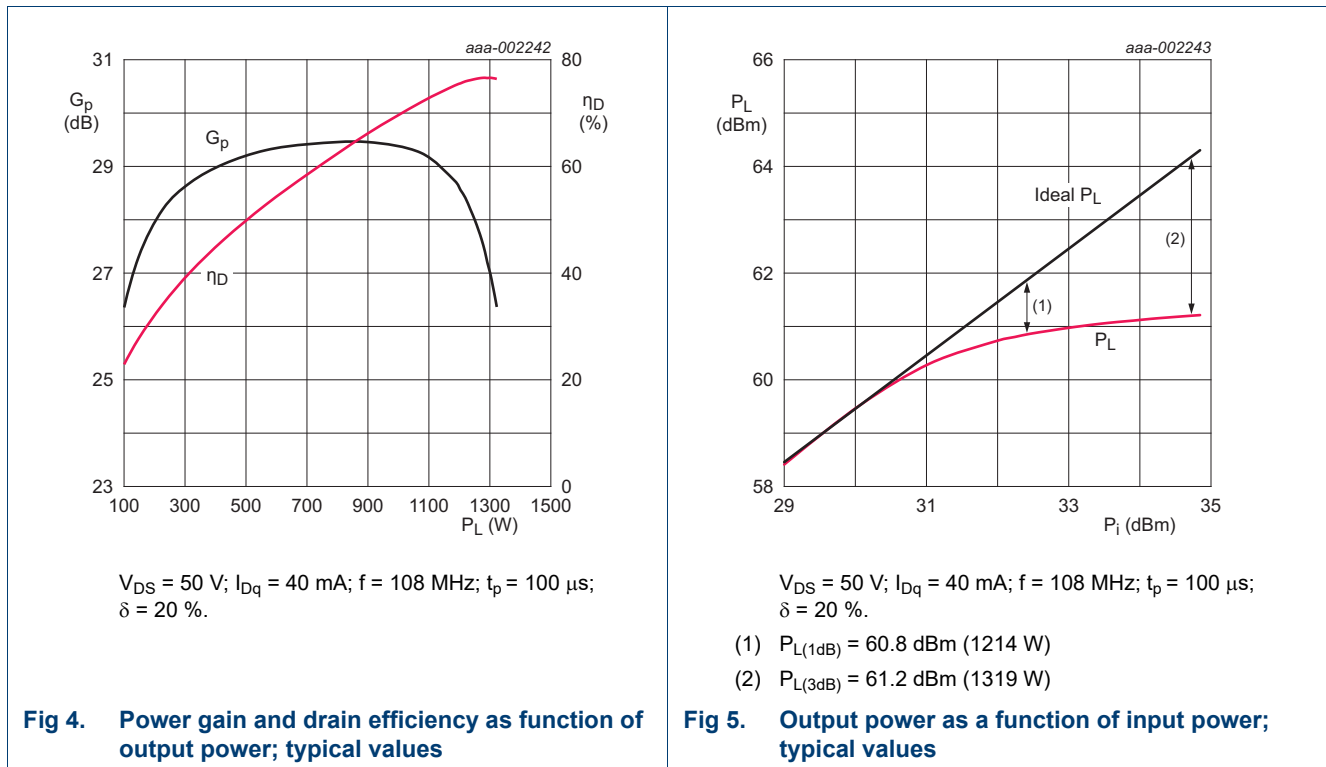


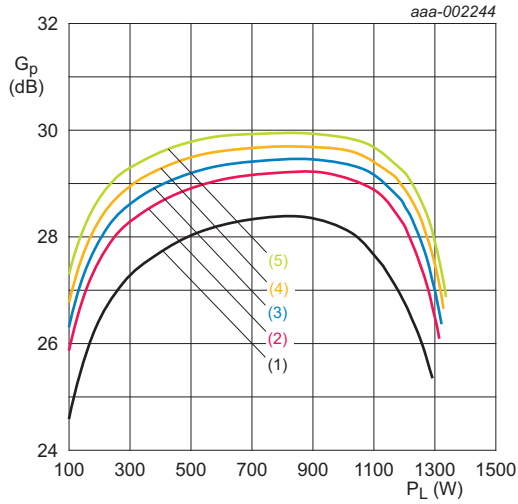
**Fig 3. Definition of transistor impedance**

### 7.2 RF performance

The following figures are measured in a class-AB production test circuit.

#### 7.2.1 1-Tone CW pulsed

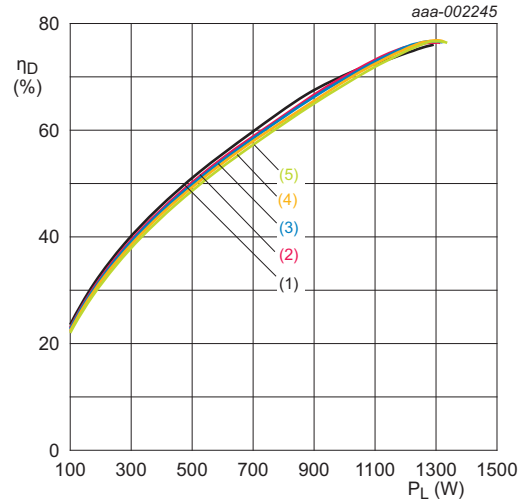




$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$ .

- (1)  $I_{Dq} = 0 \text{ mA}$
- (2)  $I_{Dq} = 20 \text{ mA}$
- (3)  $I_{Dq} = 40 \text{ mA}$
- (4)  $I_{Dq} = 80 \text{ mA}$
- (5)  $I_{Dq} = 160 \text{ mA}$

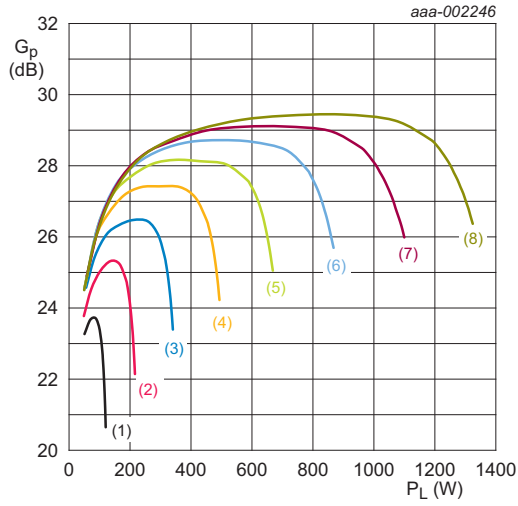
**Fig 6. Power gain as a function of output power; typical values**



$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$ .

- (1)  $I_{Dq} = 0 \text{ mA}$
- (2)  $I_{Dq} = 20 \text{ mA}$
- (3)  $I_{Dq} = 40 \text{ mA}$
- (4)  $I_{Dq} = 80 \text{ mA}$
- (5)  $I_{Dq} = 160 \text{ mA}$

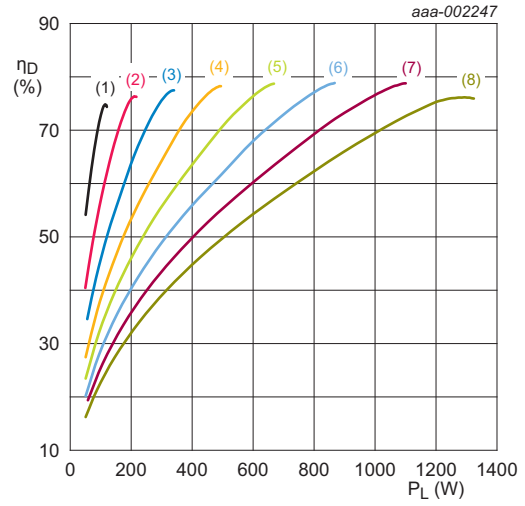
**Fig 7. Drain efficiency as a function of output power; typical values**



$I_{Dq} = 40 \text{ mA}$ ;  $f = 108 \text{ MHz}$ ;  $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 20 \text{ \%}$ .

- (1)  $V_{DS} = 15 \text{ V}$
- (2)  $V_{DS} = 20 \text{ V}$
- (3)  $V_{DS} = 25 \text{ V}$
- (4)  $V_{DS} = 30 \text{ V}$
- (5)  $V_{DS} = 35 \text{ V}$
- (6)  $V_{DS} = 40 \text{ V}$
- (7)  $V_{DS} = 45 \text{ V}$
- (8)  $V_{DS} = 50 \text{ V}$

**Fig 8. Power gain as a function of output power; typical values**

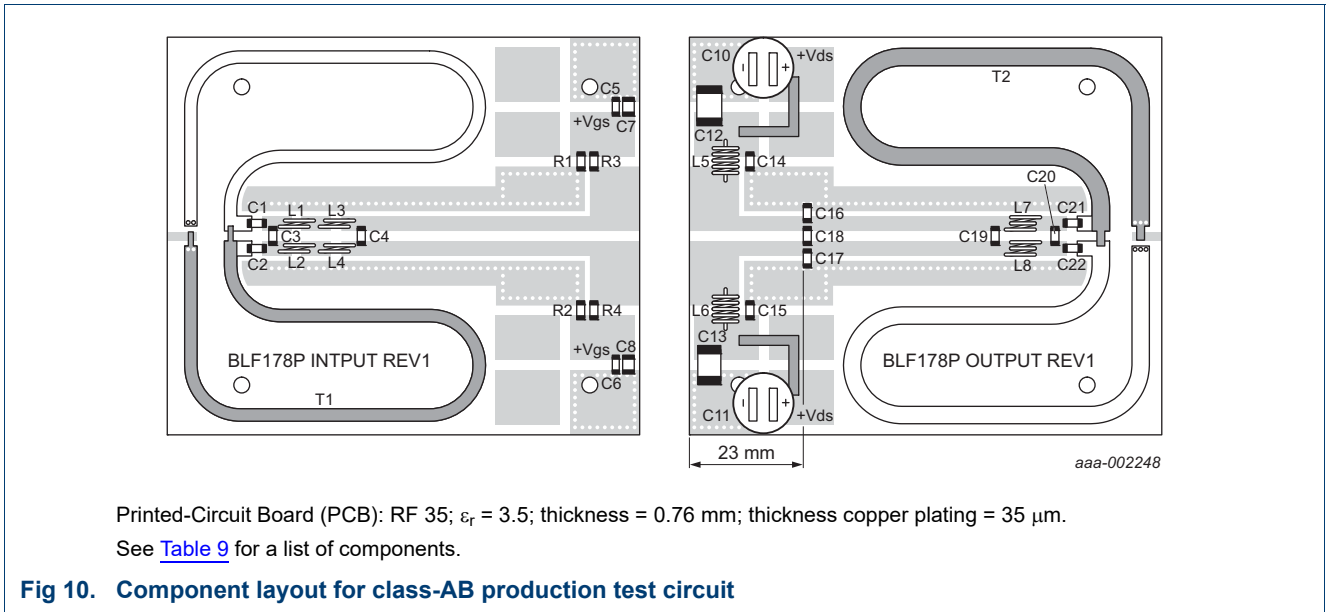


$I_{Dq} = 40 \text{ mA}$ ;  $f = 108 \text{ MHz}$ ;  $t_p = 100 \text{ }\mu\text{s}$ ;  $\delta = 20 \text{ \%}$ .

- (1)  $V_{DS} = 15 \text{ V}$
- (2)  $V_{DS} = 20 \text{ V}$
- (3)  $V_{DS} = 25 \text{ V}$
- (4)  $V_{DS} = 30 \text{ V}$
- (5)  $V_{DS} = 35 \text{ V}$
- (6)  $V_{DS} = 40 \text{ V}$
- (7)  $V_{DS} = 45 \text{ V}$
- (8)  $V_{DS} = 50 \text{ V}$

**Fig 9. Drain efficiency as a function of output power; typical values**

7.3 Test circuit



**Table 9. List of components**

For test circuit see [Figure 10](#).

Component	Description	Value	Remarks
C1, C2, C5, C6, C14, C15, C21, C22	multilayer ceramic chip capacitor	1 nF	[1]
C3	multilayer ceramic chip capacitor	82 pF	[1]
C4	multilayer ceramic chip capacitor	240 pF	[1]
C7, C8	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ ; 50 V	
C10, C11	electrolytic capacitor	1000 $\mu\text{F}$ ; 63 V	
C12, C13	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ ; 100 V	
C16, C17	multilayer ceramic chip capacitor	120 pF	[1]
C18	multilayer ceramic chip capacitor	82 pF	[1]
C19	multilayer ceramic chip capacitor	110 pF	[1]
C20	multilayer ceramic chip capacitor	56 pF	[1]
L1, L2, L3, L4	1.5 turn 0.8 mm copper wire	D = 3 mm; length = 2 mm	
L5, L6	5 turn 0.8 mm copper wire	D = 3 mm; length = 4.5 mm	
L7, L8	2.5 turn 0.8 mm copper wire	D = 3 mm; length = 3 mm	
R1, R2	SMD resistor	100 $\Omega$	Philips 1206
R3, R4	SMD resistor	9.1 $\Omega$	Philips 1206
T1	semi rigid coax	25 $\Omega$ ; 160 mm	UT-090C-25
T2	semi rigid coax	25 $\Omega$ ; 160 mm	UT-141C-25

[1] American Technical Ceramics type 800B or capacitor of same quality.

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

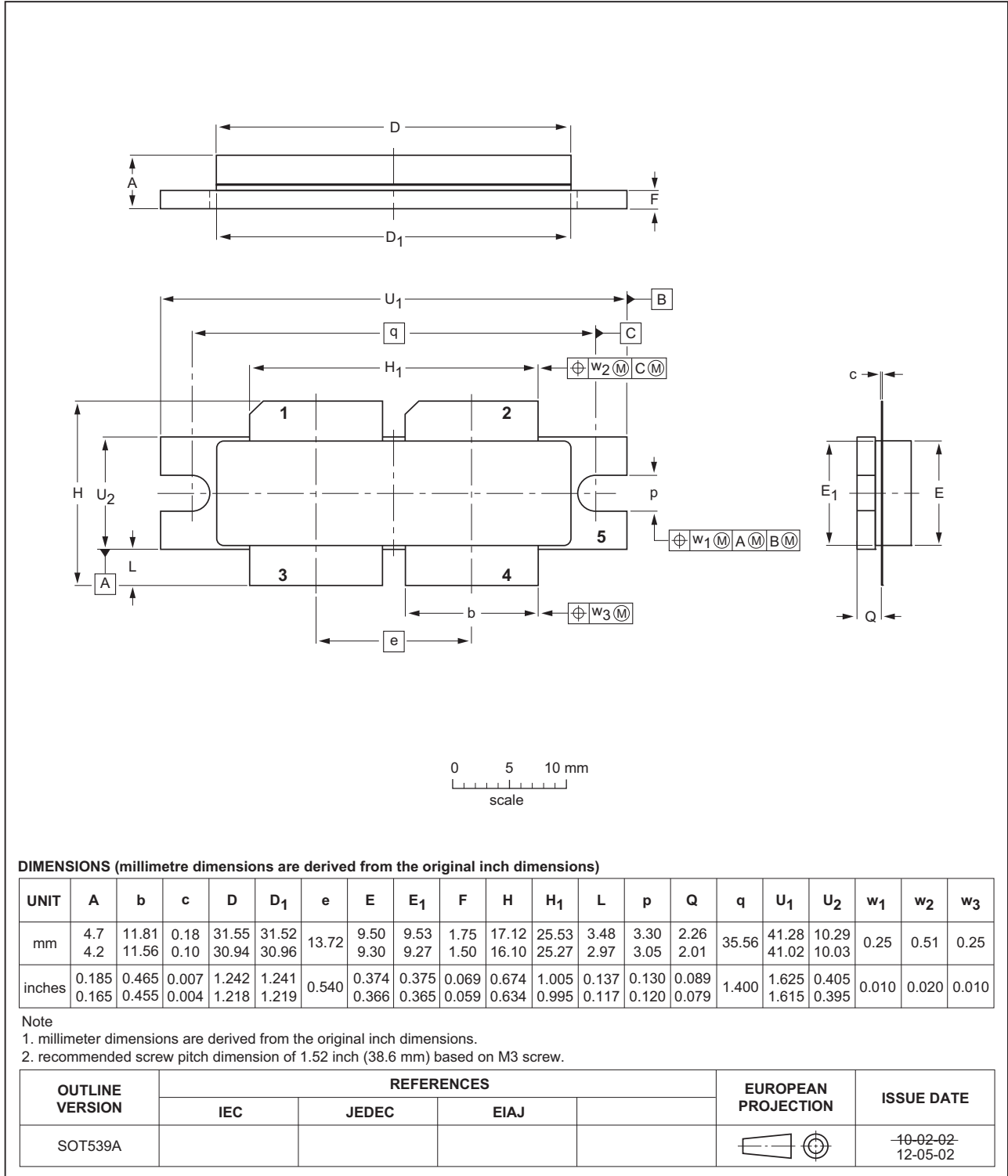


Fig 11. Package outline SOT539A

## 9. Handling information

### CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
DC	Direct Current
ESD	ElectroStatic Discharge
FM	Frequency Modulation
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
RF	Radio Frequency
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF178P#3	20150901	Product data sheet	-	BLF178P v.2
Modifications:	<ul style="list-style-type: none"> <li>The format of this document has been redesigned to comply with the new identity guidelines of Ampleon.</li> <li>Legal texts have been adapted to the new company name where appropriate.</li> </ul>			
BLF178P v.2	20120216	Product data sheet	-	BLF178P v.1
BLF178P v.1	20110405	Objective data sheet	-	-

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Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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