



**THE DATASHEET OF
BLF182XRSU**



BLF182XR; BLF182XRS

Power LDMOS transistor

Rev. 3 — 3 February 2016

AMMPELON

Product data sheet

1. Product profile

1.1 General description

A 250 W extremely rugged LDMOS power transistor for broadcast and industrial applications in the HF to 600 MHz band.

Table 1. Application information

Test signal	f	V _{DS}	P _L	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	108	50	250	28	75
CW	81.36	50	235	28	82

1.2 Features and benefits

- Easy power control
- Integrated double sided ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 600 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLF182XR (SOT1121A)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
BLF182XRS (SOT1121B)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF182XR	-	flanged LDMOST ceramic package; 2 mounting holes; 4 leads	SOT1121A
BLF182XRS	-	earless flanged ceramic package; 4 leads	SOT1121B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	135	V
V_{GS}	gate-source voltage		-6	+11	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

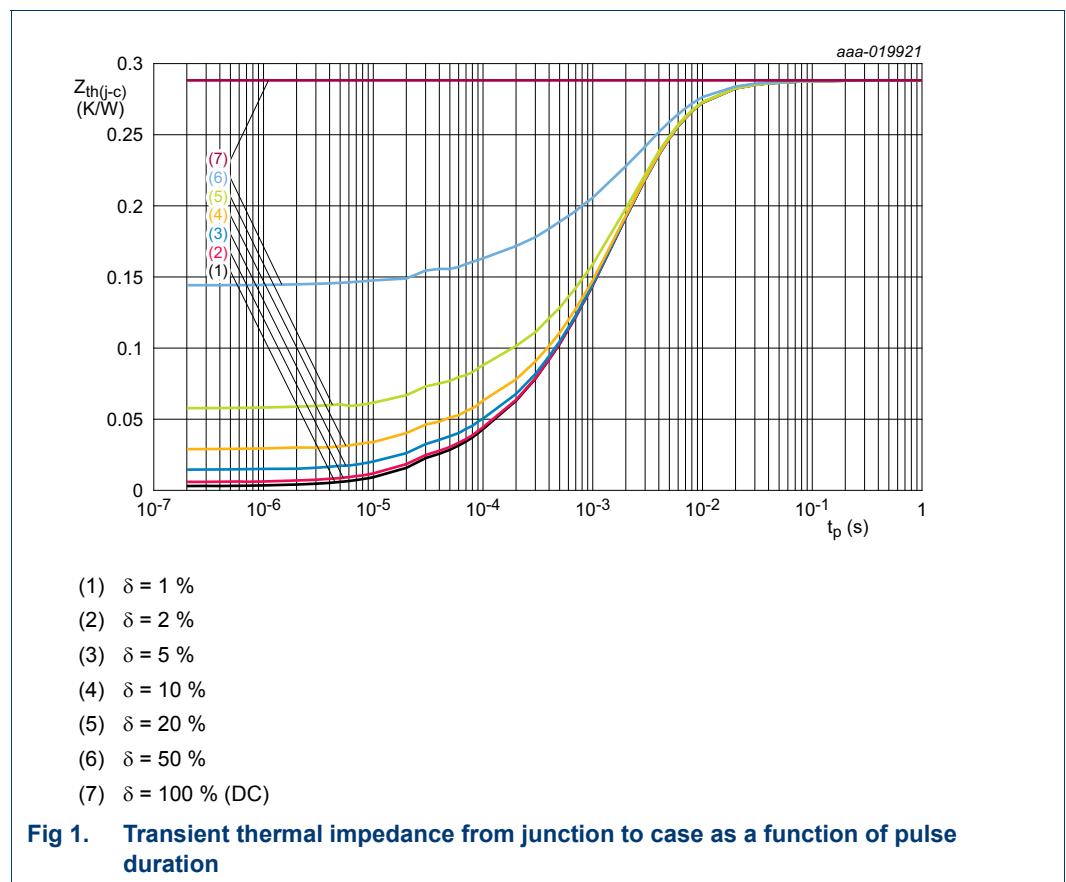
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	$T_j = 115\text{ °C}$ [1][2]	0.29	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_j = 150\text{ °C}$; $t_p = 100\text{ }\mu\text{s}$; $\delta = 20\%$ [3]	0.088	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}$; $I_D = 1.0\text{ mA}$	135	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}$; $I_D = 100\text{ mA}$	1.33	1.9	2.33	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50\text{ V}$; $I_D = 50\text{ mA}$	-	2.1	-	V

Table 6. DC characteristics ...continued
T_j = 25 °C; per section unless otherwise specified.

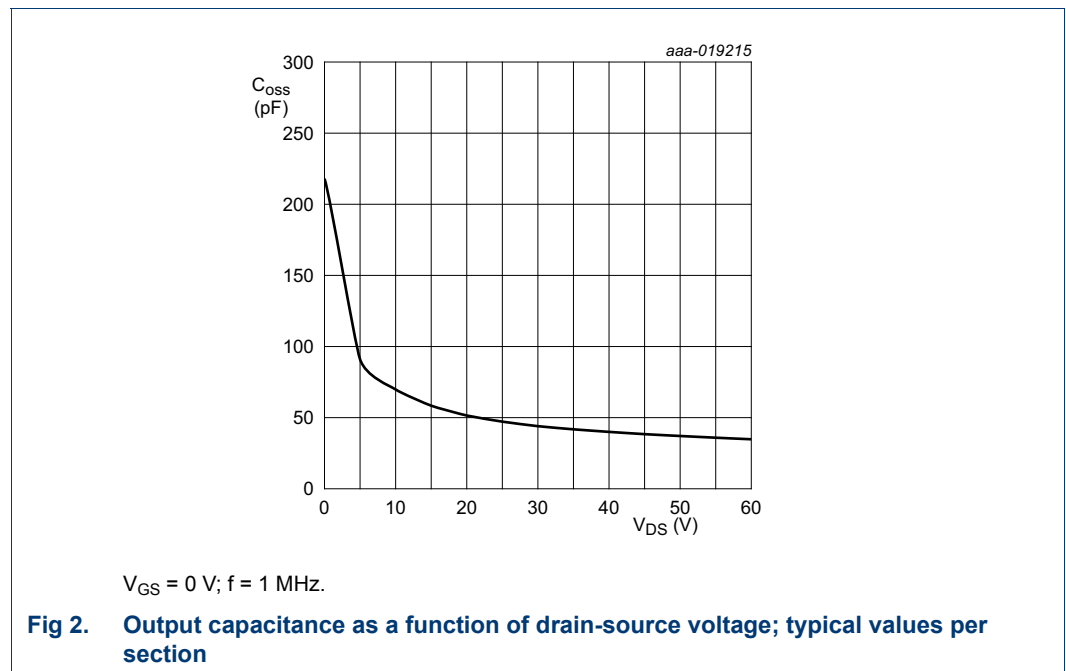
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	1.4	μA
I _{DSX}	drain cut-off current	V _{GS} = V _{GS(th)} + 3.75 V; V _{DS} = 10 V	-	15	-	A
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = V _{GS(th)} + 3.75 V; I _D = 3.5 A	-	0.40	-	Ω

Table 7. AC characteristics
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C _{rs}	feedback capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	0.7	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	116	-	pF
C _{oss}	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	37	-	pF

Table 8. RF characteristics
Test signal: pulsed RF; t_p = 100 μs; δ = 20 %; f = 108 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 100 mA; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G _p	power gain	P _L = 250 W	26.8	28	-	dB
RL _{in}	input return loss	P _L = 250 W	-	-12	-9	dB
η _D	drain efficiency	P _L = 250 W	72	75	-	%



7. Test information

7.1 Ruggedness in class-AB operation

The BLF182XR and BLF182XRS are capable of withstanding a load mismatch corresponding to VSWR > 65 : 1 through all phases under the following conditions: $V_{DS} = 50\text{ V}$; $I_{DQ} = 100\text{ mA}$; $P_L = 250\text{ W}$ pulsed; $f = 108\text{ MHz}$.

7.2 Impedance information

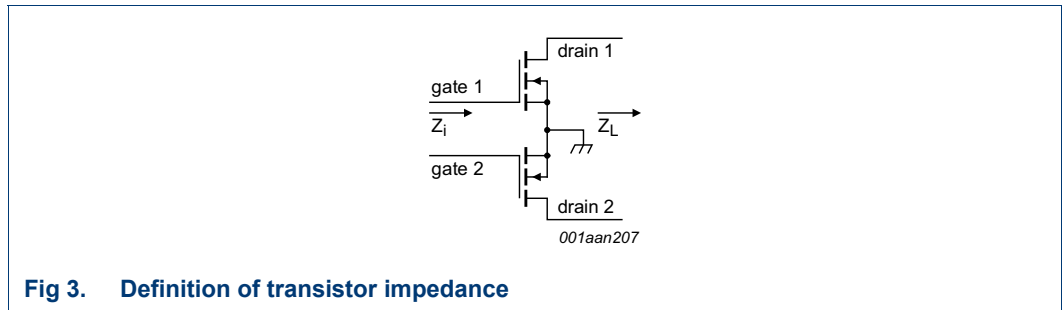


Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at $V_{DS} = 50\text{ V}$ and $P_L = 250\text{ W}$.

f (MHz)	Z_i (Ω)	Z_L (Ω)
108	14.9 – 49.5j	15.3 + 3.5j

7.3 UIS avalanche energy

Table 10. Typical avalanche data per section

$T_{amb} = 25\text{ }^\circ\text{C}$; typical test data; test jig without water cooling.

I_{AS} (A)	E_{AS} (J)
8	2.0
9	1.2
10	0.9

For information see application note AN10273.

7.4 Test circuit

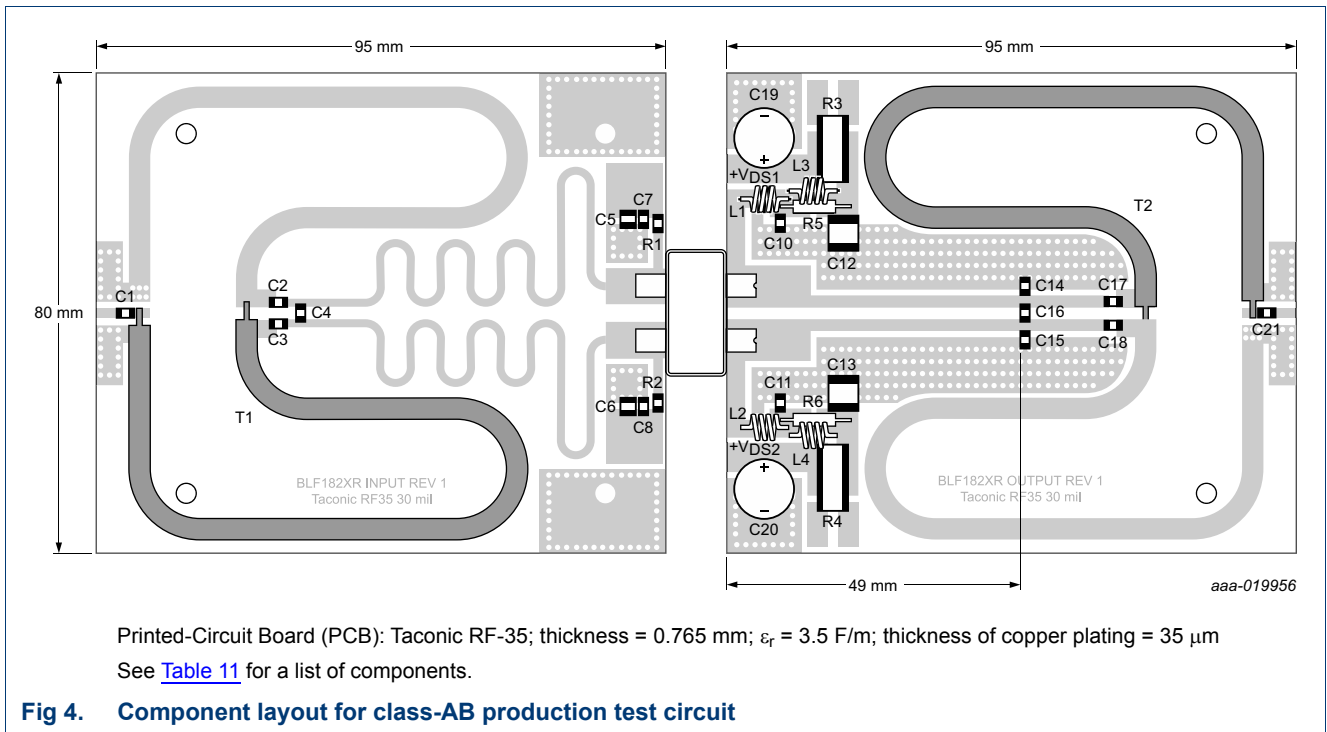


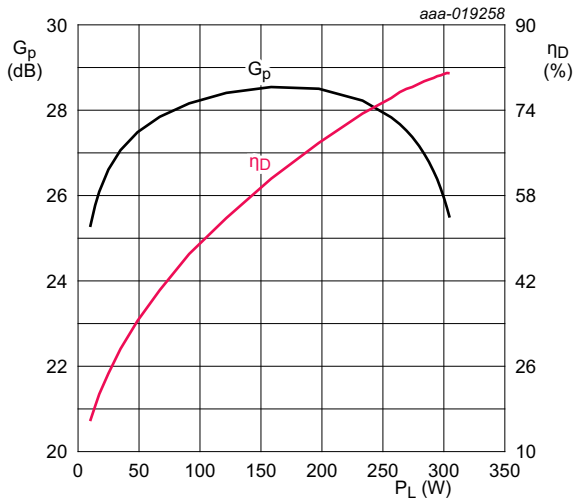
Table 11. List of components

For test circuit see [Figure 4](#).

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	510 pF	[1]
C2, C3	multilayer ceramic chip capacitor	220 pF	[1]
C4	multilayer ceramic chip capacitor	91 pF	[1]
C5, C6	multilayer ceramic chip capacitor	4.7 μF , 50 V	
C7, C8, C10, C11	multilayer ceramic chip capacitor	820 pF	[1]
C12, C13	multilayer ceramic chip capacitor	4.7 μF , 100 V	
C14, C15	multilayer ceramic chip capacitor	43 pF	[1]
C16	multilayer ceramic chip capacitor	6.8 pF	[1]
C17, C18	multilayer ceramic chip capacitor	130 pF	[1]
C19, C20	electrolytic capacitor	2200 μF , 64 V	
C21	multilayer ceramic chip capacitor	56 pF	[1]
L1, L2	copper wire inductor	10 turns, D = 2 mm, d = 0.5 mm	
L3, L4	copper wire inductor	6 turns, D = 2 mm, d = 0.5 mm	
R1, R2	chip resistor	4.7 k Ω	SMD 1206
R3, R4	shunt resistor	0.01 Ω	Ohmite: FC4L110R010FER
R5, R6	metal film resistor	10 Ω , 0.6 W	
T1, T2	semi rigid coax	50 Ω , 160 mm	EZ Form: EZ-141-AL-TP-M17

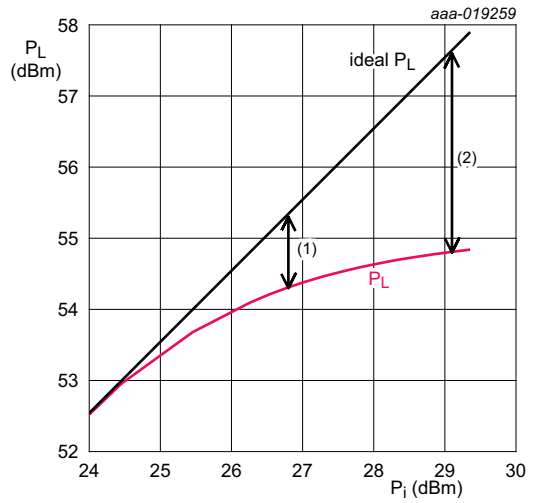
[1] American Technical Ceramics type 100B or capacitor of same quality.

7.5 Graphical data



$V_{DS} = 50 \text{ V}$; $I_{Dq} = 100 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$;
 $\delta = 20 \text{ \%}$.

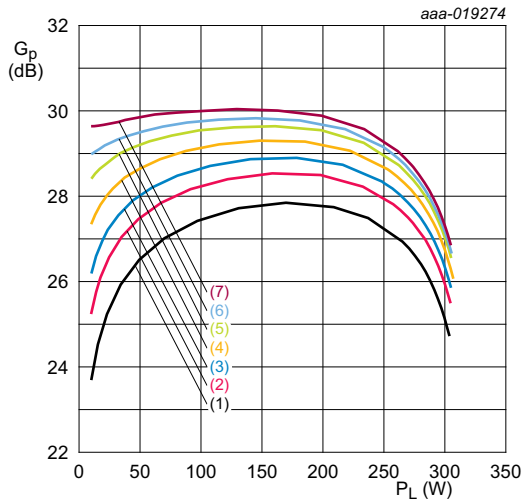
Fig 5. Power gain and drain efficiency as function of output power; typical values



$V_{DS} = 50 \text{ V}$; $I_{Dq} = 100 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$;
 $\delta = 20 \text{ \%}$.

- (1) $P_{L(1dB)} = 54.3 \text{ dBm}$ (269 W)
- (2) $P_{L(3dB)} = 54.8 \text{ dBm}$ (304 W)

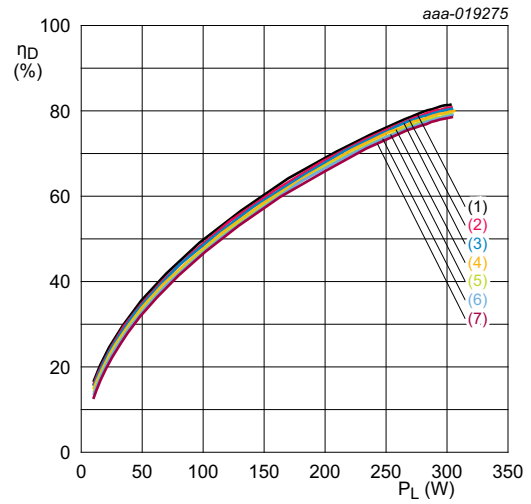
Fig 6. Output power as a function of input power; typical values



$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 400 \text{ mA}$
- (5) $I_{Dq} = 600 \text{ mA}$
- (6) $I_{Dq} = 800 \text{ mA}$
- (7) $I_{Dq} = 1000 \text{ mA}$

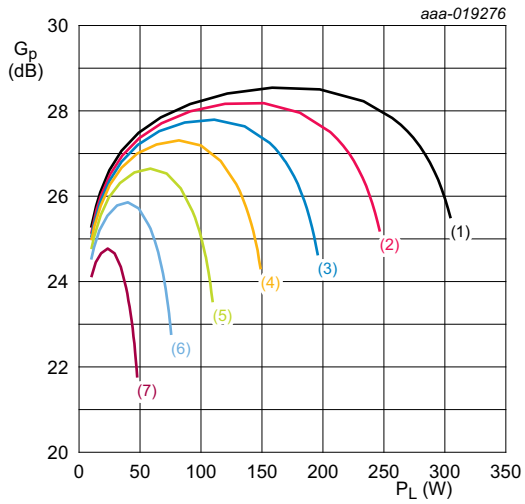
Fig 7. Power gain as a function of output power; typical values



$V_{DS} = 50 \text{ V}; f = 108 \text{ MHz}; t_p = 100 \text{ }\mu\text{s}; \delta = 20 \text{ \%}$.

- (1) $I_{Dq} = 20 \text{ mA}$
- (2) $I_{Dq} = 100 \text{ mA}$
- (3) $I_{Dq} = 200 \text{ mA}$
- (4) $I_{Dq} = 400 \text{ mA}$
- (5) $I_{Dq} = 600 \text{ mA}$
- (6) $I_{Dq} = 800 \text{ mA}$
- (7) $I_{Dq} = 1000 \text{ mA}$

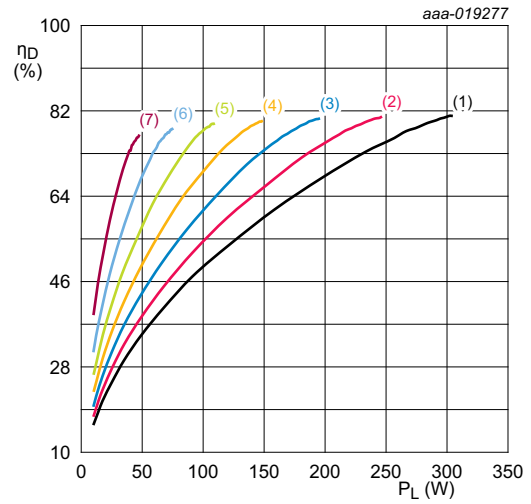
Fig 8. Drain efficiency as a function of output power; typical values



$I_{Dq} = 100 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$; $\delta = 20 \text{ \%}$.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



$I_{Dq} = 100 \text{ mA}$; $f = 108 \text{ MHz}$; $t_p = 100 \text{ }\mu\text{s}$; $\delta = 20 \text{ \%}$.

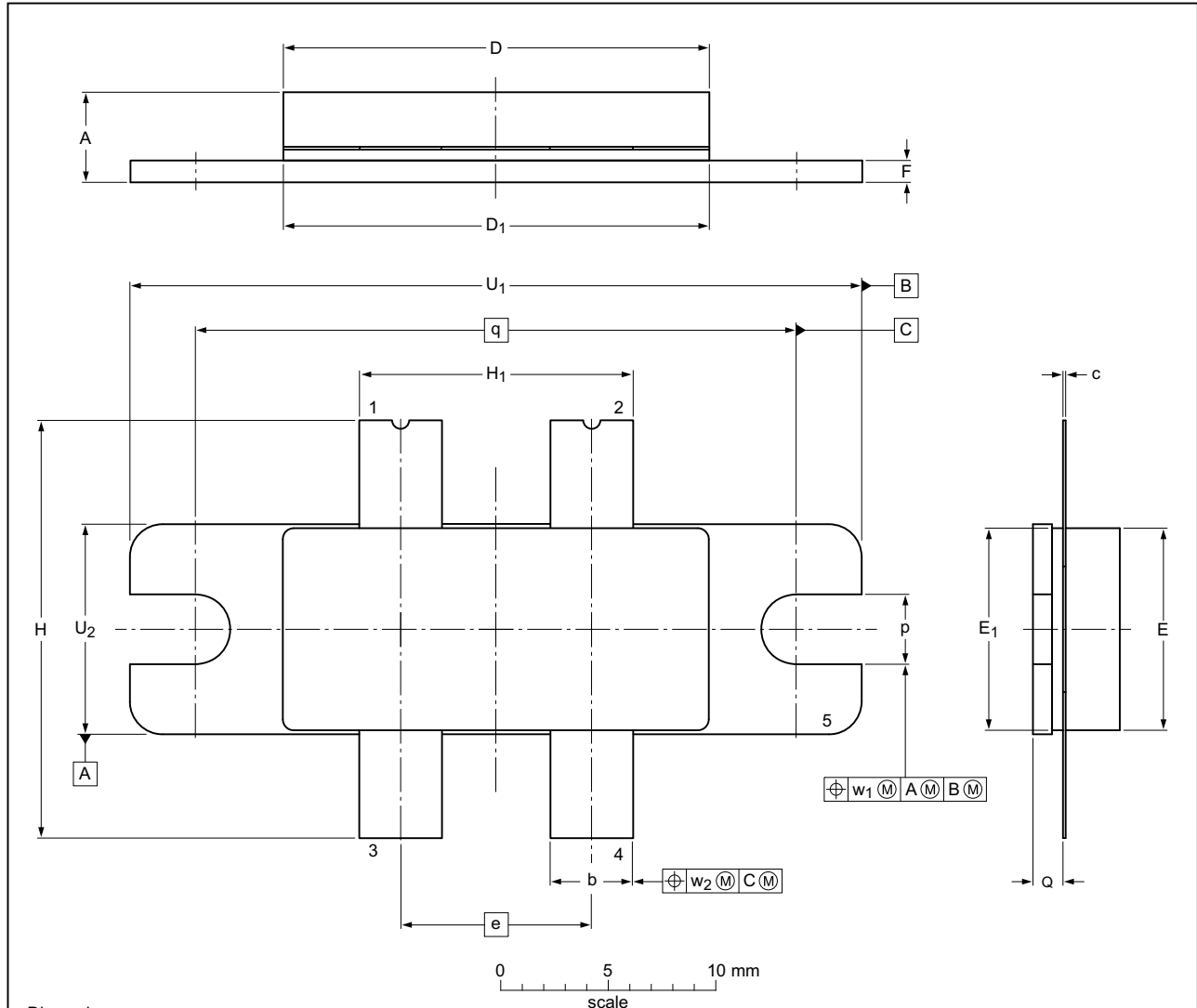
- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged LDMOST ceramic package; 2 mounting holes; 4 leads

SOT1121A



Dimensions

Unit ⁽¹⁾	A	b	c	D	D ₁	e	E	E ₁	F	H	H ₁	p	Q ⁽²⁾	q	U ₁	U ₂	w ₁	w ₂
mm	max 4.75	3.94	0.18	20.02	19.96		9.53	9.53	1.14	19.94	12.83	3.38	1.70		34.16	9.91		
	nom					8.89								27.94			0.25	0.51
	min	3.45	3.68	0.10	19.61	19.66	9.27	9.27	0.89	18.92	12.57	3.12	1.45		33.91	9.65		
inches	max 0.187	0.155	0.007	0.788	0.786		0.375	0.375	0.045	0.785	0.505	0.133	0.067		1.345	0.39		
	nom					0.35								1.1			0.01	0.02
	min	0.136	0.145	0.004	0.772	0.774	0.365	0.365	0.035	0.745	0.495	0.123	0.057		1.335	0.38		

Note

- 1. millimeter dimensions are derived from the original inch dimensions.
- 2. dimension is measured 0.030 inch (0.76 mm) from the body.

sot1121a_po

Outline version	References			European projection	Issue date
	IEC	JEDEC	JEITA		
SOT1121A					09-10-12 10-02-02

Fig 11. Package outline SOT1121A

Earless flanged ceramic package; 4 leads

SOT1121B

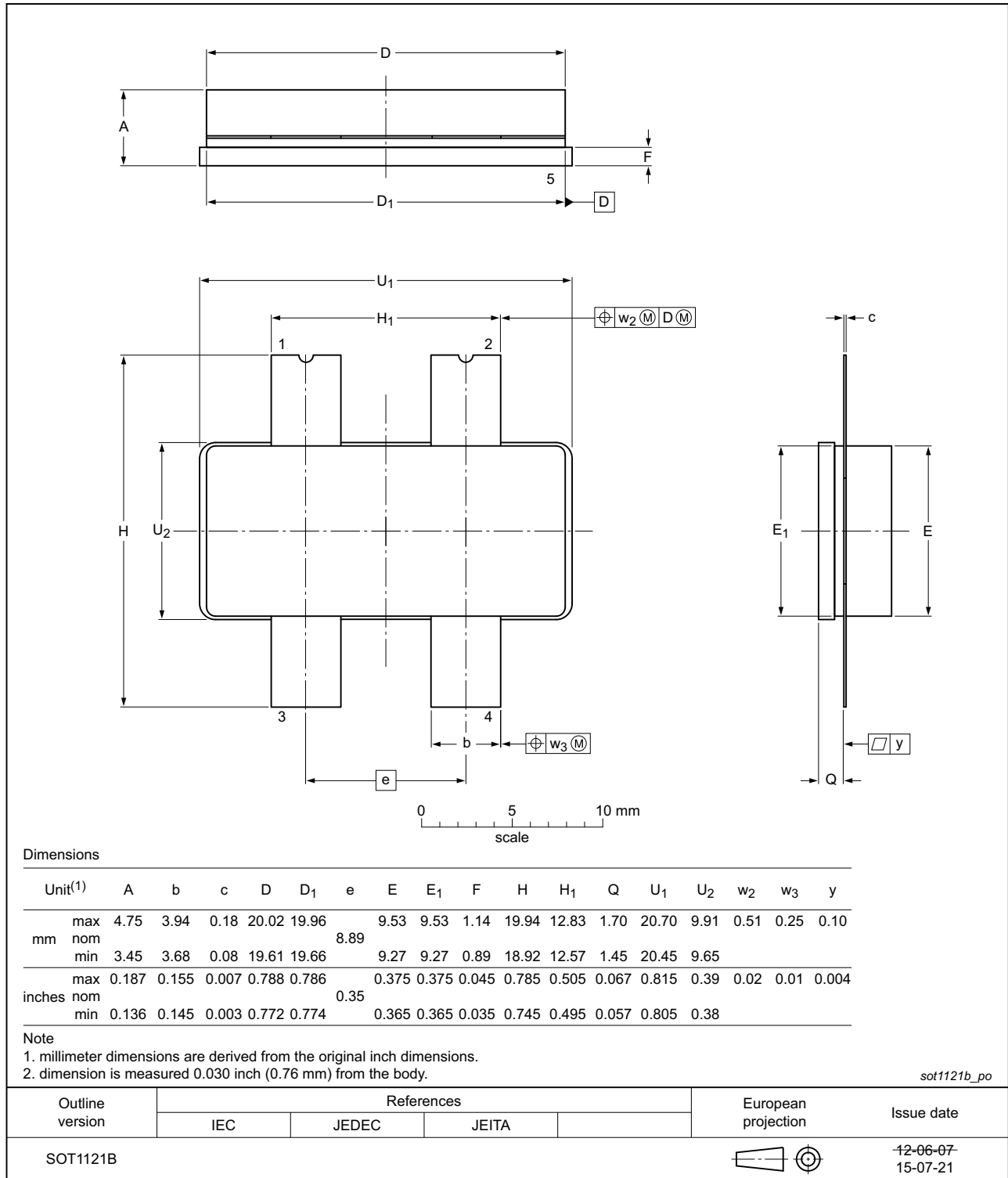


Fig 12. Package outline SOT1121B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
LDMOST	Laterally Diffused Metal-Oxide Semiconductor Transistor
MTF	Median Time to Failure
SMD	Surface Mounted Device
UIS	Unclamped Inductive Switching
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF182XR_BLF182XRS v.3	20160203	Product data sheet	-	BLF182XR_BLF182XRS#2
Modifications:	<ul style="list-style-type: none"> • Table 1 on page 1: table has been updated • Section 1.2 on page 1: section has been updated • Table 5 on page 3: table has been updated • Figure 1 on page 3: figure has been added • Table 6 on page 3: table has been updated • Table 8 on page 4: table has been updated • Table 9 on page 5: some values have been added • Table 10 on page 5: table has been updated • Section 7.4 on page 6: section has been added • Section 7.5 on page 7: section has been added 			
BLF182XR_BLF182XRS#2	20150901	Objective data sheet	-	BLF182XR_BLF182XRS v.1
BLF182XR_BLF182XRS v.1	20150723	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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 Document identifier: BLF182XR_BLF182XRS

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