



**THE DATASHEET OF  
BLF888DSU**



# BLF888D; BLF888DS

UHF power LDMOS transistor

Rev. 4 — 18 February 2016

AMPLEON

Product data sheet

## 1. Product profile

### 1.1 General description

A 600 W LDMOS RF power transistor for broadcast Doherty transmitter applications. The excellent ruggedness of this device makes it ideal for digital and analog transmitter applications.

**Table 1. Application information**

*RF performance at  $V_{DS} = 50$  V in an ultra wide Doherty application.*

Test signal	f	$P_{L(AV)}$	$G_p$	$\eta_D$	$IMD_{shldr}$	PAR
	(MHz)	(W)	(dB)	(%)	(dBc)	(dB)
DVB-T (8k OFDM)	470 to 860	115 to 134 [1]	17	40 to 48 [1]	-38 to -44 [2]	8 [3]

[1] Depending on selected channel.

[2] Depending on exciter used.

[3] PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

### 1.2 Features and benefits

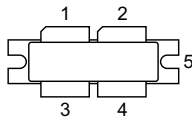
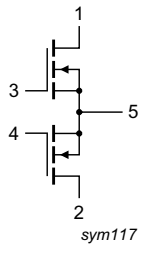
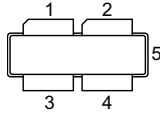
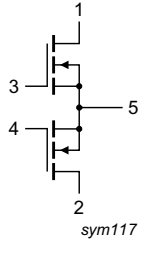
- High efficiency
- High power gain
- Excellent ruggedness (VSWR  $\geq$  40 : 1 through all phases)
- Excellent thermal stability
- Integrated ESD protection
- One Doherty design covers the full bandwidth from 470 MHz to 860 MHz
- Internal input matching for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

### 1.3 Applications

- Broadcast transmitter applications in the UHF band
- Digital broadcasting

## 2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
<b>BLF888D (SOT539A)</b>			
1	drain1 (peak)		 sym117
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source <a href="#">[1]</a>		
<b>BLF888DS (SOT539B)</b>			
1	drain1 (peak)		 sym117
2	drain2 (main)		
3	gate1 (peak)		
4	gate2 (main)		
5	source <a href="#">[1]</a>		

[1] Connected to flange.

## 3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF888D	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLF888DS	-	earless flanged balanced ceramic package; 4 leads	SOT539B

## 4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage		-	104	V
$V_{GS}$	gate-source voltage		-0.5	+11	V
$T_{stg}$	storage temperature		-65	+150	°C
$T_j$	junction temperature	<a href="#">[1]</a>	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

## 5. Thermal characteristics

**Table 5. Thermal characteristics**

Symbol	Parameter	Conditions	Typ	Unit	
$R_{th(j-c)}$	thermal resistance from junction to case	$T_{case} = 75\text{ °C}; V_{DS} = 50\text{ V}; I_{DS} = 2.7\text{ A (main)}; I_{DS} = 0\text{ A (peak)}$	[1]	0.27	K/W
		$T_{case} = 90\text{ °C}; V_{DS} = 50\text{ V}; P_L = 115\text{ W}; PAR = 8\text{ dB}$	[2]	0.16	K/W

[1] Measured under DC test conditions, with peak section off.

[2] Measured in an ultra wide Doherty application, using a DVB-T (8k OFDM) signal, PAR (of output signal) at 0.01 % probability on CCDF; PAR of input signal = 9.5 dB at 0.01 % probability on CCDF.

## 6. Characteristics

**Table 6. DC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 2.4\text{ mA}$	104	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 240\text{ mA}$	1.4	1.9	2.4	V
$I_{DSS}$	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	0.061	2.8	$\mu\text{A}$
$I_{DSX}$	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	37	-	A
$I_{GSS}$	gate leakage current	$V_{GS} = 10\text{ V}; V_{DS} = 0\text{ V}$	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 8.5\text{ A}$	-	120	-	$\text{m}\Omega$

**Table 7. AC characteristics**

$T_j = 25\text{ °C}$ ; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	210	-	pF
$C_{oss}$	output capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	70	-	pF
$C_{rss}$	reverse transfer capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}; f = 1\text{ MHz}$	-	1.3	-	pF

**Table 8. RF characteristics**

$V_{DS} = 50\text{ V}; I_{Dq} = 1.3\text{ A}; T_{case} = 25\text{ °C}$  unless otherwise specified; in a class-AB production test circuit.

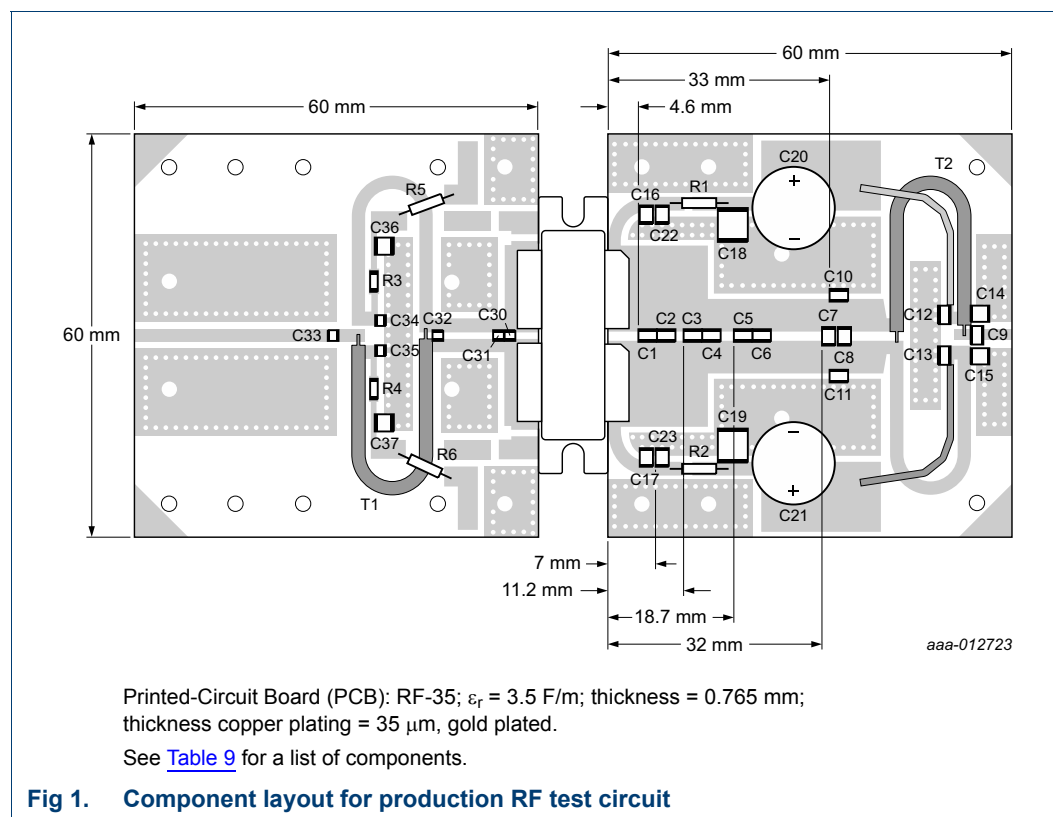
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Test signal: 2-tone CW</b>						
$P_{L(AV)}$	average output power	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	-	250	-	W
$G_p$	power gain	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	19	21	-	dB
$\eta_D$	drain efficiency	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	43	45	-	%
IMD3	third-order intermodulation distortion	$f_1 = 860\text{ MHz}; f_2 = 860.1\text{ MHz}$	-	-32	-29	dBc
<b>Test signal: pulsed CW</b>						
$P_{L(3dB)}$	output power at 3 dB gain compression	$f = 860\text{ MHz}; t_p = 100\text{ }\mu\text{s}; \delta = 10\text{ %}$	540	580	-	W

## 7. Test information

### 7.1 Ruggedness in Doherty operation

The BLF888D and BLF888DS are capable of withstanding a load mismatch corresponding to  $V_{SWR} \geq 40 : 1$  through all phases under the following conditions:  $V_{DS} = 50 \text{ V}$ ;  $f = 810 \text{ MHz}$  at rated load power.

### 7.2 Test circuit



**Table 9. List of components**

For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	12 pF	[1]
C2, C3, C4, C5, C6	multilayer ceramic chip capacitor	8.2 pF	[1]
C7	multilayer ceramic chip capacitor	6.8 pF	[2]
C8	multilayer ceramic chip capacitor	4.7 pF	[2]
C9, C12, C13	multilayer ceramic chip capacitor	100 pF	[1]
C10, C11	multilayer ceramic chip capacitor	10 pF	[1]
C14, C15	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 50 V	
C16, C17	multilayer ceramic chip capacitor	3.6 pF	[2]
C18, C19	multilayer ceramic chip capacitor	4.7 $\mu\text{F}$ , 50 V	
C20, C21	electrolytic capacitor	470 $\mu\text{F}$ , 63 V	

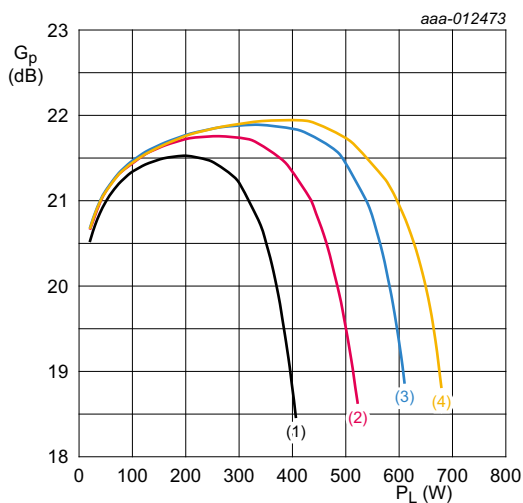
**Table 9. List of components ...continued**  
For test circuit see [Figure 1](#).

Component	Description	Value	Remarks
C22, C23	multilayer ceramic chip capacitor	47 pF	[2]
C30	multilayer ceramic chip capacitor	15 pF	[3]
C31	multilayer ceramic chip capacitor	5.6 pF	[3]
C32	multilayer ceramic chip capacitor	2.7 pF	[3]
C33, C34, C35	multilayer ceramic chip capacitor	100 pF	[3]
C36, C37	multilayer ceramic chip capacitor	470 μF, 50 V	
R1, R2	resistor	10 Ω	
R3, R4	resistor	5.6 Ω	SMD 1206
R5, R6	resistor	100 Ω	
R3, R4	resistor	510 Ω	SMD 1206
T1, T2	semi rigid coax	25 Ω, length = 160 mm	Micro-Coax UT-090C-25

- [1] American Technical Ceramics type 180R or capacitor of same quality.
- [2] American Technical Ceramics type 100B or capacitor of same quality.
- [3] American Technical Ceramics type 100A or capacitor of same quality.

### 7.3 Graphical data

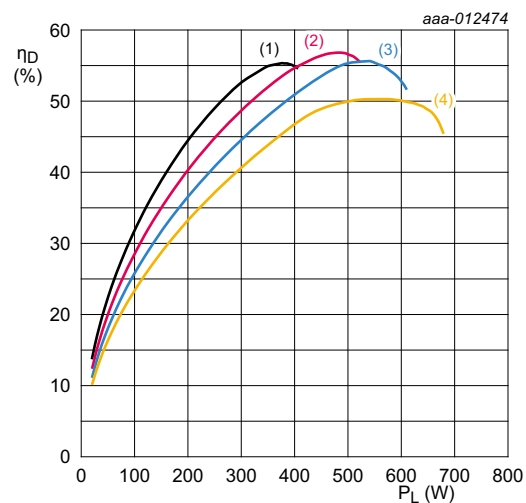
#### 7.3.1 1-Tone CW pulsed



$I_{Dq} = 2 \times 650 \text{ mA}$ ;  $t_p = 100 \text{ μs}$ ;  $\delta = 10 \%$ .

- (1)  $V_{DS} = 40 \text{ V}$
- (2)  $V_{DS} = 45 \text{ V}$
- (3)  $V_{DS} = 50 \text{ V}$
- (4)  $V_{DS} = 55 \text{ V}$

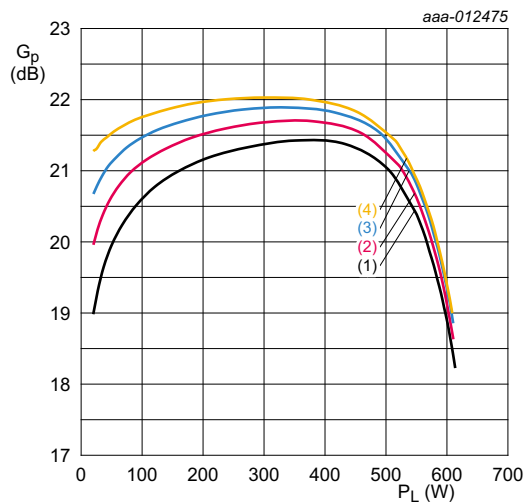
**Fig 2. Power gain as a function of output power; typical values**



$I_{Dq} = 2 \times 650 \text{ mA}$ ;  $t_p = 100 \text{ μs}$ ;  $\delta = 10 \%$ .

- (1)  $V_{DS} = 40 \text{ V}$
- (2)  $V_{DS} = 45 \text{ V}$
- (3)  $V_{DS} = 50 \text{ V}$
- (4)  $V_{DS} = 55 \text{ V}$

**Fig 3. Drain efficiency as a function of output power; typical values**



$V_{DS} = 50 \text{ V}$ ;  $t_p = 100 \mu\text{s}$ ;  $\delta = 10 \%$ .

- (1)  $I_{Dq} = 2 \times 250 \text{ mA}$
- (2)  $I_{Dq} = 2 \times 450 \text{ mA}$
- (3)  $I_{Dq} = 2 \times 650 \text{ mA}$
- (4)  $I_{Dq} = 2 \times 850 \text{ mA}$

**Fig 4. Power gain as a function of output power; typical values**

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

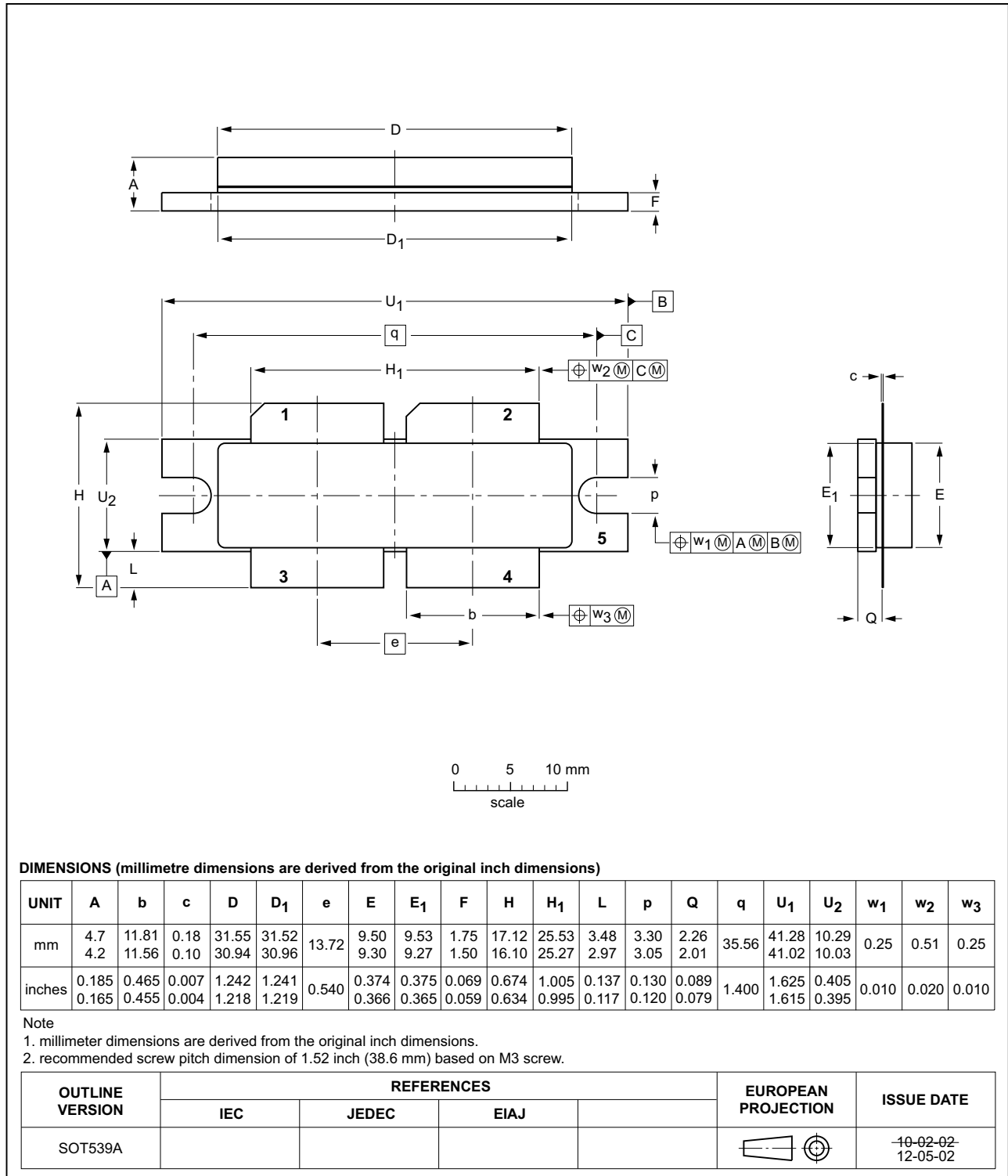


Fig 5. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

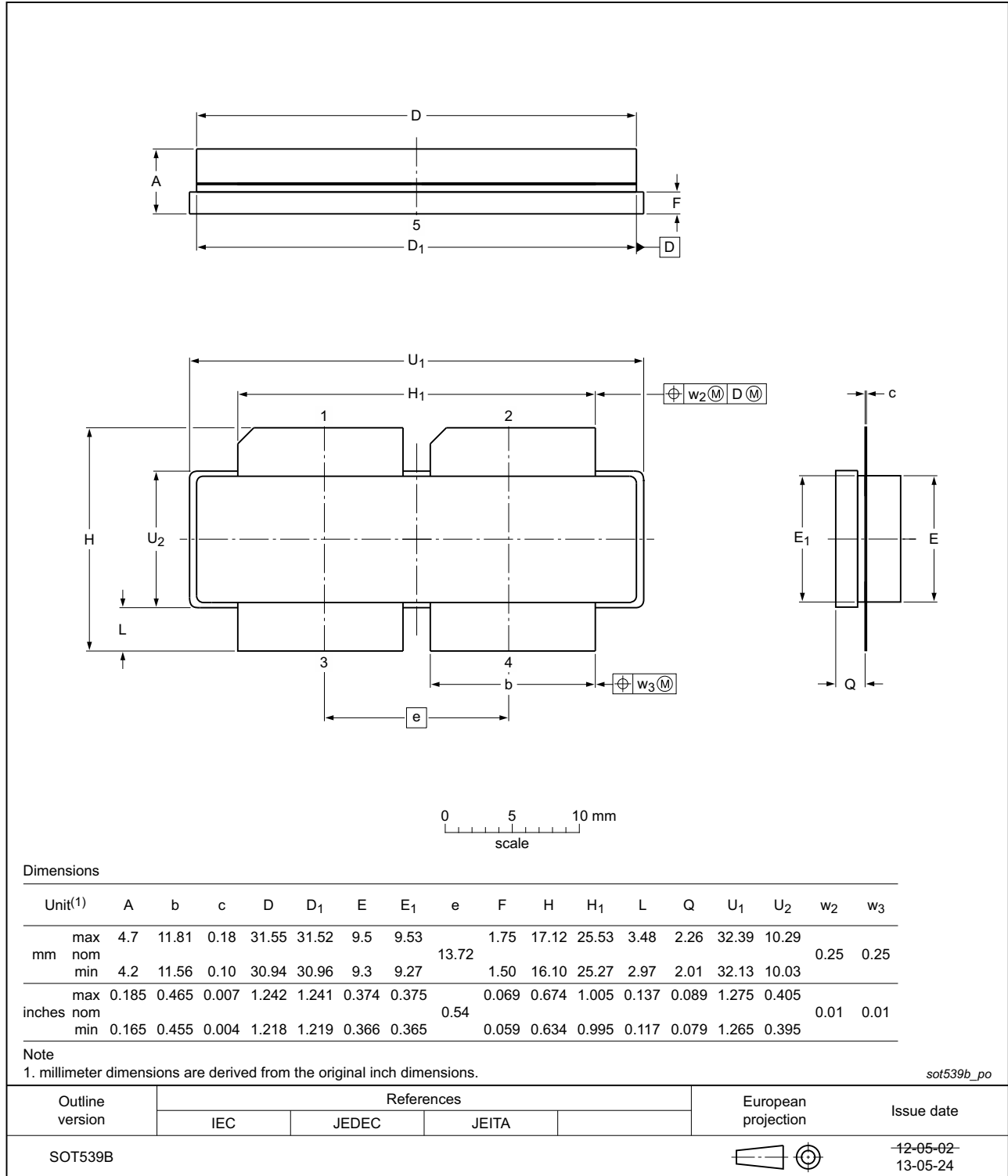


Fig 6. Package outline SOT539B

## 9. Handling information

**CAUTION**



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

## 10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Wave
DVB-T	Digital Video Broadcast - Terrestrial
ESD	ElectroStatic Discharge
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
OFDM	Orthogonal Frequency Division Multiplexing
PAR	Peak-to-Average Ratio
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VSWR	Voltage Standing-Wave Ratio

## 11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF888D_BLF888DS v.4	20160218	Product data sheet	-	BLF888D_BLF888DS#3
Modifications:	<ul style="list-style-type: none"> <li><a href="#">Table 8 on page 3</a>: unit of last row has been corrected from “dB” to “W”</li> </ul>			
BLF888D_BLF888DS#3	20150901	Product data sheet	-	BLF888D_BLF888DS v.2
BLF888D_BLF888DS v.2	20140627	Product data sheet	-	BLF888D_BLF888DS v.1
BLF888D_BLF888DS v.1	20140305	Objective data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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