



**THE DATASHEET OF
BSP612PH6327XTSA1**

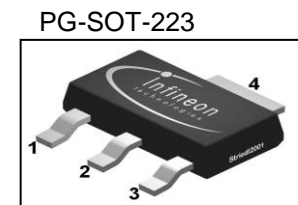
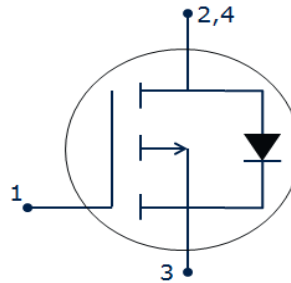


OptiMOS™-P Small-Signal-Transistor
Features

- P-channel
- Enhancement mode
- Logic level (4.5V rated)
- Avalanche rated
- Qualified according to AEC Q101
- 100% lead-free; RoHS compliant
- Halogen-free according to AEC61249-2-21

Product Summary

V_{DS}		-60	V
$R_{DS(on),max}$	$V_{GS}=10\text{ V}$	120	m Ω
	$V_{GS}=4.5\text{ V}$	170	
I_D		-3	A



Type	Package	Tape and Reel Information	Marking	Halogen Free	Packing
BSS612P	SOT223	H6327: 1000 pcs/ reel	BSP612P	Yes	Non dry

Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current	I_D	$T_A=25\text{ °C}$	-3.0	A
		$T_A=70\text{ °C}$	-2.44	
Pulsed drain current	$I_{D,pulse}$	$T_A=25\text{ °C}$	-12	
Avalanche energy, single pulse	E_{AS}	$I_D=-3\text{ A}$, $V_{DD}=-25\text{ V}$, $R_{GS}=25\text{ }\Omega$	150	mJ
Reverse diode dv/dt	dv/dt	$I_D=-3\text{ A}$, $V_{DS}=-48\text{ V}$, $di/dt=200\text{ A}/\mu\text{s}$, $T_{j,max}=150\text{ °C}$	6	kV/ μs
Gate source voltage	V_{GS}		± 20	V
Power dissipation ¹⁾	P_{tot}	$T_A=25\text{ °C}$	1.8	W
Operating and storage temperature	T_j, T_{stg}		-55 ... 150	$^{\circ}\text{C}$
ESD Class		JESD22-A114 -HBM	1C	V
Soldering Temperature			260 $^{\circ}\text{C}$	$^{\circ}\text{C}$
IEC climatic category; DIN IEC 68-1			55/150/56	$^{\circ}\text{C}$

OptiMOS™-P Small-Signal-Transis	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics						
Thermal resistance, junction - soldering point (Pin 4)	R_{thJS}				25	K/W
Thermal resistance, junction - ambient	R_{thJA}	minimal footprint			100	
Thermal resistance, junction - ambient	R_{thJA}	6 cm ² cooling area ¹⁾	-	-	70	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified
Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=-250\text{ }\mu\text{A}$	-	-	-60	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=0\text{ V}, I_D=-1\text{ mA}$	-2.0	-1.5	-1.0	
Drain-source leakage current	I_{DSS}	$V_{DS}=-60\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	-	-40	nA
		$V_{DS}=-60\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ °C}$	-	-	-20	μA
Gate-source leakage current	I_{GSS}	$V_{GS}=-20\text{ V}, V_{DS}=0\text{ V}$	-	-	-100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=-4.5\text{ V}, I_D=-2.3\text{ A}$	-	140	170	m Ω
		$V_{GS}=-10\text{ V}, I_D=-3\text{ A}$	-	101	120	
Transconductance	g_{fs}	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=2.44\text{ A}$		4.6	-	S

¹⁾ Device on 40mm x 40mm x 1.5mm epoxy PCB FR4 with 6cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

OptiMOS™-P Small-Signal-Transis	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=-25\text{ V},$ $f=1\text{ MHz}$	-	814	1083	pF
Output capacitance	C_{oss}		-	248	330	
Reverse transfer capacitance	C_{rss}		-	109	163	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=-30\text{ V}, V_{GS}=-$ $10\text{ V}, I_D=-3\text{ A},$ $R_{G,ext}=2.7\ \Omega$	-	8.3	12.5	ns
Rise time	t_r		-	10.4	15.6	
Turn-off delay time	$t_{d(off)}$		-	43.2	64.8	
Fall time	t_f		-	11.3	17.0	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=-48\text{ V}, I_D=-3\text{ A},$ $V_{GS}=0\text{ to }-10\text{ V}$	-	-2.42	-3.2	nC
Gate to drain charge	Q_{gd}		-	-10.1	-15.2	
Gate charge total	Q_g		-	-26.3	-39.4	
Gate plateau voltage	$V_{plateau}$		-	-3.1	-	V

Reverse Diode

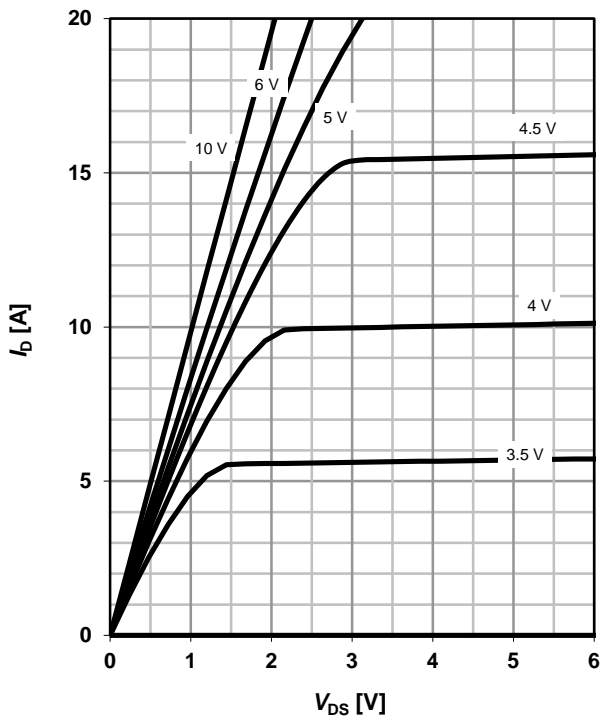
Diode continuous forward current	I_S	$T_A=25\text{ °C}$	-	-	-3.0	A
Diode pulse current	$I_{S,pulse}$		-	-	-12	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=-3\text{ A},$	-	0.80	1.1	V
Reverse recovery time ²⁾	t_{rr}	$V_R=-30\text{ V}, I_F=-3\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	44.8	67.2	ns
Reverse recovery charge ²⁾	Q_{rr}		-	62.9	94.4	nC

²⁾ Defined by design. Not subjected to production test

5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ °C}$

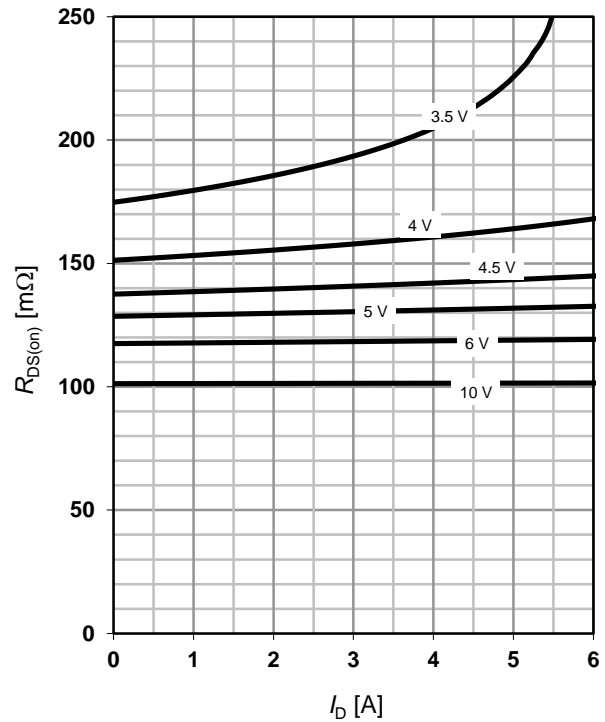
parameter: V_{GS}



6 Typ. drain-source on resistance

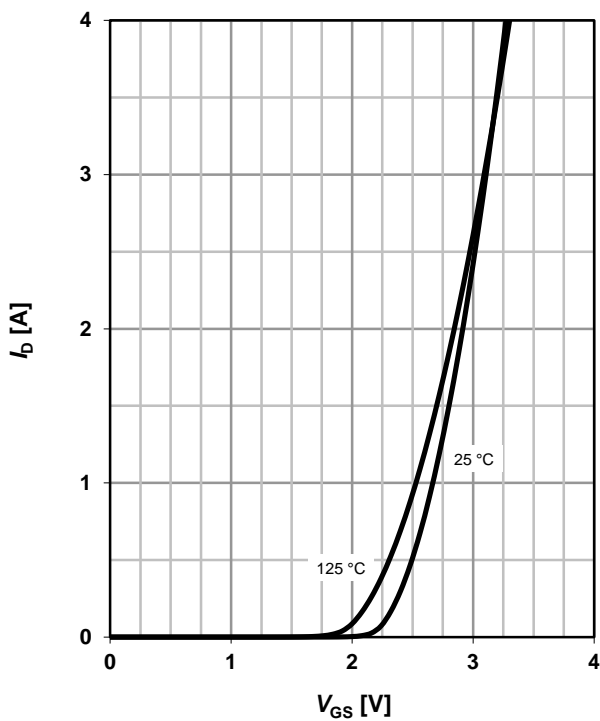
$R_{DS(on)} = f(I_D); T_j = 25\text{ °C}$

parameter: V_{GS}



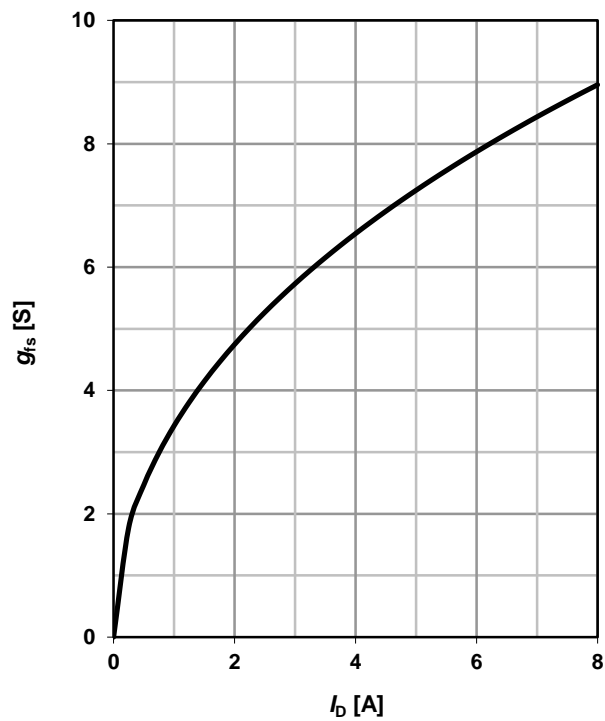
7 Typ. transfer characteristics

$I_D = f(V_{GS}); |V_{DS}| > 2I_D R_{DS(on)max}$



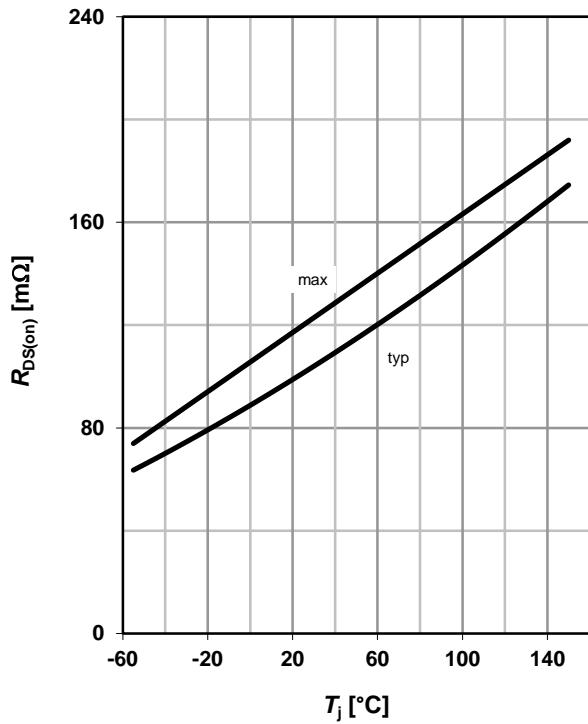
8 Typ. forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ °C}$



9 Drain-source on-state resistance

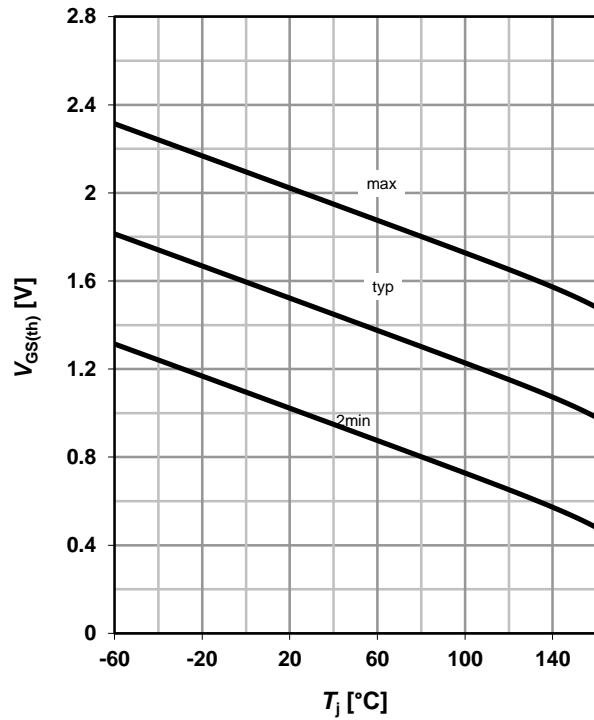
$R_{DS(on)}=f(T_j); I_D=-3\text{ A}; V_{GS}=-10\text{ V}$



10 Typ. gate threshold voltage

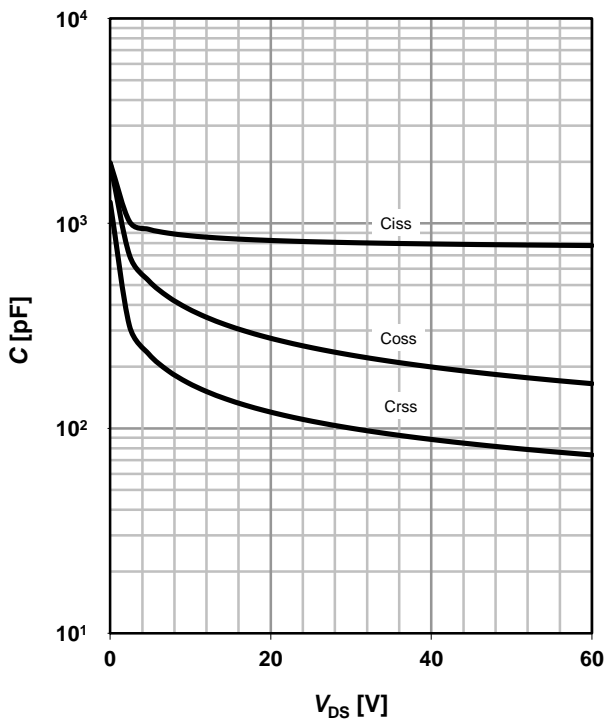
$V_{GS(th)}=f(T_j); V_{DS}=V_{GS}; I_D=-1\text{ mA}$

parameter: I_D



11 Typ. capacitances

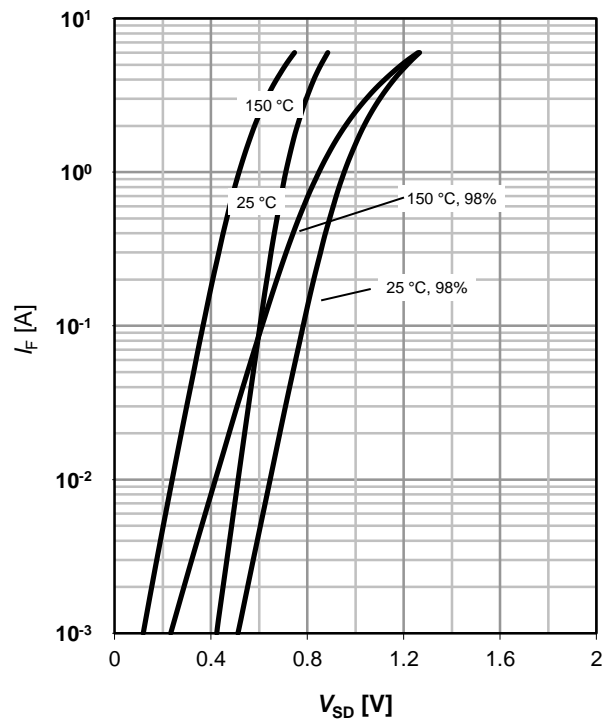
$C=f(V_{DS}); V_{GS}=0\text{ V}; f=1\text{ MHz}; T_j=25^\circ\text{C}$



12 Forward characteristics of reverse diode

$I_F=f(V_{SD})$

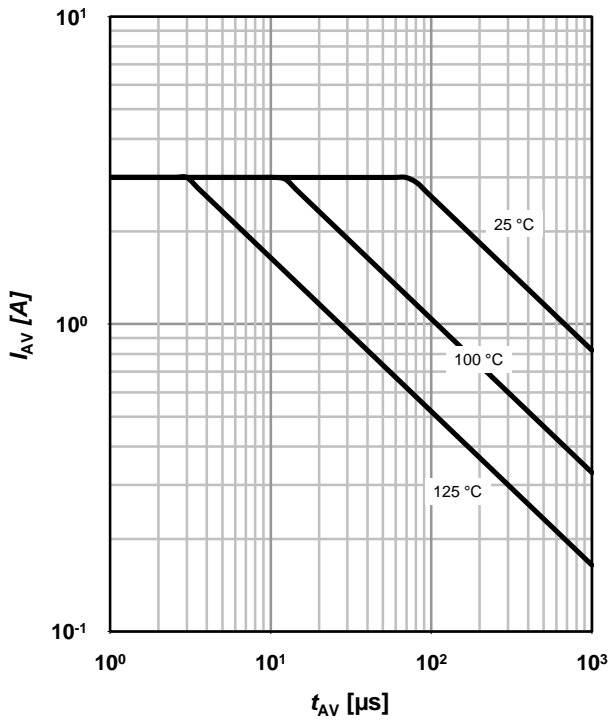
parameter: T_j



13 Avalanche characteristics

$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega$

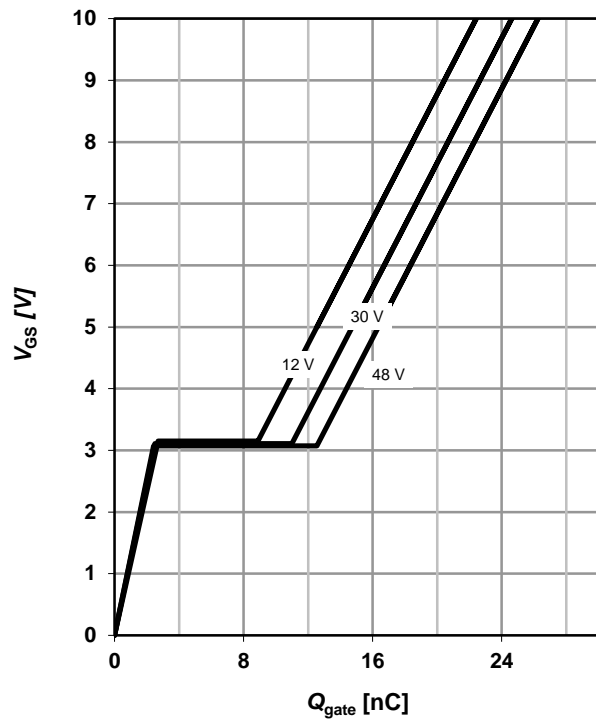
parameter: $T_{j(\text{start})}$



14 Typ. gate charge

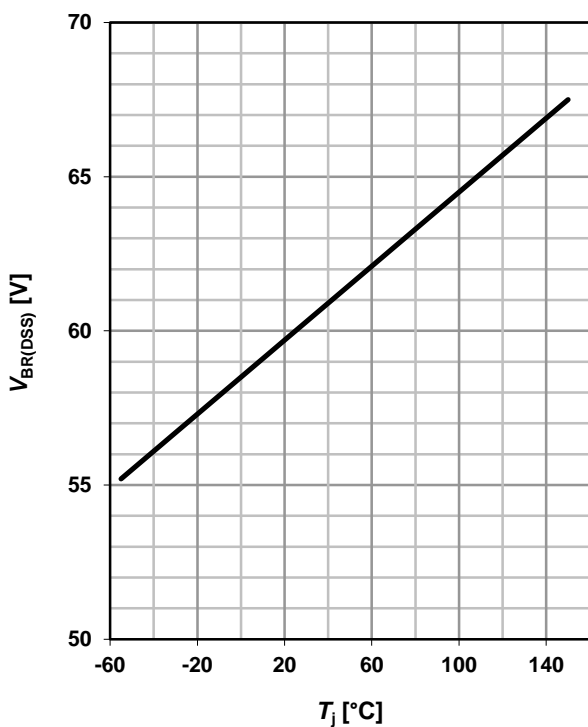
$V_{GS}=f(Q_{\text{gate}}); I_D=-3 \text{ A pulsed}$

parameter: V_{DD}

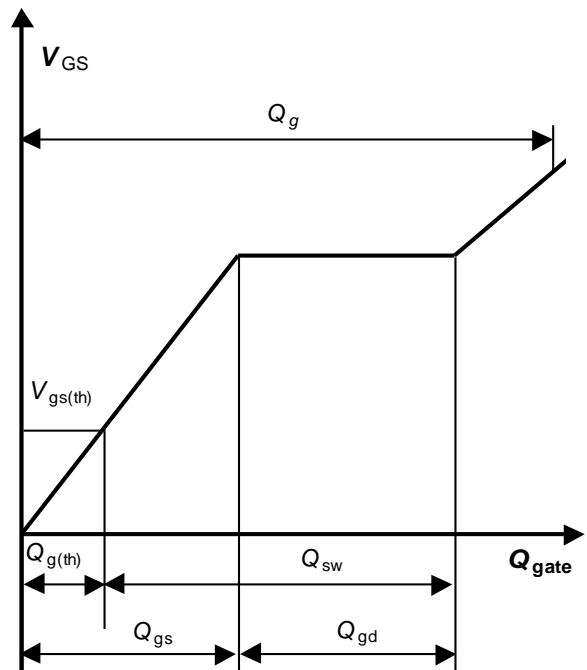


15 Drain-source breakdown voltage

$V_{BR(DSS)}=f(T_j); I_D=250 \mu\text{A}$

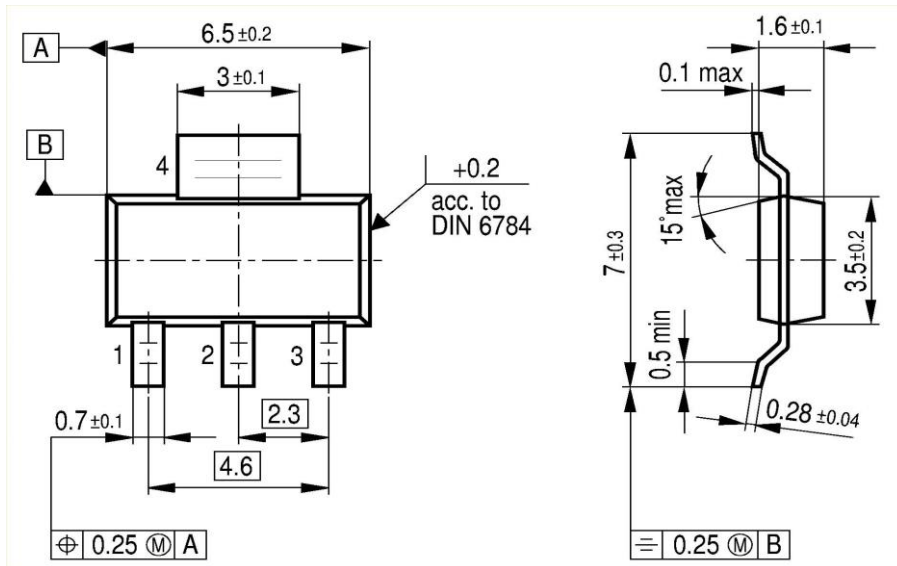


16 Gate charge waveforms



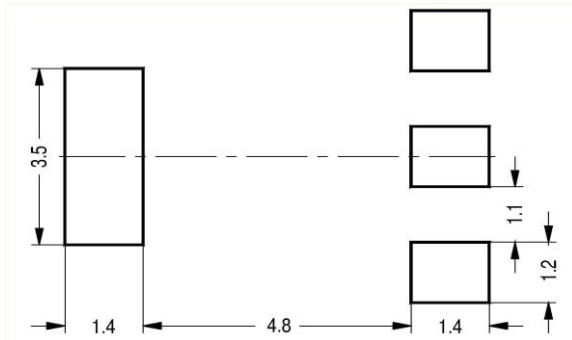
SOT223

Package Outline:

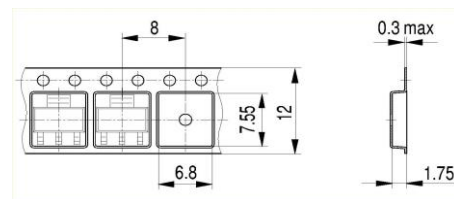


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Footprint:



Packaging:



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