



THE DATASHEET OF CDC930DL



CDC930

133-MHz DIFFERENTIAL CLOCK SYNTHESIZER/DRIVER FOR PC MOTHERBOARDS WITH 3-STATE OUTPUTS

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- Generates Clocks for Pentium®4 Microprocessors
- Uses a 14.318 MHz Crystal Input to Generate Multiple Output Frequencies
- Includes Spread Spectrum Clocking (SSC), 0.6% Downspread for Reduced EMI With Theoretical EMI Damping of 7 dB†
- Power Management Control Terminals
- Low Output Skew and Jitter for Clock Distribution
- Operates From Single 3.3-V Supply
- Consumes Less Than 30-mA Power-Down Current
- Generates the Following Clocks:
 - 4 HCLK (Host) (Different Pairs– 100/133 MHz)
 - 1 3VMREF Pair (3.3 V, 180° Shifted 50/66 MHz)
 - 10 PCI (3.3 V, 33.3 MHz)
 - 2 REF (3.3 V, 14.318 MHz)
 - 4 3V66 MHz (3.3 V, 66 MHz)
 - 2 3V48 MHz (3.3 V, 48 MHz)
- Packaged in 56-Pin SSOP Package

DL PACKAGE
(TOP VIEW)

GND	1	56	V _{DD} 3.3V
REF0/MultSel0	2	55	3VMREF
REF1/MultSel1	3	54	3VMREF
V _{DD} 3.3V	4	53	GND
XIN	5	52	SPREAD
XOUT	6	51	HCLK(1)
GND	7	50	HCLK(1)
PCI0	8	49	V _{DD} 3.3V
PCI1	9	48	HCLK(2)
V _{DD} 3.3V	10	47	HCLK(2)
PCI2	11	46	GND
PCI3	12	45	HCLK(3)
GND	13	44	HCLK(3)
PCI4	14	43	V _{DD} 3.3V
PCI5	15	42	HCLK(4)
V _{DD} 3.3V	16	41	HCLK(4)
PCI6	17	40	GND
PCI7	18	39	I_REF
GND	19	38	V _{DD} 3.3V
PCI8	20	37	GND
PCI9	21	36	V _{DD} 3.3V
V _{DD} 3.3V	22	35	3V66(0)
SEL100/133	23	34	3V66(1)
GND	24	33	GND
3V48(0)/SelA	25	32	GND
3V48(1)/SelB	26	31	3V66(2)
V _{DD} 3.3V	27	30	3V66(3)
PWRDWN	28	29	V _{DD} 3.3V

description

The CDC930 is a differential clock synthesizer/driver that generates HCLK/HCLK, 3VMREF/3VMREF, PCI, 3V66, 3V48, REF system clock signals to support a computer system with a Pentium®4 microprocessor and a Direct Rambus™ memory subsystem.

All output frequencies are generated from a 14.318-MHz crystal input. A reference clock input can be provided at the XIN input instead of a crystal. Two phase-locked loops (PLLs) are used to generate the host frequencies and the 48-MHz clock frequencies. On-chip loop filters and internal feedback eliminate the need for external components. The host, PCI clock and 48-MHz clock outputs provide low-skew/low-jitter clock signals for reliable clock operation. All outputs have 3-state capability, which can be selected using control inputs SEL133, SelA and SelB.

The outputs are either differential host clock or 3.3-V single-ended CMOS buffers. When PWRDWN is set to high, the device operates in normal mode. When PWRDWN is set low, the device transitions to a power-down mode in which HCLK is driven at 2×I_{REF}, HCLK is not driven, and all others are set low.



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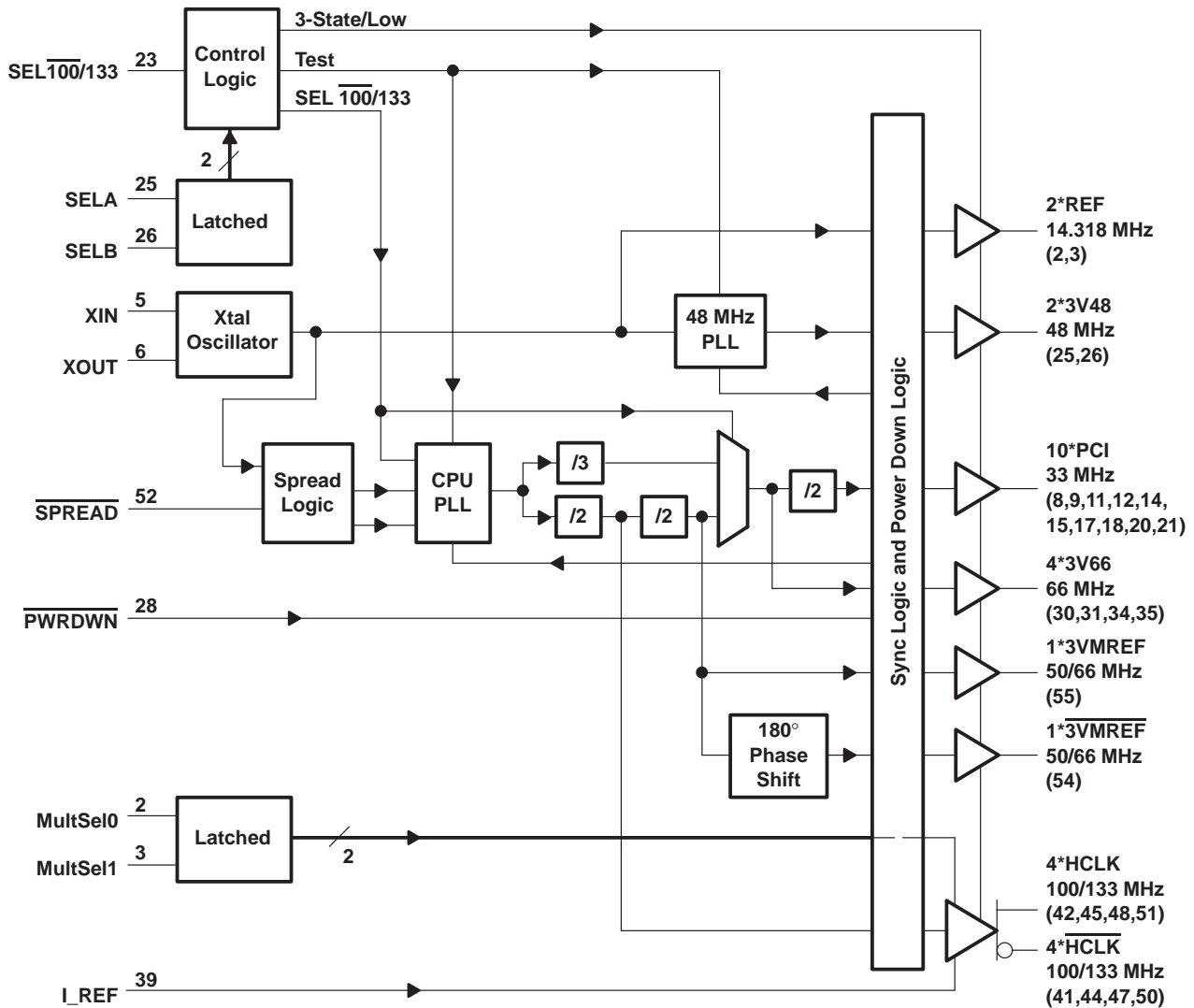
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description (continued)

The HOST bus operates at 100 MHz or 133 MHz. The MREF bus operates at 50 MHz or 66 MHz. Output frequency selection is accomplished with corresponding setting for SEL100/133 control input. The PCI bus frequency is fixed to 33 MHz.

Since the CDC930 is based on PLL circuitry, it requires a stabilization time to achieve phase-lock of the PLL. This stabilization time is required following power up as well as changes to SEL inputs. With use of external reference clock, this signal must be fixed-frequency and fixed-phase prior stabilization time starts.

functional block diagram



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Terminal Functions

TERMINAL NAME	NO.	I/O	DESCRIPTION
3V48(0)/SelA	25	I/O	Dual function 3.3 V, Type 3, 48-MHz clock output that latches the state of SelA during power up
3V48(1)/SelB	26	I/O	Dual function 3.3 V, Type 3, 48-MHz clock output that latches the state of SelB during power up
3V66[0–3]	30, 31, 34, 35	O	3.3 V, Type 5, 66-MHz clock outputs
3VMREF	55	O	3.3 V, Type 5, 50/66-MHz memory clock output
$\overline{3VMREF}$	54	O	3.3 V, Type 5, 50/66-MHz memory clock output (180° out of phase with 3VMREF)
GND	1, 7, 13, 19, 24, 32, 33, 37, 40, 46, 53		Ground for core and HCLK/HCLK, 3VMREF/ $\overline{3VMREF}$, 3V48, 3V66 and PCI outputs
HCLK[1–4]	42, 45, 48, 51	O	Type X1, host clock outputs
\overline{HCLK} [1–4]	41, 44, 47, 50	O	Type X1, host complementary clock outputs
I_REF	39	Special	Current reference pin for the host clock pairs. I_REF uses a fixed precision resistor tied to ground to establish the appropriate current.
PCI[0–9]	8, 9, 11, 12, 14, 15, 17, 18, 20, 21	O	3.3 V, Type 5, 33-MHz PCI clock outputs
\overline{PWRDWN}	28	I	Power down for complete device with HOST at $2 \times I_{REF}$, HCLK not driven and all other outputs forced low.
REF0/MultSel0	2	I/O	Dual function 3.3 V, Type 3, 14.318-MHz reference clock output. The state of MultSel0 is latched during power up. MultSel0 configures the I _{OH} amplitude (and thus the V _{OH} swing amplitude) of the HCLK pair outputs.
REF1/MultSel1	3	I/O	Dual function 3.3 V, Type 3, 14.318-MHz reference clock output. The state of MultSel1 is latched during power up. MultSel1 configures the I _{OH} amplitude (and thus the V _{OH} swing amplitude) of the HCLK pair outputs.
$\overline{SEL100/133}$	23	I	Active low LVTTTL level logic select. $\overline{SEL100/133}$ is used for enabling 100/133 MHz. Low=100 MHz, high=133 MHz
\overline{SPREAD}	52	I	LVTTTL level logic select. \overline{SPREAD} pin enables/disables the spread spectrum for the HCLK/HCLK, 3VMREF/ $\overline{3VMREF}$, 3V66 and PCI outputs.
V _{DD} 3.3V	4, 10, 16, 22, 27, 29, 36, 38, 43, 49, 56	I	3.3-V power for core and the HCLK/HCLK, 3VMREF/ $\overline{3VMREF}$, 3V48, 3V66, and PCI outputs.
XIN	5	I	Crystal input – 14.318 MHz
XOUT	6	O	Crystal output – 14.318 MHz

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Function Tables

SELECT FUNCTIONS

INPUTS			OUTPUTS						FUNCTION
SEL100/133	SelA	SelB	HOST, HCLK	3VMREF, 3VMREF	PCI	3V66	3V48	REF	
0	0	0	100 MHz	50 MHz	33 MHz	66 MHz	48 MHz	14.318 MHz	Active 100 MHz
0	1	1	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Hi-Z	All outputs 3-stated
1	0	0	133 MHz	66 MHz	33 MHz	66 MHz	48 MHz	14.318 MHz	Active 133 MHz
1	1	1	TCLK/2	TCLK/4	TCLK/8	TCLK/4	TCLK/2	TCLK	Test Mode

ENABLE FUNCTION

INPUT	OUTPUTS						
SEL100/133	HCLK	HCLK	3VMREF, 3VMREF	PCI	3V66	3V48	REF
0	2×I _{REF}	Not driven	L	L	L	L	L
1	On	On	On	On	On	On	On

SPREAD SPECTRUM FUNCTION

INPUT	OUTPUTS	
SPREAD	0	Spread spectrum clocking active, -0.6% at HCLK/HCLK, 3VMREF/3VMREF, 3V66, PCI
	1	Spread spectrum clocking nonactive

OUTPUT BUFFER SPECIFICATIONS

BUFFER NAME	V _{DD} RANGE (V)	IMPEDANCE (Ω)	BUFFER TYPE
3V48, REF	3.135 – 3.465	20–60	TYPE 3
PCI, 3V66	3.135 – 3.465	12–65	TYPE 5
3VMREF/3VMREF	3.135 – 3.465	12–55	TYPE 5
HCLK/HCLK			TYPE X1

OUTPUT BUFFER SPECIFICATIONS

INPUTS		BOARD TARGET TRACE/TERM Z	REFERENCE R _f , I _{REF} = V _{DD} /3×R _f)	OUTPUT CURRENT	V _{OH} AT Z I _{REF} = 2.32 mA
MultSel0	MultSel1				
0	0	60 Ω	R_f = 475 1%, I_{REF} = 2.32 mA	I_{OH} = 5×I_{REF}	0.71 V at 60 Ω
0	0	50 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 5×I _{REF}	0.59 V at 50 Ω
0	1	60 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 6×I _{REF}	0.85 V at 60 Ω
0	1	50 Ω	R_f = 475 1%, I_{REF} = 2.32 mA	I_{OH} = 6×I_{REF}	0.71 V at 50 Ω
1	0	60 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 4×I _{REF}	0.56 V at 60 Ω
1	0	50 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 4×I _{REF}	0.47 V at 50 Ω
1	1	60 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 7×I _{REF}	0.99 V at 60 Ω
1	1	50 Ω	R _f = 475 1%, I _{REF} = 2.32 mA	I _{OH} = 7×I _{REF}	0.82 V at 50 Ω

NOTE: The entries in **boldface** are the primary system configurations of interest. The outputs should be optimized for these configurations



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recommended operating conditions (see Note 2)

		MIN	NOM†	MAX	UNIT
Supply voltage, V_{DD}		3.135		3.465	V
High-level input voltage, V_{IH}		2		$V_{DD} + 0.3\text{ V}$	V
Low-level input voltage, V_{IL}		GND – 0.3 V		0.8	V
Input voltage, V_I		0		V_{DD}	V
High-level output current, I_{OH}	HCLK/HCLK			-20	mA
	3VMREF/3VMREF			-15	
	48MHz, REFx			-16	
	PCIx, 3V66x			-15	
Low-level output current, I_{OL}	HCLK/HCLK			5	μA
	3VMREF/3VMREF			10	
	48MHz, REFx			10	
	PCIx, 3V66x			10	
Reference frequency, $f_{(XIN)}‡$	Test mode		14	MHz	
Crystal frequency, $f_{(XTAL)}§$	Normal mode		13.8 14.318 14.8	MHz	
Operating free-air temperature, T_A		0		85	°C

† All nominal values are measured at their respective nominal V_{DD} values.

‡ Reference frequency is a test clock driven on the XIN input during the device test mode and normal mode. In test mode, XIN can be driven externally up to $f_{(XIN)} = 16$ MHz. If XIN is driven externally, XOUT is floating.

§ This is a series fundamental crystal with $f_O = 14.31818$ MHz.

NOTES: 4. Unused inputs must be held high or low to prevent them from floating.

5. V_{IH} , V_{IL} : All input levels referenced to $V_{DD} = 3.30$ V.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{IK}	Input clamp voltage	V _{DD} = 3.135 V, I _I = -18 mA				-1.2	V
R _I	Input resistance	XIN-XOUT	V _{DD} = 3.465 V, V _I = V _{DD} - 0.5 V		100		kΩ
I _{IH}	High-level input current	XOUT	V _{DD} = 3.135 V, V _I = V _{DD} - 0.5 V			50	mA
		MultSel0, MultSel1, SelA, SelB	V _{DD} = 3.465 V, V _I = V _{DD}			10	μA
		SEL100/133 SPREAD, PWRDWN	V _{DD} = 3.465 V, V _I = V _{DD}			5	μA
I _{IL}	Low-level input current	XOUT	V _{DD} = 3.135 V, V _O = 0 V			-5	mA
		MultSel0, MultSel1, SelA, SelB,	V _{DD} = 3.465 V, V _I = GND			-10	μA
		SEL100/133 SPREAD, PWRDWN	V _{DD} = 3.465 V, V _I = GND			-5	μA
		I_REF	V _{DD} = 3.465 V, R _r = 221			-5.5	mA
I _{OZ}	High-impedance-state output current	V _{DD} = 3.465 V	SELA, SELB = H, SEL100/133 H → L V _O = V _{DD} or GND PWRDWN = H			±10	μA
I _{DD(Z)}	High-impedance-state supply current	V _{DD} = 3.465 V	SELA, SELB = H, SEL100/133 H → L PWRDWN = H			40	mA
I _{DD(PD)}	PWRDWN state supply current	V _{DD} = 3.465 V,	PWRDWN = L			30	mA
I _{DD}	Dynamic supply current	V _{DD} = 3.465 V	PWRDWN = H, HCLK = 133 MHz, SSC = ON/OFF, C _L = MAX R _{ref} = 475 Ω, I _O UT = 6 × I _{ref}			250	mA
C _I	Input capacitance‡	V _{DD} = 3.3 V,	V _I = V _{DD} or GND		2	5	pF
C _(XTAL)	Crystal terminal capacitance	V _{DD} = 3.3 V,	V _I = 0.3 V			18	pF

† All typical values are measured at their respective nominal V_{DD} values.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.

Control SELx, PWRDWN, SPREAD threshold levels during FUNC w/c level tests.

C_L = MAX = 5 pF, R_S = 33.2 Ω, R_P = 49.9 Ω at HCLK/HCLK (Type X1)

C_L = MAX = 20 pF, R_L = 500 Ω at 48 MHz, REF (Type 3)

C_L = MAX = 30 pF, R_L = 500 Ω at PC1x, 3V66, 3VMREF, 3VMREF (Type 5)

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (continued)

HCLK/HCLK (Type X1)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
I _{OH} High-level output current	I _{ref} = 2.32 mA × 4	V _{DD} = 3.135 V	V _{OH} at Z = 50 Ω	-8.1		mA
		V _{DD} = 3.465 V				
	I _{ref} = 2.32 mA × 5	V _{DD} = 3.135 V		-10.1		mA
		V _{DD} = 3.465 V				
	I _{ref} = 2.32 mA × 6	V _{DD} = 3.135 V		-12.1		mA
		V _{DD} = 3.465 V				
	I _{ref} = 2.32 mA × 7	V _{DD} = 3.135 V		-14.1		mA
		V _{DD} = 3.465 V				
C _O Output capacitance‡	V _O = V _{DD} or GND			3.5		pF

† All typical values are measured at their respective nominal V_{DD} values.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.

48MHz, REFx (Type 3), C_L = 20 pF, R_L = 500 Ω

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	V _{DD} = min to max, I _{OH} = -1 mA		V _{DD} - 0.1 V			V
	V _{DD} = 3.135 V, I _{OH} = -14 mA		2.4			
V _{OL} Low-level output voltage	V _{DD} = min to max, I _{OL} = 1 mA				0.1	V
	V _{DD} = 3.135 V, I _{OL} = 9 mA				0.4	
I _{OH} High-level output current	V _{DD} = 3.135 V, V _O = 1 V		-29			mA
	V _{DD} = 3.3 V, V _O = 1.65 V			-41		
	V _{DD} = 3.465 V, V _O = 3.135 V				-23	
I _{OL} Low-level output current	V _{DD} = 3.135 V, V _O = 1.95 V		29			mA
	V _{DD} = 3.3 V, V _O = 1.65 V			53		
	V _{DD} = 3.465 V, V _O = 0.4 V				27	
C _O Output capacitance‡	V _{DD} = 3.3 V, V _O = V _{DD} or GND		2		5	pF

† All typical values are measured at their respective nominal V_{DD} values.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.

PC1x, 3V66x, MREF/MREF (Type 5), C_L = 20 pF, R_L = 500 Ω

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V _{OH} High-level output voltage	V _{DD} = min to max, I _{OH} = -1 mA		V _{DD} - 0.1 V			V
	V _{DD} = 3.135 V, I _{OH} = -18 mA		2.4			
V _{OL} Low-level output voltage	V _{DD} = min to max, I _{OL} = 1 mA				0.1	V
	V _{DD} = 3.135 V, I _{OL} = 12 mA				0.4	
I _{OH} High-level output current	V _{DD} = 3.135 V, V _O = 1 V		-33			mA
	V _{DD} = 3.3 V, V _O = 1.65 V			-53		
	V _{DD} = 3.465 V, V _O = 3.135 V				-33	
I _{OL} Low-level output current	V _{DD} = 3.135 V, V _O = 1.95 V		30			mA
	V _{DD} = 3.3 V, V _O = 1.65 V			70		
	V _{DD} = 3.465 V, V _O = 0.4 V				38	
C _O Output capacitance‡	V _{DD} = 3.3 V, V _O = V _{DD} or GND		2		5	pF

† All typical values are measured at their respective nominal V_{DD} values.

‡ These parameters are ensured by design and lab characterization, not 100% production tested.



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switching characteristics, $V_{DD} = \text{MIN to MAX}$, $T_A = 0^\circ\text{C to } 85^\circ\text{C}$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT		
v_{over} Overshoot [†]			HCLK/HCLK 0.7 V amplitude			$V_{\text{OH}}+200$	mV		
v_{under} Undershoot [†]						$V_{\text{OL}}-200$			
v_{over} Overshoot [†]			Other clocks, $C_L = \text{Worst case}$	GND-0.7			V		
v_{under} Undershoot [†]						$V_{\text{DD}}+0.7$			
t_{PZL} Output enable time to low level	SEL100/133	HCLK/ HCLK	$f(\text{HCL}) = 100 \text{ or } 133 \text{ MHz}$, SEL $\overline{\text{A}}$, SELB = H, SEL100/133 L \rightarrow H, $R_{\text{ref}} = 475 \Omega$			100	ns		
t_{PZH} Output enable time to high level						100	ns		
t_{PHZ} Output disable time from high level					$f(\text{HCL}) = 100 \text{ or } 133 \text{ MHz}$, SEL $\overline{\text{A}}$, SELB = H, SEL100/133 H \rightarrow L, $R_{\text{ref}} = 475 \Omega$			10	ns
t_{PLZ} Output disable time from low level								10	ns
t_{PZL} Output enable time to low level	SEL100/133	REF, 3V48 3VMREF, 3VMREF, 3V66, PCI	$f(\text{HCL}) = 100 \text{ or } 133 \text{ MHz}$, SEL $\overline{\text{A}}$, SELB = H, SEL100/133 L \rightarrow H, $R_{\text{ref}} = 475 \Omega$			10	ns		
t_{PZH} Output enable time to high level						10	ns		
t_{PHZ} Output disable time from high level					$f(\text{HCL}) = 100 \text{ or } 133 \text{ MHz}$, SEL $\overline{\text{A}}$, SELB = H, SEL100/133 H \rightarrow L, $R_{\text{ref}} = 475 \Omega$			10	ns
t_{PLZ} Output disable time from low level								10	ns
t_{stab} Stabilization time [†]			After power up			3	ms		

[†] Stabilization time is the time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. In order for phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at XIN. Until phase lock is obtained, the specifications for propagation delay and skew parameters given in the switching characteristics tables are not applicable. Stabilization time is defined as the time from when V_{DD} achieves its nominal operating level until the output frequency is stable and operating within specification.

[‡] These parameters are ensured by design and lab characterization, not 100% production tested.

HCLK/HCLK (Type X1) $C_L = 2 \text{ pF}$, $R_L > 500 \text{ k}\Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c HCLK clock period [†]			$f(\text{HCLK}) = 100 \text{ MHz}$	10		10.2	ns
			$f(\text{HCLK}) = 133 \text{ MHz}$	7.5		7.65	
$t_{\text{jit(cc)}}$ Cycle to cycle jitter			$f(\text{HCLK}) = 100 \text{ or } 133 \text{ MHz}$			200	ps
t_{dc} Duty cycle			$f(\text{HCLK}) = 100 \text{ or } 133 \text{ MHz}$ crossing point	45%		55%	
$t_{\text{sk(o)}}$ HCLK bus skew	HCLKx	HCLKx	$f(\text{HCLK}) = 100 \text{ or } 133 \text{ MHz}$ crossing point			150	ps
t_w Pulse duration width			$f(\text{HCLK}) = 100 \text{ MHz}$	4.41			ns
			$f(\text{HCLK}) = 133 \text{ MHz}$	3.29			
t_r Rise time [‡]	0.7 V amplitude		$V_O = 0.14 \text{ V to } 0.56 \text{ V}$	175		700	ps
t_f Fall time [‡]			$V_O = 0.14 \text{ V to } 0.56 \text{ V}$	175		700	ps
t_r, t_f Rise and fall time matching [‡]			$2 \times (t_r - t_f)/(t_r + t_f)$			20%	
v_{cross} Cross point voltages [‡]	0.7 V amplitude		$f(\text{HCLK}) = 100 \text{ or } 133 \text{ MHz}$ HCLK and HCLK	40% VOH		55% VOH	V

[†] The average over any 1- μs period of time is greater than the minimum specified period.

[‡] These parameters are ensured by design and lab characterization, not 100% production tested.



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switching characteristics, $V_{DD} = 3.135\text{ V to }3.465\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

3VMREF/3VMREF (Type 5) $C_L = 30\text{ pF}$, $R_L = 500\ \Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c 3VMREF/3VMREF clock period†			$f(3VMREF/3VMREF) = 50\text{ MHz}$	20	20.4		ns
			$f(3VMREF/3VMREF) = 66\text{ MHz}$	15	15.3		ns
$t_{jit(cc)}$ Cycle to cycle jitter			$f(3VMREF/3VMREF) = 66\text{ MHz}$, $f(HCLK) = 100\text{ or }133\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, Measured at 1.5 V			250	ps
t_{dc} Duty cycle			$f(3VMREF/3VMREF) = 66\text{ MHz}$	45%		55%	
$t_{sk(o)}$ 3VMREF/3VMREF output skew	3VMREF/3VMREF	3VMREF/3VMREF	$f(3VMREF/3VMREF) = 66\text{ MHz}$, $f(HCLK) = 100\text{ or }133\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, Measured at 1.5 V			250	ps
$t_{(off)}$ 3VMREF/3VMREF clock to PCI offset	3VMREF/3VMREF	PCIx	$f(3VMREF/3VMREF) = 66\text{ MHz}$, Measured points at 1.5 V, Measured at rising edges			3	ns
t_r Rise time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns
t_f Fall time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns

† The average over any 1-μs period of time is greater than the minimum specified period.

3V66 (Type 5, No SSC), $C_L = 30\text{ pF}$, $R_L = 500\ \Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c 3V66 clock period†			$f(3V66) = 66\text{ MHz}$		15.03		ns
$t_{jit(cc)}$ Cycle to cycle jitter			$f(3V66) = 66\text{ MHz}$, $f(HCLK) = 100\text{ or }133\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, Measured at 1.5 V			300	ps
t_{dc} Duty cycle			$f(3V66) = 66\text{ MHz}$	45%		55%	
$t_{sk(o)}$ 3V66 output skew	3V66x	3V66x	$f(3V66) = 66\text{ MHz}$, $f(HCLK) = 100\text{ or }133\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, Measured at 1.5 V			250	ps
$t_{(off)}$ 3V66 clock to PCI	3V66x	PCIx	$f(3V66) = 66\text{ MHz}$, Measured points at 1.5 V, Measured at rising edges	1.5		3.5	ns
t_r Rise time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns
t_f Fall time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns

† The average over any 1-μs period of time is greater than the minimum specified period.

PCI (Type 5), $C_L = 30\text{ pF}$, $R_L = 500\ \Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c PCI clock period†			$f(PCI) = 33.3\text{ MHz}$		30.06		ns
$t_{jit(cc)}$ Cycle to cycle jitter			$f(HCLK) = 100\text{ or }133\text{ MHz}$			500	ps
t_{dc} Duty cycle			$f(PCI) = 33.3\text{ MHz}$	45%		55%	
$t_{sk(o)}$ PCI output skew	PCIx	PCIx	$f(PCI) = 33.3\text{ MHz}$			500	ps
t_r Rise time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns
t_f Fall time			$V_O = 0.4\text{ V to }2.4\text{ V}$	0.5		2	ns

† The average over any 1-μs period of time is greater than the minimum specified period.



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switching characteristics, $V_{DD} = 3.135\text{ V to }3.465\text{ V}$, $T_A = 0^\circ\text{C to }85^\circ\text{C}$ (continued)

3V48 (Type 3), $C_L = 20\text{ pF}$, $R_L = 500\ \Omega$

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	3V48 clock period [†]		$f_{(3V48)} = 48\text{ MHz}$		15.03		ns
$t_{jit(cc)}$	Cycle to cycle jitter		$f_{(3V48)} = 48\text{ MHz}$, $f_{(HCLK)} = 100\text{ or }133\text{ MHz}$, $V_{DD} = 3.3\text{ V}$, Measured at 1.5 V			350	ps
t_{dc}	Duty cycle		$f_{(3V48)} = 48\text{ MHz}$	45%		55%	
$t_{sk(o)}$	3V48 output skew	3V48x	3V48x			250	ps
$t_{(off)}$	3V48 clock to PCI	3V48x	PCIx			3.5	ns
t_r	Rise time		$V_O = 0.4\text{ V to }2.4\text{ V}$	1		4	ns
t_f	Fall time		$V_O = 0.4\text{ V to }2.4\text{ V}$	1		4	ns

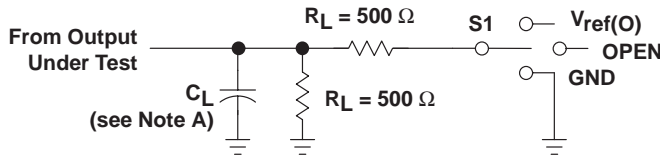
[†] The average over any 1- μs period of time is greater than the minimum specified period.

REF (Type 3), $C_L = 20\text{ pF}$, $R_L = 500\ \Omega$

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_c	REF clock period [†]		69.84		ns
$t_{jit(cc)}$	Cycle to cycle jitter			1	ps
t_{dc}	Duty cycle	52%		62%	
t_r	Rise time	1		4	ns
t_f	Fall time	1		4	ns

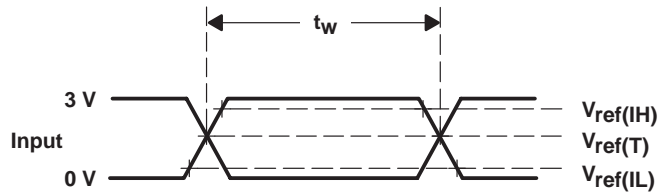
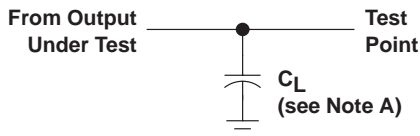
[†] The average over any 1- μs period of time is greater than the minimum specified period.

PARAMETER MEASUREMENT INFORMATION



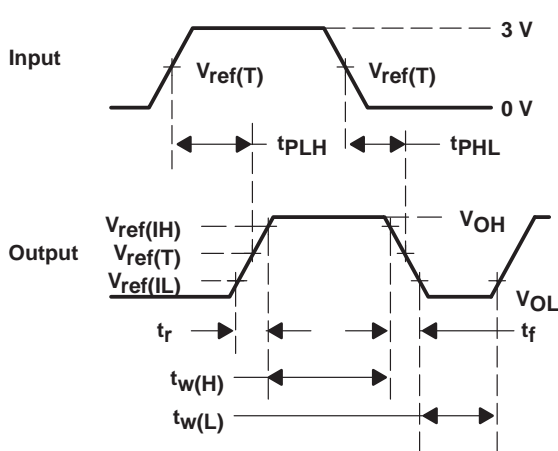
TEST	S1
tPLH/tPHL	Open
tPLZ/tPZL	Vref(OFF)
tPHZ/tPZH	GND

LOAD CIRCUIT of single-ended outputs for t_{pd} and t_{sk}

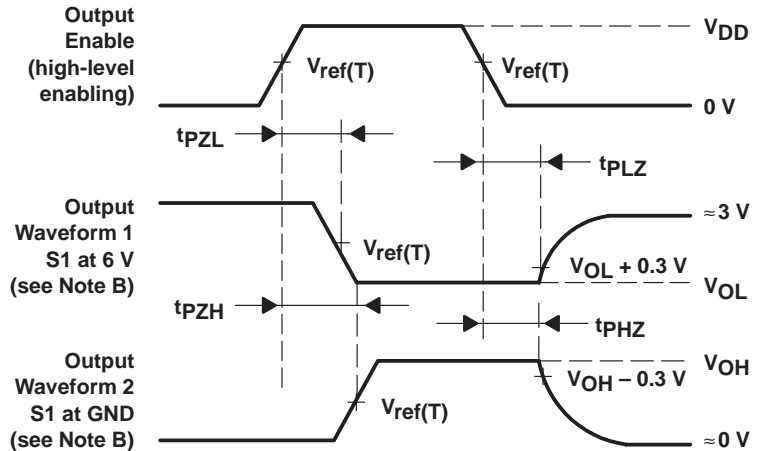


LOAD CIRCUIT of single-ended outputs for t_r and t_f

VOLTAGE WAVEFORMS



VOLTAGE WAVEFORMS



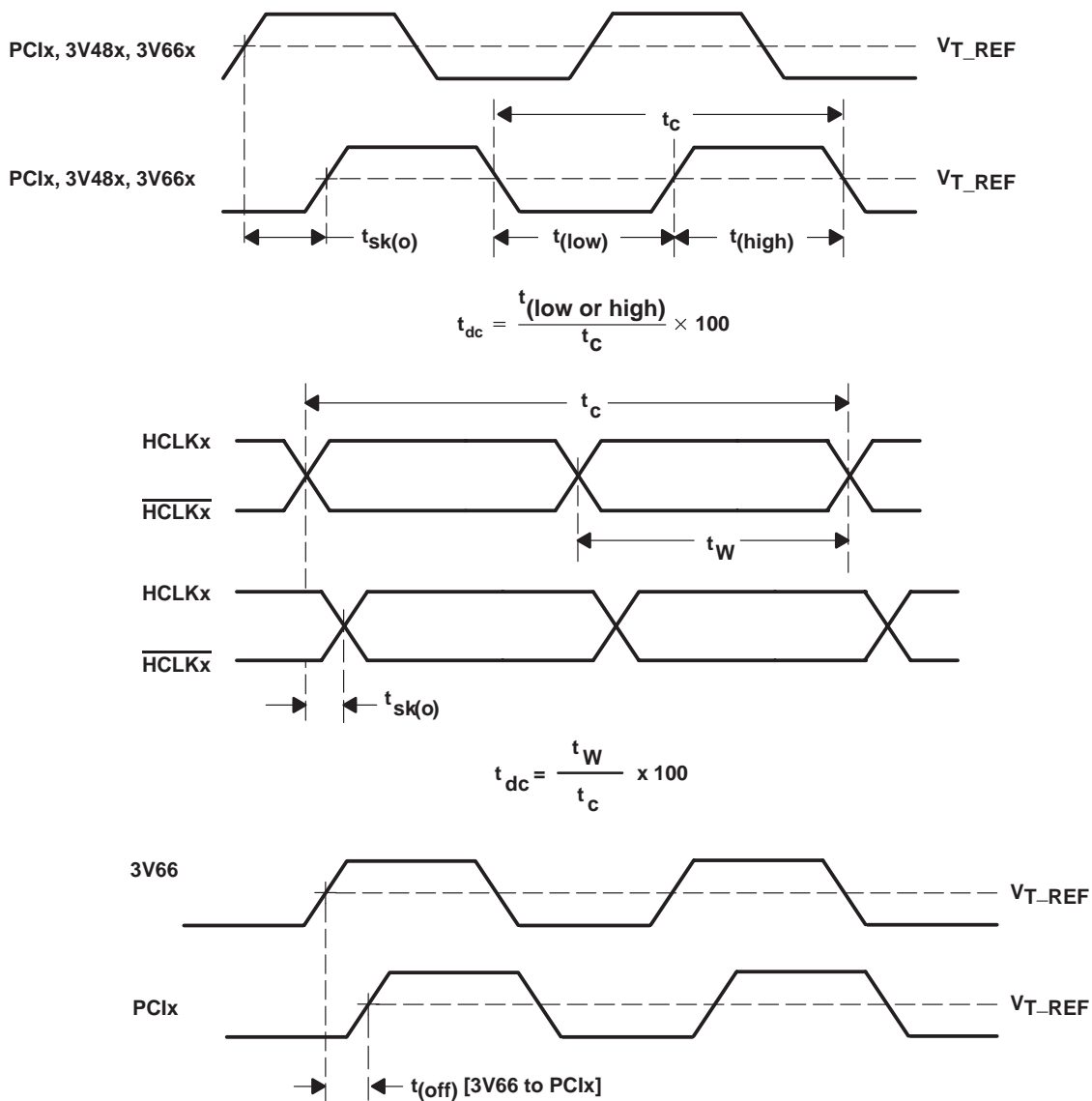
VOLTAGE WAVEFORMS

- NOTES: A. C_L includes probe and jig capacitance. C_L = 2 pF (HCLK, HCLK), C_L = 20 pF (48MHZ, REF), C_L = 30 pF (PC1x, 3VMREF, 3V66).
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 14.318 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 D. The outputs are measured one at a time with one transition per measurement.

PARAMETER		3.3-V INTERFACE	2.5-V INTERFACE	UNIT
V _{ref(IH)}	High-level reference voltage	2.4	2	V
V _{ref(IL)}	Low-level reference voltage	0.4	0.4	V
V _{ref(T)}	Input threshold reference voltage	1.5	1.25	V
V _{ref(OFF)}	Off-state reference voltage	6	4.6	V

Figure 1. Load Circuit and Voltage Waveforms

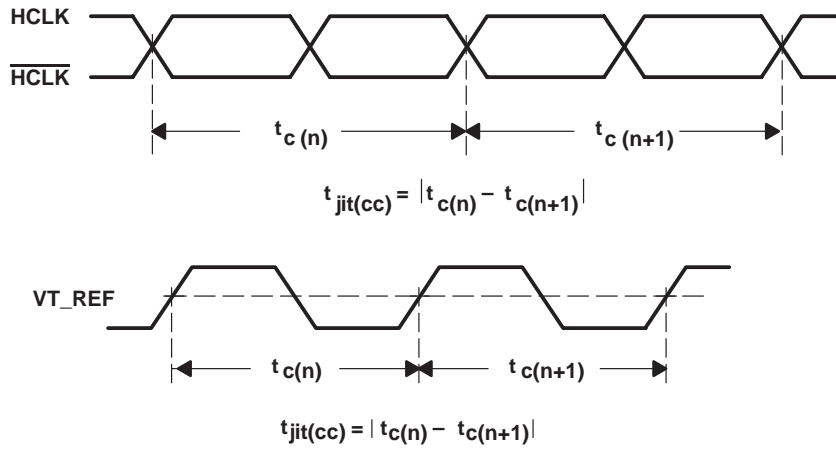
PARAMETER MEASUREMENT INFORMATION



PARAMETER	3.3-V INTERFACE	UNIT
VT_REF Input threshold reference voltage	1.5	V

Figure 2. Waveforms for Calculation of Output Skew, Duty Cycle, and Offset

PARAMETER MEASUREMENT INFORMATION



PARAMETER	3.3-V INTERFACE	UNIT
VT_REF Input threshold reference voltage	1.5	V

Figure 3. Waveforms for Calculation of Cycle-Cycle Jitter

PARAMETER MEASUREMENT INFORMATION

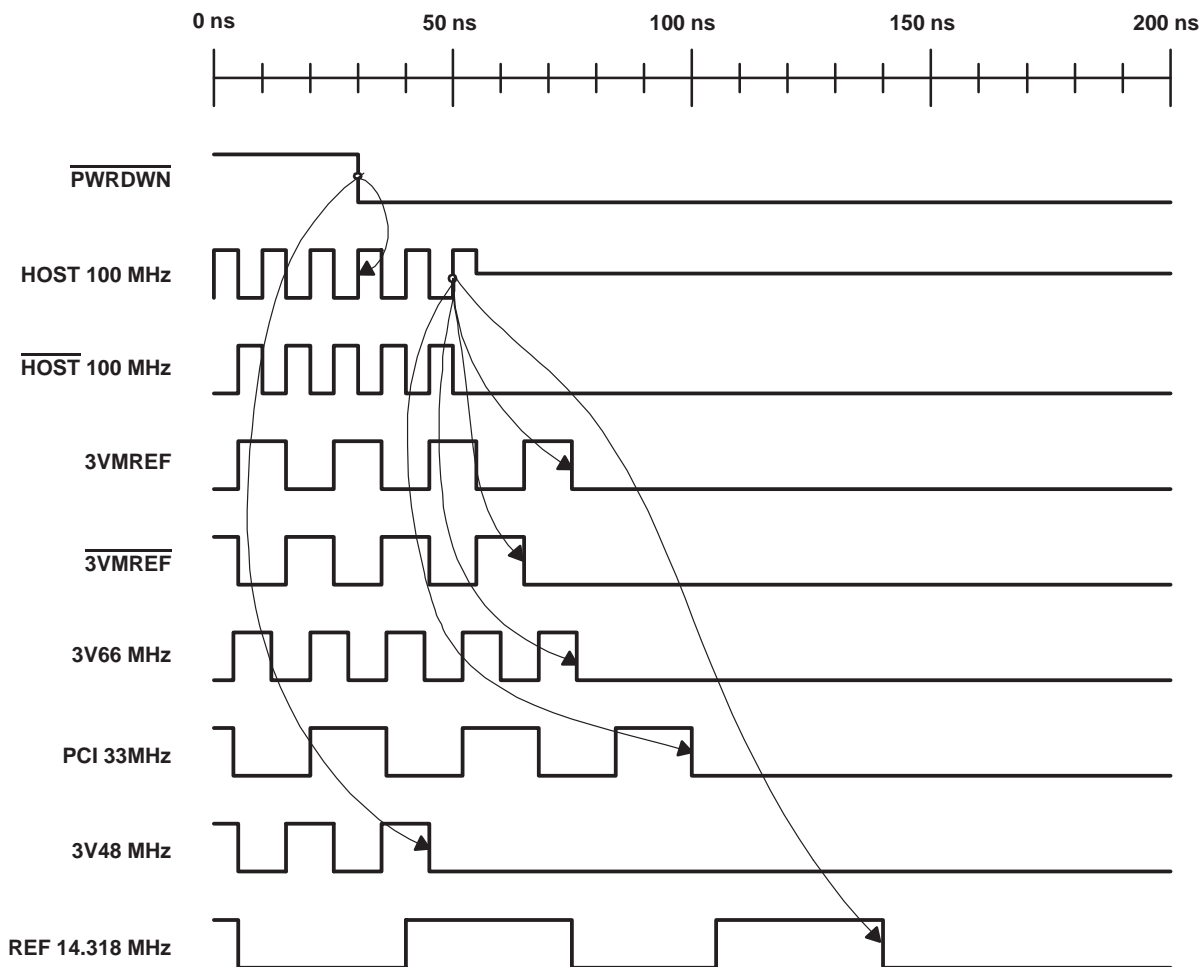
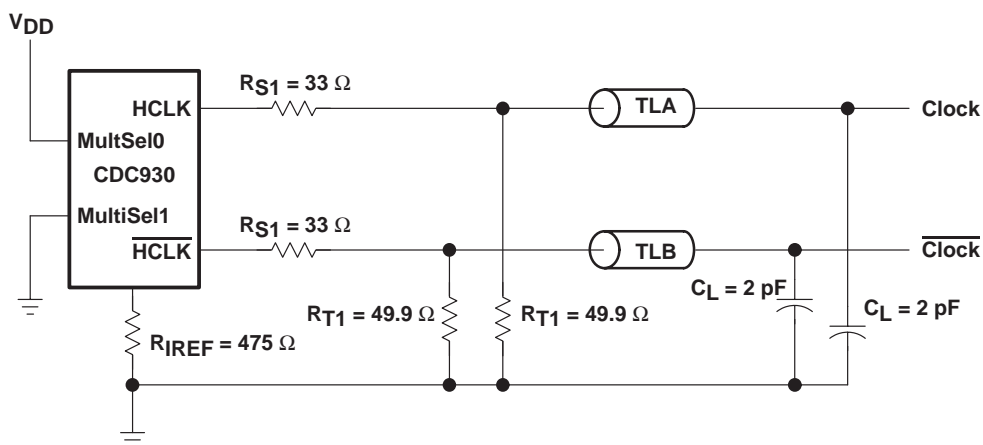


Figure 4. Power DOWN Timing



NOTE A: $Z(TLA) = Z(TLB) = 50 \Omega$, $L(TLA) = L(TLB) = 3.5"$, C_L represents probe and jig capacitance.

Figure 5. Load Circuit for 0.7 V Amplitude HCLK/HCLK Bus

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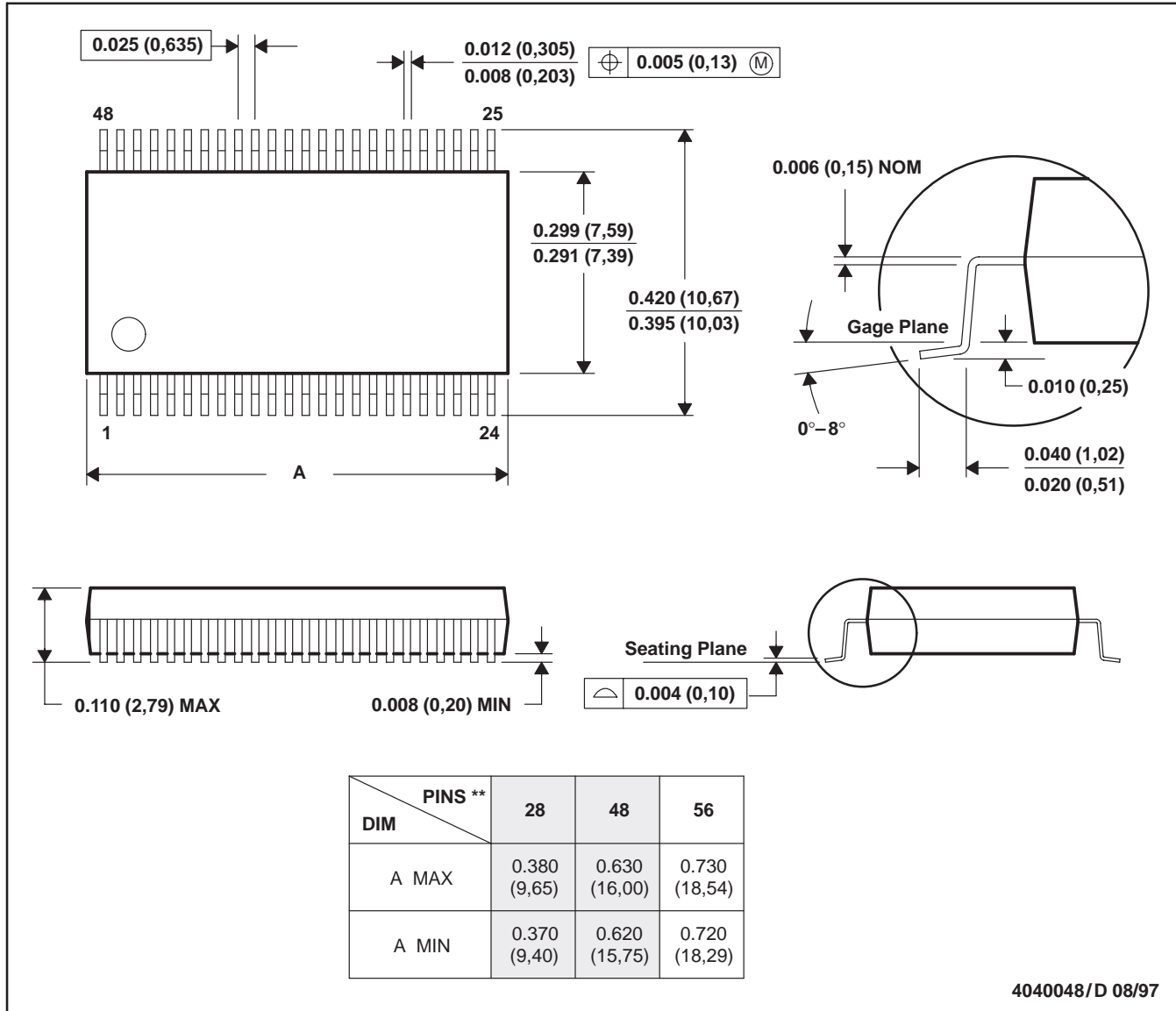
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MECHANICAL DATA

DL (R-PDSO-G)**

PLASTIC SMALL-OUTLINE PACKAGE

48-PIN SHOWN



4040048/D 08/97

- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

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