# THE DATASHEET OF

# CHL8325B-00CRT

## FEATURES

- 5-phase dual output PWM Controller
- Phases are flexibly assigned between Loops 1 & 2
- Intel® VR12, AMD® SVI/G34 & Memory MPoL modes
- Dual OCP support for I-spike enhanced AMD CPUs
- SMB_Alert Pin for Servers
- PMBus Address pin or Variable Gate Drive (CHL8325A)
- 2nd Temperature Sense for VR12 Desktop (CHL8325B)
- Overclocking & Gaming Mode with Vmax setting
- Switching frequency from 200kHz to 1.2MHz per phase
- CHiL Efficiency Shaping Features including Variable Gate Drive (CHL8325A only), Dynamic Phase Control
- Programmable 1-phase or 2-phase for Light Loads and Active Diode Emulation for Very Light Loads
- CHiL Adaptive Transient Algorithm (ATA) on both loops minimizes output bulk capacitors and system cost
- Designed for use with coupled inductors
- Auto-Phase Detection with auto-compensation
- Per-Loop Fault Protection: OVP, UVP, OCP, OTP, CFP
- I2C/SMBus/PMBus system interface for telemetry of Temperature, Voltage, Current & Power for both loops
- Non-Volatile Memory (NVM) for custom configuration
- Compatible with CHiL ATL and 3.3V tri-state Drivers
- +3.3V supply voltage; 0ºC to 85ºC ambient operation
- Pb-Free, RoHS, 6x6 40 pin QFN package

## DESCRIPTION

The CHL8325A/B are dual-loop digital multi-phase buck controllers that drive up to 5 phases. The CHL8325A/B is fully Intel® VR12 and AMD® SVI compliant on both loops and provides a Vtt tracking function for DDR memory.

NVM storage saves pins and enables a small package size.

The CHL8325A/B includes the CHiL Efficiency Shaping Technology to deliver exceptional efficiency at minimum cost across the entire load range. CHiL Variable Gate Drive optimizes the MOSFET gate drive voltage as a function of real-time load current. CHiL Dynamic Phase Control adds/drops active phases based upon load current. The CHL8325A/B can be configured to enter 1-phase operation and active diode emulation mode automatically or by command.

CHiL's unique Adaptive Transient Algorithm (ATA), based on proprietary non-linear digital PWM algorithms, minimizes output bulk capacitors. In addition, a coupled inductor mode, with phases added/dropped in pairs, enables further improvement in transient response and form factor.

The I2C/PMBus interface can communicate with up to 16 CHL8325A/B based VR loops. Device configuration and fault parameters are easily defined using the CHiL Intuitive Power Designer (IPD) GUI and stored in on-chip NVM.

The CHL8325A/B provides extensive OVP, UVP, OCP and OTP fault protection and includes thermistor based temperature sensing with VRHOT signal.

The CHL8325A/B also includes numerous features like register diagnostics for fast design cycles and platform differentiation, truly simplifying VRD design and enabling fastest time-to-market with its "set-and-forget" methodology.

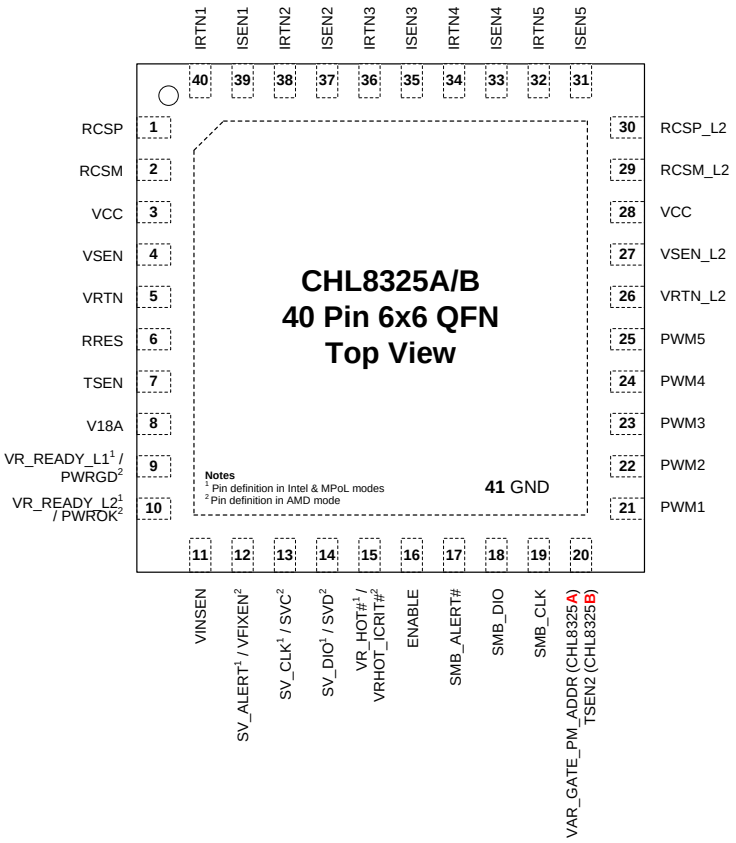


**Figure 1: CHL8325A & CHL8325B Packages**

## APPLICATIONS

- Intel® VR12 & AMD® SVI based systems
- DDR Memory with Vtt tracking
- Overclocked & Gaming platforms





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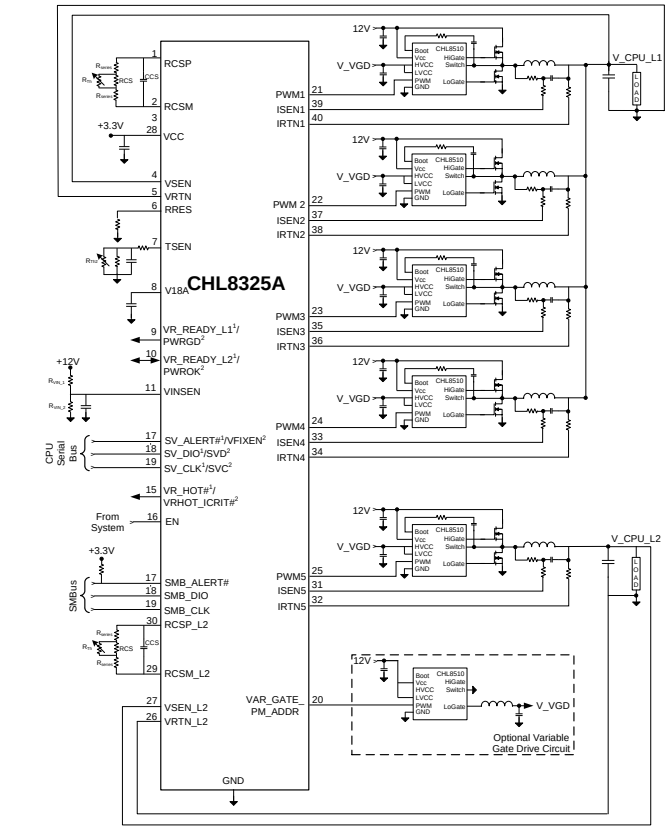
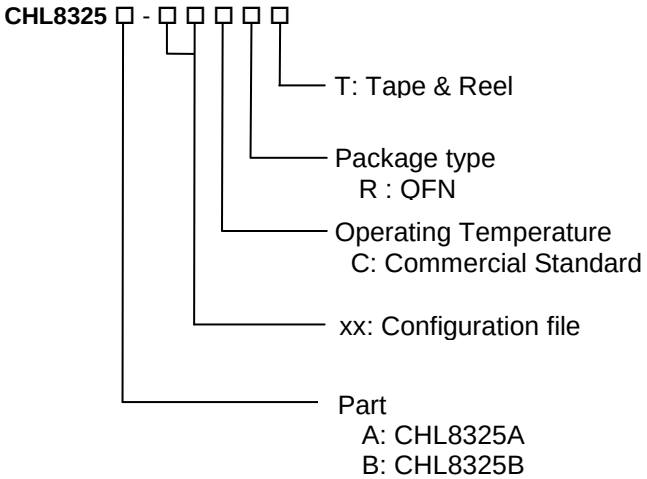
## TYPICAL APPLICATIONS BLOCK DIAGRAM




**Notes**
[1] Pin definition in Intel & MPoL modes
[2] Pin definition in AMD mode

## ORDERING INFORMATION




| Package | Tape & Reel Qty | Part Number |
|---|---|---|
| QFN | 3000 | CHL8325A-00CRT[1] |
| QFN | 3000 | CHL8325A-xxCRT[2] |
| QFN | 3000 | CHL8325B-00CRT[1] |
| QFN | 3000 | CHL8325B-xxCRT[2] |

**Notes**

**1** For unprogrammed/default parts, use configuration file 00. Unprogrammed parts will not start up until programmed in order to insure a safe power up.

**2** -xx indicates a customer specific configuration file

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View CHL8325B-00CRT on WIN SOURCE
- Infineon Technologies Information

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- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management