16-bit and 20-bit, 8-pin ΔΣ ADCs

Features

- Delta-sigma Analog-to-digital Converter
  - Linearity Error: 0.0015% FS
  - Noise-free Resolution: Up to 17 Bits
- Differential Bipolar Analog Inputs
- V_{REF} Input Range from 250 mV to 5 V
- 50/60 Hz Simultaneous Rejection (CS5510/12)
- 16 to 326 Sps Output Word Rate
- On-chip Oscillator (CS5511/13)
- Power Supply Configurations:
  - V+ = 5 V, V- = 0 V
  - Multiple Dual-supply Arrangements
- Low Power Consumption
  - Normal Mode, 2.5 mW
  - Sleep Mode, 10 µW
- Low-cost, Compact, 8-pin Package
- Lead-free Device Package Options

General Description

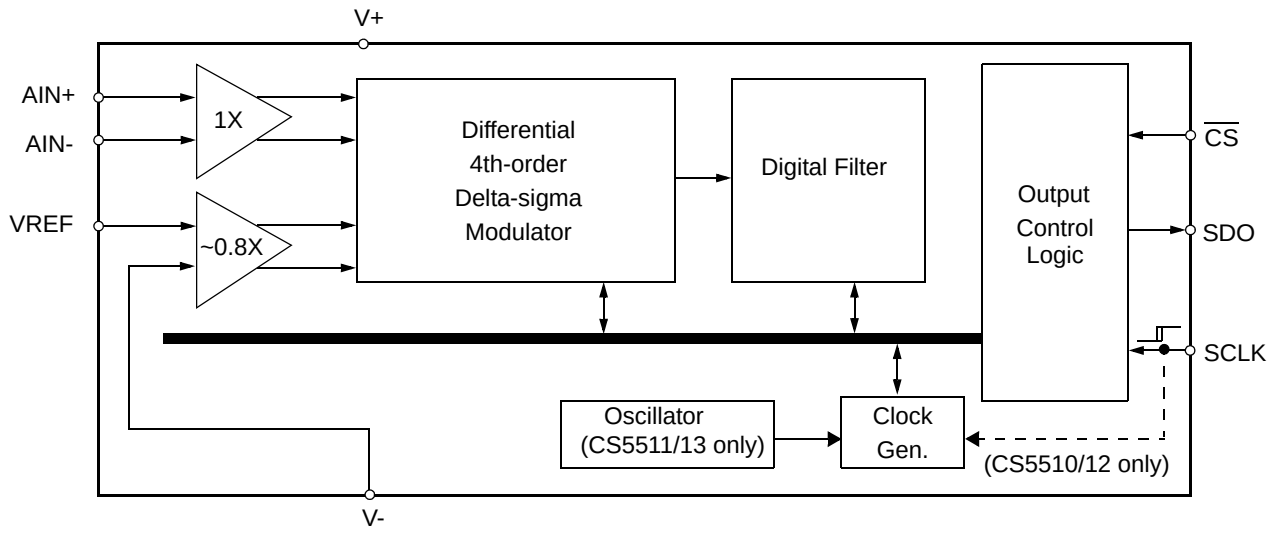
The CS5510/11/12/13 are low-cost, easy-to-use, ΔΣ analog-to-digital converters (ADCs) which use charge-balance techniques to achieve 16-bit (CS5510/11) and 20-bit (CS5512/13) performance. The ADCs are available in a space-efficient, 8-pin SOIC package and are optimized for measuring signals in weigh scale, process control, and other industrial applications.

To accommodate these applications, the ADCs include a fourth-order ΔΣ modulator and a digital filter. When configured with an external master clock of 32.768 kHz, the filter in the CS5510/12 provides better than 80 dB of simultaneous 50 and 60 Hz line rejection, and outputs conversion words at 53.5 Sps. The CS5511/13 include an on-chip oscillator which eliminates the need for an external clock source.

Low-power, flexible supply configurations, compact pinout, and ease of use make these products ideal solutions for cost-conscience and space-constrained applications.

ORDERING INFORMATION

See page 23.



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1. CHARACTERISTICS AND SPECIFICATIONS

ANALOG CHARACTERISTICS

(T_A = 25° C; V+ = 5 V ±5%; V- = 0 V; VREF = 2.5 V (relative to V-);
CS5510/12, SCLK = 32.768 kHz; CS5511/13, f_{osc} = 64 kHz ±32 kHz; OWR (Output Word Rate) = 53.5 Sps for CS5510/12; OWR = 107 Sps ± 50% for CS5511/13)
(See Note 1.)

Parameter		Min	Typ	Max	Unit
Accuracy					
Linearity Error (CS5510/11)		-	±0.0015	±0.003	% FS
Linearity Error (CS5512/13)		-	±0.0007	±0.0015	% FS
No Missing Codes (CS5510/11)		16	-	-	Bits
No Missing Codes (CS5512/13)		20	-	-	Bits
Bipolar Offset (CS5510/11)	(Note 2)	-	±3	±7	LSB_{16}
Bipolar Offset (CS5512/13)	(Note 2)	-	±40	±100	LSB_{20}
Offset Drift Over Temperature	(Notes 2 and 3)	-	60	-	nV/°C
Gain Drift Over Temperature	(Note 3)	-	1	-	ppm/°C
Analog Input					
Common Mode + Signal on AIN+ or AIN-	Dual Supply	V-	-	V+	V
Input Range (Bipolar)	|(AIN+ - AIN-)/(VREF - V-)|	72	80	88	% VREF
Common Mode Rejection	dc 50, 60Hz (CS5510/12)	- -	120 120	- -	dB dB
Input Capacitance		-	12	-	pF
CVF Current	AIN+, AIN- (Note 6)	-	10	-	nA

Typical Noise (Notes 4, 5 and 7)		
Output Word Rate (Hz)	**-3 dB Filter Frequency (Hz)**	**Noise (µV RMS)**
53.5	12.5	7.5

Notes:
1. Specifications guaranteed by design, characterization, and/or test.
2. Specification applies to the device only and does not include any effects by external parasitic thermocouples.
3. Drift over specified temperature range after power-up at 25° C.
4. Wideband noise aliased into the baseband. Referred to the input. Typical values shown for 25° C.
5. For peak-to-peak noise multiply by 6.6.
6. See the section of the data sheet which discusses Analog Input Models.
7. For CS5511/13, OWR = 107 Sps ± 50%.

Specifications are subject to change without notice.

ANALOG CHARACTERISTICS (Continued)

Parameter			Min	Typ	Max	Unit
Voltage Reference Input						
Range	{(VREF) - (V-)}	(Note 8)	0.250	2.5	(V+) - (V-)	V
Input Capacitance			-	7	-	pF
CVF current			-	6	-	nA
Power Supplies						
Supply Voltages	{(V+) - (V-)}		4.75	5	5.25	V
DC Power Supply Currents		(Note 9)				
	I_{V+}	CS5510	-	275	360	µA
		CS5511	-	290	380	µA
		CS5512	-	360	470	µA
		CS5513	-	385	500	µA
	I_{V-}	CS5510	-	275	360	µA
		CS5511	-	290	380	µA
		CS5512	-	360	470	µA
		CS5513	-	385	500	µA
Power Consumption		(Note 10)				
		CS5510	-	1.4	1.9	mW
		CS5511	-	1.5	2.0	mW
		CS5512	-	1.8	2.5	mW
		CS5513	-	1.9	2.7	mW
	Sleep	(Note 11)	-	10	-	µW
Power Supply Rejection	dc Positive Supply		-	85	-	dB
	dc Negative Supply		-	85	-	dB

Notes: 8. VREF is referenced to V- and must be less than or equal to V+.
9. Due to current through the $\overline{CS}$ pin, I_{V+} and I_{V-} may not always be the same value.
10. All outputs unloaded. All inputs CMOS levels (> (V+ - 0.6 V) or < (V- + 0.6 V)).
11. $\overline{CS}$ must be inactive (logic high) during sleep to meet this power specification.

DIGITAL CHARACTERISTICS

(T_A = 25° C; V+ = 5 V ±5%; V- = 0 V) (See Notes 1 and 12.)

Parameter		Symbol	Min	Typ	Max	Unit
High-Level Input Voltage:	CS and SCLK	V_{IH}	V+ - 0.45	-	-	V
Low-Level Input Voltage:	(Note 13) $\overline{CS}$	$\overline{CS}_{Low}$	-	-	V_{L1}	V
	SCLK	V_{IL}	-	-	V_{L1}	V
Input Current:	(Note 14) $\overline{CS}$	I_{CS}	-	-	1.0	mA
High-Level Output Voltage:	SDO, I_{source} = 5.0mA	V_{OH}	(V+) - 0.6	-	-	V
Low-Level Output Voltage:	(Note 14) SDO, I_{sink} = 1.0mA	V_{OL}	-	-	(CS_{Low}) + 0.6	V
Input Leakage Current	SCLK	I_{in}	-	±0.015	±10	µA
3-State Leakage Current	SCLK	I_{OZ}	-	-	±10	µA

Notes: 12. All measurements performed under static conditions.
13. V_{L1} is 0.5 (V+ - V-) + 0.6 V + V-.
14. The $\overline{CS}$ signal provides the sink current path for the SDO pin when $\overline{CS}$ is low. The external drive logic to $\overline{CS}$, therefore, must be able to handle the logic-low current drive levels for all devices attached to SDO. The voltage specified for SDO is relative to $\overline{CS}_{Low}$. See Section 2.3.1, *"Digital Logic Levels"* and Figure 11 for more details.

DYNAMIC CHARACTERISTICS

Parameter		Symbol	Ratio	Units
Modulator Sampling Frequency	CS5510/12	f_S	SCLK/4	Hz
	CS5511/13	f_S	$f_{osc}/4$	Hz
Output Word Rate	CS5510/12	OWR	SCLK/612	Sps
	CS5511/13	OWR	$f_{osc}/612$	Sps
Filter Settling Time to 1/2 LSB (Full Scale Step)		t_s	4/OWR	s

ABSOLUTE MAXIMUM RATINGS

(V- = 0 V) (See Note 15.)

Parameter		Symbol	Min	Typ	Max	Unit
DC Power Supplies	(Note 16)					
	Positive	V+	-0.3	-	+6.0	V
	Negative	V-	-6.0	-	+0.3	V
Input Current, Any Pin Except Supplies	(Notes 17 and 18)	I_{IN}	-	-	±10	mA
Output Current		I_{OUT}	-	-	±25	mA
Package Power Dissipation	(Note 19)	PDN	-	-	400	mW
Analog Input Voltage	AIN pins	V_{INA}	(V-)+(-0.3)	-	(V+)+0.3	V
Digital Input Voltage		V_{IND}	($\overline{V\text{-}}$)+(-0.3)	-	(V+)+0.3	V
Ambient Operating Temperature		T_A	-40	-	+85	°C
Storage Temperature		T_{stg}	-65	-	+150	°C

Notes: 15. All voltages with respect to V-.

16. V+ and V- must satisfy $0.0V \le \{(V+) - (V-)\} \le +6.0$ V.

17. Applies to all pins including continuous overvoltage conditions at the analog input (AIN) pins.

18. Transient current of up to 100 mA will not cause SCR latch-up. Maximum input current for a power supply pin is ±50 mA.

19. Total power dissipation, including all input currents and output currents.

WARNING: Operation at or beyond these limits may result in permanent damage to the device. Normal operation is not guaranteed at these extremes.

SWITCHING CHARACTERISTICS - CS5510/12

(T_A = 25° C; V+ = 5 V ±5%; V- = 0 V; Input Levels: Logic 0 = 0 V, Logic 1 = V+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Master Clock Timing						
Master Clock Frequency (CS5510)	(Note 20)	SCLK	10	32.768	130	kHz
Master Clock Frequency (CS5512)	(Note 20)	SCLK	10	32.768	200	kHz
Master Clock Duty Cycle			40	-	60	%
Rise Times	(Note 21)	t_{rise}				
	CSB		-	-	1.0	µs
	SCLK		-	-	10	µs
	SDO		-	50	-	ns
Fall Times	(Note 21)	t_{fall}				
	CSB		-	-	1.0	µs
	SCLK		-	-	10	µs
	SDO		-	50	-	ns
Serial Port Timing						
Serial Clock Frequency (CS5510)	(Note 22)	SCLK	10	32.768	130	kHz
Serial Clock Frequency (CS5512)	(Note 22)	SCLK	10	32.768	200	kHz
SCLK High to Enter Sleep	(Note 22)	t_{SLP}	200	-	2000	µs
SCLK Low to Exit Sleep	(Note 22)	t_{WAKE}	10	-	-	µs
Serial Clock	Pulse Width High	t_1	2	-	60	µs
	Pulse Width Low	t_2	2	-	60	µs
SDO Read Timing						
$\overline{CS}$ to Data Valid		t_3	-	-	150	ns
SCLK Falling to New Data Bit		t_4	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_5	-	-	150	ns
$\overline{CS}$ Falling to SCLK Rising		t_{11}	200	-	-	ns

Notes: 20. Device parameters are specified with 32.768 kHz clock; however, clocks up to 130 kHz (CS5510) or 200 kHz (CS5512) can be used for increased throughput. Higher clock rates will result in degraded linearity specifications, as shown in Figures 14 and 15.

21. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

22. On the CS5510/12, the serial clock input (SCLK) provides the master clock to operate the converter as well as the serial data clock used to read conversion data. If SCLK is held high (logic 1) for t_{SLP} or longer, the CS5510/12 enters sleep. To exit from sleep mode, SCLK must be held low (logic 0) for t_{WAKE} or longer.

SWITCHING CHARACTERISTICS - CS5511/13

(T_A = 25° C; V+ = 5 V ±5%; V- = 0 V; Input Levels: Logic 0 = 0 V, Logic 1 = V+; C_L = 50 pF)

Parameter		Symbol	Min	Typ	Max	Unit
Internal Oscillator Timing						
Internal Oscillator Frequency	(Note 23)	f_{osc}	32	64	100	kHz
Internal Oscillator Drift Over Temperature		-	-	-0.02	-	%/°C
Serial Port Timing						
Serial Clock Frequency	(Note 24)	SCLK	-	-	2	MHz
SCLK High to Enter Sleep	(Notes 24 and 25)	t_{SLP}	200	-	2000	µs
SCLK Low to Exit Sleep	(Notes 24 and 25)	t_{WAKE}	10	-	-	µs
Rise Times	(Note 26)	t_{rise}				
	CSB		-	-	1.0	µs
	SCLK		-	-	10	µs
	SDO		-	50	-	ns
Fall Times	(Note 26)	t_{fall}				
	CSB		-	-	1.0	µs
	SCLK		-	-	10	µs
	SDO		-	50	-	ns
Serial Clock	Pulse Width High	t_6	200	-	-	ns
	Pulse Width Low	t_7	200	-	-	ns
SDO Read Timing						
$\overline{CS}$ to Data Valid		t_8	-	-	150	ns
SCLK Falling to New Data Bit		t_9	-	-	150	ns
$\overline{CS}$ Rising to SDO Hi-Z		t_{10}	-	-	150	ns
$\overline{CS}$ Falling to SCLK Rising		t_{11}	200	-	-	ns

Notes: 23. The internal oscillator in the CS5511/13 provides the master clock for performing conversions. Data is retrieved from the serial port using the SCLK input pin.

24. The minimum SCLK rate for the CS5511/13 assumes that SCLK is logic 0 when idle. When data is being read from the ADC, SCLK must be burst at a minimum rate of 10 kHz and with a minimum of a 10 percent duty cycle. Rates slower than this can potentially put the ADC into sleep as the sleep mode is entered after SCLK is logic 1 for t_{SLP} time.

25. On the CS5511/13, the serial clock (SCLK) is used to transfer data from the CS5511/13. If SCLK is held high (logic 1) for t_{SLP} or longer, the CS5511/13 enters sleep mode. To exit from sleep mode, SCLK must be held low (logic 0) for t_{WAKE} or longer.

26. Specified using 10% and 90% points on waveform of interest. Output loaded with 50 pF.

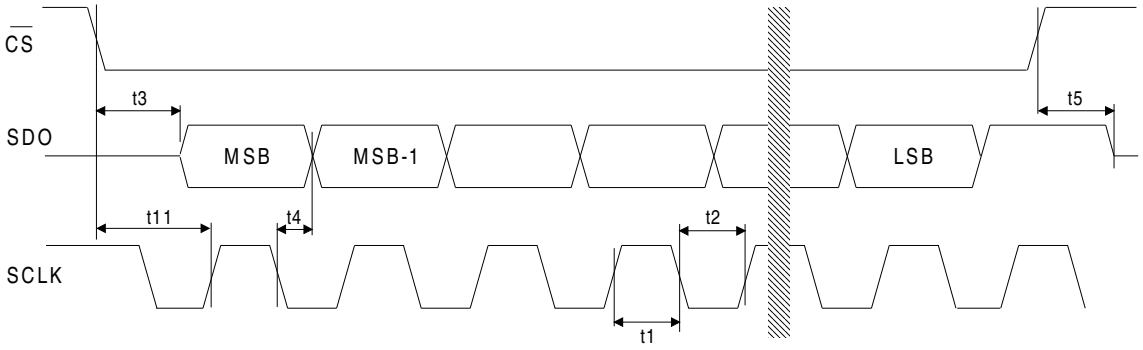


Figure 1. SDO Read Timing CS5510/12 (Not to Scale).

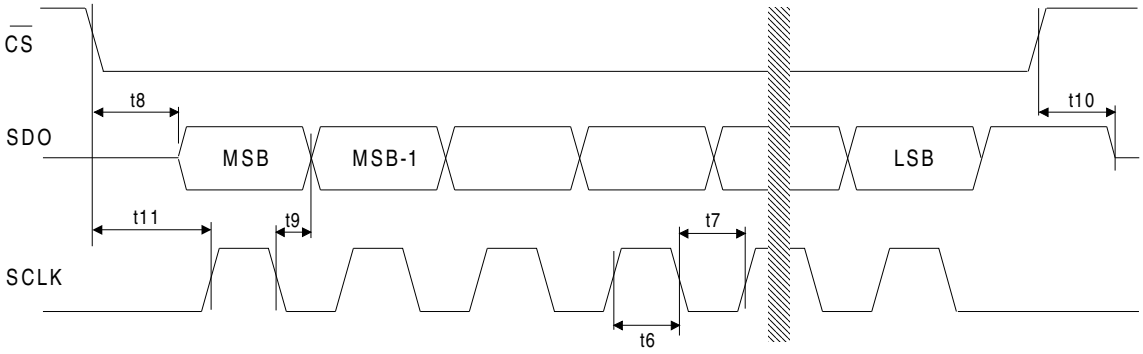


Figure 2. SDO Read Timing CS5511/13 (Not to Scale).

2. GENERAL DESCRIPTION

The CS5510/11/12/13 are low-cost, easy-to-use, ΔΣ analog-to-digital converters (ADCs) which use charge balance techniques to achieve 16-bit (CS5510/11) and 20-bit (CS5512/13) performance. The ADCs are available in a space-efficient, 8-pin, SOIC package and are optimized for measuring signals in weigh scale, process control, and other industrial applications.

To accommodate these applications, the ADCs include a fourth-order ΔΣ modulator and a digital filter. When configured with an external master clock of 32.768 kHz, the filter in the CS5510/12 provides better than 80 dB of simultaneous 50 and 60 Hz line rejection, and outputs conversion words at 53.5 Sps. The CS5511/13 include an on-chip oscillator which eliminates the need for an external clock source.

The CS5510/11/12/13 ADCs are designed to operate from a single +5 V supply or a variety dual-supply configurations and are optimized to digitize bipolar signals in industrial applications.

To achieve low cost, the CS5510/11/12/13 family of converters have no on-chip calibration features. The CS5510/11/12/13 offer very low offset drift, low gain drift, and excellent linearity.

2.1 Analog Input

The CS5510/11/12/13 provides a differential input span of approximately ±(0.80 ± 0.08) times the differential voltage reference (VREF - V-). This translates to typically ±4.0 V fully differential when the reference voltage between VREF and V- is 5 V, and typically ±2.0 V fully differential at 2.5 V.

Note: When a smaller reference voltage is used, the resulting code widths are smaller. Since the output codes exhibit more changing codes for a fixed amount of noise, the converter appears noisier.

2.1.1 Analog Input Model

Figure 3 illustrates the input model for the AIN pins. The model includes a coarse/fine charge buffer which reduces the dynamic current demands from the signal source. The buffer is designed to accommodate rail-to-rail (common-mode plus signal) input voltages. Typical CVF (sampling) current is about 10 nA. Application Note 30, *"Switched-capacitor A/D Input Structures"*, details various input architectures.

2.2 Voltage Reference Input

The voltage between the VREF and V- pins of the converter determines the voltage reference for the converter. This voltage can be as low as 250 mV, or as great as (V+) - (V-). The VREF pin can be connected directly to the V+ pin. This will establish a voltage reference equal to (V+) - (V-) for the converter. The effective resolution of the part (noise-free bits for a single sample with no averaging) will vary with VREF. Figure 4 shows how the VREF voltage affects the noise-free resolution of the

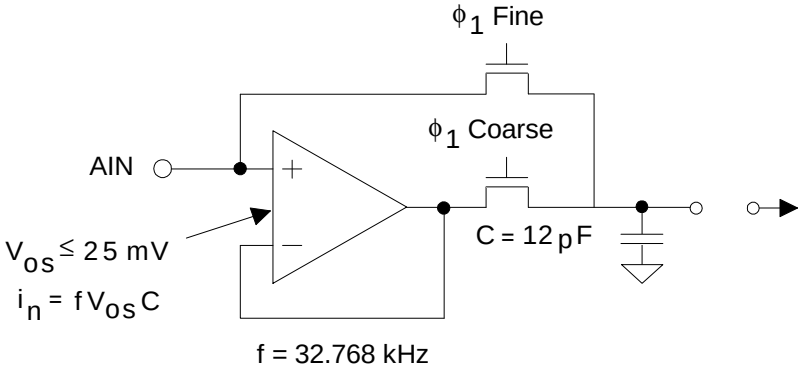


Figure 3. Input models for AIN+ and AIN- pins.

CS5512/13. The CS5510/11 follow the same curve, but are limited to 16 bits of resolution. Note that the reference voltage should not be established prior to having the supply voltages on the V+ and V- pins.

2.2.1 Voltage Reference Input Model

Figure 5 illustrates the input model for the VREF pin. It includes a coarse/fine charge buffer which reduces the dynamic current demand of the external reference. Typical CVF (sampling) current is about 6 nA (See Figure 5).

The nominal input span of the converter is defined to be a bipolar span equal to ±(VREF - V-)*(0.80 ±0.08).

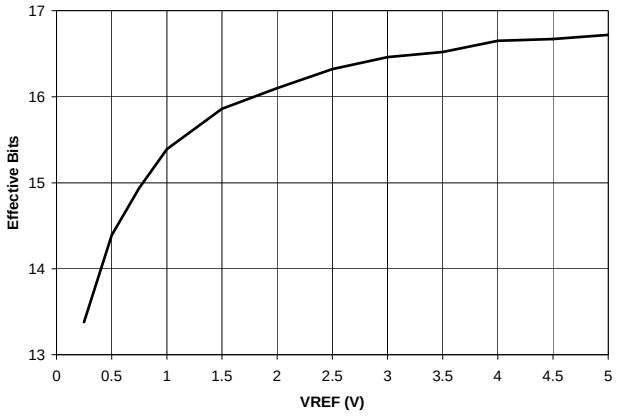


Figure 4. CS5512/13 Measured Noise-Free Bits vs. VREF.

2.3 Power Supply Arrangements

The CS5510/11/12/13 are designed to operate from single or dual supplies. Figure 6 illustrates the CS5510/11/12/13 connected with a single +5 V supply to measure differential inputs relative to a common mode of 2.5 V. Figure 7 illustrates the CS5510/11/12/13 connected with ±2.5 V analog supplies to measure ground-referenced, bipolar signals. It is not necessary that the dual supples on the ADCs be balanced, however, they must sum to five volts. Figure 8 illustrates the ADCs configured with V+ = +3.3 V and V- = -1.7 V, accommodating a +3.3 V digital supply.

2.3.1 Digital Logic Levels

The many power supply configurations available in the CS5510/11/12/13 allow for a wide range of digital logic levels. The logic-high input and output levels are determined by the V+ pin. The logic-low output on SDO is referenced to and driven by the current logic-low voltage on $\overline{CS}$. Since the CS5510/11/12/13 do not include a dedicated

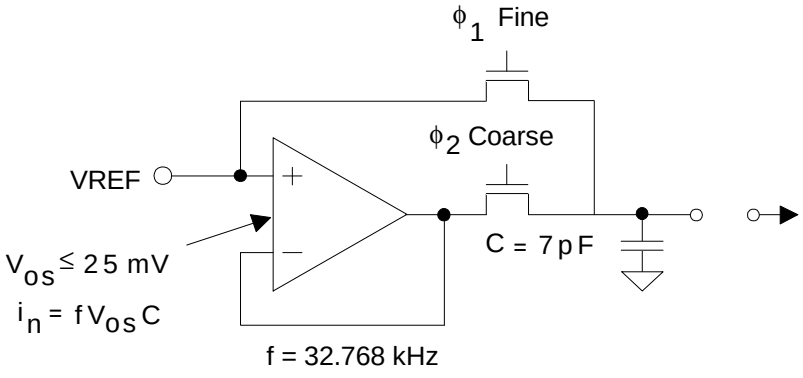


Figure 5. Input model for VREF pin.

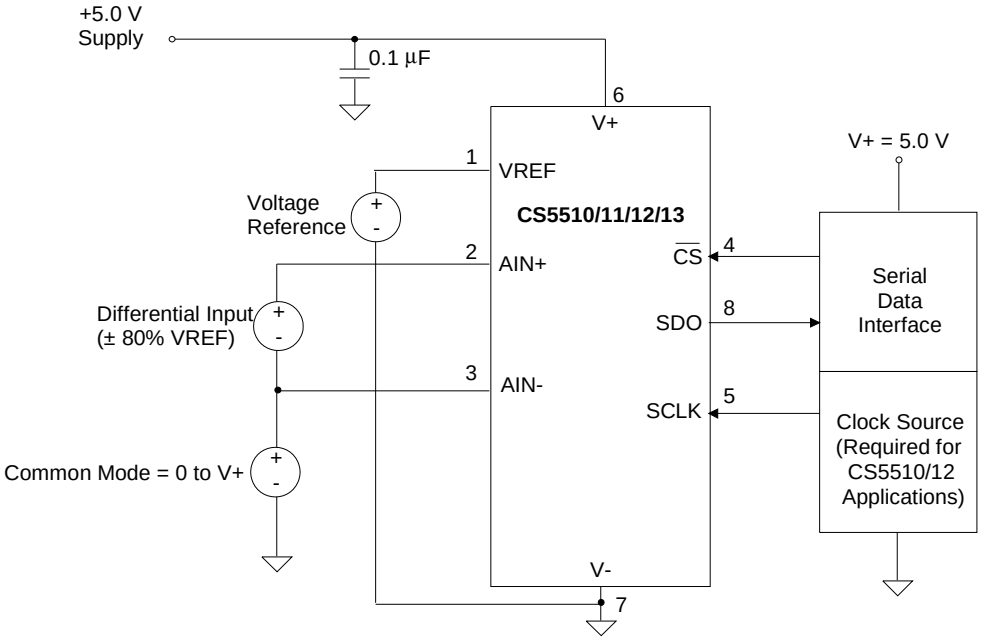


Figure 6. CS5510/11/12/13 Configured with a +5.0 V Analog Supply.

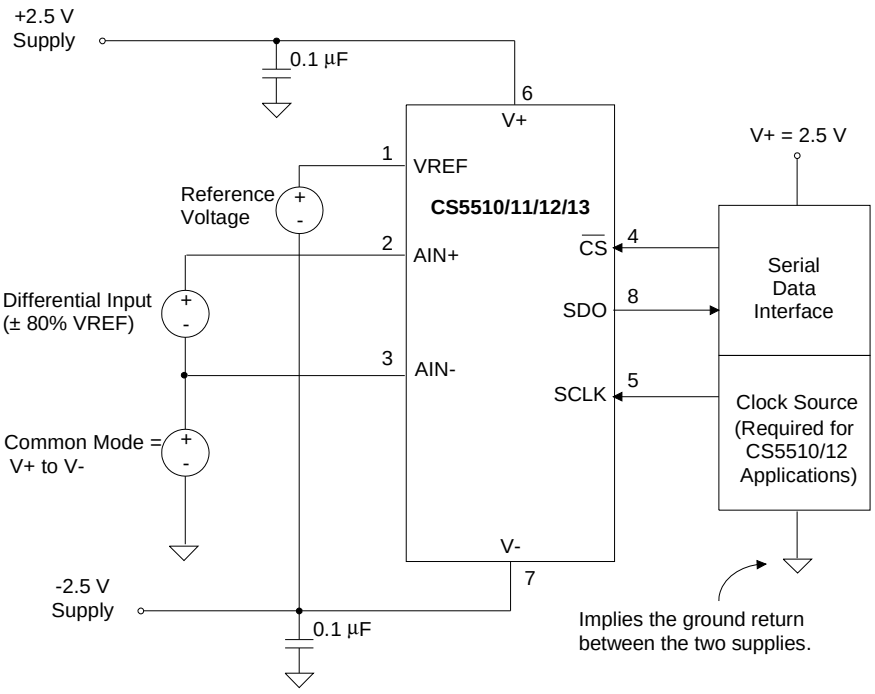


Figure 7. CS5510/11/12/13 Configured with ±2.5 V Analog Supplies.

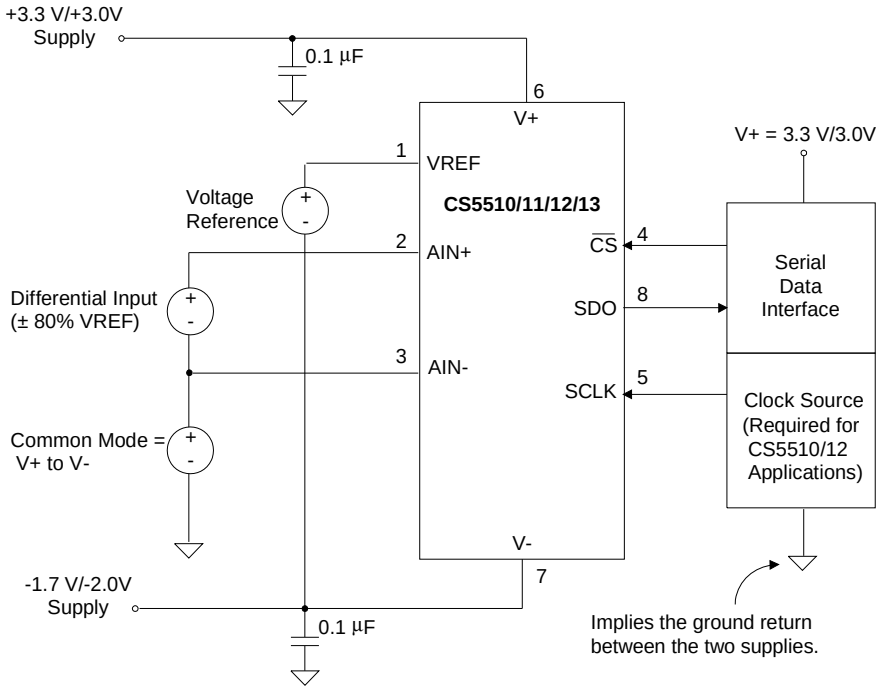


Figure 8. CS5510/11/12/13 Configured with V+ = +3.3 V and V- = -1.7 V; or V+ = +3.0 V and V- = -2.0 V.

ground pin, $\overline{CS}_{Low}$ defines the logic-low level for the digital interface. Figures 9 and 10 illustrate the threshold levels of the CS5510/11/12/13 serial interface ($\overline{CS}$, SCLK, and SDO).

To accommodate opto-isolators, the SCLK input is designed with a Schmitt-trigger to allow an opto-isolator with slower rise and fall times to directly drive the pin. Additionally, SDO is capable of sinking up to 1 mA or sourcing up to 5 mA to directly drive an opto-isolator LED. SDO will have less than a 600 mV loss in the drive voltage when sinking or sourcing its current. As shown in Figure 11, the $\overline{CS}$ signal provides the sink current path for the SDO pin when its voltage is low (i.e. the voltage specified for SDO is relative to $\overline{CS}_{Low}$.).

2.4 Clock Generator

The CS5510/12 and CS5511/13 provide distinct modes for generating the master clock for the ADCs. The CS5510/12 uses the SCLK input pin as its operating clock. The CS5511/13 has an on-chip oscillator that provides its master clock. The SCLK pin on the CS5511/13 is used only to read data and to put the part into sleep mode.

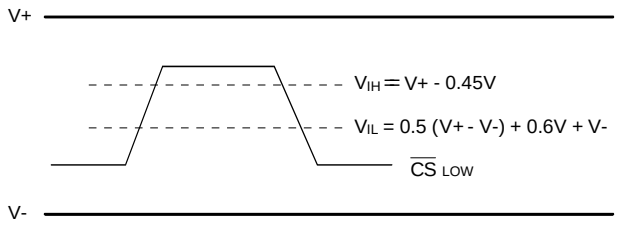


Figure 9. $\overline{CS}$ and SCLK Digital Input Levels.

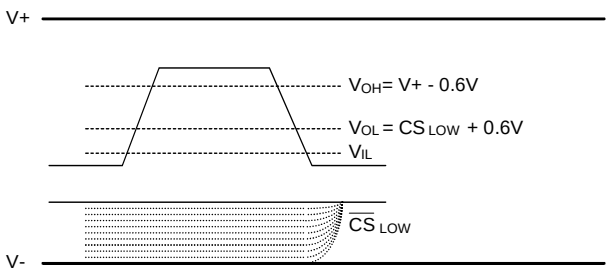


Figure 10. SDO Digital Output Levels.

2.4.1 External Clock Source for CS5510/12

The user must provide an external (CMOS compatible) clock to the CS5510/12. The clock is input to SCLK where it is then divided down to provide the master clock for the ADC. The output word rate (OWR) for the CS5510/12 is derived from the SCLK, and is equal to SCLK/612. Figure 12 illustrates an external 32.768-kHz, CMOS-compatible clock oscillator that a user might consider.

Another clock generation option is to use a microcontroller. Some microcontrollers have dedicated timer/counter circuitry which can generate a clock signal on an output pin with no software overhead. Such a microcontroller circuit is shown in Figure 13.

Note that the CS5510 can operate with an external, CMOS-compatible clock at frequencies up to 130 kHz, and the CS5512 can operate with an external clock of up to 200 kHz with a maximum 22 ns of jitter. Linearity performance is degraded slightly with higher clock speeds, as shown in Figures 14 and 15. The noise performance of the parts, however, is not affected by higher clock speeds.

2.4.2 Internal Oscillator for CS5511/13

The CS5511/13 includes an on-chip oscillator. This oscillator provides the master clock for the

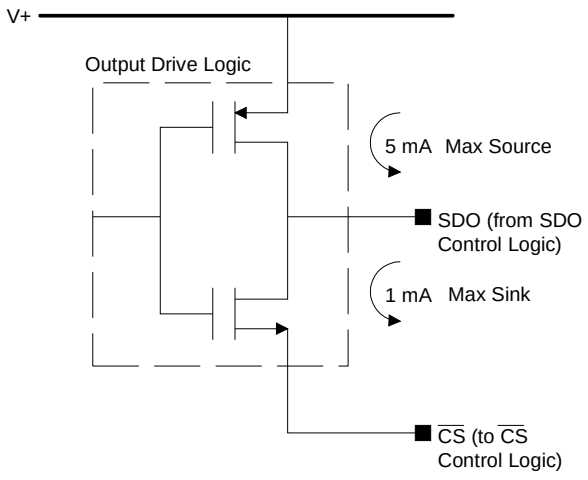


Figure 11. Serial Port Output Drive Logic.

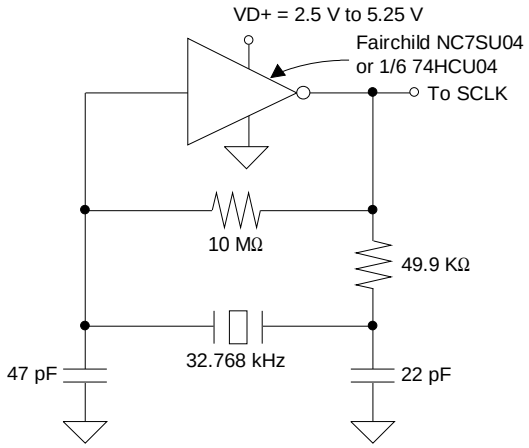


Figure 12. External (CMOS Compatible) Clock

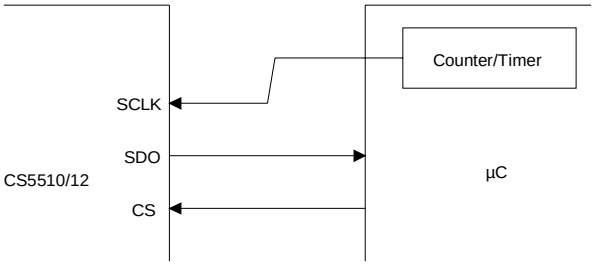


Figure 13. Using a Microcontroller as a Clock

CS5511/13 and oscillates at 64 kHz ±32 kHz. The output word rate (OWR) for the CS5511/13 is derived from the internal oscillator, and is equal to $f_{osc}/612$. Due to the part-to-part variances in the oscillator frequency, the OWR of the CS5511/13 can vary between 53 Sps and 159 Sps.

2.5 Performing Conversions

After power and a clock source are established to the CS5510/11/12/13, the ADCs begin performing conversions. The three sections that follow explain how to read conversion data from each ADC, and decode the conversion word into the respective flag and data bits. Keep in mind that in the CS5510/12, SCLK provides the external clock source for the converter. Data is clocked from the CS5510/12 at the rate set by the external clock source (typically 32.768 kHz). The CS5511/13 provides an on-chip oscillator for the master clock. In the CS5511/13, SCLK is asynchronous to the on-chip oscillator and can be clocked at a rate up to 2 MHz.

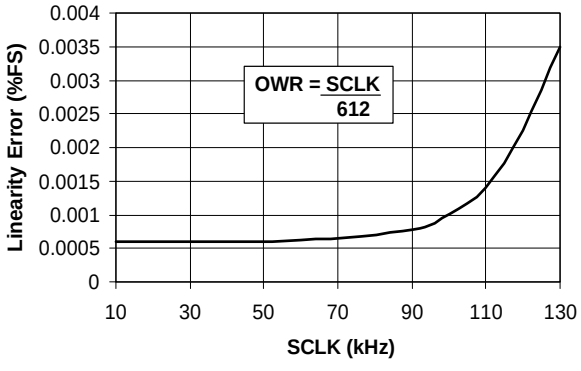


Figure 14. Typical Linearity Error for CS5510.

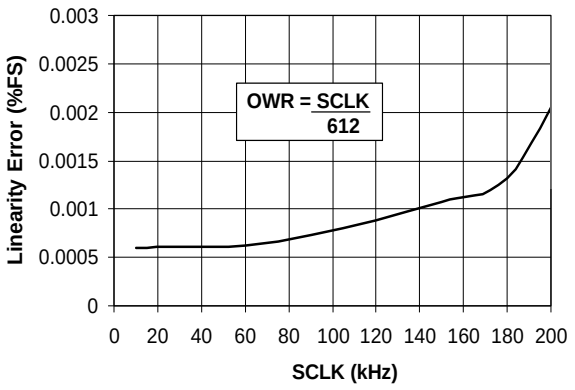


Figure 15. Typical Linearity Error for CS5512.

2.5.1 Reading Conversions - CS5510/12

After power-up, the CS5510/12 will begin converting once a clock source is applied to the SCLK pin. When a conversion has completed, and there is new data in the output register, the SDO line will fall to a logic-low level if $\overline{CS}$ is also at a logic-low state (SDO will always be high-impedance when $\overline{CS}$ is high). If $\overline{CS}$ is low at the end of the conversion cycle, SDO will fall on the rising edge of an SCLK. After SCLK falls, the next SCLK cycle (high, then low) will begin clocking out the data. The first data bit therefore, is 1-½ SCLK cycles wide. Twenty-four SCLK cycles (after the initial high-low transition) are needed to retrieve the conversion word from the device (see Figures 16 and 17). The data bits can be read on the rising edge of SCLK, and the next data bit is output to SDO on the falling edge of SCLK. Once the entire data word has been read, SDO will return to a logic-high state until there is a new conversion word available. If $\overline{CS}$ is at a logic-high at the end of the conversion cycle, the data will not be shifted out of the part until $\overline{CS}$ is brought to a logic-low state during the next conversion cycle. If a new conversion becomes available while the current data is being read, the data register will not be updated, and the new conversion word will be lost. The user need not read every conversion. If the user chooses not to read a conversion, $\overline{CS}$ should remain at a logic-high state for the duration of the conversion cycle. Note that if $\overline{CS}$ goes to a logic-high state during a read, the current conversion data will be lost and replaced by a new conversion word when the new conversion data is available.

2.5.2 Reading Conversions - CS5511/13

After power-up, the CS5511/13 begins converting and updating the output register. When there is new data in the output register (at the end of a conversion cycle) the SDO line will fall to a logic-low level if $\overline{CS}$ is also at a logic-low state (SDO will always be high-impedance when $\overline{CS}$ is high). Twenty-four SCLK cycles are needed to retrieve the conversion word from the device (see Figures 18 and 19). The data bits can be read on the rising edge of SCLK, and the next data bit is output to SDO on the falling edge of SCLK. Once the entire data word has been read, SDO will return to a logic-high state until there is a new conversion word available. If new conversions become available while the current data is being read, the data register will not be updated, and the new conversions will be lost. The user need not read every conversion. If the user chooses not to read a conversion after SDO falls, SDO will rise seventeen oscillator clock cycles (of the internal oscillator) before the next conversion word is available and then fall again to signal that the conversion is complete. Note that if a conversion word is not read before the next conversion word is ready, or if $\overline{CS}$ goes to a logic-high state during a read, the current conversion data will be lost and replaced by a new conversion word when the new conversion data is available.

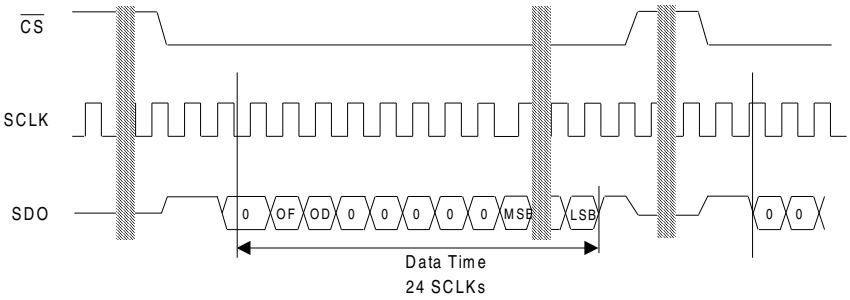


Figure 16. Data Word Timing for the CS5510.

2.5.3 Output Coding

As shown in Tables 1 and 2, the CS5510/11/12/13 present output conversions as 24-bit conversion words. The first bit of the conversion word indicates that a conversion is done through SDO falling from a logic high to a logic low level. The first and the fourth bits output will always be zero. The second and third bits are error flags, representing an overflow or oscillation condition. In the CS5510/11, there are four more bits of zero, and the remaining 16 bits are the conversion data, output MSB first (Table 2). In the CS5512/13, the final 20 bits are the conversion data, which is output MSB first (Table 1).

Bits D22-D21 are the two flag bits. The OF (Overrange Flag) bit is set to a logic 1 any time the input signal is more positive than positive full scale, or more negative than negative full scale. It is cleared back to logic 0 whenever a conversion word occurs which is not overranged. The OD (Oscillation Detect) bit is set to a logic 1 any time that an oscillatory condition is detected in the modulator. This does not occur under normal operating conditions, but may occur whenever the input to the converter is ex-

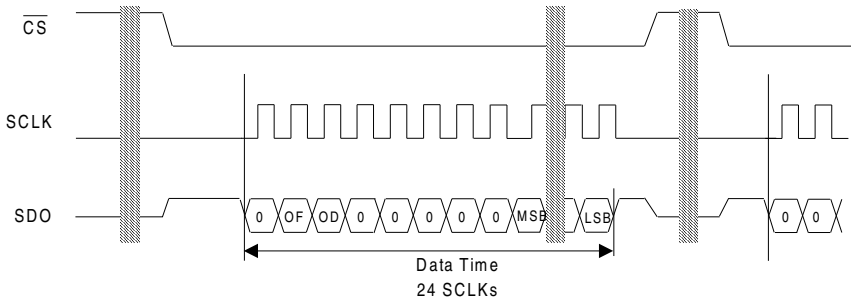


Figure 17. Data Word Timing for the CS5511.

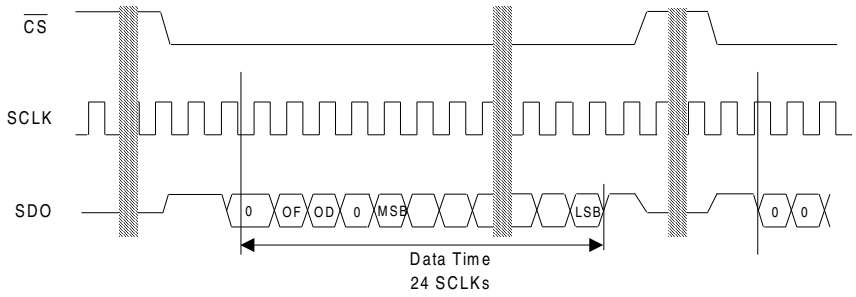


Figure 18. Data Word Timing for the CS5512.

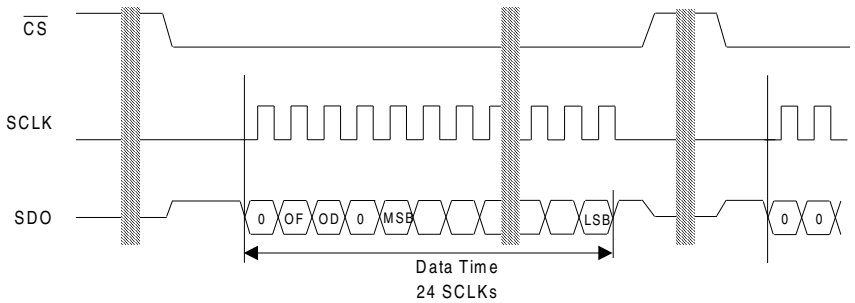


Figure 19. Data Word Timing for the CS5513.

Bipolar Input Voltage	Two's Complement (20-Bit)	Two's Complement (16-Bit)
>(VFS-1.5 LSB)	7FFFF	7FFF
VFS-1.5 LSB	7FFFF ----- 7FFFE	7FFF ----- 7FFE
-0.5 LSB	00000 ----- FFFFF	0000 ----- FFFF
-VFS+0.5 LSB	80001 ----- 80000	8001 ----- 8000

Note: VFS in the table equals the voltage between AIN+ and AIN-. See text about error flags under overrange conditions.

Table 3. CS5510/11/12/13 Output Coding.

cessively overranged. If the OD bit is set, the conversion data bits can be completely erroneous. The OD flag bit will be cleared to logic 0 four output words after the modulator becomes stable again. The OD flag can occur independent of OF with a spike on the input. Both flag bits should be tested if any overrange condition occurs.

Table 3 illustrates the output coding for the CS5510/11/12/13. Conversions are output as two's complement values representing bipolar input signals.

2.5.4 Digital Filter

The CS5510/11/12/13 have a modified $Sinc^4$ digital filter that provides CLK/612 Hz conversion rates (CLK represents SCLK for the CS5510/12 and the internal oscillator for the CS5511/13). The filters are optimized to yield better than 80 dB rejection between 47 Hz to 63 Hz (i.e. 80 dB minimum rejection for both 50 Hz and 60 Hz) when the master clock is 32.768 kHz. The filter has a response as shown in Figure 20. Table 4 shows the filter response for frequencies from 38 Hz to 71 Hz. Note that the response of the CS5511/13 will be similar, but the frequencies scale with the on-chip oscillator's frequency, which can be from 32 kHz to 96 kHz (i.e. conversion rates can vary between 53 Sps to 159 Sps). Further note that after initial power up, or after returning from sleep mode, the filter requires four conversion cycles to produce a

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	OF	OD	0	MSB	18	17	16	15	14	13	12
D11	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
11	10	9	8	7	6	5	4	3	2	1	LSB

Table 1. CS5512/13 Output Conversion Data Register Description (Flags + 20 bits).

D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12
0	OF	OD	0	0	0	0	0	MSB	14	13	12
D11	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
11	10	9	8	7	6	5	4	3	2	1	LSB

Table 2. CS5510/11 Output Conversion Data Register Description (Flags + 16 bits).

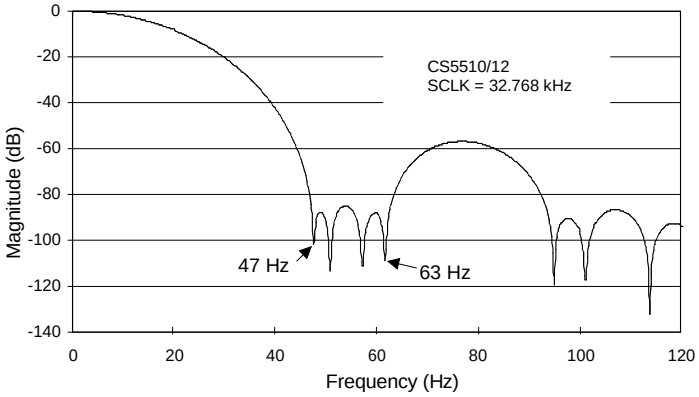


Figure 20. Digital Filter Response.

Frequency (Hz)	Rejection (dB)	Frequency (Hz)	Rejection (dB)	Frequency (Hz)	Rejection (dB)	Frequency (Hz)	Rejection (dB)
38	37	47	84	56	91	65	73
39	39	48	92	57	109	66	69
40	42	49	88	58	94	67	66
41	46	50	92	59	89	68	64
42	49	51	105	60	88	69	63
43	54	52	89	61	92	70	61
44	58	53	86	62	104	71	60
45	64	54	85	63	84	-	-
46	72	55	87	64	77	-	-

Table 4. Digital Filter Response at 32.768 kHz.

valid conversion due to the modified $Sinc^4$ filter characteristics.

2.5.5 Multiplexed Applications

The settling performance of the CS5510/11/12/13 in multiplexed applications is determined by the $Sinc^4$ filter. To settle, a step input requires 4 full conversion cycles after the analog input has switched. In this case, the throughput is reduced by a factor of four as the first three conversions after the step is applied will not be fully settled.

If the application does not require the maximum throughput possible from the ADC, the multiplexer can be switched at any time. In this case, the system must wait for at least five conversion cycles for a fully-settled result from the ADC.

If maximum throughput is required in a multiplexed application, the multiplexer must be switched at the correct time during the data collection process. For maximum throughput with the CS5510/12, switching of a multiplexer should occur 595 SCLK cycles after SDO falls. For maximum throughput with the CS5511/13, switching of a multiplexer should occur on the rising edge of SDO during a conversion in which the data word is not read. The conversion data that is immediately available when SDO falls again is valid, and represents the analog input from the previous multiplexer setting. The next three conversions from the part will be unsettled values, and the fourth conversion will represent a fully-settled result from the new multiplexer setting. The multiplexer should be switched again at the appro-

priate time during the third conversion cycle to ensure the maximum possible throughput.

2.6 Digital Off-chip System Calibration

The CS5510/11/12/13 exhibit excellent linearity with low offset and gain drift, without the need for calibration. If precision voltage measurements are required by the system, however, software-based offset and gain calibration can be performed by the system.

To perform a software offset calibration, the "zero-point" of the system should be established by applying an input to the system equal to zero. Then, the user can obtain a conversion and store it in memory as the system's zero point (ZP). This number can then be used as the zero point for any subsequent conversion words. In the 20-bit devices (CS5512 and CS5513), multiple conversions can be averaged to arrive at a more accurate offset value. In the 16-bit devices (CS5510 and CS5511), averaging may not be meaningful, because the noise will be below the size of one LSB when using nominal voltages for VREF (2.5 V).

A software gain calibration can be performed by bringing the system to a known calibration Voltage value (Vcal) and acquiring a conversion (note that Vcal should be low enough to compensate for the possible gain error of the ADC). Multiple conversions can be averaged at this point to improve the accuracy of the calibration. The code obtained from this conversion is the real value (Cr) of the calibration Voltage input, and will differ from the ideal value. The ideal value for this conversion (Ci) will be equivalent to: 0x7FFF*Vcal/(0.80*Vref) for the CS5510/11, and 0x7FFF*Vcal/(0.80*Vref) for the CS5512/13. The gain error (GE) is equal to: (Cr - ZP)/Ci. To correct for both offset and gain error in subsequent conversions, subtract the offset error, and then divide by the gain error.

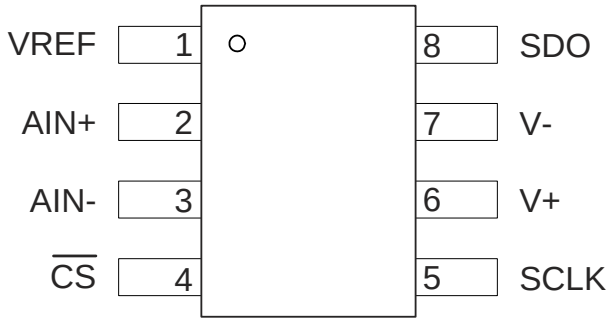
2.7 Power Consumption, Sleep and Reset

The CS5510/11/12/13 accommodates two power modes: *normal* and *sleep*. The normal mode is the default mode and is entered after power is established to the ADC. In normal mode, the ADCs typically consumes 2.5 mW. Sleep is entered when the user leaves SCLK high for at least 200 µs. The ADCs are guaranteed to be in sleep after SCLK is high (logic 1) for 2 ms. The sleep mode reduces the consumed power to less than 10 µW when $\overline{CS}$ is high (logic 1). If $\overline{CS}$ is low (logic 0) at this time, the SDO drive logic will still be active, and the consumed sleep power will be greater. To exit sleep and return to normal mode, the user must return SCLK low for at least 10 µs. After a sleep is exited, the ADCs reset all their internal logic, including their digital filters, and begin performing conversions. Since the filters are reset, the first three conversion after returning to normal mode will not be fully settled.

2.8 PCB Layout

The CS5510/11/12/13 should be placed entirely over the analog ground. Place the analog-digital plane split immediately adjacent to the digital pins of the chip.

3. PIN DESCRIPTIONS



Control Pins and Serial Data I/O

$\overline{CS}$ - Chip Select, Pin 4

$\overline{CS}$ is a dual function pin, which determines the state of SDO, as well as the digital logic-low output level. When $\overline{CS}$ is low, SDO will be active. When high, the SDO pin will output a high-impedance state. The logic-low level of SDO will match the active-low voltage on $\overline{CS}$.

SDO - Serial Data Output, Pin 8

SDO is the serial data output. It will output a high-impedance state if $\overline{CS}$ = 1. The logic-low level of SDO will match the active-low voltage on $\overline{CS}$.

SCLK - Serial Clock Input, Pin 5

SCLK is the serial bit-clock which controls the shifting of data from the ADCs. This input goes through a Schmitt trigger to allow for slow rise and fall time signals. If held high, the device will enter sleep mode. In the CS5510/12, this input is also used as a master clock source which determines conversion speeds and throughput. In the CS5511/13, SCLK is only used to read the conversion data and put the part in sleep mode.

Measurement and Reference Inputs

AIN+, AIN- - Differential Analog Input, Pins 2, 3

Differential input pins into the device

VREF - Voltage Reference Input, Pin 1

Input Voltage which establishes the voltage reference, with respect to V-, for the on-chip modulator

Power Supply Connections

V+ - Positive Power, Pin 6

Positive supply voltage

V- - Negative Supply, Pin 7

Negative supply voltage

4. SPECIFICATION DEFINITIONS

Linearity Error

The deviation of a code from a straight line which connects the two end points of the A/D Converter transfer function. One end point is located 1/2 LSB below the first code transition and the other end point is located 1/2 LSB beyond the code transition to all ones. Units in percent of full-scale.

Differential Nonlinearity

The deviation of a code's width from the ideal width. Units in LSBs.

Full Scale Error

The deviation of the last code transition from the ideal [{(VREF) - (V-)} - 3/2 LSB]. Units are in LSBs.

Bipolar Offset

The deviation of the mid-scale transition (111...111 to 000...000) from the ideal (1/2 LSB below the voltage on the AIN- pin). Units are in LSBs.LK

5. ORDERING INFORMATION

Device Number	Oscillator	Resolution	Linearity Error (Max)	Temperature Range	Package
CS5510-ASZ	External	16 Bits	±0.003%	-40°C to +85°C	8-pin SOIC Lead-free
CS5511-ASZ	Internal				
CS5512-BSZ	External	20 Bits	±0.0015%		
CS5513-BSZ	Internal				

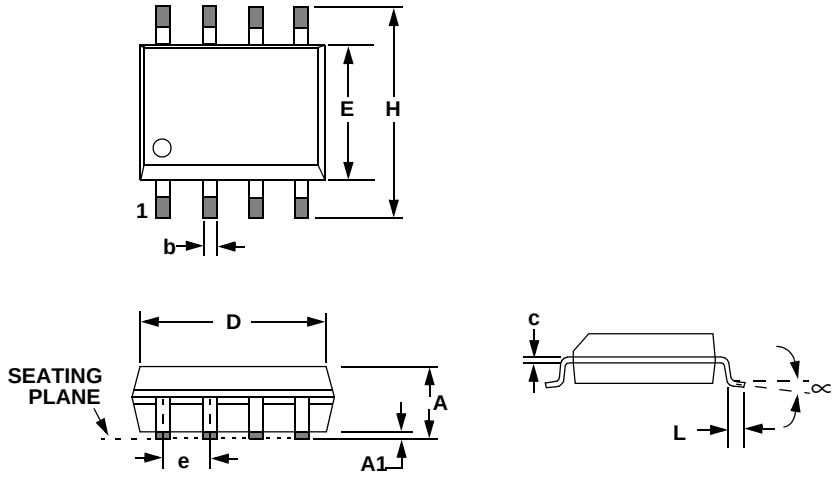
6. ENVIRONMENTAL, MANUFACTURING, & HANDLING INFORMATION

Model Number	Peak Reflow Temp	MSL Rating*	Max Floor Life
CS5510-ASZ	260 °C	3	7 Days
CS5511-ASZ			
CS5512-BSZ			
CS5513-BSZ			

* MSL (Moisture Sensitivity Level) as specified by IPC/JEDEC J-STD-020.

7. PACKAGE DIMENSIONS

8L SOIC (208 MIL BODY) PACKAGE DRAWING



	INCHES			MILLIMETERS		
DIM	**MIN**	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**
A	0.076	0.080	0.084	1.93	2.03	2.13
A1	0.004	0.007	0.010	0.10	0.175	0.25
b	0.013	0.016	0.020	0.33	0.406	0.51
C	0.006	0.008	0.010	0.15	0.20	0.25
D	0.206	0.208	0.210	5.23	5.28	5.33
E	0.204	0.208	0.212	5.18	5.28	5.38
e	0.040	0.050	0.060	1.02	1.27	1.52
H	0.302	0.310	0.318	7.67	7.88	8.08
L	0.019	0.025	0.030	0.48	0.64	0.76
∝	0°	4°	8°	0°	4°	8°

EIAJ PACKAGE

Controlling Dimension is Inches

8. REVISION HISTORY

Revision	Date	Changes
F2	MAR 2005	Added lead-free (Pb) device ordering information.
F3	AUG 2005	Updated lead-free (Pb) device ordering information. Added MSL data.
F4	JUL 2009	Removed devices containing lead (Pb) from ordering information.

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