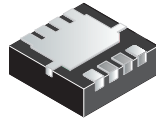




**THE DATASHEET OF  
CSD16323Q3C**





## N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD16323Q3C](#)

### FEATURES

- DualCool™ Package
- Optimized for 5V Gate Drive
- Ultra Low  $Q_g$  and  $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm × 3.3-mm Plastic Package

### APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control or Synchronous FET Applications

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and optimized for 5V gate drive applications.

### PRODUCT SUMMARY

$V_{DS}$	Drain to Source Voltage	25	V
$Q_g$	Gate Charge Total (4.5V)	6.2	nC
$Q_{gd}$	Gate Charge Gate to Drain	1.1	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	5.4 mΩ
		$V_{GS} = 4.5V$	4.4 mΩ
		$V_{GS} = 8V$	3.8 mΩ
$V_{th}$	Threshold Voltage	1.1	V

### ORDERING INFORMATION

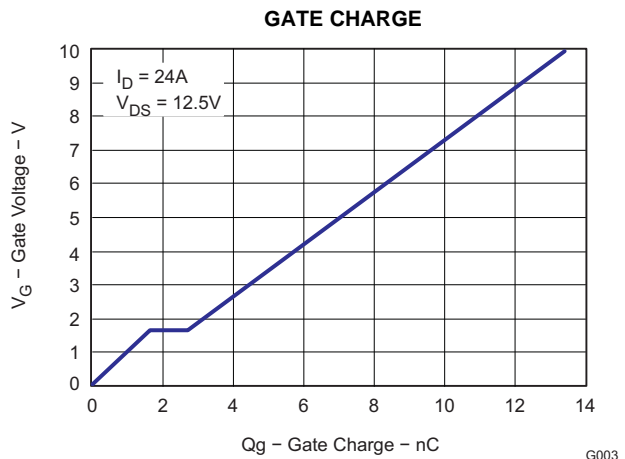
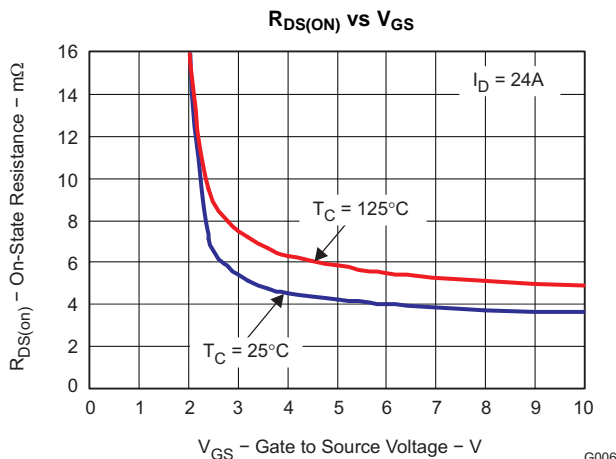
Device	Package	Media	Qty	Ship
CSD16323Q3C	SON 3.3-mm × 3.3-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

### ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
$V_{GS}$	Gate to Source Voltage	+10 / -8	V
$I_D$	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current <sup>(1)</sup>	21	A
$I_{DM}$	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ <sup>(2)</sup>	112	A
$P_D$	Power Dissipation <sup>(1)</sup>	3	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	°C
$E_{AS}$	Avalanche Energy, single pulse $I_D = 50A$ , $L = 0.1mH$ , $R_G = 25\Omega$	125	mJ

(1) Typical  $R_{\theta JA} = 43^\circ\text{C/W}$  when mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration  $\leq 300\mu\text{s}$ , duty cycle  $\leq 2\%$



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## ELECTRICAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

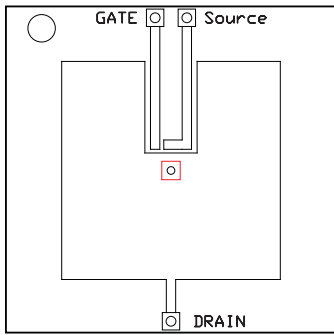
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>Static Characteristics</b>						
B <sub>V</sub> DSS	Drain to Source Voltage	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA	25			V
I <sub>DSS</sub>	Drain to Source Leakage Current	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 20V			1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>DS</sub> = 0V, V <sub>GS</sub> = +10/-8V			100	nA
V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	0.9	1.1	1.4	V
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 3V, I <sub>D</sub> = 24A		5.4	7.2	mΩ
		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 24A		4.4	5.5	mΩ
		V <sub>GS</sub> = 8V, I <sub>D</sub> = 24A		3.8	4.5	mΩ
g <sub>fs</sub>	Transconductance	V <sub>DS</sub> = 12.5V, I <sub>D</sub> = 24A		108		S
<b>Dynamic Characteristics</b>						
C <sub>ISS</sub>	Input Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 12.5V, f = 1MHz		1020	1300	pF
C <sub>OSS</sub>	Output Capacitance			740	960	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			50	65	pF
R <sub>g</sub>	Series Gate Resistance			1.4	2.8	Ω
Q <sub>g</sub>	Gate Charge Total (4.5V)	V <sub>DS</sub> = 12.5V, I <sub>D</sub> = 24A		6.2	8.4	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain			1.1		nC
Q <sub>gs</sub>	Gate Charge Gate to Source			1.8		nC
Q <sub>g(th)</sub>	Gate Charge at V <sub>th</sub>			1		nC
Q <sub>OSS</sub>	Output Charge	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 0V		14		nC
t <sub>d(on)</sub>	Turn On Delay Time	V <sub>DS</sub> = 12.5V, V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 24A R <sub>G</sub> = 2Ω		5.3		ns
t <sub>r</sub>	Rise Time			15		ns
t <sub>d(off)</sub>	Turn Off Delay Time			13		ns
t <sub>f</sub>	Fall Time			6.3		ns
<b>Diode Characteristics</b>						
V <sub>SD</sub>	Diode Forward Voltage	I <sub>S</sub> = 24A, V <sub>GS</sub> = 0V		0.85	1	V
Q <sub>rr</sub>	Reverse Recovery Charge	V <sub>DD</sub> = 12.5V, I <sub>F</sub> = 24A, di/dt = 300A/μs		21		nC
t <sub>rr</sub>	Reverse Recovery Time	V <sub>DD</sub> = 12.5V, I <sub>F</sub> = 24A, di/dt = 300A/μs		16		ns

## THERMAL CHARACTERISTICS

(T<sub>A</sub> = 25°C unless otherwise stated)

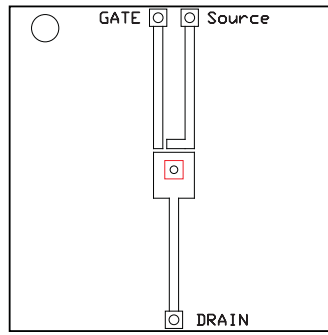
PARAMETER		MIN	TYP	MAX	UNIT
θ <sub>JC(top)</sub>	Junction-to-case (top) thermal resistance			3.5	°C/W
θ <sub>JC(bot)</sub>	Junction-to-case (bottom) thermal resistance <sup>(1)</sup>			2.7	°C/W
θ <sub>JA</sub>	Junction to Ambient thermal resistance <sup>(1) (2)</sup>			58	°C/W

- (1) R<sub>θJC</sub> is determined with the device mounted on a 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. R<sub>θJC</sub> is specified by design, whereas R<sub>θJA</sub> is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm thick) Cu.



Max  $R_{\theta JA} = 58^{\circ}\text{C/W}$   
when mounted on 1  
inch<sup>2</sup> (6.45 cm<sup>2</sup>) of  
2-oz. (0.071-mm thick)  
Cu.

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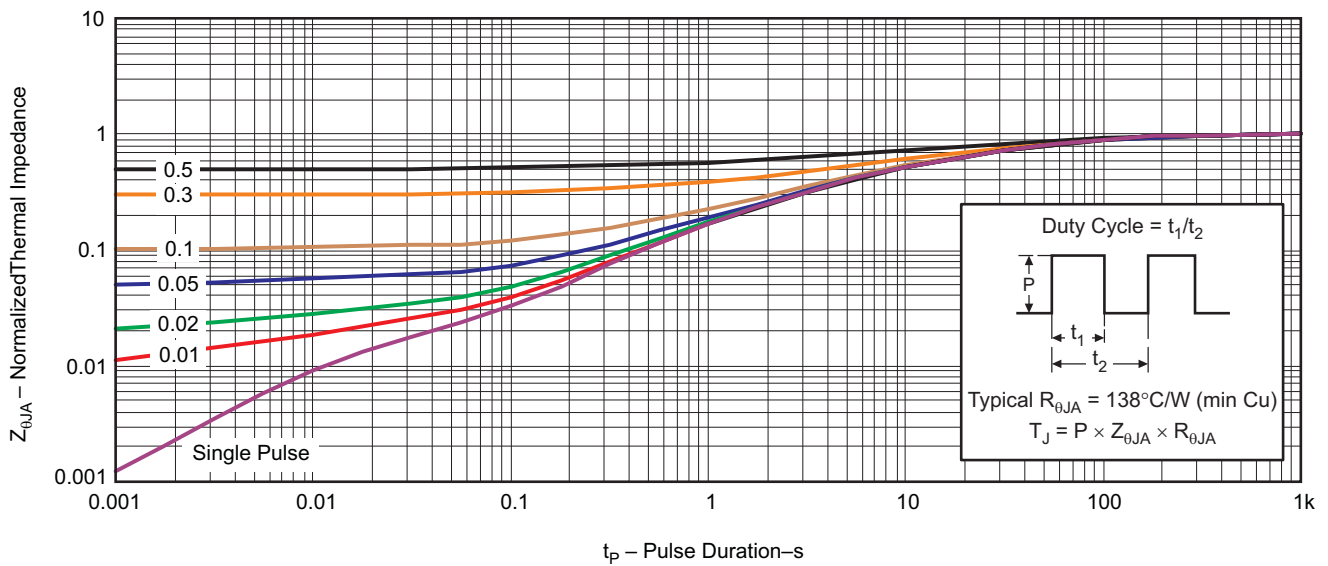


Max  $R_{\theta JA} = 162^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz. (0.071-mm thick)  
Cu.

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### TYPICAL MOSFET CHARACTERISTICS

( $T_A = 25^{\circ}\text{C}$  unless otherwise stated)

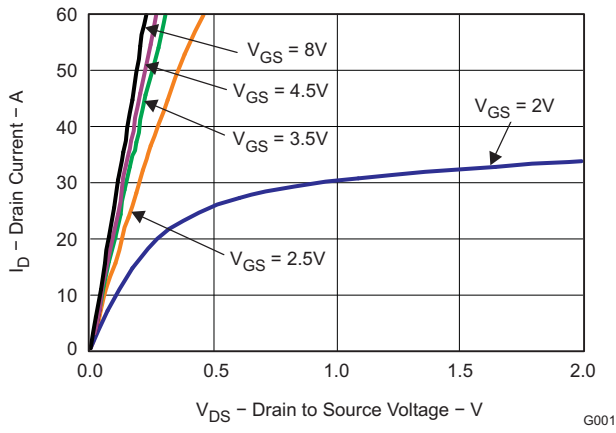


G012

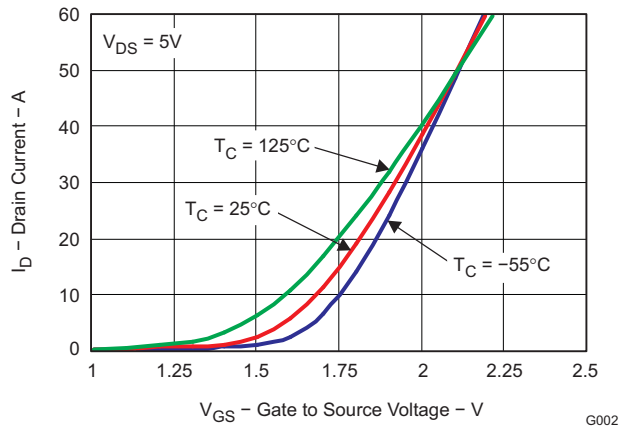
Figure 1. Transient Thermal Impedance

**TYPICAL MOSFET CHARACTERISTICS (continued)**

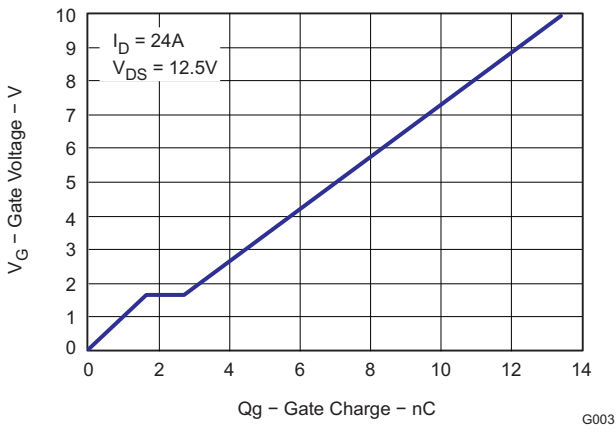
( $T_A = 25^\circ\text{C}$  unless otherwise stated)



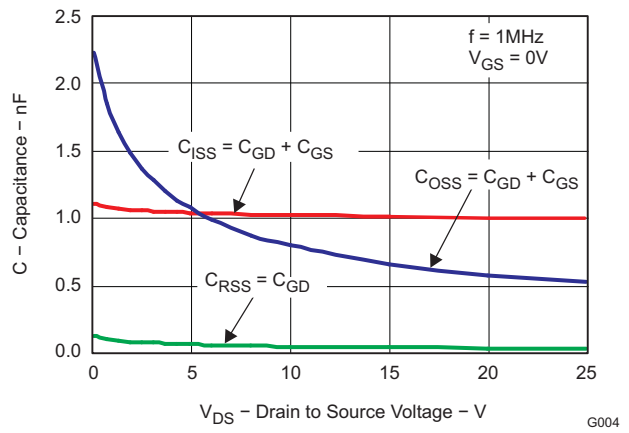
**Figure 2. Saturation Characteristics**



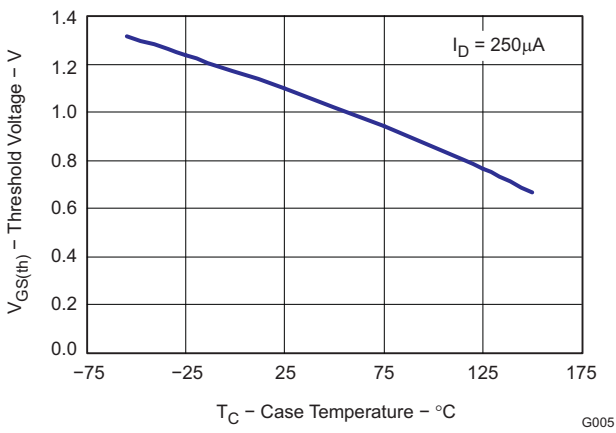
**Figure 3. Transfer Characteristics**



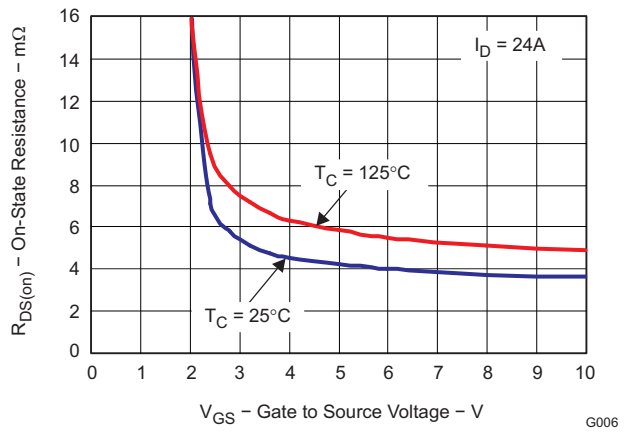
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Threshold Voltage vs. Temperature**



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

TYPICAL MOSFET CHARACTERISTICS (continued)

( $T_A = 25^\circ\text{C}$  unless otherwise stated)

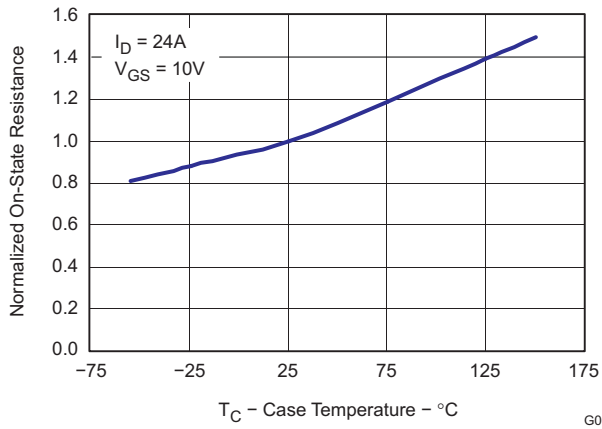


Figure 8. Normalized On-State Resistance vs. Temperature

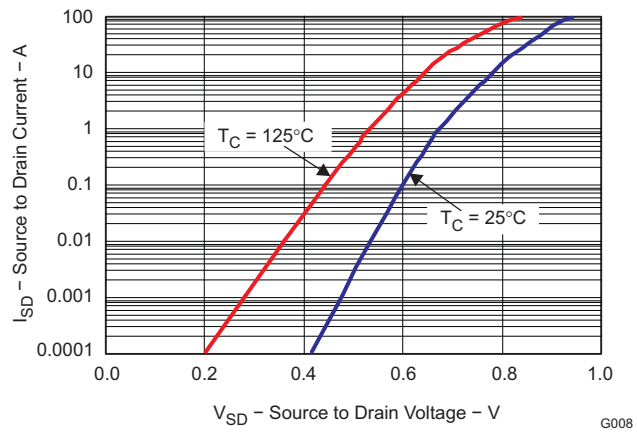


Figure 9. Typical Diode Forward Voltage

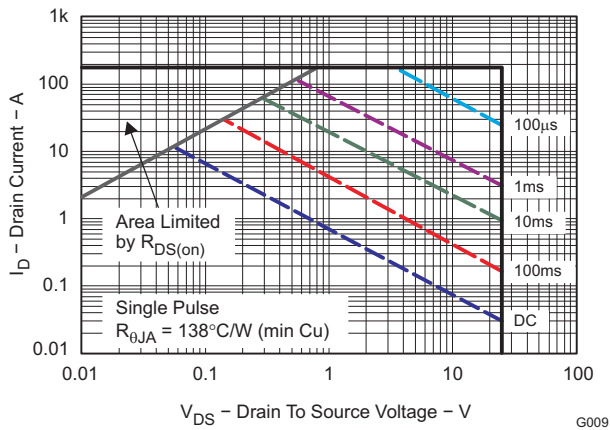


Figure 10. Maximum Safe Operating Area

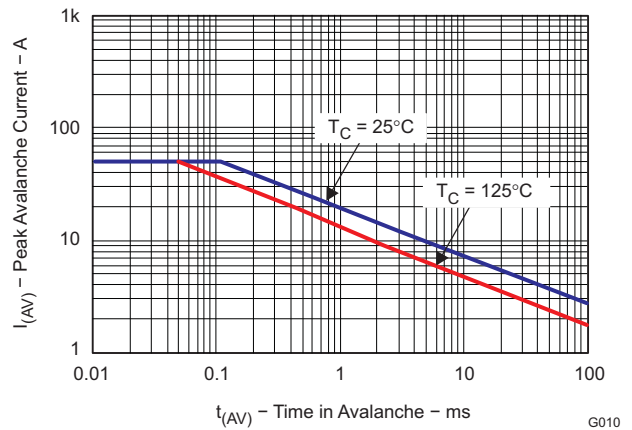


Figure 11. Single Pulse Unclamped Inductive Switching

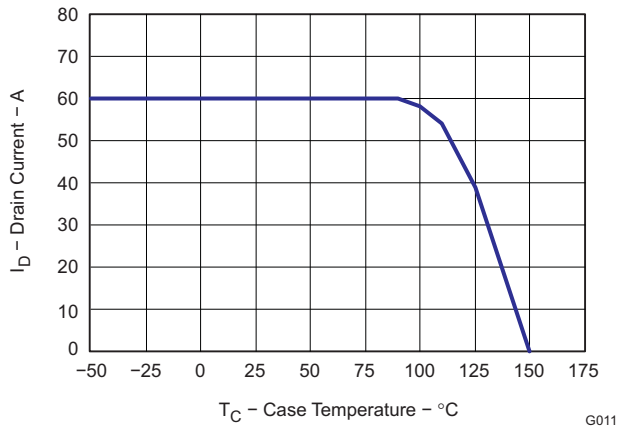
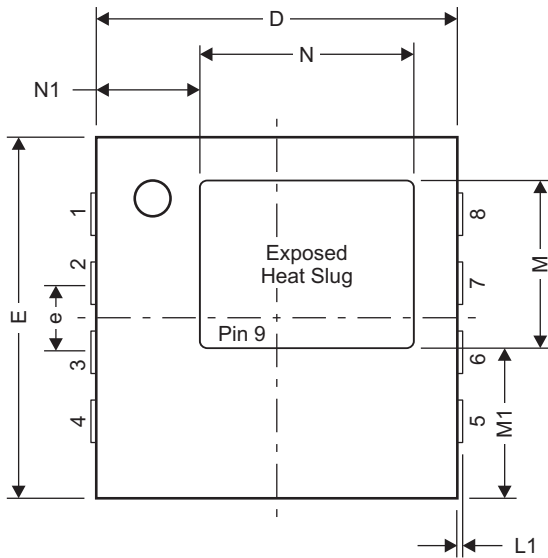


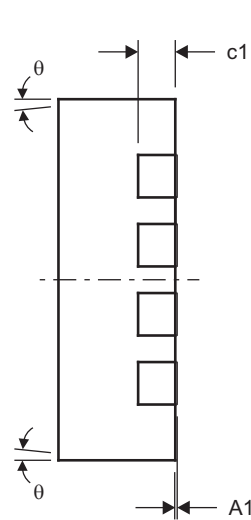
Figure 12. Maximum Drain Current vs. Temperature

**MECHANICAL DATA**

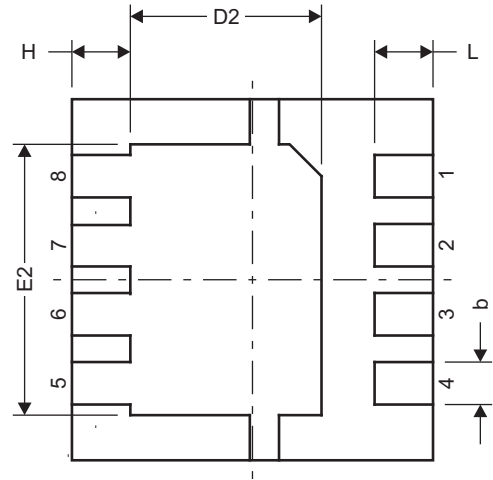
**Q3C Package Dimensions**



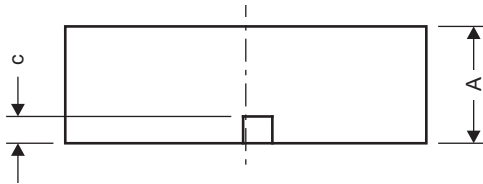
Top View



Side View



Bottom View



Front View

Pinout	
Pin #	Label
1, 2, 3, 9	Source
4	Gate
5, 6, 7, 8	Drain

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DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
c1	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	-
M	1.561	1.661	1.761	0.061	0.065	0.069
M1	1.130	1.230	1.330	0.044	0.048	0.052
N	1.854	1.954	2.054	0.073	0.077	0.081
N1	0.846	0.946	1.046	0.033	0.037	0.041
θ	-	-	-	-	-	-



**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD16323Q3C	NRND	VSON-CLIP	DQV	8		TBD	Call TI	Call TI	0 to 0		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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