



**THE DATASHEET OF
CSD17575Q3T**



CSD17575Q3 30-V N-Channel NexFET™ Power MOSFET

1 Features

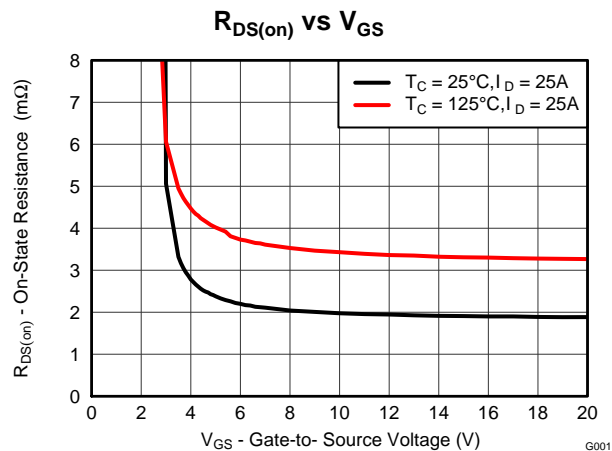
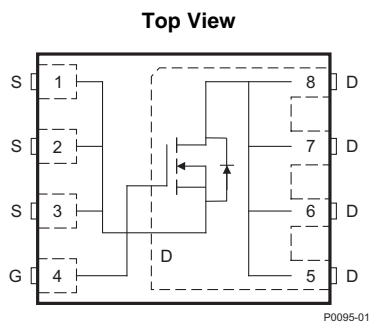
- Low Q_g and Q_{gd}
- Low $R_{DS(on)}$
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3 mm × 3.3 mm Plastic Package

2 Applications

- Point of Load Synchronous Buck Converter for Applications in Networking, Telecom, and Computing Systems
- Optimized for Synchronous FET Applications

3 Description

This 1.9 m Ω , 30 V, SON 3×3 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.



Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain-to-Source Voltage	30		V
Q_g	Gate Charge Total (4.5V)	23		nC
Q_{gd}	Gate Charge Gate-to-Drain	5.4		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	2.6	m Ω
		$V_{GS} = 10\text{ V}$	1.9	
V_{th}	Threshold Voltage	1.4		V

Ordering Information⁽¹⁾

Device	Media	Qty	Package	Ship
CSD17575Q3	13-Inch Reel	2500	SON 3.3 × 3.3 mm Plastic Package	Tape and Reel
CSD17575Q3T	13-Inch Reel	250		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage	30	V
V_{GS}	Gate-to-Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limit)	60	A
	Continuous Drain Current (Silicon Limit), $T_C = 25^\circ\text{C}$	182	
	Continuous Drain Current ⁽¹⁾	27	
I_{DM}	Pulsed Drain Current ⁽²⁾	240	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	108	
T_J , T_{stg}	Operating Junction and Storage Temperature Range	-55 to 150	°C
E_{AS}	Avalanche Energy, single pulse $I_D = 48$, $L = 0.1\text{ mH}$, $R_G = 25\ \Omega$	115	mJ

(1) Typical $R_{\theta JA} = 45^\circ\text{C}/\text{W}$ on 1-inch² Cu (2 oz.) on 0.060-inch thick FR4 PCB.

(2) Max $R_{\theta JC} = 1.5^\circ\text{C}/\text{W}$, pulse duration $\leq 100\ \mu\text{s}$, duty cycle $\leq 1\%$

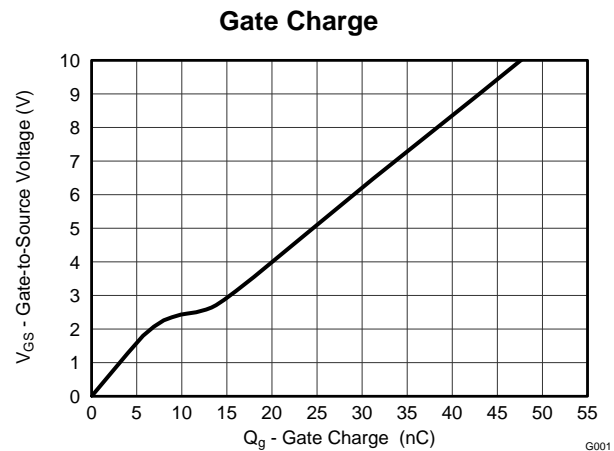


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4 Revision History

Changes from Original (June 2014) to Revision A	Page
<ul style="list-style-type: none"> • Added b1, d, d1, and K dimensions to the mechanical information table 8 	8

5 Specifications

5.1 Electrical Characteristics

(T_A = 25°C unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
B _V DSS	Drain-to-Source Voltage	V _{GS} = 0 V, I _D = 250 μA	30			V
I _{DSS}	Drain-to-Source Leakage Current	V _{GS} = 0 V, V _{DS} = 24 V			1	μA
I _{GSS}	Gate-to-Source Leakage Current	V _{DS} = 0 V, V _{GS} = ±20 V			100	nA
V _{GS(th)}	Gate-to-Source Threshold Voltage	V _{DS} = V _{GS} , I _D = 250 μA	1.1	1.4	1.8	V
R _{DS(on)}	Drain-to-Source On-Resistance	V _{GS} = 4.5 V, I _D = 25 A		2.6	3.2	mΩ
		V _{GS} = 10 V, I _D = 25 A		1.9	2.3	
g _{fs}	Transconductance	V _{DS} = 3 V, I _D = 25 A		118		S
DYNAMIC CHARACTERISTICS						
C _{ISS}	Input Capacitance	V _{GS} = 0 V, V _{DS} = 15 V, f = 1 MHz		3400	4420	pF
C _{OSS}	Output Capacitance			393	511	pF
C _{RSS}	Reverse Transfer Capacitance			157	204	pF
R _g	Series Gate Resistance	V _{DS} = 15 V, I _D = 25 A		0.9	1.8	Ω
Q _g	Gate Charge Total (4.5 V)			23	30	nC
Q _{gd}	Gate Charge Gate-to-Drain			5.4		nC
Q _{gs}	Gate Charge Gate-to-Source			8.5		nC
Q _{g(th)}	Gate Charge at V _{th}			4.6		nC
Q _{OSS}	Output Charge	V _{DS} = 15 V, V _{GS} = 0 V		11.6		nC
t _{d(on)}	Turn On Delay Time	V _{DS} = 15 V, V _{GS} = 4.5 V I _D = 25 A R _G = 2 Ω		4		ns
t _r	Rise Time			10		ns
t _{d(off)}	Turn Off Delay Time			20		ns
t _f	Fall Time			3		ns
DIODE CHARACTERISTICS						
V _{SD}	Diode Forward Voltage	I _S = 25 A, V _{GS} = 0 V		0.8	1	V
Q _{rr}	Reverse Recovery Charge	V _{DD} = 15 V, I _F = 25 A, di/dt = 300 A/μs		15		nC
t _{rr}	Reverse Recovery Time			13		ns

5.2 Thermal Information

(T_A = 25°C unless otherwise stated)

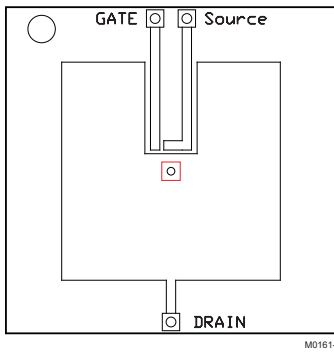
THERMAL METRIC		MIN	TYP	MAX	UNIT
R _{θJC}	Junction-to-Case Thermal Resistance ⁽¹⁾			1.5	°C/W
R _{θJA}	Junction-to-Ambient Thermal Resistance ⁽¹⁾⁽²⁾			55	

- (1) R_{θJC} is determined with the device mounted on a 1-inch² (6.45-cm²), Cu pad on a 1.5-inches × 1.5-inches thick FR4 PCB. R_{θJC} is specified by design, whereas R_{θJA} is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² 2-oz.Cu.

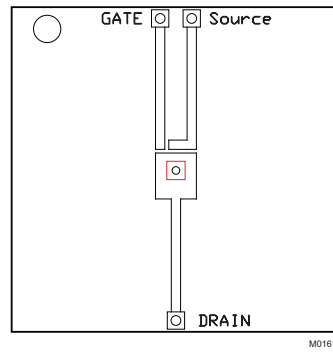
CSD17575Q3

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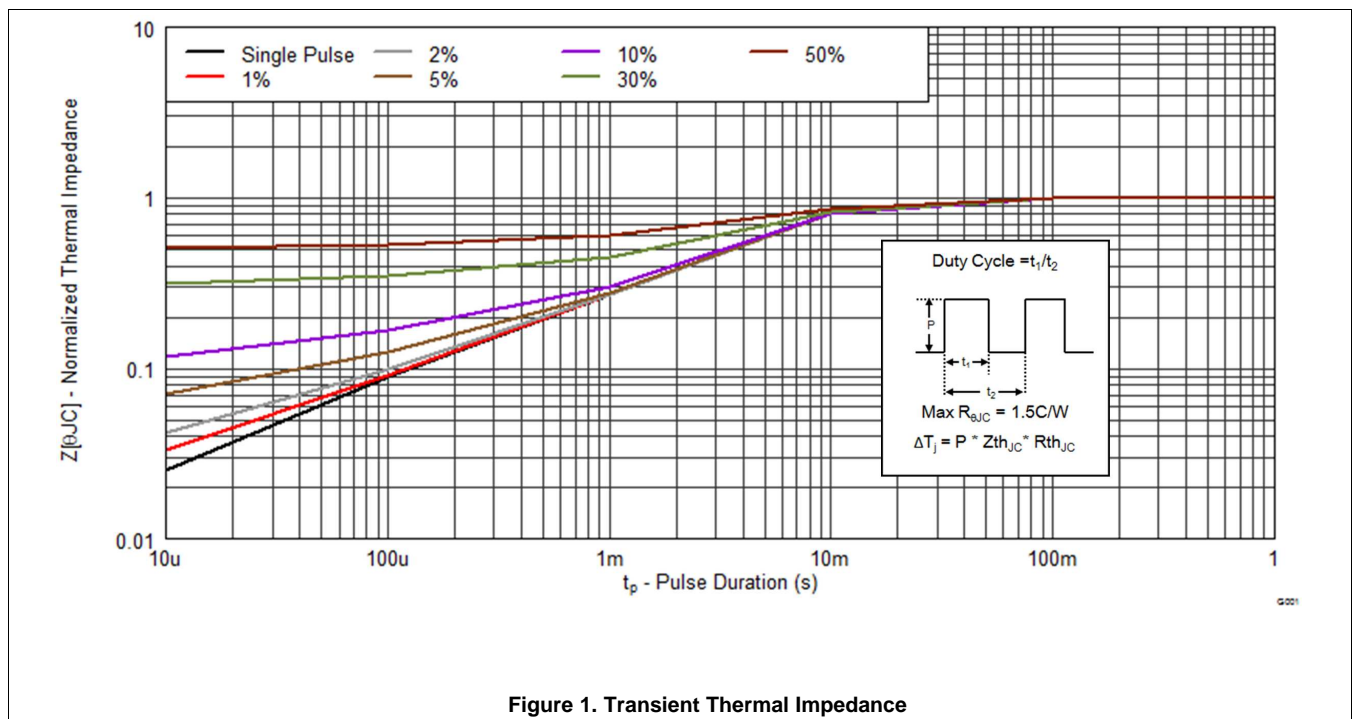
Max $R_{\theta JA} = 55^{\circ}\text{C/W}$
when mounted on
1 inch² of 2 oz. Cu.



Max $R_{\theta JA} = 160^{\circ}\text{C/W}$
when mounted on
minimum pad area of
2 oz. Cu.

5.3 Typical MOSFET Characteristics

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

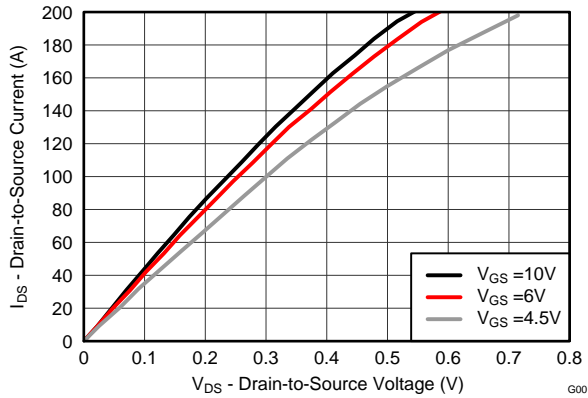


Figure 2. Saturation Characteristics

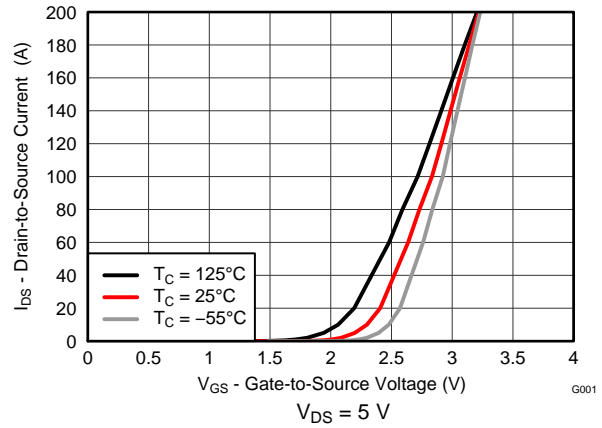


Figure 3. Transfer Characteristics

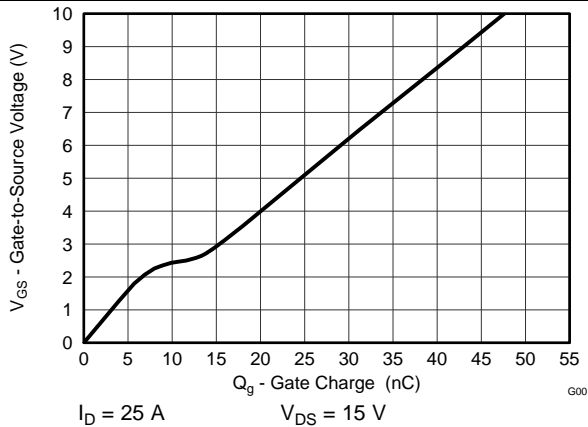


Figure 4. Gate Charge

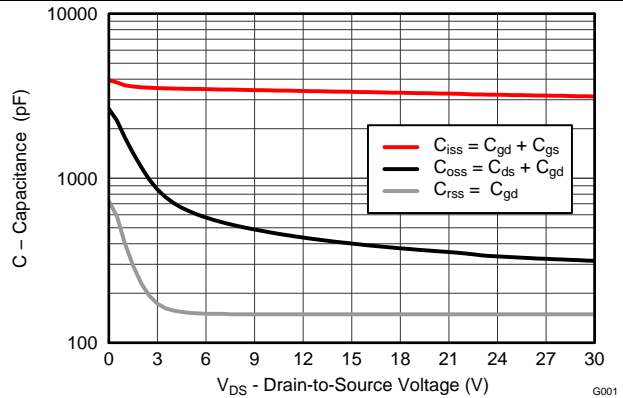


Figure 5. Capacitance

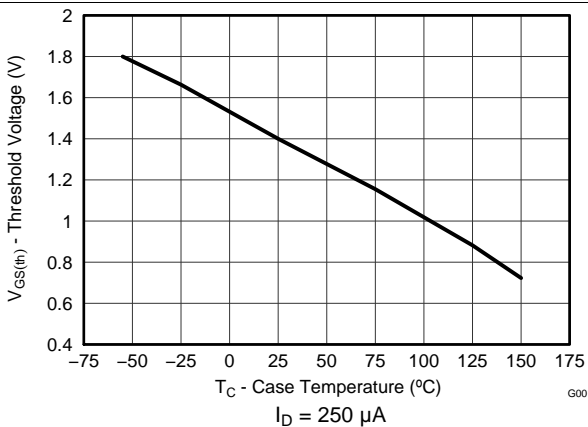


Figure 6. Threshold Voltage vs Temperature

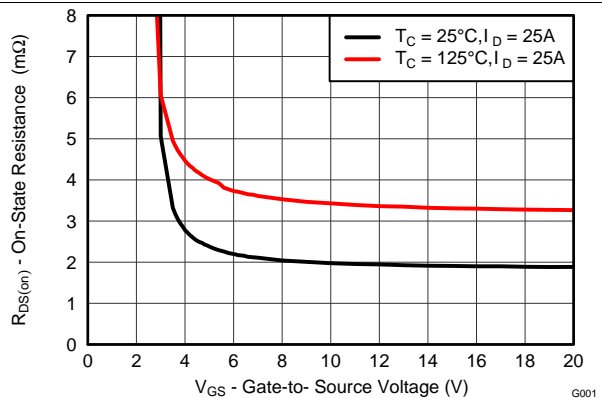


Figure 7. On-State Resistance vs Gate-to-Source Voltage

Typical MOSFET Characteristics (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

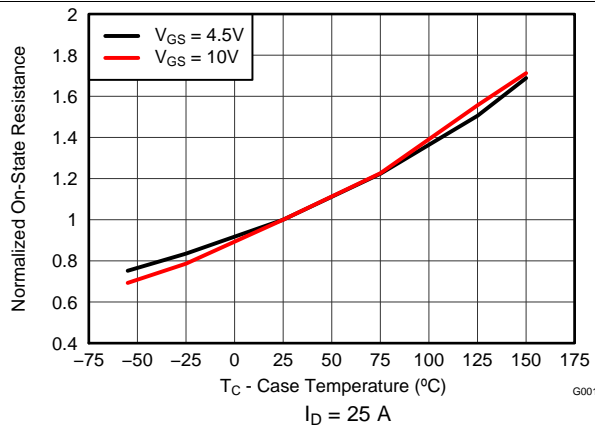


Figure 8. Normalized On-State Resistance vs Temperature

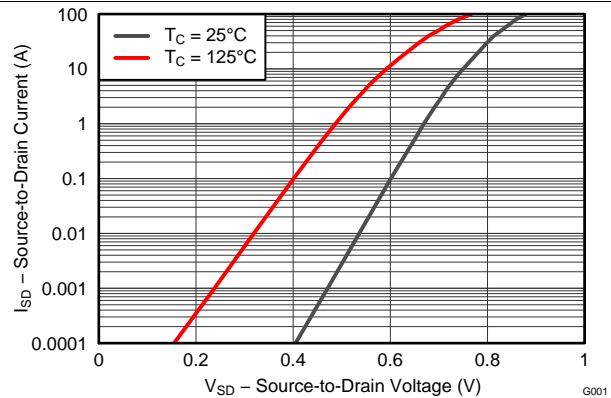


Figure 9. Typical Diode Forward Voltage

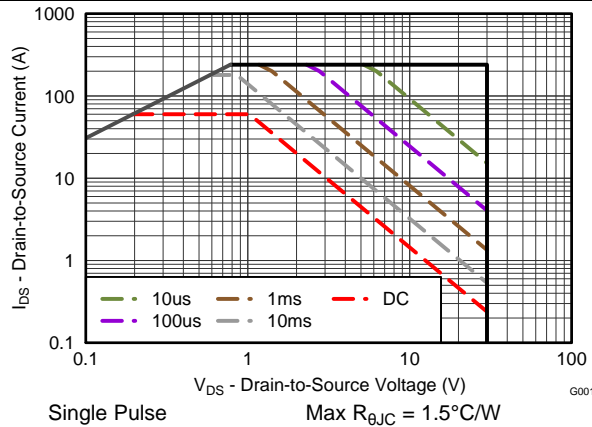


Figure 10. Maximum Safe Operating Area

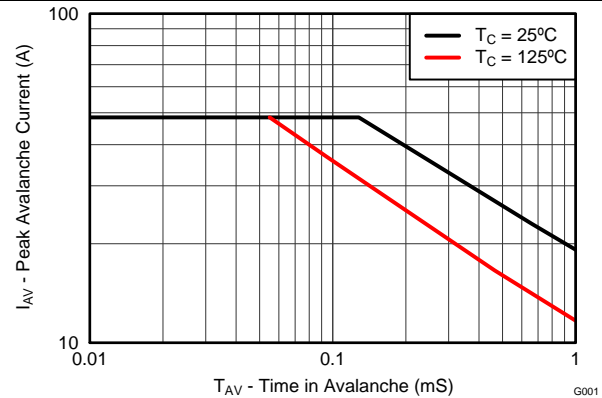


Figure 11. Single Pulse Unclamped Inductive Switching

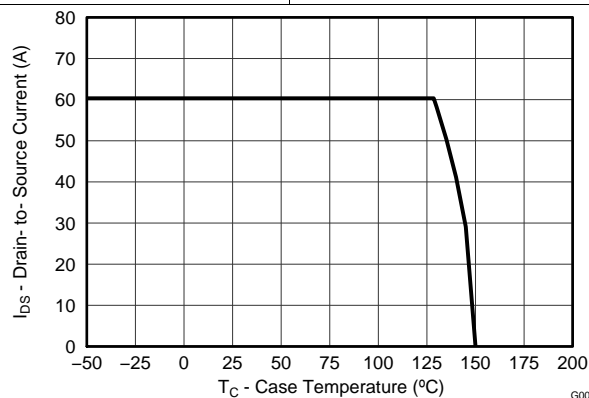


Figure 12. Maximum Drain Current vs Temperature

6 Device and Documentation Support

6.1 Trademarks

NexFET is a trademark of Texas Instruments.

6.2 Electrostatic Discharge Caution



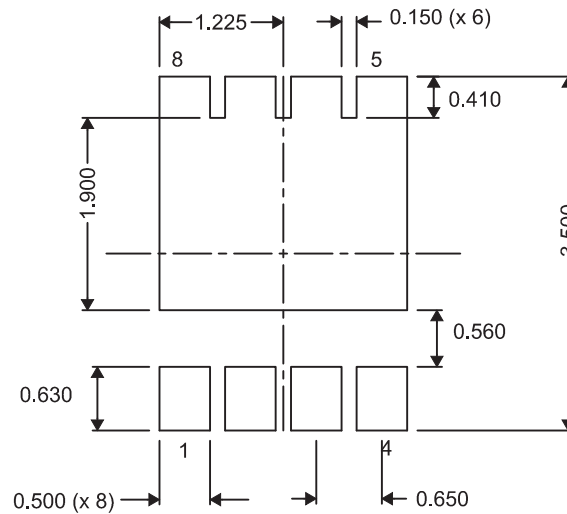
These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

6.3 Glossary

[SLYZ022](#) — *TI Glossary*.

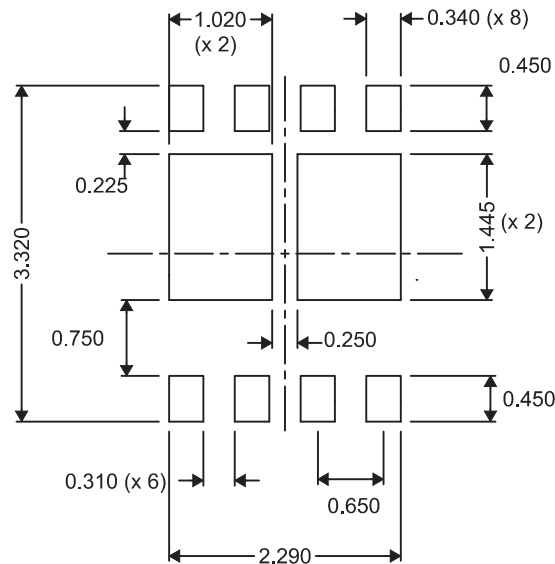
This glossary lists and explains terms, acronyms, and definitions.

7.2 Recommended PCB Pattern



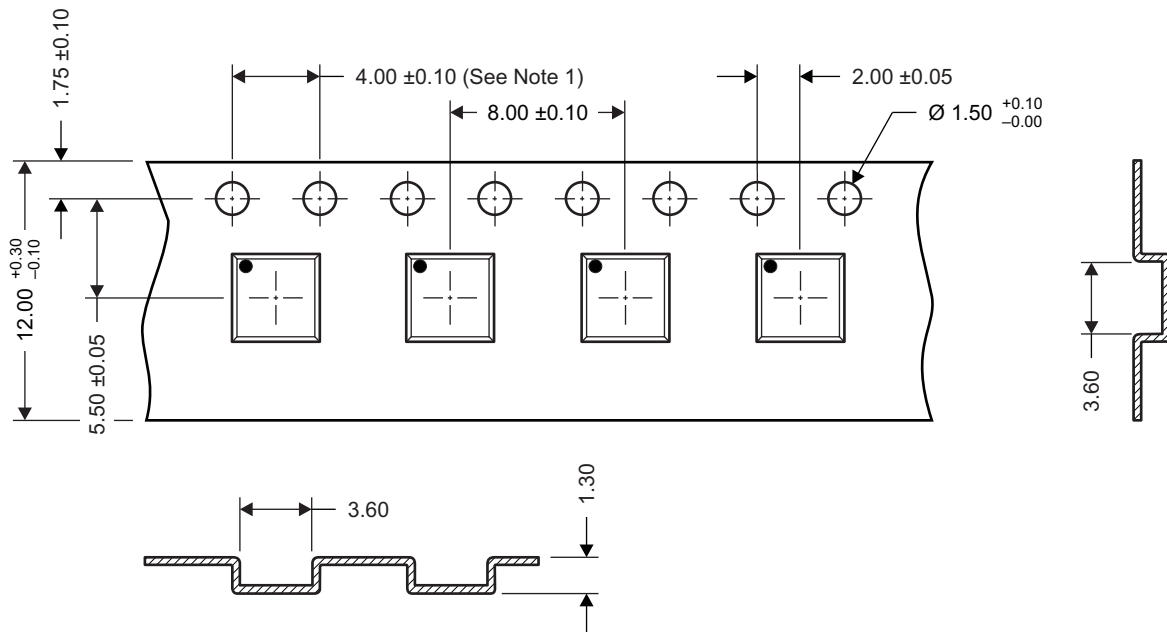
For recommended circuit layout for PCB designs, see application note [SLPA005](#) – *Reducing Ringing Through PCB Layout Techniques*.

7.3 Recommended Stencil Opening



All dimensions are in mm, unless otherwise specified.

7.4 Q3 Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD17575Q3	ACTIVE	VSON-CLIP	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM		CSD17575	Samples
CSD17575Q3T	ACTIVE	VSON-CLIP	DQG	8	250	Pb-Free (RoHS Exempt)	CU SN	Level-1-260C-UNLIM	-55 to 150	CSD17575	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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