



**THE DATASHEET OF  
CSD18532Q5BT**



# CSD18532Q5B 60-V N-Channel NexFET™ Power MOSFETs

## 1 Features

- Ultra-Low  $Q_g$  and  $Q_{gd}$
- Low-Thermal Resistance
- Avalanche Rated
- Logic Level
- Lead-Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 5-mm × 6-mm Plastic Package

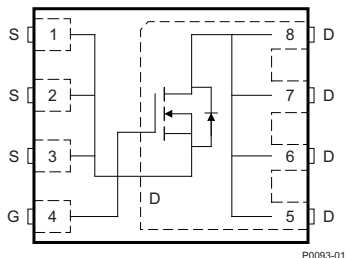
## 2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Isolated Converter Primary Side Switch
- Motor Control

## 3 Description

This 2.5-m $\Omega$ , 60-V SON 5-mm × 6-mm NexFET™ power MOSFET is designed to minimize losses in power conversion applications.

Top View



## Product Summary

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
$V_{DS}$	Drain-to-Source Voltage	60		V
$Q_g$	Gate Charge Total (10 V)	44		nC
$Q_{gd}$	Gate Charge Gate-to-Drain	6.9		nC
$R_{DS(on)}$	Drain-to-Source On-Resistance	$V_{GS} = 4.5\text{ V}$	3.3	m $\Omega$
		$V_{GS} = 10\text{ V}$	2.5	
$V_{GS(th)}$	Threshold Voltage	1.8		V

## Device Information<sup>(1)</sup>

DEVICE	QTY	MEDIA	PACKAGE	SHIP
CSD18532Q5B	2500	13-Inch Reel	SON 5.00-mm × 6.00-mm Plastic Package	Tape and Reel
CSD18532Q5BT	250	13-Inch Reel		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

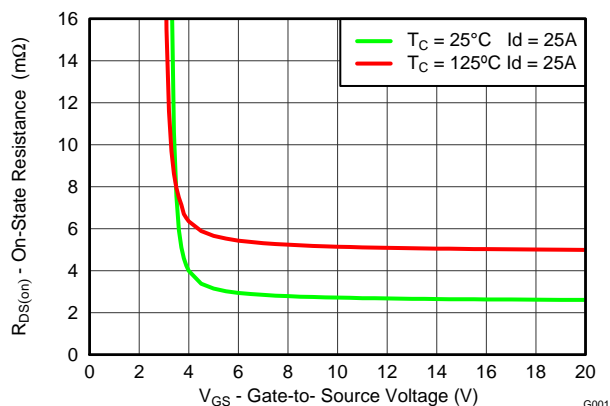
## Absolute Maximum Ratings

$T_A = 25^\circ\text{C}$		VALUE	UNIT
$V_{DS}$	Drain-to-Source Voltage	60	V
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$I_D$	Continuous Drain Current (Package Limited)	100	A
	Continuous Drain Current (Silicon Limited), $T_C = 25^\circ\text{C}$	172	
	Continuous Drain Current <sup>(1)</sup>	23	
$I_{DM}$	Pulsed Drain Current <sup>(2)</sup>	400	A
$P_D$	Power Dissipation <sup>(1)</sup>	3.2	W
	Power Dissipation, $T_C = 25^\circ\text{C}$	156	
$T_J$ , $T_{stg}$	Operating Junction Temperature, Storage Temperature	-55 to 150	$^\circ\text{C}$
$E_{AS}$	Avalanche Energy, Single Pulse $I_D = 80\text{ A}$ , $L = 0.1\text{ mH}$ , $R_G = 25\ \Omega$	320	mJ

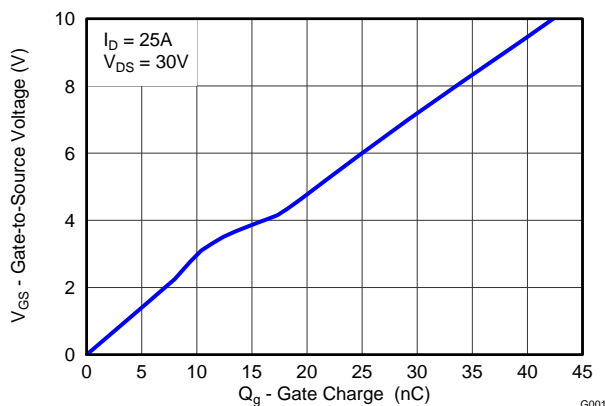
(1) Typical  $R_{\theta JA} = 40^\circ\text{C/W}$  on a 1-in<sup>2</sup>, 2-oz Cu pad on a 0.06-in thick FR4 PCB.

(2) Max  $R_{\theta JC} = 0.8^\circ\text{C/W}$ , pulse duration  $\leq 100\ \mu\text{s}$ , duty cycle  $\leq 1\%$ .

$R_{DS(on)}$  vs  $V_{GS}$



Gate Charge



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## 4 Revision History

Changes from Revision C (May 2017) to Revision D	Page
<ul style="list-style-type: none"> <li>• Extended the <math>V_{DS}</math> on <a href="#">Figure 5</a> to 60 V..... 4</li> </ul>	4
Changes from Revision B (July 2014) to Revision C	Page
<ul style="list-style-type: none"> <li>• Added the <i>Receiving Notification of Documentation Updates</i> and <i>Community Resources</i> sections to <i>Device and Documentation Support</i>. ..... 7</li> <li>• Changed the dimension between pads 3 and 4 from 0.028 inches: to 0.050 inches in the <i>Recommended PCB Pattern</i> section diagram ..... 9</li> </ul>	9
Changes from Revision A (May 2014) to Revision B	Page
<ul style="list-style-type: none"> <li>• Changed "7-Inch Reel" to state "13-Inch Reel". ..... 1</li> </ul>	1
Changes from Original (Nov 2012) to Revision A	Page
<ul style="list-style-type: none"> <li>• Updated the device description. .... 1</li> <li>• Specified <math>Q_g</math> at 10 V. .... 1</li> <li>• Added small reel option. .... 1</li> <li>• Increased pulsed drain current to 400 A. .... 1</li> <li>• Added line for max power dissipation with case temperature held to 25°C. .... 1</li> <li>• Updated the pulsed drain current conditions. .... 1</li> <li>• Eliminated <math>Q_g</math> at 4.5 V. .... 3</li> <li>• Changed <a href="#">Figure 1</a> from a normalized <math>R_{\theta JA}</math> curve to a <math>R_{\theta JC}</math> curve..... 4</li> <li>• Updated the safe operating area in <a href="#">Figure 10</a>. .... 6</li> <li>• Updated the mechanical drawing. .... 8</li> </ul>	8

## 5 Specifications

### 5.1 Electrical Characteristics

 $T_A = 25^\circ\text{C}$  unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>STATIC CHARACTERISTICS</b>						
$V_{DSS}$	Drain-to-source voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
$I_{DSS}$	Drain-to-source leakage current	$V_{GS} = 0\text{ V}, V_{DS} = 48\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate-to-source leakage current	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.5	1.8	2.2	V
$R_{DS(on)}$	Drain-to-source on-resistance	$V_{GS} = 4.5\text{ V}, I_D = 25\text{ A}$		3.3	4.3	m $\Omega$
		$V_{GS} = 10\text{ V}, I_D = 25\text{ A}$		2.5	3.2	
$g_{fs}$	Transconductance	$V_{DS} = 30\text{ V}, I_D = 25\text{ A}$		143		S
<b>DYNAMIC CHARACTERISTICS</b>						
$C_{iss}$	Input capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 30\text{ V}, f = 1\text{ MHz}$		3900	5070	pF
$C_{oss}$	Output capacitance			470	611	pF
$C_{rss}$	Reverse transfer capacitance			13	17	pF
$R_G$	Series gate resistance			1.2	2.4	$\Omega$
$Q_g$	Gate charge total (10 V)	$V_{DS} = 30\text{ V}, I_D = 25\text{ A}$		44	58	nC
$Q_{gd}$	Gate charge gate-to-drain			6.9		nC
$Q_{gs}$	Gate charge gate-to-source			10		nC
$Q_{g(th)}$	Gate charge at $V_{th}$			6.3		nC
$Q_{oss}$	Output charge	$V_{DS} = 30\text{ V}, V_{GS} = 0\text{ V}$		52		nC
$t_{d(on)}$	Turnon delay time	$V_{DS} = 30\text{ V}, V_{GS} = 10\text{ V}, I_{DS} = 25\text{ A}, R_G = 0\ \Omega$		5.8		ns
$t_r$	Rise time			7.2		ns
$t_{d(off)}$	Turnoff delay time			22		ns
$t_f$	Fall time			3.1		ns
<b>DIODE CHARACTERISTICS</b>						
$V_{SD}$	Diode forward voltage	$I_{SD} = 25\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
$Q_{rr}$	Reverse recovery charge	$V_{DS} = 30\text{ V}, I_F = 25\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		111		nC
$t_{rr}$	Reverse recovery time			49		ns

### 5.2 Thermal Information

 $T_A = 25^\circ\text{C}$  unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance <sup>(1)</sup>			0.8	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-ambient thermal resistance <sup>(1)(2)</sup>			50	$^\circ\text{C}/\text{W}$

- $R_{\theta JC}$  is determined with the device mounted on a 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz. (0.071-mm) thick Cu pad on a 1.5-in x 1.5-in (3.81-cm x 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB.  $R_{\theta JC}$  is specified by design, whereas  $R_{\theta JA}$  is determined by the user's board design.
- Device mounted on FR4 material with 1-in<sup>2</sup> (6.45-cm<sup>2</sup>), 2-oz (0.071-mm) thick Cu.

CSD18532Q5B

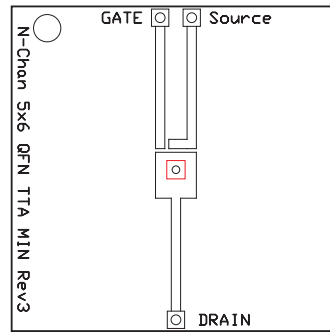
SLPS322D –NOVEMBER 2012–REVISED FEBRUARY 2018

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M0137-01

Max  $R_{\theta JA} = 50^{\circ}\text{C/W}$   
when mounted on 1 in<sup>2</sup>  
(6.45 cm<sup>2</sup>) of  
2-oz (0.071-mm) thick  
Cu.

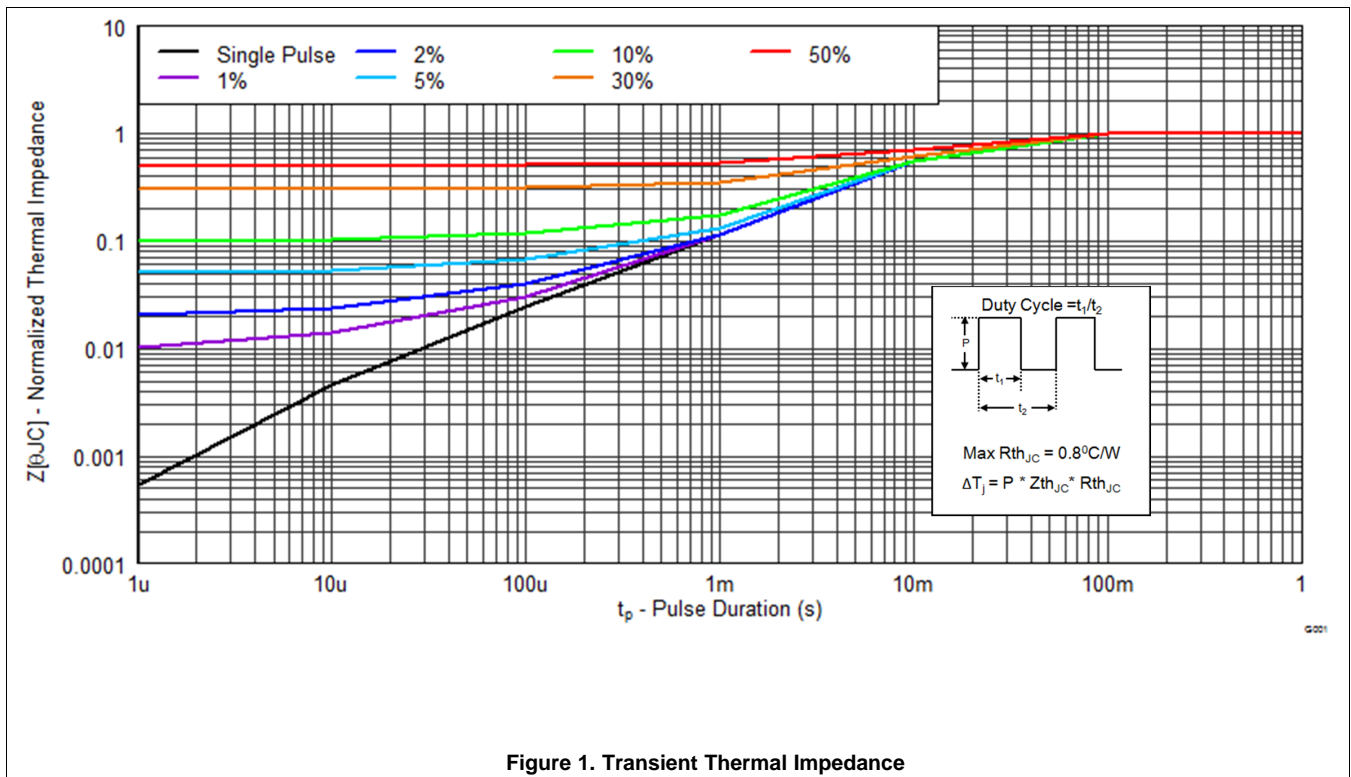


M0137-02

Max  $R_{\theta JA} = 125^{\circ}\text{C/W}$   
when mounted on a  
minimum pad area of  
2-oz (0.071-mm) thick  
Cu.

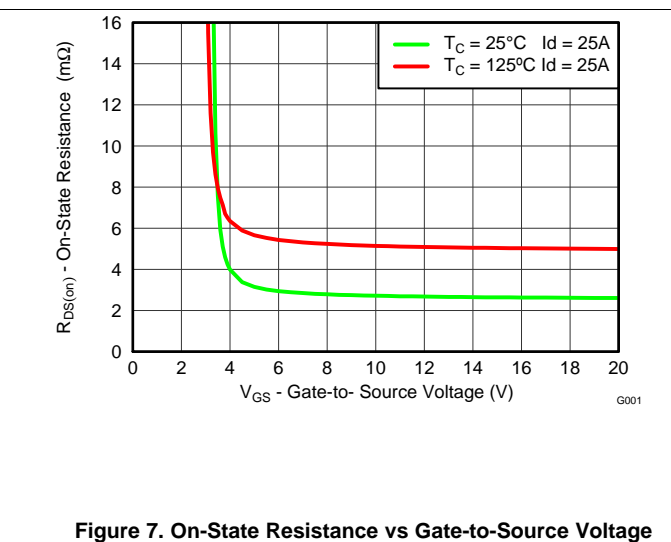
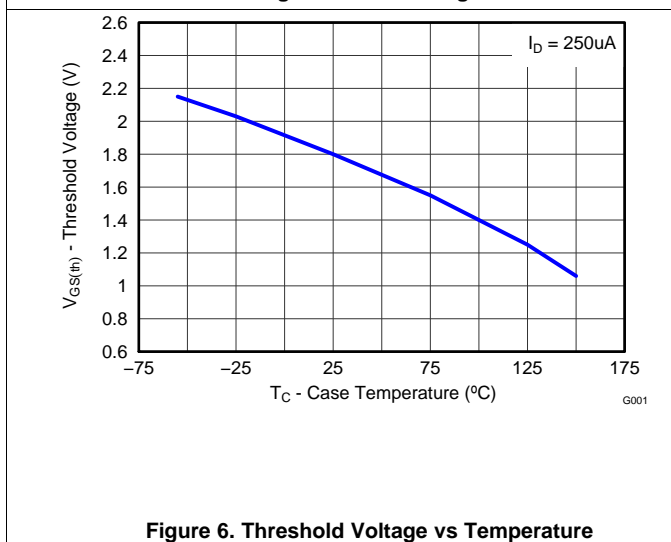
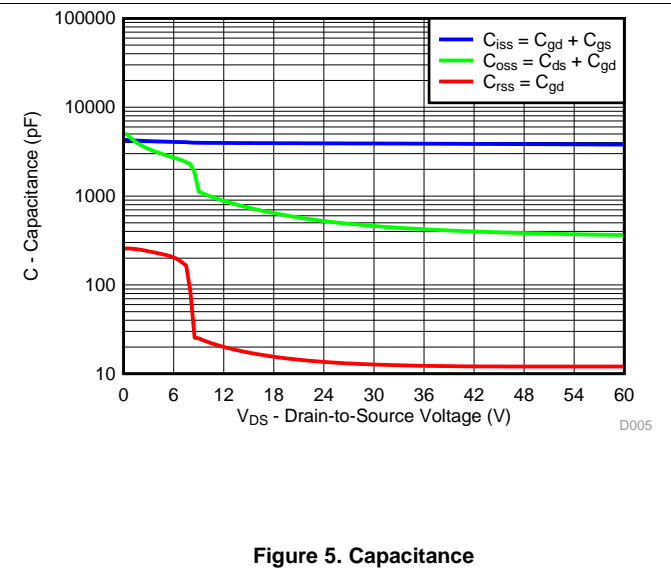
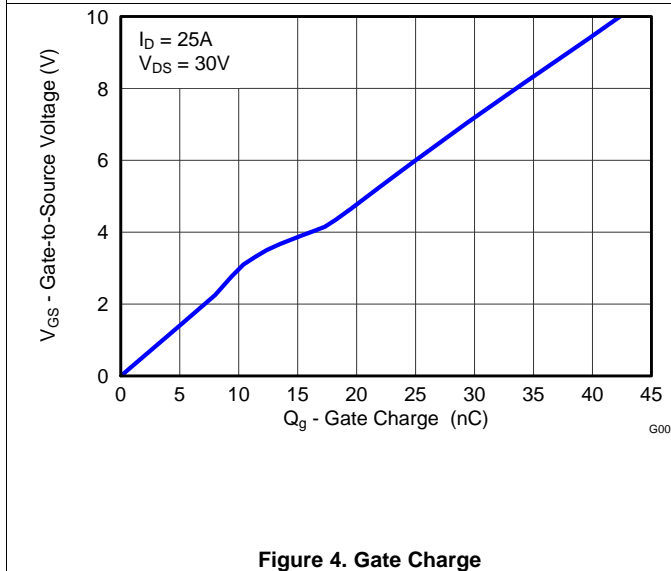
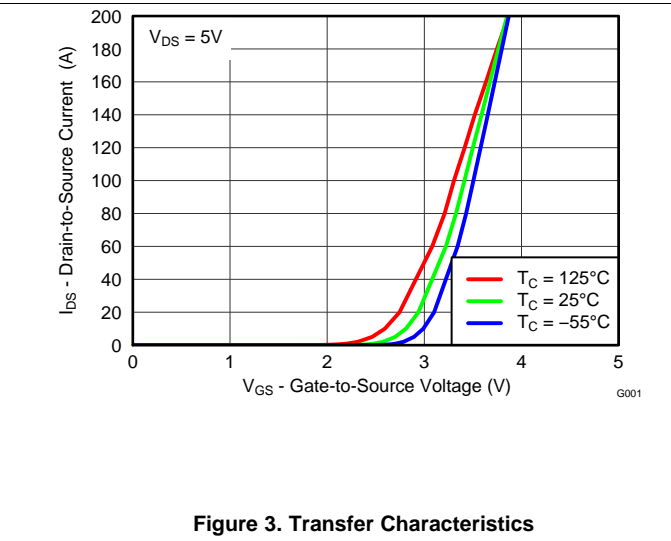
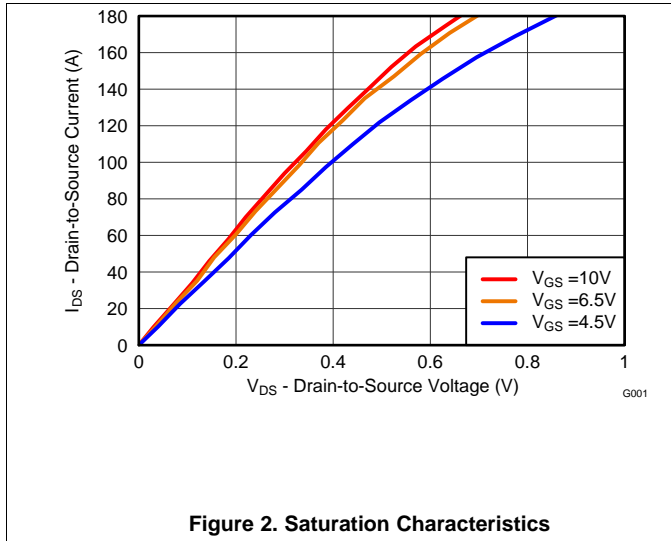
5.3 Typical MOSFET Characteristics

$T_A = 25^{\circ}\text{C}$  unless otherwise stated



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C unless otherwise stated



Typical MOSFET Characteristics (continued)

T<sub>A</sub> = 25°C unless otherwise stated

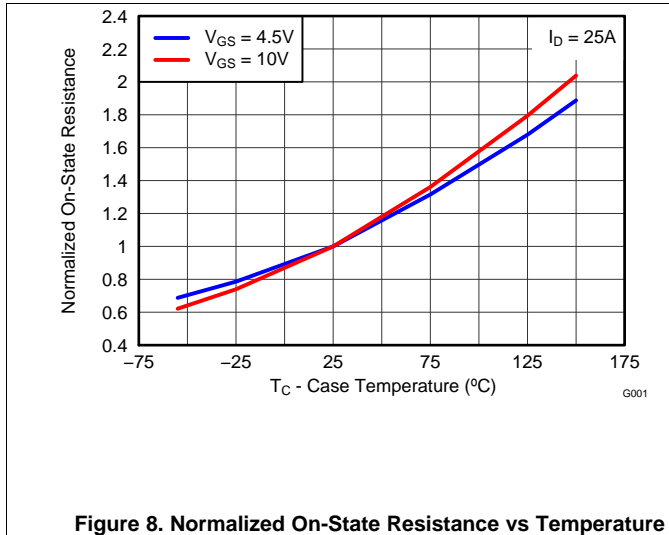


Figure 8. Normalized On-State Resistance vs Temperature

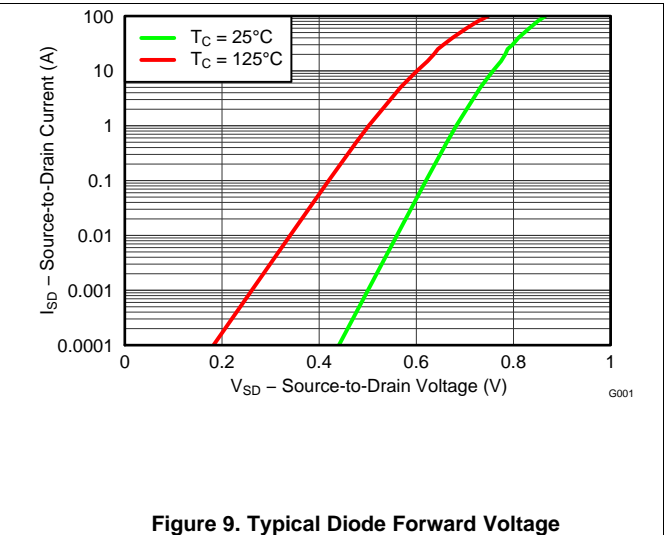


Figure 9. Typical Diode Forward Voltage

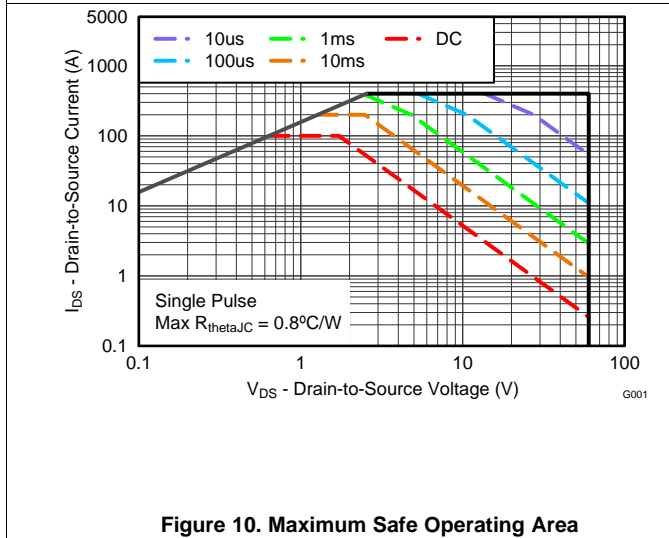


Figure 10. Maximum Safe Operating Area

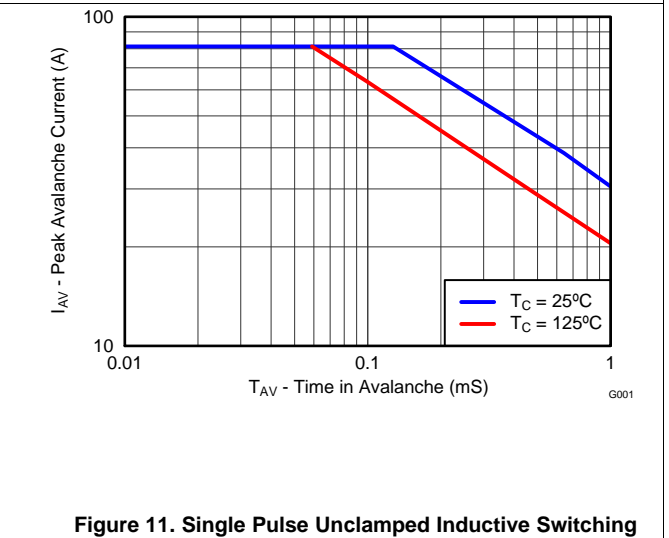


Figure 11. Single Pulse Unclamped Inductive Switching

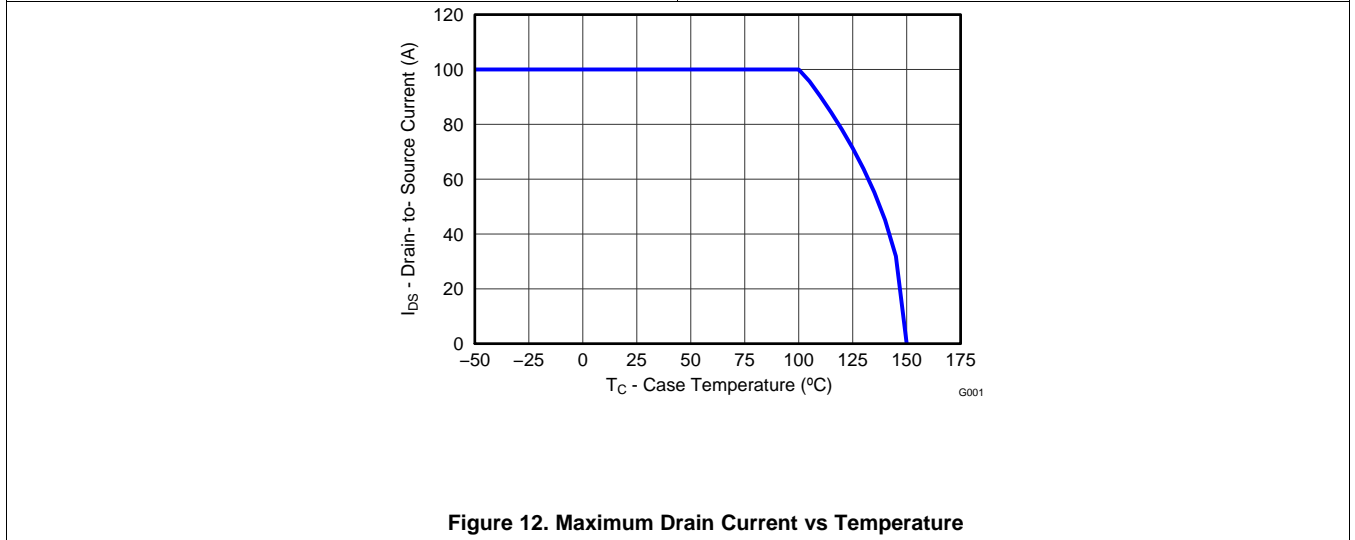


Figure 12. Maximum Drain Current vs Temperature

## 6 Device and Documentation Support

### 6.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

### 6.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

**TI E2E™ Online Community** *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

**Design Support** *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

### 6.3 Trademarks

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### 6.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 6.5 Glossary

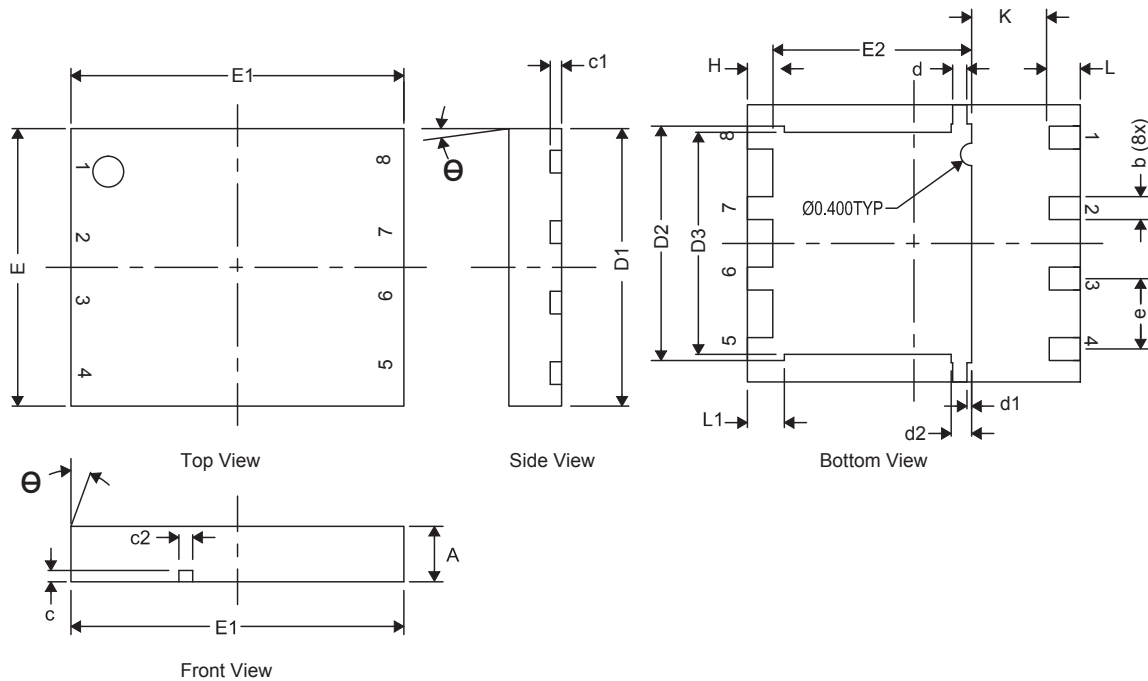
[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 7 Mechanical, Packaging, and Orderable Information

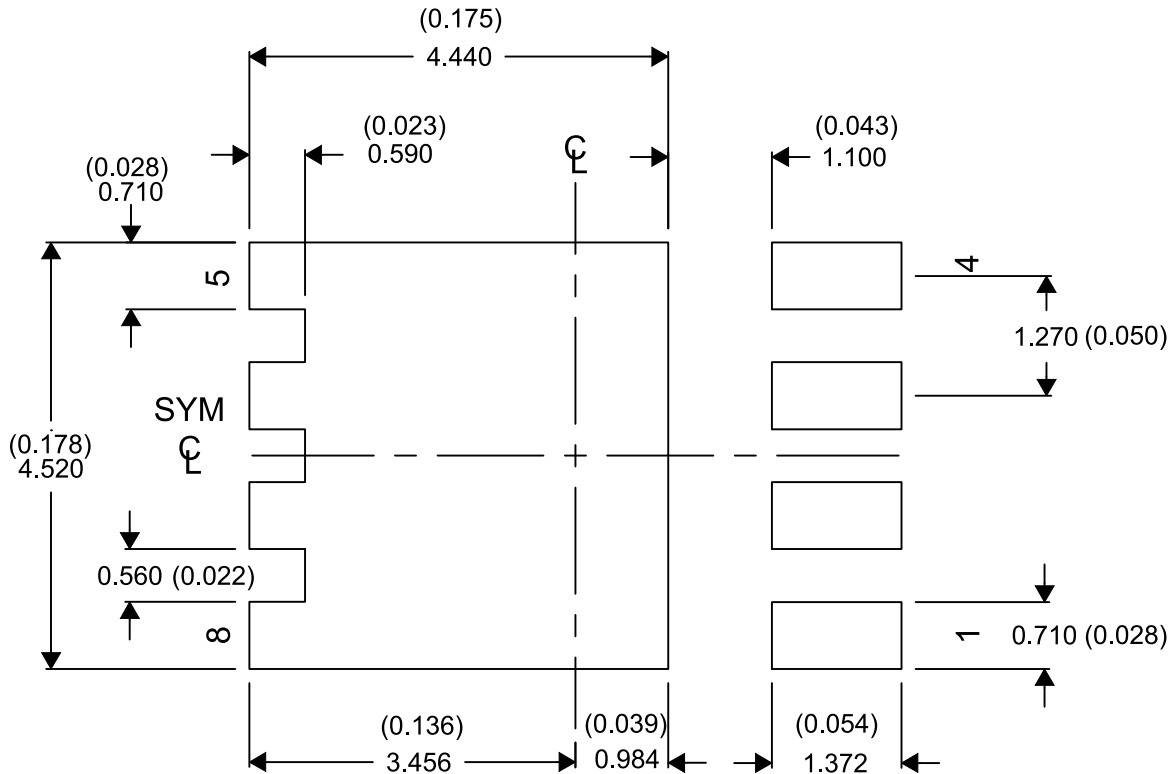
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

### 7.1 Q5B Package Dimensions



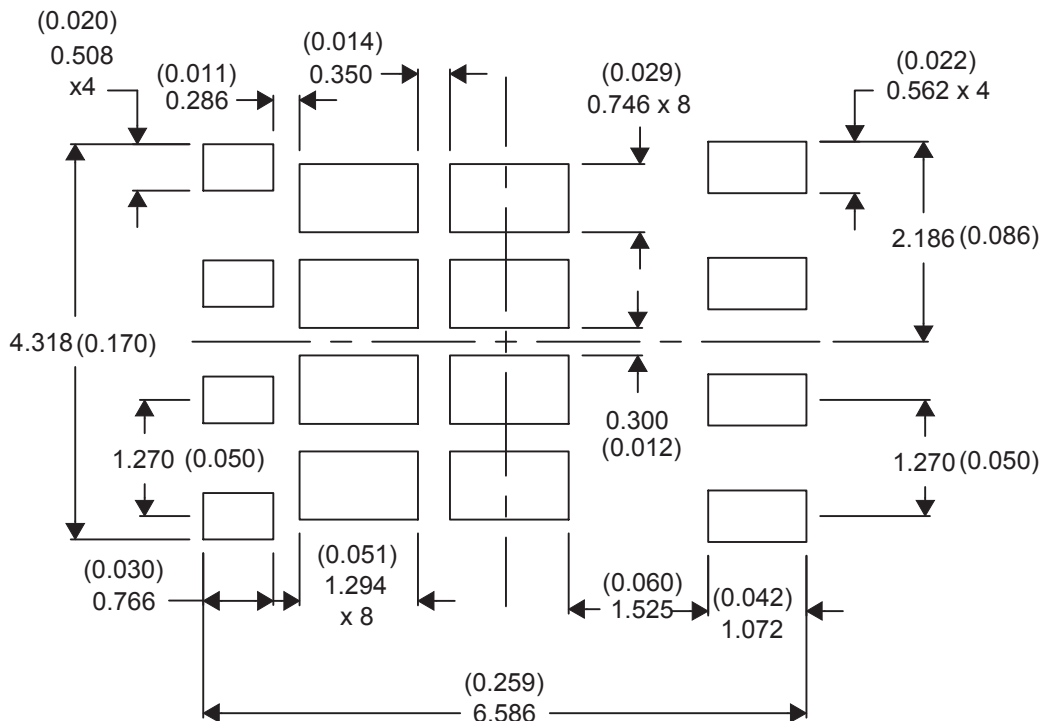
DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
D3	3.90	4.00	4.10
d	0.20	0.25	0.30
d1	0.085 TYP		
d2	0.319	0.369	0.419
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e	1.27 TYP		
H	0.36	0.46	0.56
L	0.46	0.56	0.66
L1	0.57	0.67	0.77
θ	0°	—	—
K	1.40 TYP		

### 7.2 Recommended PCB Pattern

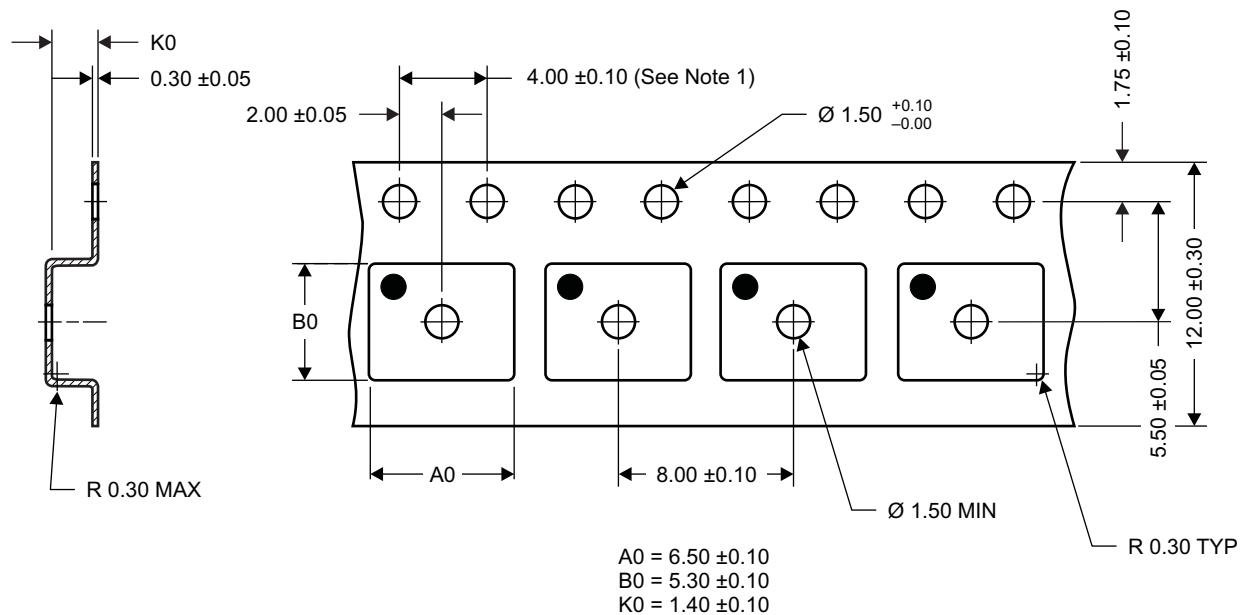


For recommended circuit layout for PCB designs, see [Reducing Ringing Through PCB Layout Techniques \(SLPA005\)](#).

### 7.3 Recommended Stencil Pattern



## 7.4 Q5B Tape and Reel Information



M0138-01

### Notes:

1. 10-sprocket hole-pitch cumulative tolerance  $\pm 0.2$ .
2. Camber not to exceed 1 mm in 100 mm, noncumulative over 250 mm.
3. Material: black static-dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified).
5. A0 and B0 measured on a plane 0.3 mm above the bottom of the pocket.

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18532Q5B	ACTIVE	VSON-CLIP	DNK	8	2500	Pb-Free (RoHS Exempt)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18532	<a href="#">Samples</a>
CSD18532Q5BT	ACTIVE	VSON-CLIP	DNK	8	250	Pb-Free (RoHS Exempt)	CU NIPDAU   CU SN	Level-1-260C-UNLIM	-55 to 150	CSD18532	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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