THE DATASHEET OF

DS7505U+T&R

General Description

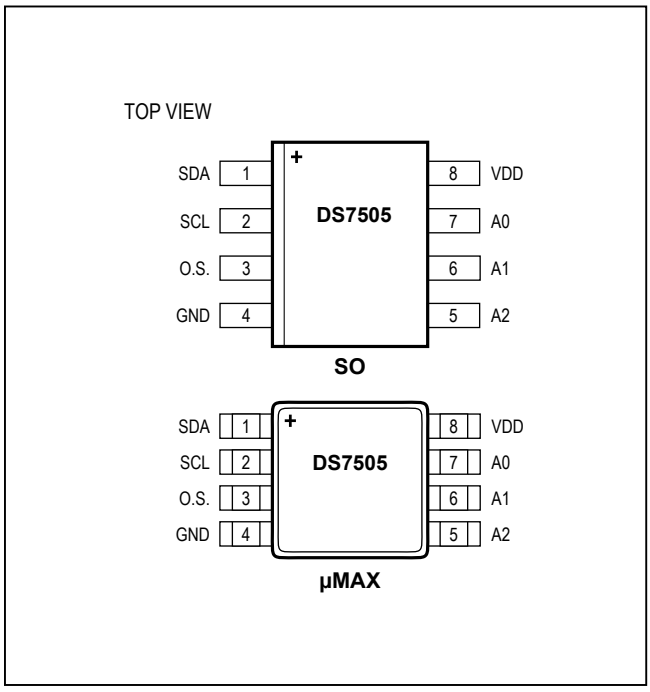
The DS7505 low-voltage (1.7V to 3.7V) digital thermometer and thermostat provides 9-, 10-, 11-, or 12-bit digital temperature readings over a -55°C to +125°C range with ±0.5°C accuracy over a -0°C to +70°C range. A 9-bit resolution mode is software compatible with the LM75.

The DS7505 thermostat has a dedicated open-drain output (O.S.) and programmable fault tolerance, which allows the user to define the number of consecutive error conditions that must occur before O.S. is activated. There are two thermostatic operating modes that control thermostat operation based on user-defined trip points (T_{OS} and T_{HYST}) that are stored in EEPROM registers.

Applications

- Networking Equipment
- Cellular Base Stations
- Office Equipment
- Medical Equipment
- Any Thermally Sensitive System

Pin Configurations



Benefits and Features

- Extends Performance Range with a Low-Voltage, 1.7V to 3.7V Operating Range
- Maximizes System Accuracy in Broad Range of Thermal Management Applications
  - Measures Temperature from -55°C to +125°C (-67°F to +257°F)
  - ±0.5°C Accuracy Over a 0°C to +70°C Range
  - User-Configurable Resolution from 9 Bits (Default) to 12 Bits (0.5°C to 0.0625°C Resolution)
- Reduces Cost with No External Components and Stand Alone Thermostat Capability
- Increases Reliability and System Robustness
  - Internally Filtered Data Lines for Noise Immunity (50ns Deglitch)
  - Bus Timeout Feature Prevents Lockup on a 2-Wire Interface
- Simplifies Distributed Temperature-Sensing Applications with Multidrop Capability
  - Up to Eight Devices Can Operate on a 2-Wire Bus
- Fast 25ms (max) 9-Bit Conversion Time
- Flexible and Nonvolatile (NV) User-Defined Thermostatic Modes

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
DS7505S+	-55°C to +125°C	8 SO (150 mils)
DS7505S+T&R	-55°C to +125°C	8 SO (150 mils), 2500-Piece T&R
DS7505U+	-55°C to +125°C	8 µMAX®
DS7505U+T&R	-55°C to +125°C	8 µMAX, 3000-Piece T&R

+Denotes a lead(Pb)-free/RoHS-compliant package.

T&R = Tape and reel.

Commands are capitalized for clarity.

µMAX is a registered trademark of Maxim Integrated Products, Inc.

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Absolute Maximum Ratings

Voltage Range on VDD Relative to Ground.....-0.3V to +4.0V
Voltage Range on Any Other Pin
Relative to Ground.....-0.3V to +6.0V

Operating Temperature Range..... -55°C to +125°C
Storage Temperature Range..... -55°C to +125°C
Soldering Temperature ..... Refer to the IPC/JEDEC J-STD-020 Specification.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(1.7V ≤ V_{DD} ≤ 3.7V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Supply Voltage	V_{DD}		1.7	3.7	V
Input Voltage Range (SDA, SCL, O.S., A0, A1, A2)		(Note 1)	-0.3	+5.5	V
Thermometer Error (Note 2, 3)	T_{ERR}	0°C to +70°C		±0.5	°C
		-55°C to +125°C		±2.0	
Input Logic-High	V_{IH}	(Note 1)	0.7 x V_{DD}		V
Input Logic-Low	V_{IL}	(Note 1)		0.3 x V_{DD}	V
SDA Output Logic-Low Voltage	V_{OL1}	6mA sink current (Note 1)	0	0.6	V
O.S. Saturation Voltage	V_{OL2}	4mA sink current (Notes 1, 2)		0.8	V
Input Current Each I/O pin		0.4V < $V_{I/O}$ < 0.9 x V_{DD}	-10	+10	µA
I/O Capacitance	$C_{I/O}$			10	pF
Standby Current	I_{DD1}	(Notes 4, 5, 6)		2	µA
Active Current (Notes 4, 5, 6)	I_{DD}	Active temp conversions		750	µA
		Communication only		100	
		E^2 Copy only		500	

AC Electrical Characteristics

(1.7V ≤ V_{DD} ≤ 3.7V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resolution			9		12	Bits
Temperature Conversion Time	t_{CONVT}	9-bit conversions			25	ms
		10-bit conversions			50	
		11-bit conversions			100	
		12-bit conversions			200	
SCL Frequency	f_{SCL}				400	kHz
EEPROM Copy Time	t_{WR}	-40°C to +85°C			10	ms
EEPROM Copy Endurance	N_{EEWR}	-40°C ≤ T_A ≤ +85°C (Note 7)	10k	20k		Cycles
		T_A = +25°C (Note 7)	40k	80k		

AC Electrical Characteristics (continued)

(1.7V ≤ V_{DD} ≤ 3.7V, T_A = -55°C to +125°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
EEPROM Data Retention	t_{EEDR}	-40°C to +125°C (Note 8)	10			Years
Bus Free Time Between a STOP and START Condition	t_{BUF}	(Note 9)	1.3			µs
START and Repeated START Hold Time from Falling SCL	$t_{HD:STA}$	(Notes 9, 10)	600			ns
Low Period of SCL	t_{LOW}	(Note 9)	1.3			µs
High Period of SCL	t_{HIGH}	(Note 9)	0.6			µs
Repeated START Condition Setup Time to Rising SCL	$t_{SU:STA}$	(Note 9)	600			ns
Data-Out Hold Time from Falling SCL	$t_{HD:DAT}$	(Notes 9, 11)	0		0.9	µs
Data-In Setup Time to Rising SCL	$t_{SU:DAT}$	(Note 9)	100			ns
Rise Time of SDA and SCL (Receive)	t_R	(Notes 9, 12)			1000	ns
Fall Time of SDA and SCL (Receive)	t_F	(Notes 9, 12)			300	ns
Spike Suppression Filter Time (Deglitch Filter)	t_{SS}		0		50	ns
STOP Setup Time to Rising SCL	$t_{SU:STO}$	(Note 9)	600			ns
Capacitive Load for Each Bus Line	C_B				400	pF
Input Capacitance	C_I			5		pF
Serial Interface Reset Time	$t_{TIMEOUT}$	SDA time low (Note 12)	75		325	ms

Note 1: All voltages are referenced to ground.

Note 2: Internal heating caused by O.S. loading causes the DS7505 to read approximately 0.5°C higher if O.S. is sinking the max-rated current.

Note 3: Specified in 12-bit conversion mode. Quantization error must be considered when converting in lower resolutions.

Note 4: I_{DD} specified with O.S. pin open.

Note 5: I_{DD} specified with V_{DD} at 3.0V and SDA, SCL = 3.0V, T_A = -55°C to +85°C.

Note 6: I_{DD} specified with A0, A1, A2 = 0V or V_{DD}.

Note 7: V_{DD} must be > 2.0V.

Note 8: E^2 Copy occurs at +25°C.

Note 9: See the timing diagram (Figure 1). All timing is referenced to 0.9 x V_{DD} and 0.1 x V_{DD}.

Note 10: After this period, the first clock pulse is generated.

Note 11: The DS7505 provides an internal hold time of at least 75ns on the SDA signal to bridge the undefined region of SCL's falling edge.

Note 12: This timeout applies only when the DS7505 is holding SDA low. Other devices can hold SDA low indefinitely and the DS7505 does not reset.

Pin Description

PIN	NAME	FUNCTION
1	SDA	Data Input/Output. For 2-wire serial communication port. Open drain.
2	SCL	Clock Input. For 2-wire serial communication port.
3	O.S.	Thermostat Output. Open drain.
4	GND	Ground
5	A2	Address Input
6	A1	Address Input
7	A0	Address Input
8	VDD	Supply Voltage. +1.7V to +3.7V supply pin.

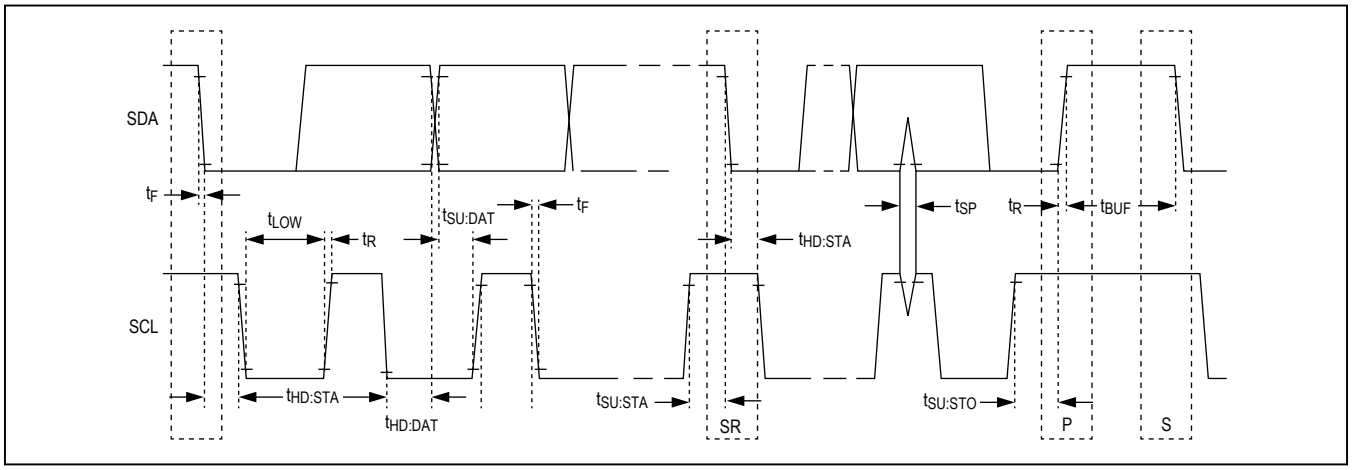

Figure 1. Timing Diagram

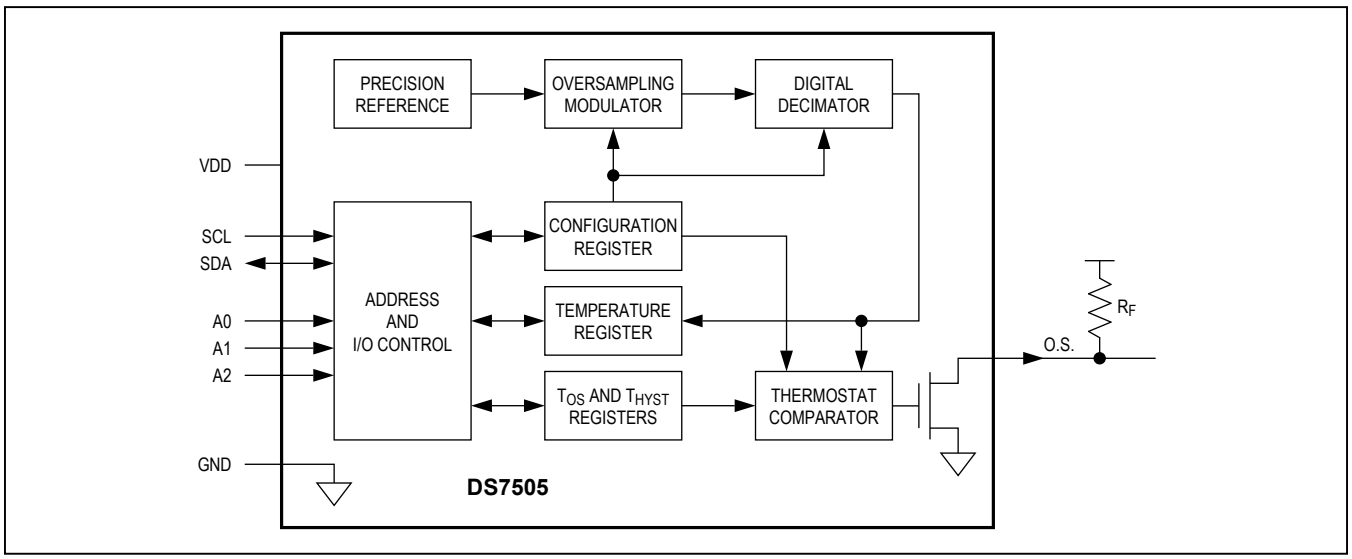

Figure 2. Block Diagram

Operation—Measuring Temperature

The DS7505 measures temperature using a bandgap temperature-sensing architecture. An on-board delta-sigma analog-to-digital converter (ADC) converts the measured temperature to a digital value that is calibrated in degrees Celsius; for Fahrenheit applications a lookup table or conversion routine must be used. The DS7505 is factory-calibrated and requires no external components to measure temperature.

The DS7505 can be configured to power up either automatically converting temperature or in a low-power standby state. The preferred power-up mode can be set using the SD bit in the configuration register as explained in the *Configuration Register* section. The resolution of the digital output data is user-configurable to 9, 10, 11, or 12 bits, corresponding to temperature increments of 0.5°C, 0.25°C, 0.125°C, and 0.0625°C, respectively. The factory default resolution at power-up is 9 bits (R1 = 0, R0 = 0), however this can be programmed to 10, 11, or 12 bits using the R0 and R1 bits in the configuration register as explained in the *Configuration Register* section. Note that the conversion time doubles for each additional bit of resolution.

After each temperature measurement and analog-to-digital (A/D) conversion, the DS7505 stores the temperature as a 16-bit two's complement number in the 2-byte temperature register (see Figure 3). The sign bit (S) indicates if the temperature is positive or negative: for positive numbers S = 0 and for negative numbers S = 1. The most recently converted digital measurement can be read from the temperature register at any time. Since temperature conversions are performed in the background, reading the temperature register does not affect the operation in progress.

Bits 3 through 0 of the temperature register are hardwired to 0. When the DS7505 is configured for 12-bit resolution, the 12 MSBs (bits 15 through 4) of the temperature register contain temperature data. For 11-bit resolution, the 11 MSBs (bits 15 through 5) of the temperature register contain data, and bit 4 reads out as 0. Likewise, for 10-bit resolution, the 10 MSBs (bits 15 through 6) contain data, and for 9-bit the 9 MSBs (bits 15 through 7) contain data and all unused LSBs contains 0s. Table 1 gives examples of 12-bit resolution digital output data and the corresponding temperatures.

	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
MS Byte	S	2^6	2^5	2^4	2^3	2^2	2^1	2^0
	Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
LS Byte	2^{-1}	2^{-2}	2^{-3}	2^{-4}	0	0	0	0

Figure 3. Temperature, T_{OS}, and T_{HYST} Register Format

Table 1. 12-Bit Resolution Temperature/Data Relationship

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	DIGITAL OUTPUT (HEX)
+125	0111 1101 0000 0000	7D00
+25.0625	0001 1001 0001 0000	1910
+10.125	0000 1010 0010 0000	0A20
+0.5	0000 0000 1000 0000	0080
0	0000 0000 0000 0000	0000
-0.5	1111 1111 1000 0000	FF80
-10.125	1111 0101 1110 0000	F5E0
-25.0625	1110 0110 1111 0000	E6F0
-55	1100 1001 0000 0000	C900

Shutdown Mode

For power-sensitive applications, the DS7505 offers a low-power shutdown mode. The SD bit in the configuration register controls shutdown mode. When SD is programmed to 1, the conversion in progress is completed and the result stored in the temperature register, after which the DS7505 goes into a low-power standby state. The O.S. output is cleared if the thermostat is operating in interrupt mode and O.S remains unchanged in comparator mode. The 2-wire interface remains operational in shutdown mode, and writing a 0 to the SD bit returns the DS7505 to normal operation. Upon power-up in shutdown mode, the DS7505 executes one temperature measurement. The result is stored in the temperature register, after which the DS7505 enters the shutdown state.

Operation—Thermostat

The DS7505 thermostat can be programmed to power up in either comparator mode or interrupt mode, which activate and deactivate the open-drain thermostat output (O.S.) based on user-programmable trip points (T_{OS} and T_{HYST}). The T_{HYST} and T_{OS} registers contain Celsius temperature values in two's complement format and consist of EEPROM that is shadowed by SRAM. Once written to the shadow SRAM, values can be stored in EEPROM by issuance of a Copy Data command from the master (see the *Command Set* section for more details). The device can operate using the shadow SRAM only or using the EEPROM. If the EEPROM is used, the values are NV and can be programmed prior to installation of the DS7505 for standalone operation. The factory power-up settings for the DS7505 are with the thermostat in comparator mode, active-low O.S. polarity, overtemperature trip-point (T_{OS}) register set to 80°C, the hysteresis trip-point (T_{HYST}) register set to +75°C, and the number of consecutive conversion to trigger O.S. set to 1. If these power-up settings are compatible with the application, the DS7505 can be used as a stand-alone thermostat (i.e., no 2-wire communication required) with no programming required prior to installation. If interrupt mode operation, active-high O.S. polarity, different T_{OS} and T_{HYST} values, or a different number of conversions to trigger O.S. are desired, they must be programmed into the EEPROM either after initial power-up or prior to IC installation. The programmed values then become the new power-up defaults.

In both operating modes, the user can program the thermostat-fault tolerance, which sets how many consecutive temperature readings (1, 2, 4, or 6) must fall outside the thermostat limits before the thermostat output is triggered. The fault tolerance is set by the F1 and F0 bits in the configuration register. The default factory power-up setting for fault tolerance is 1 (F1 = 0, F0 = 0).

The data format of the T_{OS} and T_{HYST} registers is identical to that of the temperature register (see Figure 3), i.e., a 2-byte two's complement representation of the trip-point temperature in degrees Celsius with bits 3 through 0 hardwired to 0. After every temperature conversion, the measurement is compared to the values stored in the T_{OS} and T_{HYST} registers. The O.S. output is updated based on the result of the comparison and the operating mode of the IC. The number of T_{OS} and T_{HYST} bits used during the thermostat comparison is equal to the conversion resolution set by the R1 and R0 bits in the configuration register. For example, if the resolution is 9 bits, only the 9 MSBs of T_{OS} and T_{HYST} are used by the thermostat comparator.

The active state of the O.S. output can be programmed by the POL bit in the configuration register. The powerup factory default is active low (POL = 0).

If the user does not wish to use the thermostat capabilities of the DS7505, the O.S. output should be left unconnected. Note that if the thermostat is not used, the T_{OS} and T_{HYST} registers can be used for general storage of system data.

Comparator Mode

When the thermostat is in comparator mode, O.S. can be programmed to operate with any amount of hysteresis. The O.S. output becomes active when the measured temperature exceeds the T_{OS} value a consecutive number of times as defined by the F1 and F0 fault tolerance (FT) bits in the configuration register. O.S. then stays active until the first time the temperature falls below the value stored in T_{HYST}. Putting the device into shutdown mode does not clear O.S. in comparator mode. Thermostat comparator mode operation with FT = 2 is illustrated in Figure 4.

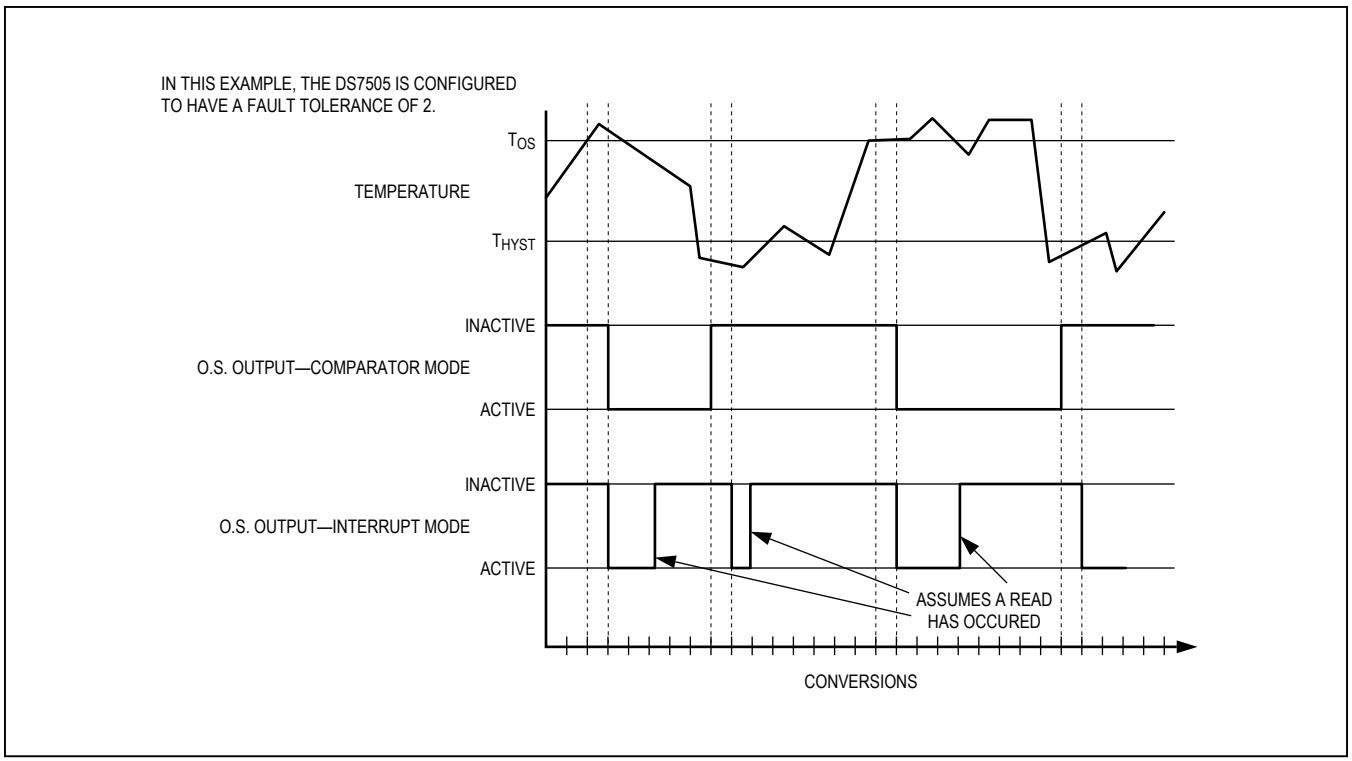

Figure 4. O.S. Output Operation Example

Interrupt Mode

In interrupt mode, the O.S. output first becomes active when the measured temperature exceeds the T_{OS} value a consecutive number of times equal to the FT value in the configuration register. Once activated, O.S. can only be cleared by either putting the DS7505 into shutdown mode or by reading from any register (temperature, configuration, T_{OS}, or T_{HYST}) on the device. Once O.S. has been deactivated, it is only reactivated when the measured temperature falls below the T_{HYST} value a consecutive number of times equal to the FT value. Again, O.S can only be cleared by putting the device into shutdown mode or reading any register. Thus, this interrupt/clear process is cyclical between T_{OS} and T_{HYST} events (i.e, T_{OS}, clear, T_{HYST}, clear, T_{OS}, clear, T_{HYST}, clear, etc.). Thermostat interrupt mode operation with FT = 2 is illustrated in Figure 4.

Configuration Register

The configuration register allows the user to program various DS7505 options such as conversion resolution, thermostat fault tolerance, thermostat polarity, thermostat operating mode, and shutdown mode. The configuration register is arranged as shown in Figure 5 and detailed descriptions of each bit are provided in Table 2. The user has read/write access to all bits in the configuration register except the MSB (NVB bit), which is a read-only bit. All bits in the register but the NVB bit are NV EEPROM backed by shadow SRAM, and thus power-up in their programmed state. Once written to the shadow SRAM, values can be stored in EEPROM by issuance of a Copy Data command from the master (see the *Command Set* section for more details). If the values are not copied to the EEPROM, the device powers up with the factory default settings or the last values that were copied to the EEPROM. The NVB bit is SRAM and powers up in the state shown in Table 2.

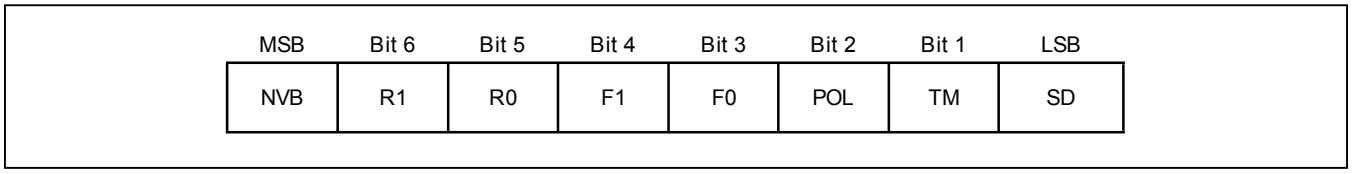

Figure 5. Configuration Register

Table 2. Configuration Register Bit Descriptions

BIT NAME	FUNCTIONAL DESCRIPTION
NVB NV Memory Status	Power-up state = 0, read only NVB = 1—Write to an NV memory cell is in progress. NVB = 0—NV memory is not busy.
R1 Conversion Resolution Bit 1	Factory power-up state = 0 Sets conversion resolution (see Table 3).
R0 Conversion Resolution Bit 0	Factory power-up state = 0 Sets conversion resolution (see Table 3).
F1 Thermostat Fault Tolerance Bit 1	Factory power-up state = 0 Sets the thermostat fault tolerance (see Table 4).
F0 Thermostat Fault Tolerance Bit 0	Factory power-up state = 0 Sets the thermostat fault tolerance (see Table 4).
POL Thermostat Output (O.S.) Polarity	Factory power-up state = 0 POL = 0—O.S. is active low. POL = 1—O.S. is active high.
TM Thermostat Operating Mode	Factory power-up state = 0 TM = 0—Comparator mode. TM = 1—Interrupt mode. See the *Operation—Thermostat* section for a detailed description of these modes.
SD Shutdown	Factory power-up state = 0 SD = 0—Active conversion and thermostat operation. SD = 1—Shutdown mode. See the *Shutdown Mode* section for a detailed description of this mode.

Table 3. Resolution Configuration

R1	R0	THERMOMETER RESOLUTION (BITS)	MAX CONVERSION TIME (ms)
0	0	9	25
0	1	10	50
1	0	11	100
1	1	12	200

Table 4. Fault Tolerance Configuration

F1	F0	CONSECUTIVE OUT-OF-LIMITS CONVERSIONS TO TRIGGER O.S.
0	0	1
0	1	2
1	0	4
1	1	6

Register Pointer

The four DS7505 registers each have a unique 2-bit pointer designation, which is defined in Table 5. When reading from or writing to the DS7505, the user must "point" the DS7505 to the register that is to be accessed. When reading from the DS7505, once the pointer is set, it remains pointed at the same register until it is changed. For example, if the user desires to perform consecutive reads from the temperature register, then the pointer only has to be set to the temperature register one time, after which all reads are automatically from the temperature register until the pointer value is changed. When writing to the DS7505, the pointer value must be refreshed each time a write is performed, even if the same register is being written to twice in a row.

At power-up, the pointer defaults to the temperature register location. The temperature register can be read immediately without resetting the pointer.

Changes to the pointer setting are accomplished as described in the *2-Wire Serial Data Bus* section.

Table 5. Pointer Definition

REGISTER	P1	P0
Temperature	0	0
Configuration	0	1
T_{HYST}	1	0
T_{OS}	1	1

2-Wire Serial Data Bus

The DS7505 communicates over a standard bidirectional 2-wire serial data bus that consists of a serial clock (SCL) signal and serial data (SDA) signal. The DS7505 interfaces to the bus through the SCL input pin and open-drain SDA I/O pin. All communication is MSB first.

The following terminology is used to describe 2-wire communication:

Master Device: Microprocessor/microcontroller that controls the slave devices on the bus. The master device generates the SCL signal and START and STOP conditions.

Slave: All devices on the bus other than the master. The DS7505 always functions as a slave.

Bus Idle or Not Busy: Both SDA and SCL remain high. SDA is held high by a pullup resistor when the bus is idle, and SCL must either be forced high by the master (if the SCL output is push-pull) or pulled high by a pullup resistor (if the SCL output is open drain).

Transmitter: A device (master or slave) that is sending data on the bus.

Receiver: A device (master or slave) that is receiving data from the bus.

START Condition: Signal generated by the master to indicate the beginning of a data transfer on the bus. The master generates a START condition by pulling SDA from high to low while SCL is high (see Figure 6). A "repeated" START is sometimes used at the end of a data transfer (instead of a STOP) to indicate that the master performs another operation.

STOP Condition: Signal generated by the master to indicate the end of a data transfer on the bus. The master generates a STOP condition by transitioning SDA from low to high while SCL is high (see Figure 6). After the STOP is issued, the master releases the bus to its idle state.

Acknowledge (ACK): When a device (either master or slave) is acting as a receiver, it must generate an acknowledge (ACK) on the SDA line after receiving every byte of data. The receiving device performs an ACK by pulling the SDA line low for an entire SCL period (see Figure 6). During the ACK clock cycle, the transmitting device must release SDA. A variation on the ACK signal is the "not acknowledge" (NACK). When the master device is acting as a receiver, it uses a NACK instead of an ACK after the last data byte to indicate that it is finished receiving data. The master indicates a NACK by leaving the SDA line high during the ACK clock cycle.

Slave Address: Every slave device on the bus has a unique 7-bit address that allows the master to access that device. The DS7505's 7-bit bus address is 1 0 0 1 A_2 A_1 A_0, where A_2, A_1, and A_0 are user-selectable through the corresponding input pins. The three address pins allow up to eight DS7505s to be multidropped on the same bus.

Address Byte: The control byte is transmitted by the master and consists of the 7-bit slave address plus a read/write (R/$\overline{W}$) bit (see Figure 7). If the master is going to read data from the slave device then R/$\overline{W}$ = 1, and if the master is going to write data to the slave device then R/$\overline{W}$ = 0.

Pointer Byte: The pointer byte is used by the master to tell the DS7505 which register is going to be accessed during communication. The six MSBs of the pointer byte (see Figure 8) are always 0 and the two LSBs correspond to the desired register as shown in Figure 8.

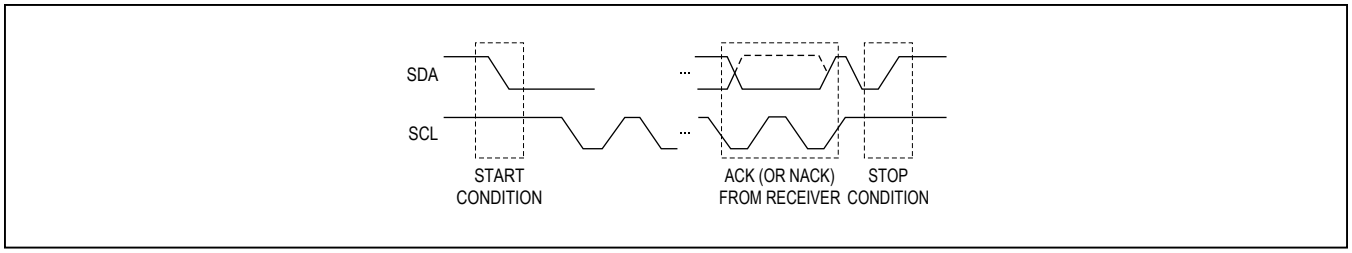

Figure 6. Start, Stop, and ACK Signals

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
1	0	0	1	A_2	A_1	A_0	R/$\overline{W}$

Figure 7. Address Byte

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	P1	P0

Figure 8. Pointer Byte

General 2-Wire Information

- All data is transmitted MSB first over the 2-wire bus.
- One bit of data is transmitted on the 2-wire bus each SCL period.
- A pullup resistor is required on the SDA line, and, when the bus is idle, both SDA and SCL must remain in a logic-high state.
- All bus communication must be initiated with a START condition and terminated with a STOP condition. During a START or STOP is the only time SDA is allowed to change states while SCL is high. At all other times, changes on the SDA line can only occur when SCL is low; SDA must remain stable when SCL is high.
- After every 8-bit (1-byte) transfer, the receiving device must answer with an ACK (or NACK), which takes one SCL period. Therefore, nine clocks are required for every 1-byte data transfer.

Writing to the DS7505: To write to the DS7505, the master must generate a START followed by an address byte containing the DS7505 bus address. The value of the R/$\overline{W}$ bit must be a 0, which indicates that a write is about to take place. The DS7505 responds with an ACK after receiving the address byte. The master then sends a pointer byte which tells the DS7505 which register is being written to. The DS7505 again responds with an ACK after receiving the pointer byte. Following this ACK the master device must immediately begin transmitting data to the DS7505. When writing to the configuration register, the master must send one byte of data (see Figure 9B), and when writing to the TOS or THYST registers the master must send two bytes of data (see Figure 9C). After receiving each data byte, the DS7505 responds with an ACK, and the transaction is finished with a STOP from the master. All writes to the DS7505 are made to shadow SRAM. Once data is written to the shadow SRAM, it is only stored to EEPROM by issuance of a Copy Data command from the master. At that time, all registers are copied to EEPROM except the Temperature register which is SRAM only.

Reading from the DS7505: When reading from the DS7505, if the pointer was already pointed to the desired register during a previous transaction, the read can be performed immediately without changing the pointer setting. In this case the master sends a START followed by an address byte containing the DS7505 bus address. The R/$\overline{W}$ bit must be a 1, which tells the DS7505 that a read is being performed. After the DS7505 sends an ACK in response to the address byte, the DS7505 begins transmitting the requested data on the next clock cycle. When reading from the configuration register, the DS7505 transmits one byte of data, after which the master must respond with a NACK followed by a STOP (see Figure 9E). For two-byte reads (i.e., from the temperature, T_{OS} or T_{HYST} register), the DS7505 transmits two bytes of data, and the master must respond to the first data byte with an ACK and to the second byte with a NACK followed by a STOP (see Figure 9A). If only the most significant byte of data is needed, the master can issue a NACK followed by a STOP after reading the first data byte in which case the transaction is the same as for a read from the configuration register.

If the pointer is not already pointing to the desired register, the pointer must first be updated as shown in Figure 9D, which shows a pointer update followed by a single-byte read. The value of the R/$\overline{W}$ bit in the initial address byte is a 0 (“write”) since the master is going to write a pointer byte to the DS7505. After the DS7505 responds to the address byte with an ACK, the master sends a pointer byte that corresponds to the desired register. The master must then perform a repeated start followed by a standard one or two byte read sequence (with R/$\overline{W}$ =1) as described in the previous paragraph.

The Recall Data command should be issued before a read if assurance is needed that the contents of the EEPROM in the Shadow SRAM when read.

Bus Timeout: The DS7505 has a bus timeout feature that prevents communication errors from leaving the IC in a state where SDA is held low disrupting other devices on the bus. If the DS7505 holds the SDA line low for a period of $t_{TIMEOUT}$, its bus interface automatically resets and release the SDA line. Bus communication frequency must be fast enough to prevent a reset during normal operation. The bus timeout feature only applies to when the DS7505 is holding SDA low. Other devices can hold SDA low for an undefined period without causing the interface to reset.

Command Set

Recall Data [B8h] **1011 1000**

Refreshes SRAM shadow register with EEPROM data. It is recommended that a Recall command be performed before reading EEPROM-backed memory locations. The master sends a START followed by an address byte containing the DS7505 bus address. The R/$\overline{W}$ bit must be a 0. The DS7505 responds with an ACK. If the next byte is a 0xB8, the DS7505 recalls all EEPROM data into shadow RAM locations.

Copy Data [48h] 0100 1000

Copies data from all SRAM shadow registers to EEPROM. It is recommended that a Copy Data command be performed after writing EEPROM-backed memory locations to guarantee data integrity in the event of a power loss. The master sends a START followed by an address byte containing the DS7505 bus address. The R/$\overline{W}$ bit must be a 0. The DS7505 responds with an ACK. If the next byte is a 0x48, the DS7505 copies all Shadow RAM locations in EEPROM memory.

Software POR [54h] 0101 0100

The master sends a START followed by an address byte containing the DS7505 bus address. The R/$\overline{W}$ bit must be a 0. The DS7505 responds with an ACK. If the next byte is a 0x54, the DS7505 resets as if power had been cycled, which stops temperature conversions and resets all registers to their power-up states. No ACK is sent by the IC after the POR command is received. Afterwards, the DS7505 makes a single temperature conversion or continuous temperature conversions, depending on the state of the SD bit.

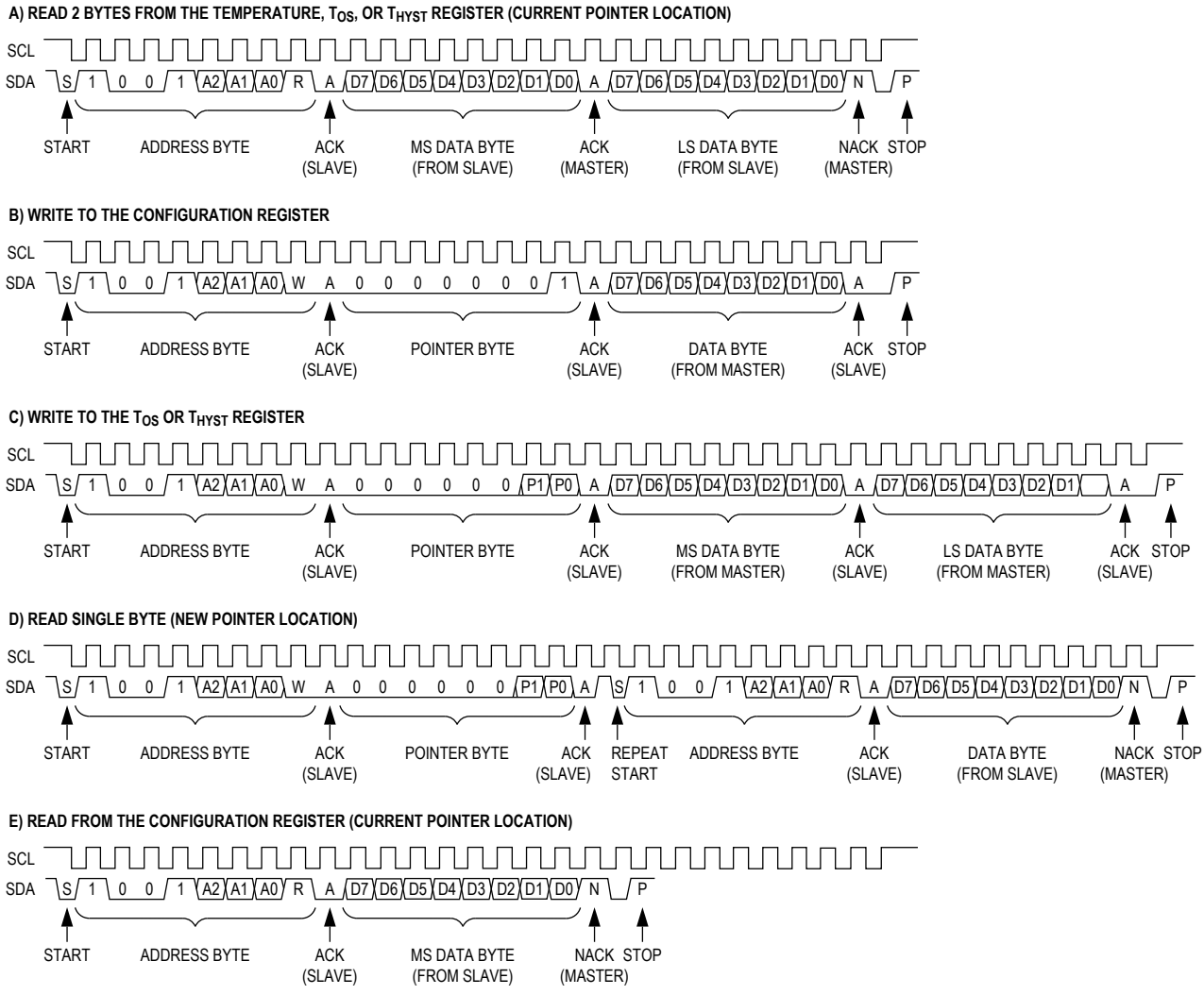

Figure 9. 2-Wire Interface Timing

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
8 SO	S8+2	**21-0041**
8 µMAX	U8+3	**21-0036**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	2/08	Initial release.	—
1	3/08	Removed references to exposed pad (µMAX package does not have an EP); corrected package information outline document number.	1, 4, 13
2	12/14	Updated *General Description* and *Benefits and Features* sections	2
3	12/15	Updated Rise/Fall Time of SDA and SCL specs in *AC Electrical Characteristics* table and deleted Note 12 of *AC Electrical Characteristics* table	3

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