



**THE DATASHEET OF
EC103D1WX**



1. General description

Planar passivated ultra sensitive gate Silicon Controlled Rectifier in a SOT223 surface mountable plastic package.

2. Features and benefits

- Planar passivated for voltage ruggedness and reliability
- Ultra sensitive gate
- Surface mountable package

3. Applications

- Electronic ballasts
- Safety shut down and protection circuits
- Sensing circuits
- Smoke detectors
- Switched Mode Power Supplies

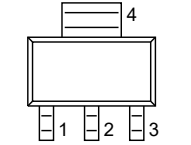

4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{RRM}	repetitive peak reverse voltage		-	-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 114\text{ °C}$; Fig. 1	-	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 114\text{ °C}$; Fig. 2 ; Fig. 3	-	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 10\text{ ms}$; Fig. 4 ; Fig. 5	-	-	8	A
		half sine wave; $T_{j(init)} = 25\text{ °C}$; $t_p = 8.3\text{ ms}$	-	-	9	A
T_j	junction temperature		-	-	125	°C
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}$; $I_T = 0.1\text{ A}$; $T_j = 25\text{ °C}$; Fig. 9	-	3	12	μA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}$; $T_j = 125\text{ °C}$; ($V_{DM} = 67\%$ of V_{DRM}); exponential waveform; gate open circuit	-	150	-	$\text{V}/\mu\text{s}$

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K	cathode	 <p>SC-73 (SOT223)</p>	 <p>A K G sym037</p>
2	A	anode		
3	G	gate		
4	mb	mounting base; connected to anode		

6. Ordering information

Table 3. Ordering information

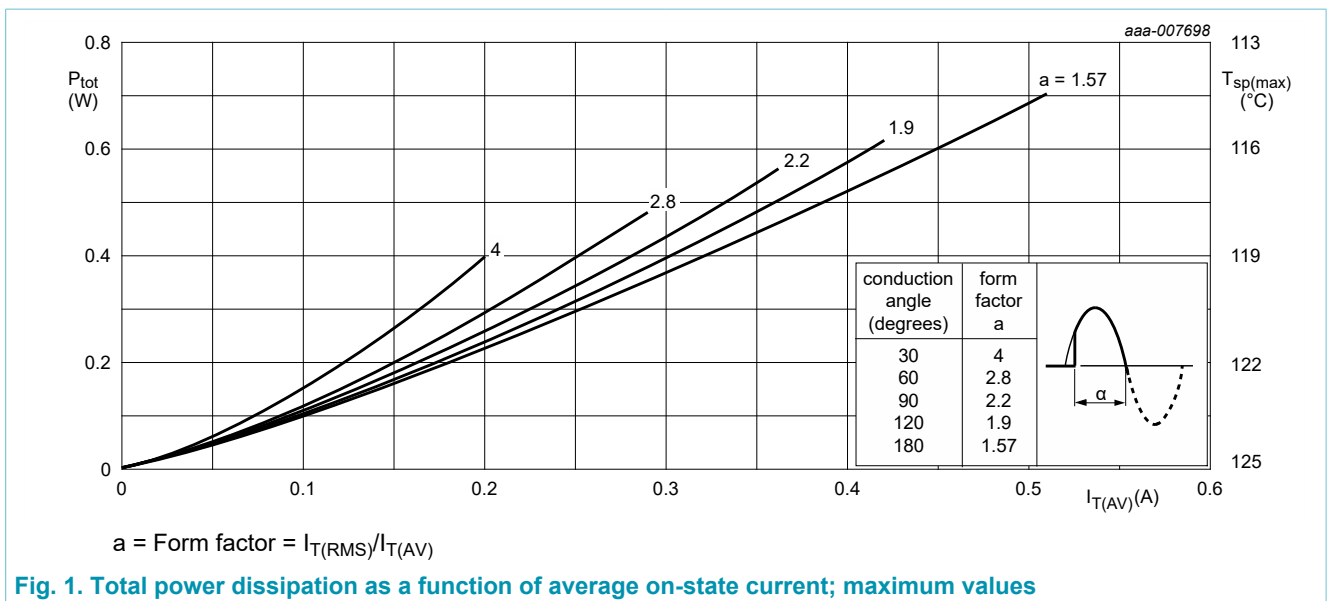
Type number	Package		
	Name	Description	Version
EC103D1W	SC-73	plastic surface-mounted package with increased heatsink; 4 leads	SOT223

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DRM}	repetitive peak off-state voltage		-	400	V
V_{RRM}	repetitive peak reverse voltage		-	400	V
$I_{T(AV)}$	average on-state current	half sine wave; $T_{sp} \leq 114\text{ }^{\circ}\text{C}$; Fig. 1	-	0.5	A
$I_{T(RMS)}$	RMS on-state current	half sine wave; $T_{sp} \leq 114\text{ }^{\circ}\text{C}$; Fig. 2; Fig. 3	-	0.8	A
I_{TSM}	non-repetitive peak on-state current	half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 10\text{ ms}$; Fig. 4; Fig. 5	-	8	A
		half sine wave; $T_{j(\text{init})} = 25\text{ }^{\circ}\text{C}$; $t_p = 8.3\text{ ms}$	-	9	A
I^2t	I^2t for fusing	$t_p = 10\text{ ms}$; sine-wave pulse	-	0.32	A^2s
dl_T/dt	rate of rise of on-state current	$I_T = 2\text{ A}$; $I_G = 0.01\text{ A}$; $dl_G/dt = 0.1\text{ A}/\mu\text{s}$	-	50	$\text{A}/\mu\text{s}$
I_{GM}	peak gate current		-	1	A
V_{RGM}	peak reverse gate voltage		-	5	V
P_{GM}	peak gate power		-	2	W
$P_{G(AV)}$	average gate power	over any 20 ms period	-	0.1	W
T_{stg}	storage temperature		-40	150	$^{\circ}\text{C}$
T_j	junction temperature		-	125	$^{\circ}\text{C}$



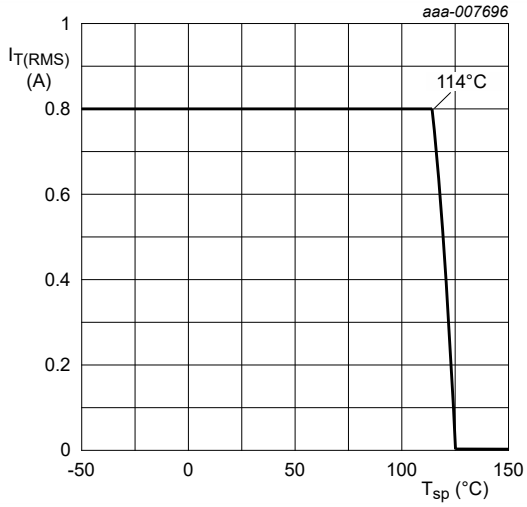


Fig. 2. RMS on-state current as a function of solder point temperature; maximum values

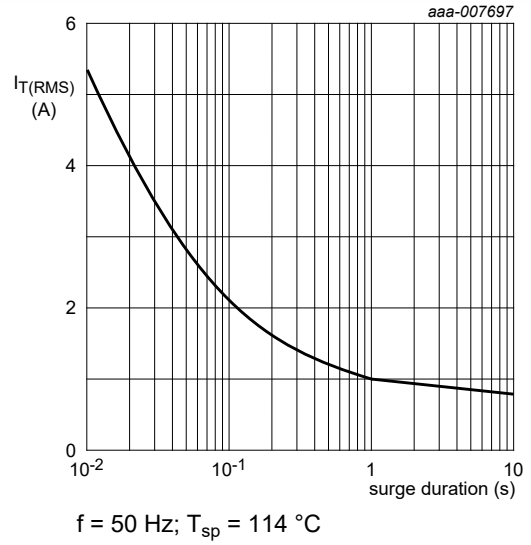


Fig. 3. RMS on-state current as a function of surge duration; maximum values

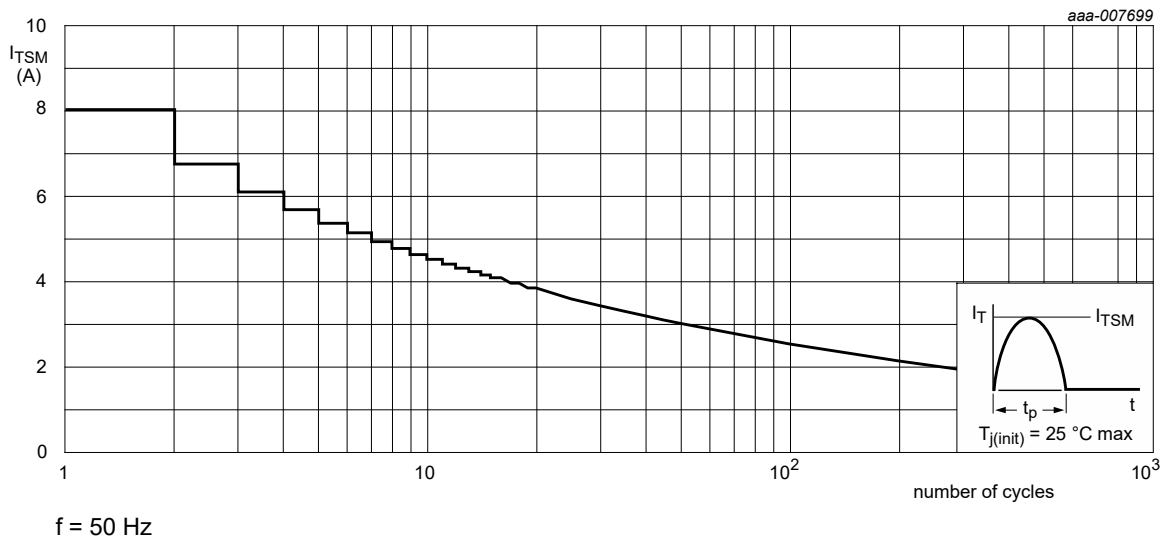
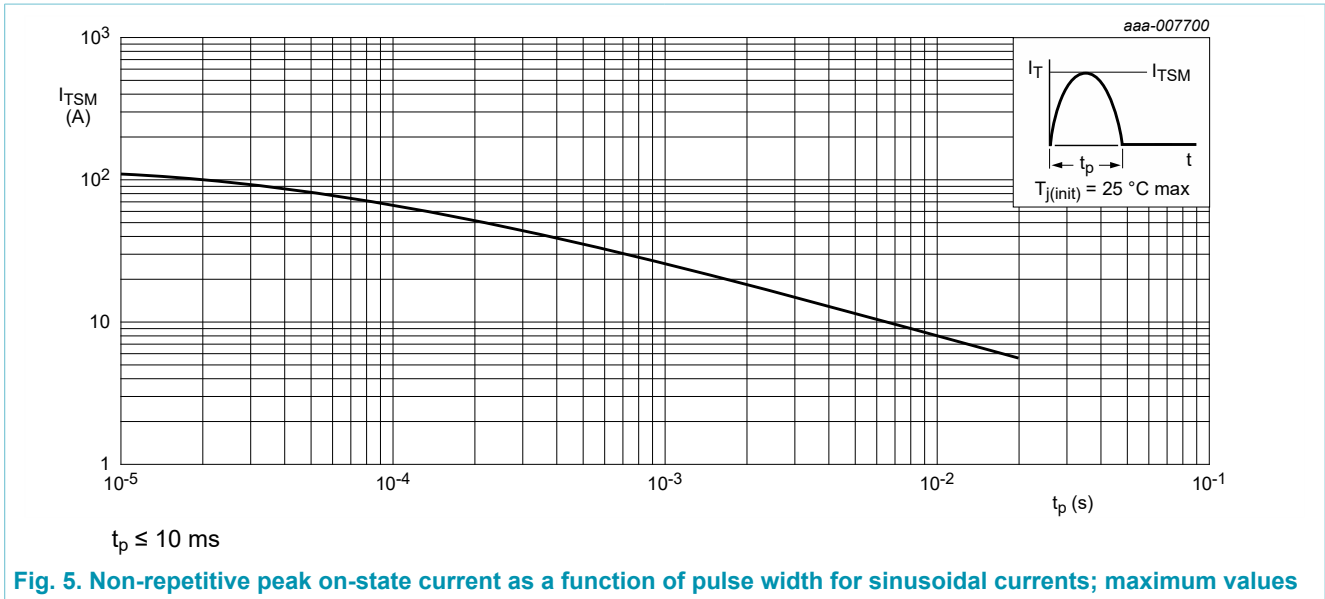


Fig. 4. Non-repetitive peak on-state current as a function of the number of sinusoidal current cycles; maximum values



8. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	Fig. 6	-	-	15	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient free air	printed circuit board mounted; minimum pad area; in free air; Fig. 7	-	70	-	K/W
		printed circuit board mounted; minimum footprint; in free air; Fig. 8	-	156	-	K/W

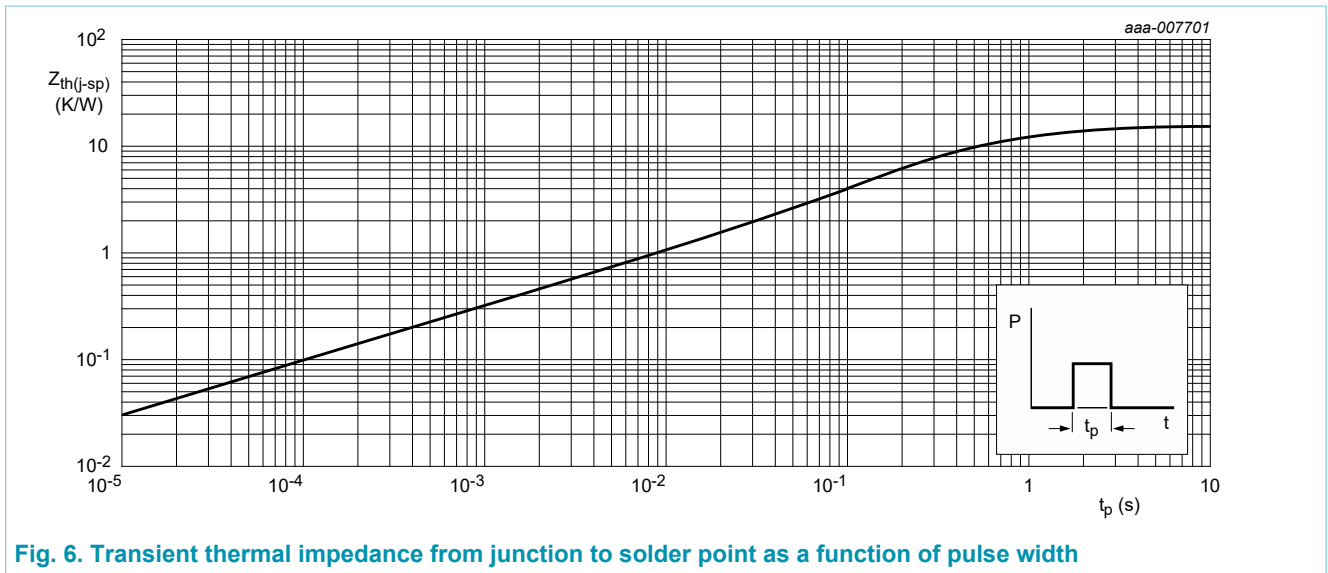
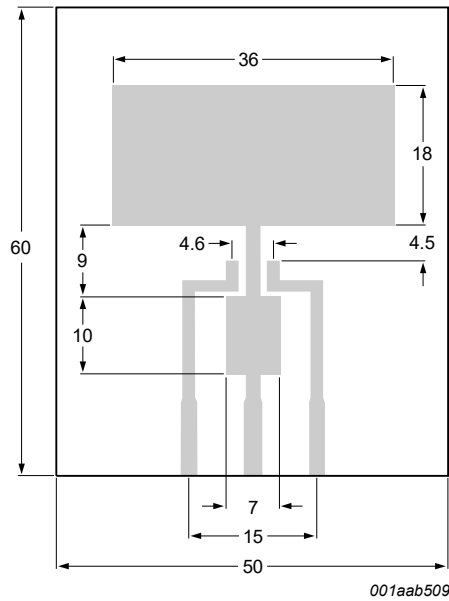
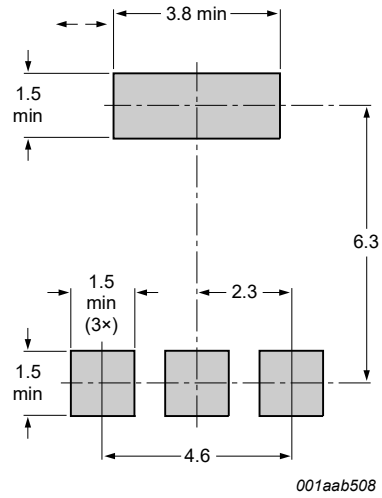


Fig. 6. Transient thermal impedance from junction to solder point as a function of pulse width



All dimensions are in mm
 Printed circuit board:
 FR4 epoxy glass (1.6 mm thick), copper laminate
 (35 um thick)

Fig. 7. Printed circuit board pad area: SOT223



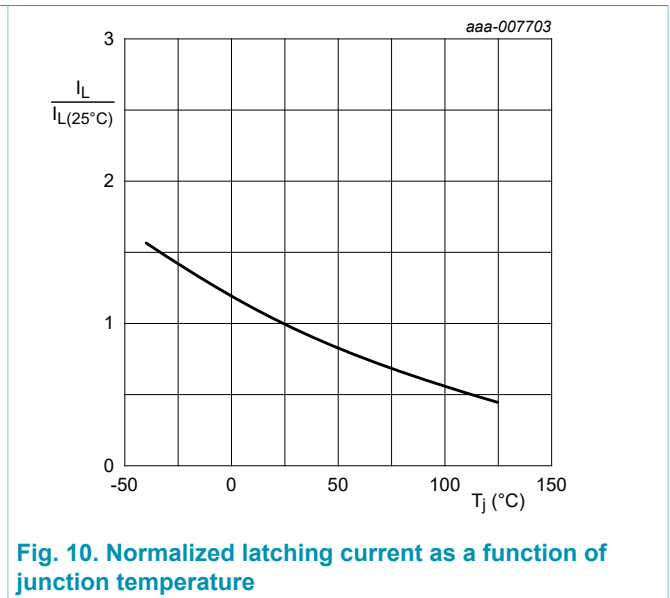
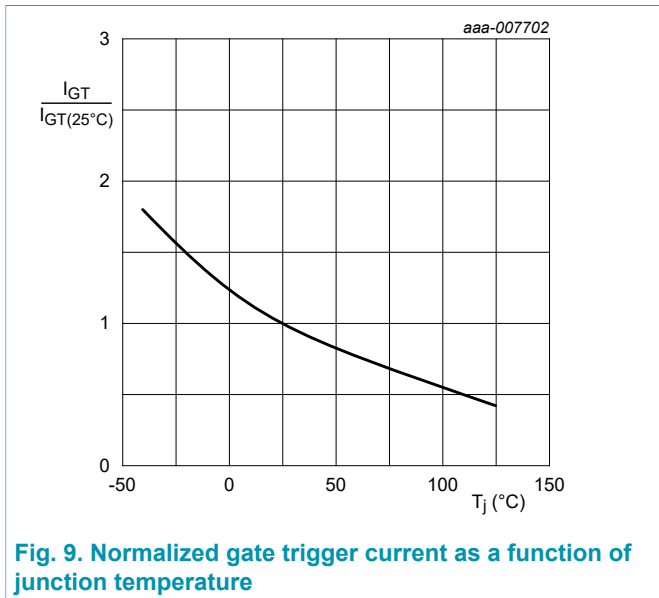
All dimensions are in mm

Fig. 8. Minimum footprint SOT223

9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
I_{GT}	gate trigger current	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 9	-	3	12	μA
I_L	latching current	$V_D = 12\text{ V}; I_G = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 10	-	2	6	mA
I_H	holding current	$V_D = 12\text{ V}; T_j = 25\text{ }^\circ\text{C};$ Fig. 11	-	2	5	mA
V_T	on-state voltage	$I_T = 1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 12	-	1.2	1.35	V
V_{GT}	gate trigger voltage	$V_D = 12\text{ V}; I_T = 0.1\text{ A}; T_j = 25\text{ }^\circ\text{C};$ Fig. 13	-	0.5	0.8	V
		$V_D = 400\text{ V}; I_T = 0.1\text{ A}; T_j = 125\text{ }^\circ\text{C};$ Fig. 13	0.2	0.3	-	V
I_D	off-state current	$V_D = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.05	0.1	mA
I_R	reverse current	$V_R = 400\text{ V}; T_j = 125\text{ }^\circ\text{C}$	-	0.05	0.1	mA
Dynamic characteristics						
dV_D/dt	rate of rise of off-state voltage	$V_{DM} = 268\text{ V}; T_j = 125\text{ }^\circ\text{C}; (V_{DM} = 67\%$ of $V_{DRM});$ exponential waveform; gate open circuit	-	150	-	V/ μs



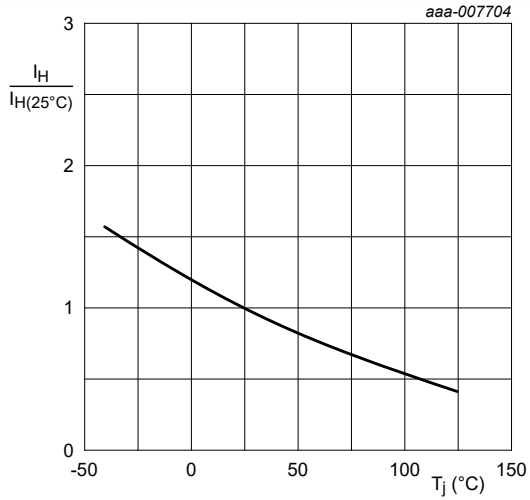
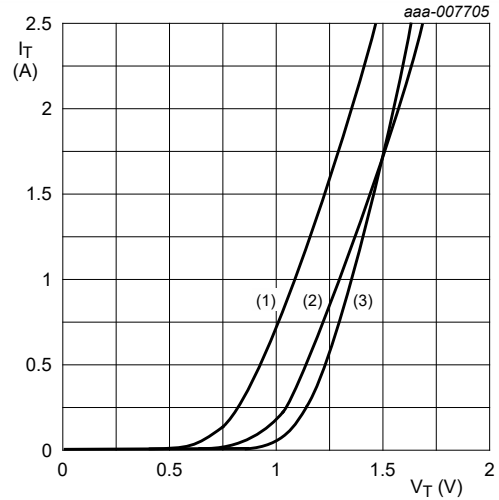


Fig. 11. Normalized holding current as a function of junction temperature



$V_o = 0.987 \text{ V}; R_s = 0.3125 \Omega$
 (1) $T_j = 125^\circ\text{C}$; typical values
 (2) $T_j = 125^\circ\text{C}$; maximum values
 (3) $T_j = 25^\circ\text{C}$; maximum values

Fig. 12. On-state current as a function of on-state voltage

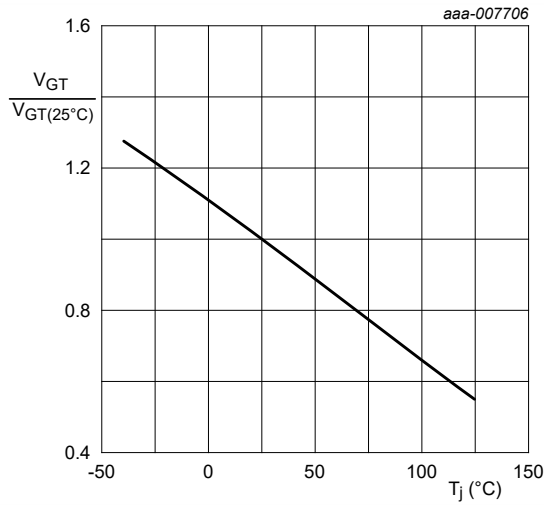


Fig. 13. Normalized gate trigger voltage as a function of junction temperature

10. Package outline

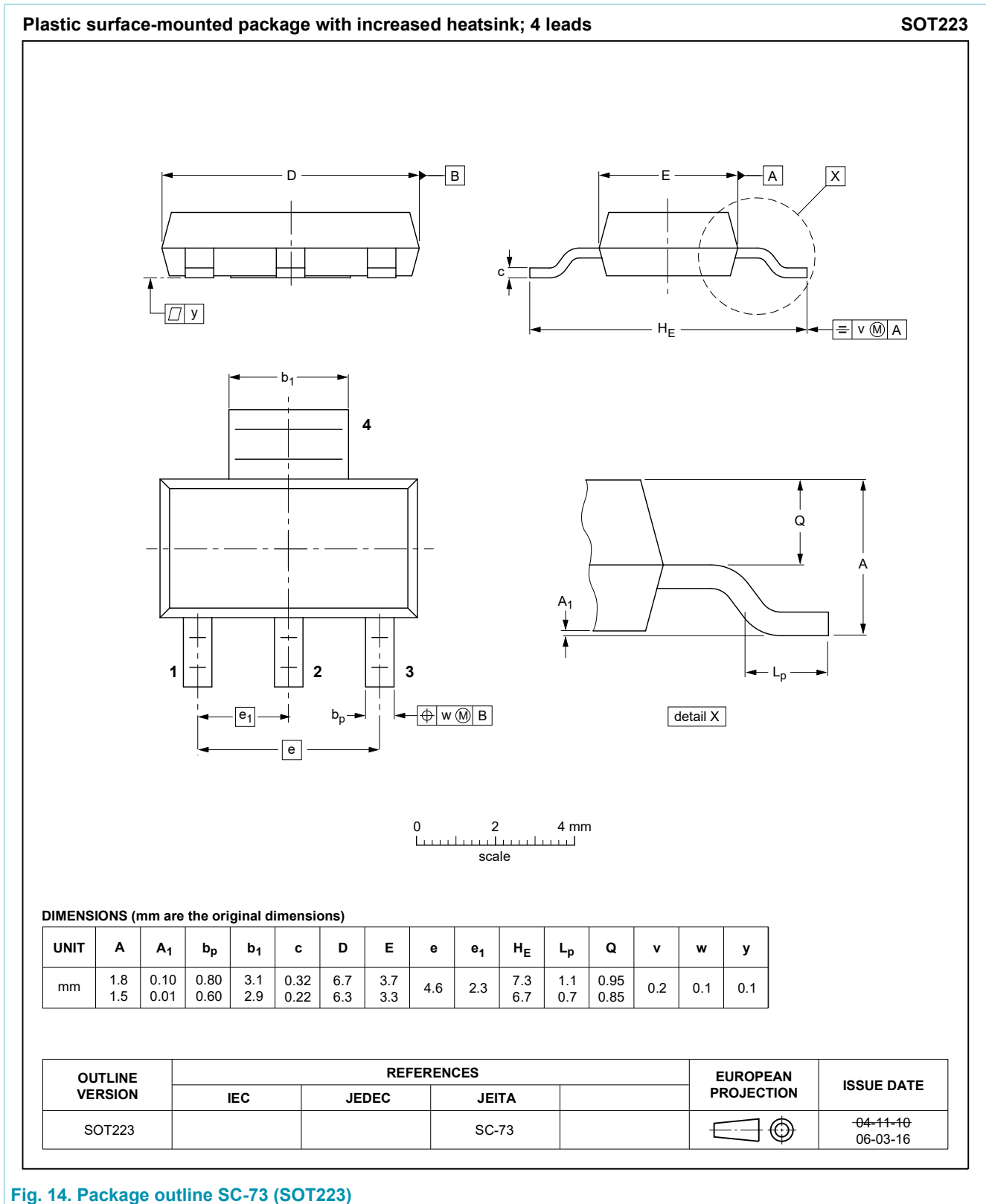


Fig. 14. Package outline SC-73 (SOT223)

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Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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