# APEX 20K

## Programmable Logic Device Family

March 2004, ver. 5.1 Data Sheet

## Features

- Industry's first programmable logic device (PLD) incorporating system-on-a-programmable-chip (SOPC) integration
  - MultiCore™ architecture integrating look-up table (LUT) logic, product-term logic, and embedded memory
  - LUT logic used for register-intensive functions
  - Embedded system block (ESB) used to implement memory functions, including first-in first-out (FIFO) buffers, dual-port RAM, and content-addressable memory (CAM)
  - ESB implementation of product-term logic used for combinatorial-intensive functions
- High density
  - 30,000 to 1.5 million typical gates (see Tables 1 and 2)
  - Up to 51,840 logic elements (LEs)
  - Up to 442,368 RAM bits that can be used without reducing available logic
  - Up to 3,456 product-term-based macrocells

*Table 1. APEX 20K Device Features* *Note (1)*

| Feature | EP20K30E | EP20K60E | EP20K100 | EP20K100E | EP20K160E | EP20K200 | EP20K200E |
|---|---|---|---|---|---|---|---|
| Maximum system gates | 113,000 | 162,000 | 263,000 | 263,000 | 404,000 | 526,000 | 526,000 |
| Typical gates | 30,000 | 60,000 | 100,000 | 100,000 | 160,000 | 200,000 | 200,000 |
| LEs | 1,200 | 2,560 | 4,160 | 4,160 | 6,400 | 8,320 | 8,320 |
| ESBs | 12 | 16 | 26 | 26 | 40 | 52 | 52 |
| Maximum RAM bits | 24,576 | 32,768 | 53,248 | 53,248 | 81,920 | 106,496 | 106,496 |
| Maximum macrocells | 192 | 256 | 416 | 416 | 640 | 832 | 832 |
| Maximum user I/O pins | 128 | 196 | 252 | 246 | 316 | 382 | 376 |

*Table 2. Additional APEX 20K Device Features* *Note (1)*

| Feature | EP20K300E | EP20K400 | EP20K400E | EP20K600E | EP20K1000E | EP20K1500E |
|---|---|---|---|---|---|---|
| Maximum system gates | 728,000 | 1,052,000 | 1,052,000 | 1,537,000 | 1,772,000 | 2,392,000 |
| Typical gates | 300,000 | 400,000 | 400,000 | 600,000 | 1,000,000 | 1,500,000 |
| LEs | 11,520 | 16,640 | 16,640 | 24,320 | 38,400 | 51,840 |
| ESBs | 72 | 104 | 104 | 152 | 160 | 216 |
| Maximum RAM bits | 147,456 | 212,992 | 212,992 | 311,296 | 327,680 | 442,368 |
| Maximum macrocells | 1,152 | 1,664 | 1,664 | 2,432 | 2,560 | 3,456 |
| Maximum user I/O pins | 408 | 502 | 488 | 588 | 708 | 808 |

*Note to Tables 1 and 2:*
(1) The embedded IEEE Std. 1149.1 Joint Test Action Group (JTAG) boundary-scan circuitry contributes up to 57,000 additional gates.

## Additional Features

- Designed for low-power operation
  - 1.8-V and 2.5-V supply voltage (see Table 3)
  - MultiVolt™ I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - ESB offering programmable power-saving mode

*Table 3. APEX 20K Supply Voltages*

| Feature | Device | |
|---|---|---|
| | EP20K100<br>EP20K200<br>EP20K400 | EP20K30E<br>EP20K60E<br>EP20K100E<br>EP20K160E<br>EP20K200E<br>EP20K300E<br>EP20K400E<br>EP20K600E<br>EP20K1000E<br>EP20K1500E |
| Internal supply voltage ($V_{CCINT}$) | 2.5 V | 1.8 V |
| MultiVolt I/O interface voltage levels ($V_{CCIO}$) | 2.5 V, 3.3 V, 5.0 V | 1.8 V, 2.5 V, 3.3 V, 5.0 V *(1)* |

*Note to Table 3:*
(1) APEX 20KE devices can be 5.0-V tolerant by using an external resistor.

- Flexible clock management circuitry with up to four phase-locked loops (PLLs)
  - Built-in low-skew clock tree
  - Up to eight global clock signals
  - ClockLock® feature reducing clock delay and skew
  - ClockBoost® feature providing clock multiplication and division
  - ClockShift™ programmable clock phase and delay shifting
- Powerful I/O features
  - Compliant with peripheral component interconnect Special Interest Group (PCI SIG) ***PCI Local Bus Specification, Revision 2.2*** for 3.3-V operation at 33 or 66 MHz and 32 or 64 bits
  - Support for high-speed external memories, including DDR SDRAM and ZBT SRAM (ZBT is a trademark of Integrated Device Technology, Inc.)
  - Bidirectional I/O performance ($t_{CO}$ + $t_{SU}$) up to 250 MHz
  - LVDS performance up to 840 Mbits per channel
  - Direct connection from I/O pins to local interconnect providing fast $t_{CO}$ and $t_{SU}$ times for complex logic
  - MultiVolt I/O interface support to interface with 1.8-V, 2.5-V, 3.3-V, and 5.0-V devices (see Table 3)
  - Programmable clamp to $V_{CCIO}$
  - Individual tri-state output enable control for each pin
  - Programmable output slew-rate control to reduce switching noise
  - Support for advanced I/O standards, including low-voltage differential signaling (LVDS), LVPECL, PCI-X, AGP, CTT, stub-series terminated logic (SSTL-3 and SSTL-2), Gunning transceiver logic plus (GTL+), and high-speed terminated logic (HSTL Class I)
  - Pull-up on I/O pins before and during configuration
- Advanced interconnect structure
  - Four-level hierarchical FastTrack® Interconnect structure providing fast, predictable interconnect delays
  - Dedicated carry chain that implements arithmetic functions such as fast adders, counters, and comparators (automatically used by software tools and megafunctions)
  - Dedicated cascade chain that implements high-speed, high-fan-in logic functions (automatically used by software tools and megafunctions)
  - Interleaved local interconnect allows one LE to drive 29 other LEs through the fast local interconnect
- Advanced packaging options
  - Available in a variety of packages with 144 to 1,020 pins (see Tables 4 through 7)
  - FineLine BGA® packages maximize board space efficiency
- Advanced software support
  - Software design support and automatic place-and-route provided by the Altera® Quartus® II development system for

Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations
- Altera MegaCore® functions and Altera Megafunction Partners Program (AMPP℠) megafunctions
- NativeLink™ integration with popular synthesis, simulation, and timing analysis tools
- Quartus II SignalTap® embedded logic analyzer simplifies in-system design evaluation by giving access to internal nodes during device operation
- Supports popular revision-control software packages including PVCS, Revision Control System (RCS), and Source Code Control System (SCCS )

*Table 4. APEX 20K QFP, BGA & PGA Package Options & I/O Count* *Notes (1), (2)*

| Device | 144-Pin TQFP | 208-Pin PQFP RQFP | 240-Pin PQFP RQFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| EP20K30E | 92 | 125 | | | | |
| EP20K60E | 92 | 148 | 151 | 196 | | |
| EP20K100 | 101 | 159 | 189 | 252 | | |
| EP20K100E | 92 | 151 | 183 | 246 | | |
| EP20K160E | 88 | 143 | 175 | 271 | | |
| EP20K200 | | 144 | 174 | 277 | | |
| EP20K200E | | 136 | 168 | 271 | 376 | |
| EP20K300E | | | 152 | | 408 | |
| EP20K400 | | | | | 502 | 502 |
| EP20K400E | | | | | 488 | |
| EP20K600E | | | | | 488 | |
| EP20K1000E | | | | | 488 | |
| EP20K1500E | | | | | 488 | |

*Table 5. APEX 20K FineLine BGA Package Options & I/O Count* *Notes (1), (2)*

| Device | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| EP20K30E | 93 | 128 | | | |
| EP20K60E | 93 | 196 | | | |
| EP20K100 | | 252 | | | |
| EP20K100E | 93 | 246 | | | |
| EP20K160E | | | 316 | | |
| EP20K200 | | | 382 | | |
| EP20K200E | | | 376 | 376 | |
| EP20K300E | | | | 408 | |
| EP20K400 | | | | 502 *(3)* | |
| EP20K400E | | | | 488 *(3)* | |
| EP20K600E | | | | 508 *(3)* | 588 |
| EP20K1000E | | | | 508 *(3)* | 708 |
| EP20K1500E | | | | | 808 |

***Notes to Tables 4 and 5:***

(1) I/O counts include dedicated input and clock pins.

(2) APEX 20K device package types include thin quad flat pack (TQFP), plastic quad flat pack (PQFP), power quad flat pack (RQFP), 1.27-mm pitch ball-grid array (BGA), 1.00-mm pitch FineLine BGA, and pin-grid array (PGA) packages.

(3) This device uses a thermally enhanced package, which is taller than the regular package. Consult the *Altera Device Package Information Data Sheet* for detailed package size information.

*Table 6. APEX 20K QFP, BGA & PGA Package Sizes*

| Feature | 144-Pin TQFP | 208-Pin QFP | 240-Pin QFP | 356-Pin BGA | 652-Pin BGA | 655-Pin PGA |
|---|---|---|---|---|---|---|
| Pitch (mm) | 0.50 | 0.50 | 0.50 | 1.27 | 1.27 | – |
| Area ($mm^2$) | 484 | 924 | 1,218 | 1,225 | 2,025 | 3,906 |
| Length × Width (mm × mm) | 22 × 22 | 30.4 × 30.4 | 34.9 × 34.9 | 35 × 35 | 45 × 45 | 62.5 × 62.5 |

*Table 7. APEX 20K FineLine BGA Package Sizes*

| Feature | 144 Pin | 324 Pin | 484 Pin | 672 Pin | 1,020 Pin |
|---|---|---|---|---|---|
| Pitch (mm) | 1.00 | 1.00 | 1.00 | 1.00 | 1.00 |
| Area ($mm^2$) | 169 | 361 | 529 | 729 | 1,089 |
| Length × Width (mm × mm) | 13 × 13 | 19 × 19 | 23 × 23 | 27 × 27 | 33 × 33 |

## General Description

APEX™ 20K devices are the first PLDs designed with the MultiCore architecture, which combines the strengths of LUT-based and product-term-based devices with an enhanced memory structure. LUT-based logic provides optimized performance and efficiency for data-path, register-intensive, mathematical, or digital signal processing (DSP) designs. Product-term-based logic is optimized for complex combinatorial paths, such as complex state machines. LUT- and product-term-based logic combined with memory functions and a wide variety of MegaCore and AMPP functions make the APEX 20K device architecture uniquely suited for system-on-a-programmable-chip designs. Applications historically requiring a combination of LUT-, product-term-, and memory-based devices can now be integrated into one APEX 20K device.

APEX 20KE devices are a superset of APEX 20K devices and include additional features such as advanced I/O standard support, CAM, additional global clocks, and enhanced ClockLock clock circuitry. In addition, APEX 20KE devices extend the APEX 20K family to 1.5 million gates. APEX 20KE devices are denoted with an "E" suffix in the device name (e.g., the EP20K1000E device is an APEX 20KE device). Table 8 compares the features included in APEX 20K and APEX 20KE devices.

*Table 8. Comparison of APEX 20K & APEX 20KE Features*

| Feature | APEX 20K Devices | APEX 20KE Devices |
|---|---|---|
| MultiCore system integration | Full support | Full support |
| SignalTap logic analysis | Full support | Full support |
| 32/64-Bit, 33-MHz PCI | Full compliance in -1, -2 speed grades | Full compliance in -1, -2 speed grades |
| 32/64-Bit, 66-MHz PCI | - | Full compliance in -1 speed grade |
| MultiVolt I/O | 2.5-V or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected for device<br>Certain devices are 5.0-V tolerant | 1.8-V, 2.5-V, or 3.3-V $V_{CCIO}$<br>$V_{CCIO}$ selected block-by-block<br>5.0-V tolerant with use of external resistor |
| ClockLock support | Clock delay reduction<br>2× and 4× clock multiplication | Clock delay reduction<br>$m/(n \times v)$ or $m/(n \times k)$ clock multiplication<br>Drive ClockLock output off-chip<br>External clock feedback<br>ClockShift<br>LVDS support<br>Up to four PLLs<br>ClockShift, clock phase adjustment |
| Dedicated clock and input pins | Six | Eight |
| I/O standard support | 2.5-V, 3.3-V, 5.0-V I/O<br>3.3-V PCI<br>Low-voltage complementary metal-oxide semiconductor (LVCMOS)<br>Low-voltage transistor-to-transistor logic (LVTTL) | 1.8-V, 2.5-V, 3.3-V, 5.0-V I/O<br>2.5-V I/O<br>3.3-V PCI and PCI-X<br>3.3-V Advanced Graphics Port (AGP)<br>Center tap terminated (CTT)<br>GTL+<br>LVCMOS<br>LVTTL<br>True-LVDS and LVPECL data pins (in EP20K300E and larger devices)<br>LVDS and LVPECL signaling (in all BGA and FineLine BGA devices)<br>LVDS and LVPECL data pins up to 156 Mbps (in -1 speed grade devices)<br>HSTL Class I<br>PCI-X<br>SSTL-2 Class I and II<br>SSTL-3 Class I and II |
| Memory support | Dual-port RAM<br>FIFO<br>RAM<br>ROM | CAM<br>Dual-port RAM<br>FIFO<br>RAM<br>ROM |

All APEX 20K devices are reconfigurable and are 100% tested prior to shipment. As a result, test vectors do not have to be generated for fault coverage purposes. Instead, the designer can focus on simulation and design verification. In addition, the designer does not need to manage inventories of different application-specific integrated circuit (ASIC) designs; APEX 20K devices can be configured on the board for the specific functionality required.

APEX 20K devices are configured at system power-up with data stored in an Altera serial configuration device or provided by a system controller. Altera offers in-system programmability (ISP)-capable EPC1, EPC2, and EPC16 configuration devices, which configure APEX 20K devices via a serial data stream. Moreover, APEX 20K devices contain an optimized interface that permits microprocessors to configure APEX 20K devices serially or in parallel, and synchronously or asynchronously. The interface also enables microprocessors to treat APEX 20K devices as memory and configure the device by writing to a virtual memory location, making reconfiguration easy.

After an APEX 20K device has been configured, it can be reconfigured in-circuit by resetting the device and loading new data. Real-time changes can be made during system operation, enabling innovative reconfigurable computing applications.

APEX 20K devices are supported by the Altera Quartus II development system, a single, integrated package that offers HDL and schematic design entry, compilation and logic synthesis, full simulation and worst-case timing analysis, SignalTap logic analysis, and device configuration. The Quartus II software runs on Windows-based PCs, Sun SPARCstations, and HP 9000 Series 700/800 workstations.

The Quartus II software provides NativeLink interfaces to other industry-standard PC- and UNIX workstation-based EDA tools. For example, designers can invoke the Quartus II software from within third-party design tools. Further, the Quartus II software contains built-in optimized synthesis libraries; synthesis tools can use these libraries to optimize designs for APEX 20K devices. For example, the Synopsys Design Compiler library, supplied with the Quartus II development system, includes DesignWare functions optimized for the APEX 20K architecture.

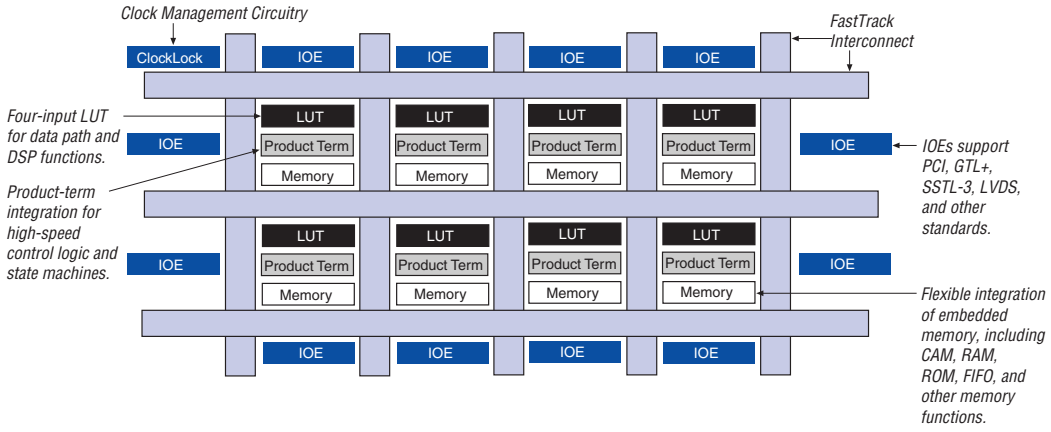
## Functional Description

APEX 20K devices incorporate LUT-based logic, product-term-based logic, and memory into one device. Signal interconnections within APEX 20K devices (as well as to and from device pins) are provided by the FastTrack® Interconnect—a series of fast, continuous row and column channels that run the entire length and width of the device.

Each I/O pin is fed by an I/O element (IOE) located at the end of each row and column of the FastTrack Interconnect. Each IOE contains a bidirectional I/O buffer and a register that can be used as either an input or output register to feed input, output, or bidirectional signals. When used with a dedicated clock pin, these registers provide exceptional performance. IOEs provide a variety of features, such as 3.3-V, 64-bit, 66-MHz PCI compliance; JTAG BST support; slew-rate control; and tri-state buffers. APEX 20KE devices offer enhanced I/O support, including support for 1.8-V I/O, 2.5-V I/O, LVCMOS, LVTTL, LVPECL, 3.3-V PCI, PCI-X, LVDS, GTL+, SSTL-2, SSTL-3, HSTL, CTT, and 3.3-V AGP I/O standards.

The ESB can implement a variety of memory functions, including CAM, RAM, dual-port RAM, ROM, and FIFO functions. Embedding the memory directly into the die improves performance and reduces die area compared to distributed-RAM implementations. Moreover, the abundance of cascadable ESBs ensures that the APEX 20K device can implement multiple wide memory blocks for high-density designs. The ESB's high speed ensures it can implement small memory blocks without any speed penalty. The abundance of ESBs ensures that designers can create as many different-sized memory blocks as the system requires. Figure 1 shows an overview of the APEX 20K device.

*Figure 1. APEX 20K Device Block Diagram*

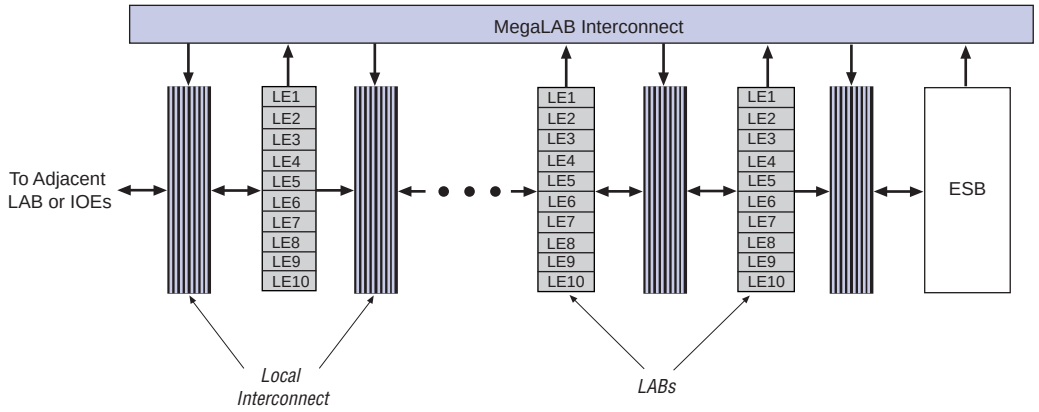


APEX 20K devices provide two dedicated clock pins and four dedicated input pins that drive register control inputs. These signals ensure efficient distribution of high-speed, low-skew control signals. These signals use dedicated routing channels to provide short delays and low skews. Four of the dedicated inputs drive four global signals. These four global signals can also be driven by internal logic, providing an ideal solution for a clock divider or internally generated asynchronous clear signals with high fan-out. The dedicated clock pins featured on the APEX 20K devices can also feed logic. The devices also feature ClockLock and ClockBoost clock management circuitry. APEX 20KE devices provide two additional dedicated clock pins, for a total of four dedicated clock pins.

## MegaLAB Structure

APEX 20K devices are constructed from a series of MegaLAB™ structures. Each MegaLAB structure contains a group of logic array blocks (LABs), one ESB, and a MegaLAB interconnect, which routes signals within the MegaLAB structure. The EP20K30E device has 10 LABs, EP20K60E through EP20K600E devices have 16 LABs, and the EP20K1000E and EP20K1500E devices have 24 LABs. Signals are routed between MegaLAB structures and I/O pins via the FastTrack Interconnect. In addition, edge LABs can be driven by I/O pins through the local interconnect. Figure 2 shows the MegaLAB structure.

*Figure 2. MegaLAB Structure*

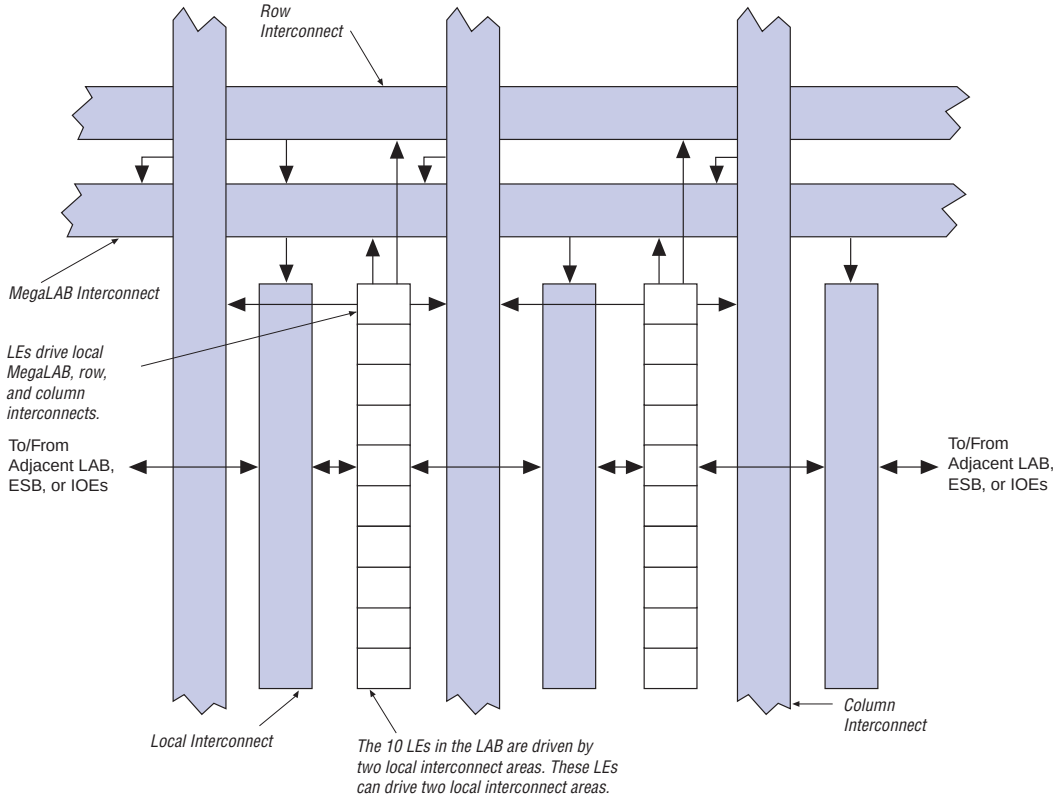


## Logic Array Block

Each LAB consists of 10 LEs, the LEs' associated carry and cascade chains, LAB control signals, and the local interconnect. The local interconnect transfers signals between LEs in the same or adjacent LABs, IOEs, or ESBs. The Quartus II Compiler places associated logic within an LAB or adjacent LABs, allowing the use of a fast local interconnect for high performance. Figure 3 shows the APEX 20K LAB.

APEX 20K devices use an interleaved LAB structure. This structure allows each LE to drive two local interconnect areas. This feature minimizes use of the MegaLAB and FastTrack interconnect, providing higher performance and flexibility. Each LE can drive 29 other LEs through the fast local interconnect.

*Figure 3. LAB Structure*



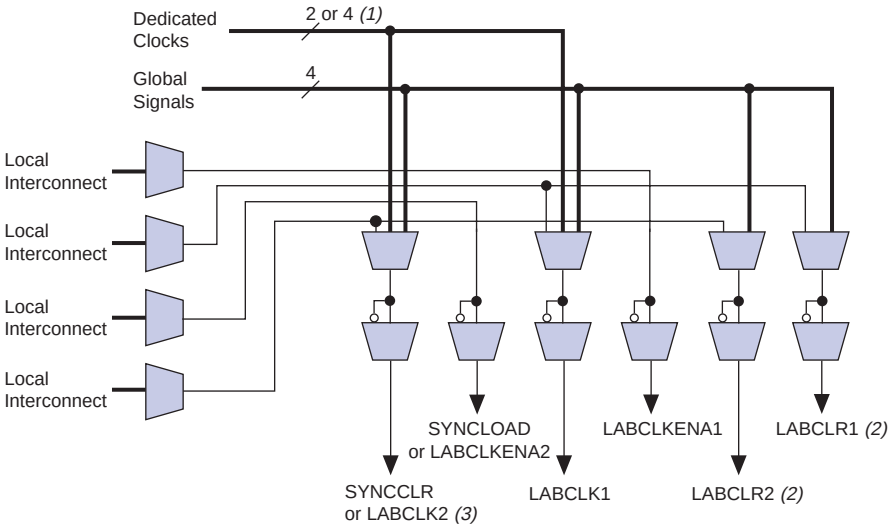
Each LAB contains dedicated logic for driving control signals to its LEs and ESBs. The control signals include clock, clock enable, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, and synchronous load signals. A maximum of six control signals can be used at a time. Although synchronous load and clear signals are generally used when implementing counters, they can also be used with other functions.

Each LAB can use two clocks and two clock enable signals. Each LAB's clock and clock enable signals are linked (e.g., any LE in a particular LAB using `CLK1` will also use `CLKENA1`). LEs with the same clock but different clock enable signals either use both clock signals in one LAB or are placed into separate LABs.

If both the rising and falling edges of a clock are used in a LAB, both LAB-wide clock signals are used.

The LAB-wide control signals can be generated from the LAB local interconnect, global signals, and dedicated clock pins. The inherent low skew of the FastTrack Interconnect enables it to be used for clock distribution. Figure 4 shows the LAB control signal generation circuit.

***Figure 4. LAB Control Signal Generation***



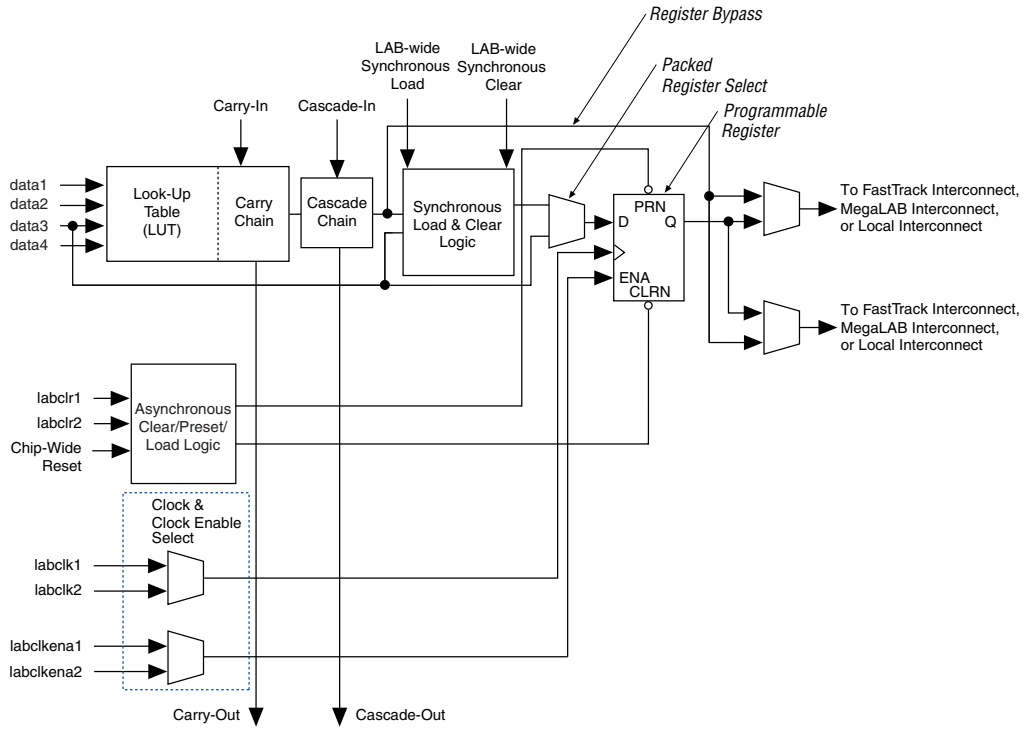

*Notes to Figure 4:*

(1) APEX 20KE devices have four dedicated clocks.
(2) The `LABCLR1` and `LABCLR2` signals also control asynchronous load and asynchronous preset for LEs within the LAB.
(3) The `SYNCCLR` signal can be generated by the local interconnect or global signals.

## Logic Element

The LE, the smallest unit of logic in the APEX 20K architecture, is compact and provides efficient logic usage. Each LE contains a four-input LUT, which is a function generator that can quickly implement any function of four variables. In addition, each LE contains a programmable register and carry and cascade chains. Each LE drives the local interconnect, MegaLAB interconnect, and FastTrack Interconnect routing structures. See Figure 5.

*Figure 5. APEX 20K Logic Element*




Each LE's programmable register can be configured for D, T, JK, or SR operation. The register's clock and clear control signals can be driven by global signals, general-purpose I/O pins, or any internal logic. For combinatorial functions, the register is bypassed and the output of the LUT drives the outputs of the LE.

Each LE has two outputs that drive the local, MegaLAB, or FastTrack Interconnect routing structure. Each output can be driven independently by the LUT's or register's output. For example, the LUT can drive one output while the register drives the other output. This feature, called register packing, improves device utilization because the register and the LUT can be used for unrelated functions. The LE can also drive out registered and unregistered versions of the LUT output.

The APEX 20K architecture provides two types of dedicated high-speed data paths that connect adjacent LEs without using local interconnect paths: carry chains and cascade chains. A carry chain supports high-speed arithmetic functions such as counters and adders, while a cascade chain implements wide-input functions such as equality comparators with minimum delay. Carry and cascade chains connect LEs 1 through 10 in an LAB and all LABs in the same MegaLAB structure.

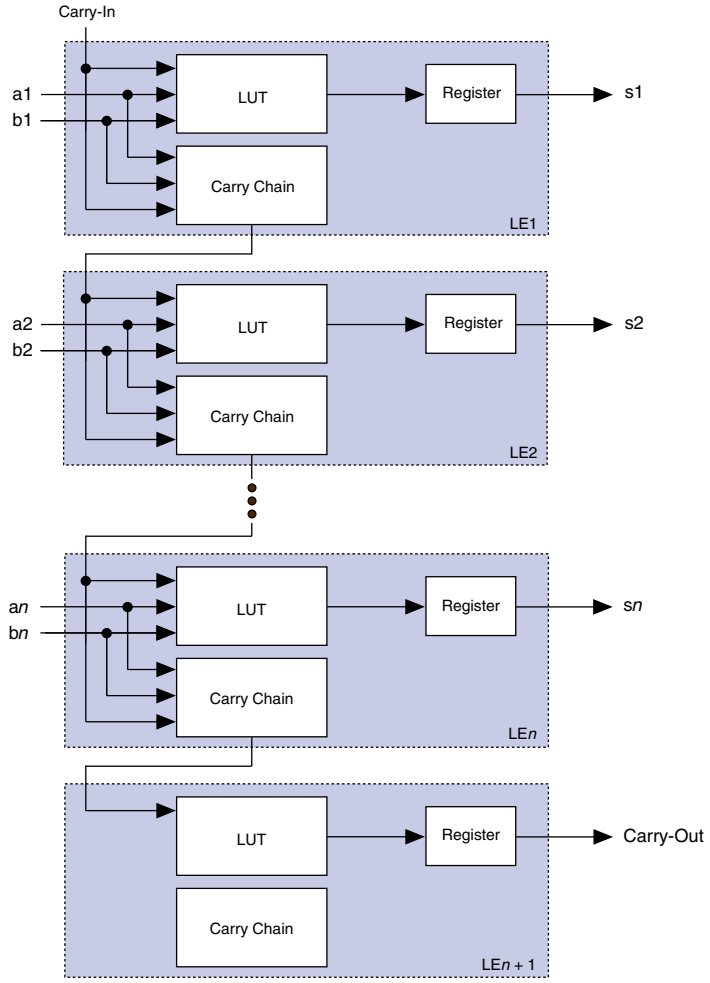
### *Carry Chain*

The carry chain provides a very fast carry-forward function between LEs. The carry-in signal from a lower-order bit drives forward into the higher-order bit via the carry chain, and feeds into both the LUT and the next portion of the carry chain. This feature allows the APEX 20K architecture to implement high-speed counters, adders, and comparators of arbitrary width. Carry chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry. Parameterized functions such as library of parameterized modules (LPM) and DesignWare functions automatically take advantage of carry chains for the appropriate functions.

The Quartus II software Compiler creates carry chains longer than ten LEs by linking LABs together automatically. For enhanced fitting, a long carry chain skips alternate LABs in a MegaLAB™ structure. A carry chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure.

Figure 6 shows how an *n*-bit full adder can be implemented in *n* + 1 LEs with the carry chain. One portion of the LUT generates the sum of two bits using the input signals and the carry-in signal; the sum is routed to the output of the LE. The register can be bypassed for simple adders or used for accumulator functions. Another portion of the LUT and the carry chain logic generates the carry-out signal, which is routed directly to the carry-in signal of the next-higher-order bit. The final carry-out signal is routed to an LE, where it is driven onto the local, MegaLAB, or FastTrack Interconnect routing structures.

*Figure 6. APEX 20K Carry Chain*

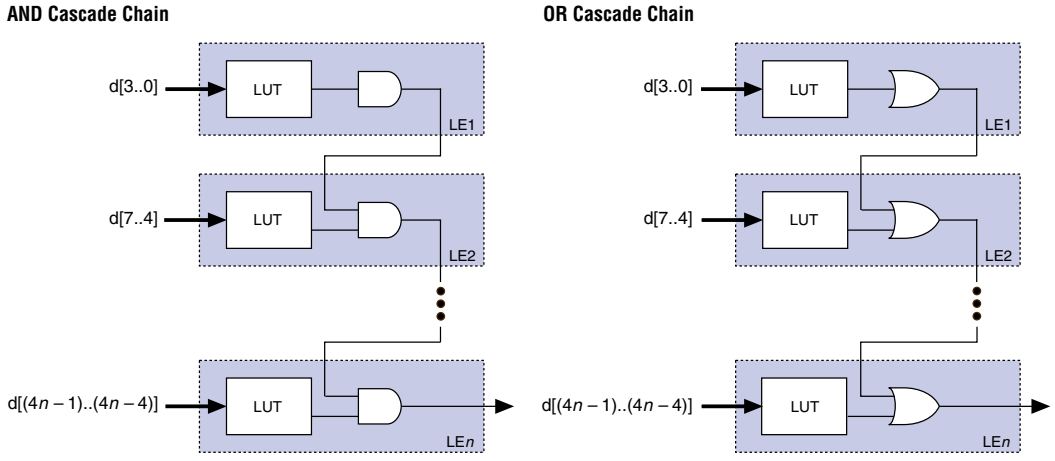


### *Cascade Chain*

With the cascade chain, the APEX 20K architecture can implement functions with a very wide fan-in. Adjacent LUTs can compute portions of a function in parallel; the cascade chain serially connects the intermediate values. The cascade chain can use a logical AND or logical OR (via De Morgan's inversion) to connect the outputs of adjacent LEs. Each additional LE provides four more inputs to the effective width of a function, with a short cascade delay. Cascade chain logic can be created automatically by the Quartus II software Compiler during design processing, or manually by the designer during design entry.

Cascade chains longer than ten LEs are implemented automatically by linking LABs together. For enhanced fitting, a long cascade chain skips alternate LABs in a MegaLAB structure. A cascade chain longer than one LAB skips either from an even-numbered LAB to the next even-numbered LAB, or from an odd-numbered LAB to the next odd-numbered LAB. For example, the last LE of the first LAB in the upper-left MegaLAB structure carries to the first LE of the third LAB in the MegaLAB structure. Figure 7 shows how the cascade function can connect adjacent LEs to form functions with a wide fan-in.

***Figure 7. APEX 20K Cascade Chain***



### *LE Operating Modes*

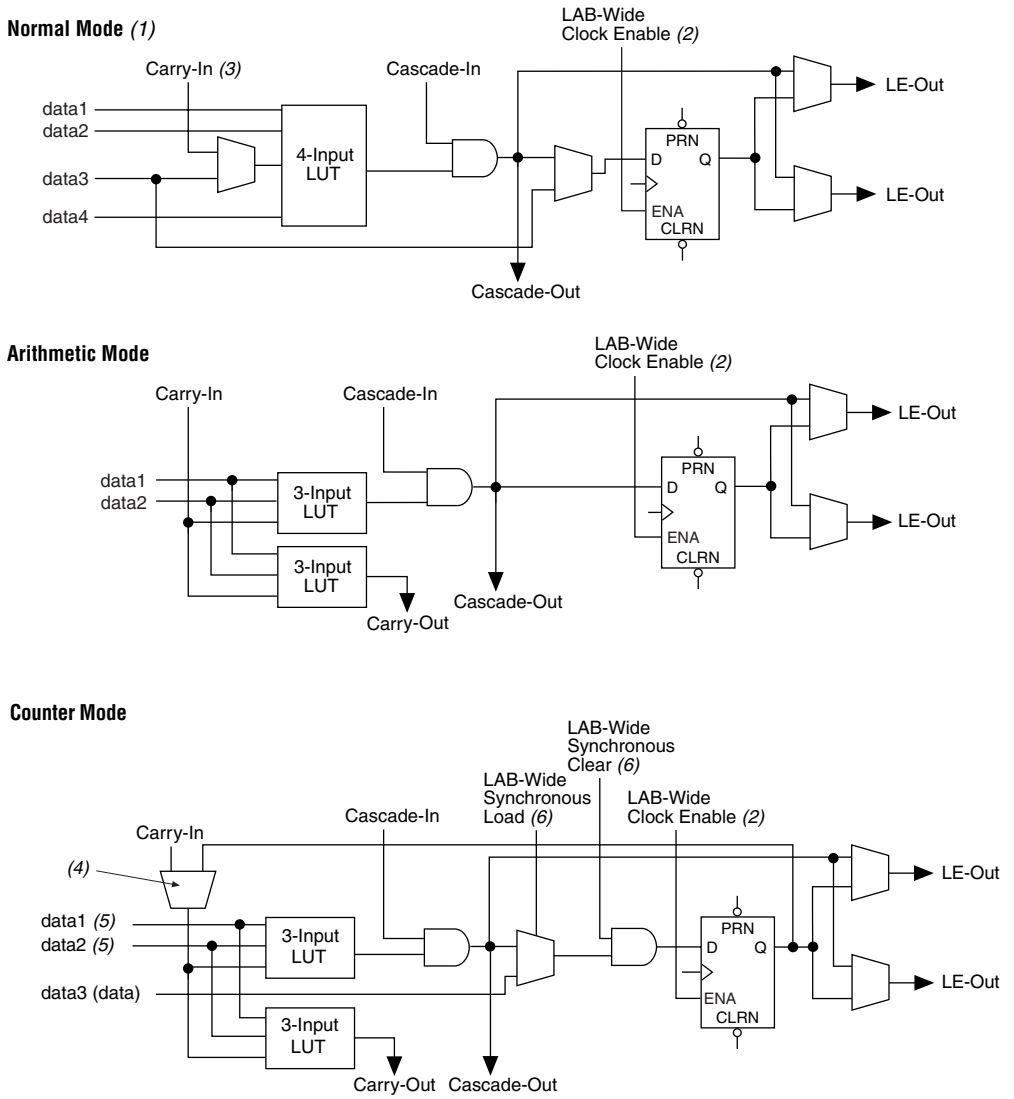
The APEX 20K LE can operate in one of the following three modes:

- Normal mode
- Arithmetic mode
- Counter mode

Each mode uses LE resources differently. In each mode, seven available inputs to the LE—the four data inputs from the LAB local interconnect, the feedback from the programmable register, and the carry-in and cascade-in from the previous LE—are directed to different destinations to implement the desired logic function. LAB-wide signals provide clock, asynchronous clear, asynchronous preset, asynchronous load, synchronous clear, synchronous load, and clock enable control for the register. These LAB-wide signals are available in all LE modes.

The Quartus II software, in conjunction with parameterized functions such as LPM and DesignWare functions, automatically chooses the appropriate mode for common functions such as counters, adders, and multipliers. If required, the designer can also create special-purpose functions that specify which LE operating mode to use for optimal performance. Figure 8 shows the LE operating modes.

*Figure 8. APEX 20K LE Operating Modes*




*Notes to Figure 8:*

(1) LEs in normal mode support register packing.
(2) There are two LAB-wide clock enables per LAB.
(3) When using the carry-in in normal mode, the packed register feature is unavailable.
(4) A register feedback multiplexer is available on LE1 of each LAB.
(5) The DATA1 and DATA2 input signals can supply counter enable, up or down control, or register feedback signals for LEs other than the second LE in an LAB.
(6) The LAB-wide synchronous clear and LAB wide synchronous load affect all registers in an LAB.

### Normal Mode

The normal mode is suitable for general logic applications, combinatorial functions, or wide decoding functions that can take advantage of a cascade chain. In normal mode, four data inputs from the LAB local interconnect and the carry-in are inputs to a four-input LUT. The Quartus II software Compiler automatically selects the carry-in or the DATA3 signal as one of the inputs to the LUT. The LUT output can be combined with the cascade-in signal to form a cascade chain through the cascade-out signal. LEs in normal mode support packed registers.

### Arithmetic Mode

The arithmetic mode is ideal for implementing adders, accumulators, and comparators. An LE in arithmetic mode uses two 3-input LUTs. One LUT computes a three-input function; the other generates a carry output. As shown in Figure 8, the first LUT uses the carry-in signal and two data inputs from the LAB local interconnect to generate a combinatorial or registered output. For example, when implementing an adder, this output is the sum of three signals: DATA1, DATA2, and carry-in. The second LUT uses the same three signals to generate a carry-out signal, thereby creating a carry chain. The arithmetic mode also supports simultaneous use of the cascade chain. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

The Quartus II software implements parameterized functions that use the arithmetic mode automatically where appropriate; the designer does not need to specify how the carry chain will be used.

### Counter Mode

The counter mode offers clock enable, counter enable, synchronous up/down control, synchronous clear, and synchronous load options. The counter enable and synchronous up/down control signals are generated from the data inputs of the LAB local interconnect. The synchronous clear and synchronous load options are LAB-wide signals that affect all registers in the LAB. Consequently, if any of the LEs in an LAB use the counter mode, other LEs in that LAB must be used as part of the same counter or be used for a combinatorial function. The Quartus II software automatically places any registers that are not used by the counter into other LABs.

The counter mode uses two three-input LUTs: one generates the counter data, and the other generates the fast carry bit. A 2-to-1 multiplexer provides synchronous loading, and another AND gate provides synchronous clearing. If the cascade function is used by an LE in counter mode, the synchronous clear or load overrides any signal carried on the cascade chain. The synchronous clear overrides the synchronous load. LEs in arithmetic mode can drive out registered and unregistered versions of the LUT output.

### *Clear & Preset Logic Control*

Logic for the register's clear and preset signals is controlled by LAB-wide signals. The LE directly supports an asynchronous clear function. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Moreover, the Quartus II software Compiler can use a programmable NOT-gate push-back technique to emulate simultaneous preset and clear or asynchronous load. However, this technique uses three additional LEs per register. All emulation is performed automatically when the design is compiled. Registers that emulate simultaneous preset and load will enter an unknown state upon power-up or when the chip-wide reset is asserted.

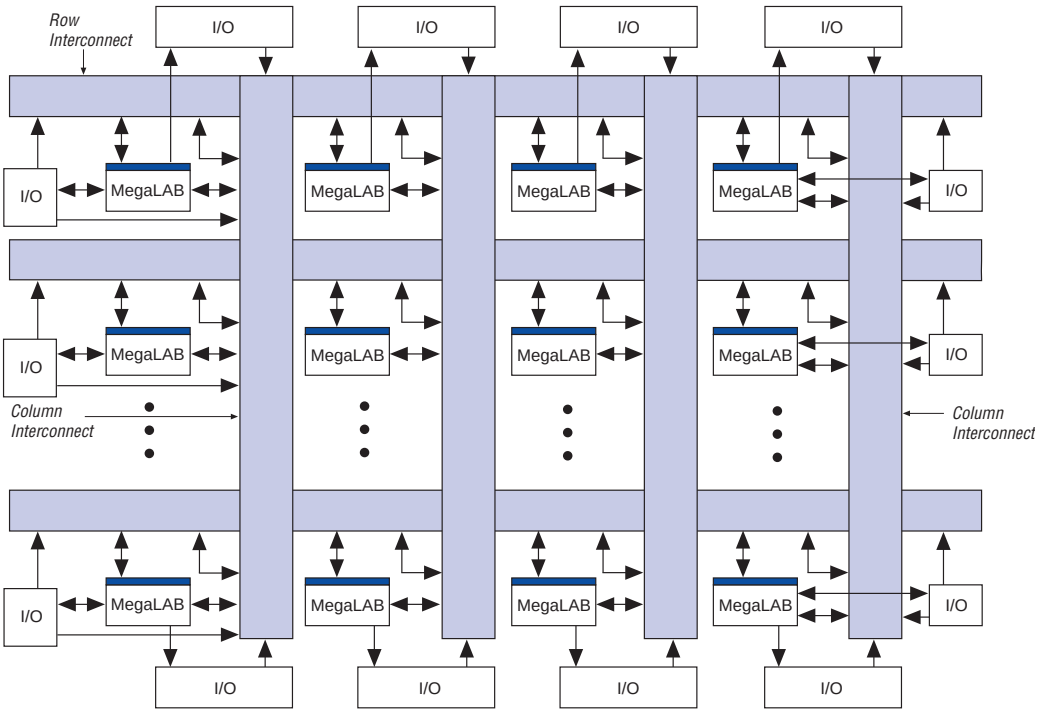
In addition to the two clear and preset modes, APEX 20K devices provide a chip-wide reset pin (DEV_CLRn) that resets all registers in the device. Use of this pin is controlled through an option in the Quartus II software that is set before compilation. The chip-wide reset overrides all other control signals. Registers using an asynchronous preset are preset when the chip-wide reset is asserted; this effect results from the inversion technique used to implement the asynchronous preset.

## FastTrack Interconnect

In the APEX 20K architecture, connections between LEs, ESBs, and I/O pins are provided by the FastTrack Interconnect. The FastTrack Interconnect is a series of continuous horizontal and vertical routing channels that traverse the device. This global routing structure provides predictable performance, even in complex designs. In contrast, the segmented routing in FPGAs requires switch matrices to connect a variable number of routing paths, increasing the delays between logic resources and reducing performance.

The FastTrack Interconnect consists of row and column interconnect channels that span the entire device. The row interconnect routes signals throughout a row of MegaLAB structures; the column interconnect routes signals throughout a column of MegaLAB structures. When using the row and column interconnect, an LE, IOE, or ESB can drive any other LE, IOE, or ESB in a device. See Figure 9.

*Figure 9. APEX 20K Interconnect Structure*




A row line can be driven directly by LEs, IOEs, or ESBs in that row. Further, a column line can drive a row line, allowing an LE, IOE, or ESB to drive elements in a different row via the column and row interconnect. The row interconnect drives the MegaLAB interconnect to drive LEs, IOEs, or ESBs in a particular MegaLAB structure.

A column line can be directly driven by LEs, IOEs, or ESBs in that column. A column line on a device's left or right edge can also be driven by row IOEs. The column line is used to route signals from one row to another. A column line can drive a row line; it can also drive the MegaLAB interconnect directly, allowing faster connections between rows.

Figure 10 shows how the FastTrack Interconnect uses the local interconnect to drive LEs within MegaLAB structures.

*Figure 10. FastTrack Connection to Local Interconnect*

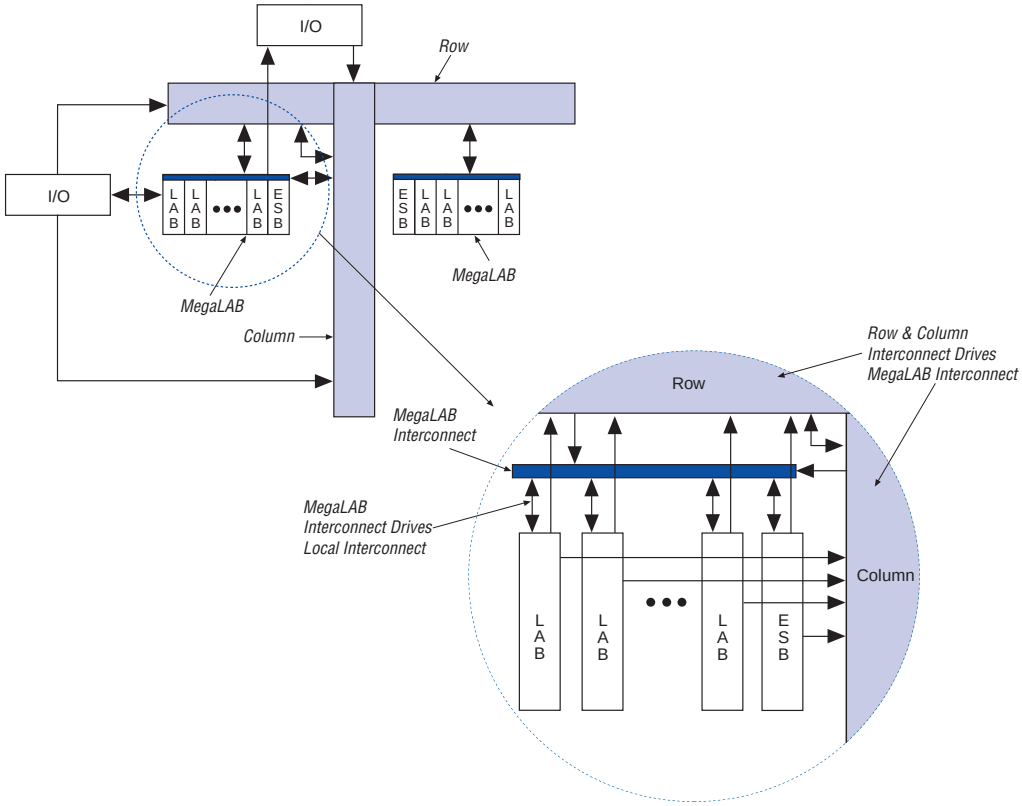
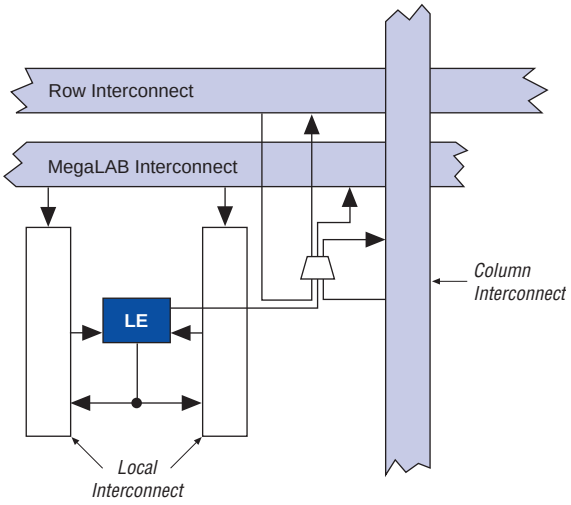


Figure 11 shows the intersection of a row and column interconnect, and how these forms of interconnects and LEs drive each other.

*Figure 11. Driving the FastTrack Interconnect*




APEX 20KE devices include an enhanced interconnect structure for faster routing of input signals with high fan-out. Column I/O pins can drive the FastRow™ interconnect, which routes signals directly into the local interconnect without having to drive through the MegaLAB interconnect. FastRow lines traverse two MegaLAB structures. Also, these pins can drive the local interconnect directly for fast setup times. On EP20K300E and larger devices, the FastRow interconnect drives the two MegaLABs in the top left corner, the two MegaLABs in the top right corner, the two MegaLABS in the bottom left corner, and the two MegaLABs in the bottom right corner. On EP20K200E and smaller devices, FastRow interconnect drives the two MegaLABs on the top and the two MegaLABs on the bottom of the device. On all devices, the FastRow interconnect drives all local interconnect in the appropriate MegaLABs except the local interconnect on the side of the MegaLAB opposite the ESB. Pins using the FastRow interconnect achieve a faster set-up time, as the signal does not need to use a MegaLAB interconnect line to reach the destination LE. Figure 12 shows the FastRow interconnect.

*Figure 12. APEX 20KE FastRow Interconnect*

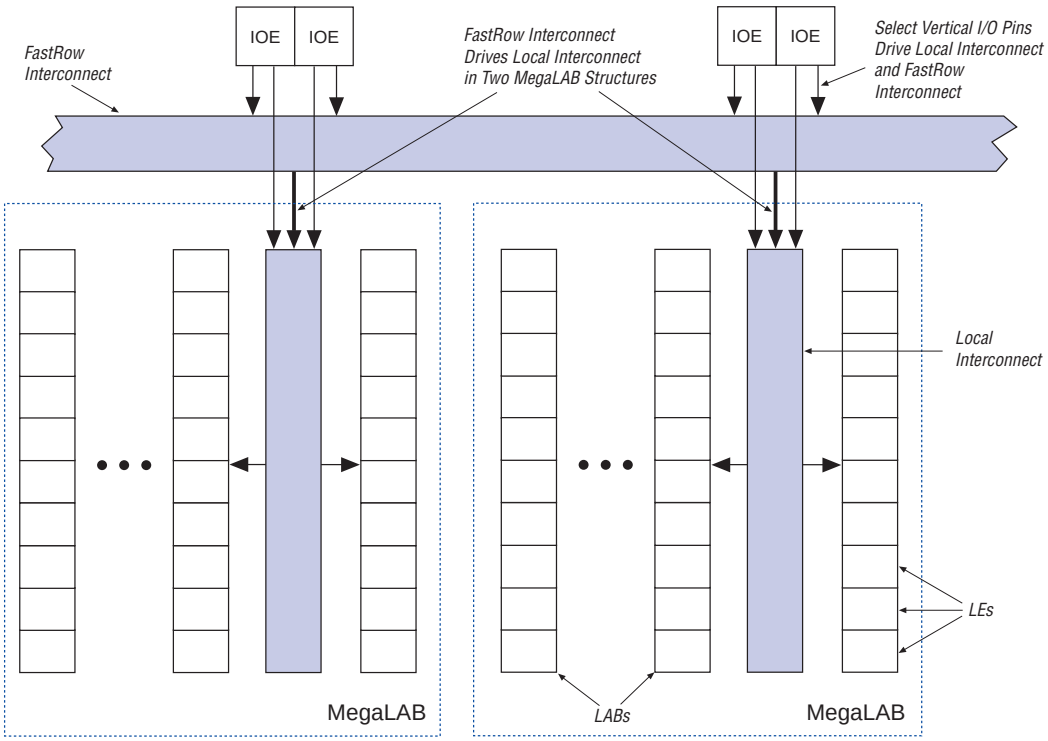



Table 9 summarizes how various elements of the APEX 20K architecture drive each other.

*Table 9. APEX 20K Routing Scheme*

| Source | Destination | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | Row I/O Pin | Column I/O Pin | LE | ESB | Local Interconnect | MegaLAB Interconnect | Row FastTrack Interconnect | Column FastTrack Interconnect | FastRow Interconnect |
| Row I/O Pin | | | | | ✓ | ✓ | ✓ | ✓ | |
| Column I/O Pin | | | | | | | | ✓ | ✓ (1) |
| LE | | | | | ✓ | ✓ | ✓ | ✓ | |
| ESB | | | | | ✓ | ✓ | ✓ | ✓ | |
| Local Interconnect | ✓ | ✓ | ✓ | ✓ | | | | | |
| MegaLAB Interconnect | | | | | ✓ | | | | |
| Row FastTrack Interconnect | | | | | | ✓ | | ✓ | |
| Column FastTrack Interconnect | | | | | | ✓ | ✓ | | |
| FastRow Interconnect | | | | | ✓ (1) | | | | |

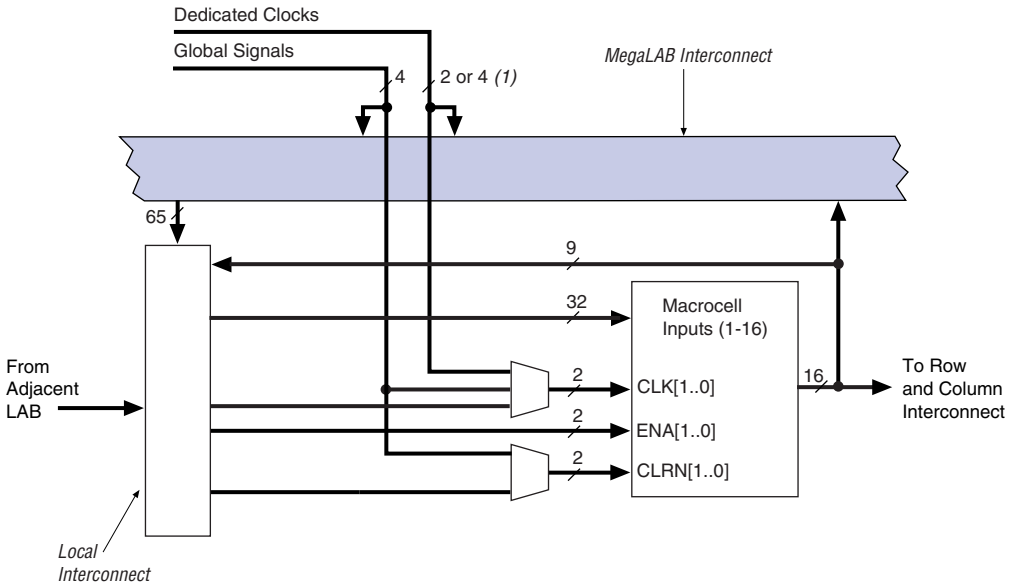
*Note to Table 9:*
(1) This connection is supported in APEX 20KE devices only.

## Product-Term Logic

The product-term portion of the MultiCore architecture is implemented with the ESB. The ESB can be configured to act as a block of macrocells on an ESB-by-ESB basis. Each ESB is fed by 32 inputs from the adjacent local interconnect; therefore, it can be driven by the MegaLAB interconnect or the adjacent LAB. Also, nine ESB macrocells feed back into the ESB through the local interconnect for higher performance. Dedicated clock pins, global signals, and additional inputs from the local interconnect drive the ESB control signals.

In product-term mode, each ESB contains 16 macrocells. Each macrocell consists of two product terms and a programmable register. Figure 13 shows the ESB in product-term mode.

*Figure 13. Product-Term Logic in ESB*



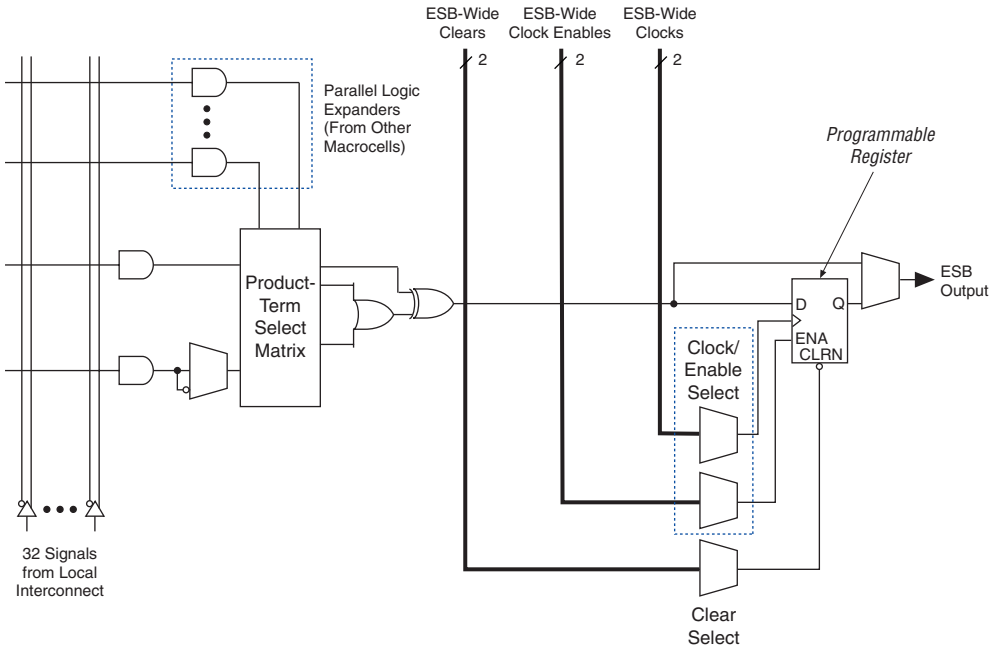

*Note to Figure 13:*
(1) APEX 20KE devices have four dedicated clocks.

### *Macrocells*

APEX 20K macrocells can be configured individually for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term select matrix, and the programmable register.

Combinatorial logic is implemented in the product terms. The product-term select matrix allocates these product terms for use as either primary logic inputs (to the OR and XOR gates) to implement combinatorial functions, or as parallel expanders to be used to increase the logic available to another macrocell. One product term can be inverted; the Quartus II software uses this feature to perform DeMorgan's inversion for more efficient implementation of wide OR functions. The Quartus II software Compiler can use a NOT-gate push-back technique to emulate an asynchronous preset. Figure 14 shows the APEX 20K macrocell.

*Figure 14. APEX 20K Macrocell*



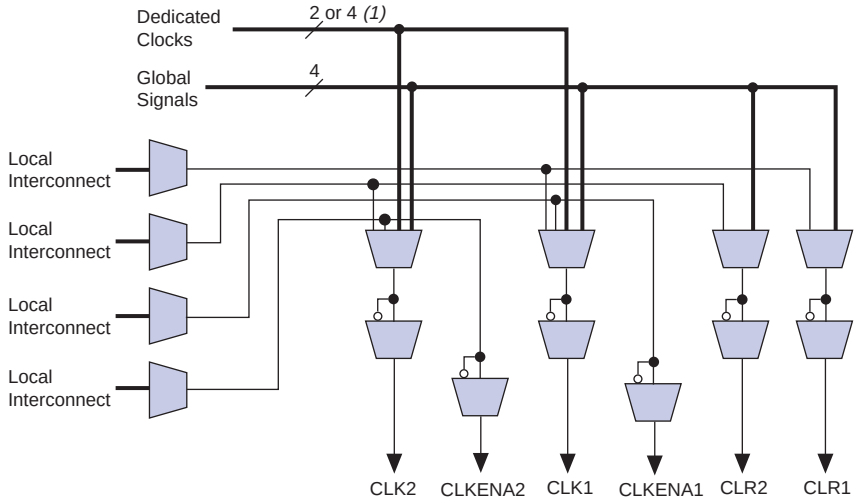

For registered functions, each macrocell register can be programmed individually to implement D, T, JK, or SR operation with programmable clock control. The register can be bypassed for combinatorial operation. During design entry, the designer specifies the desired register type; the Quartus II software then selects the most efficient register operation for each registered function to optimize resource utilization. The Quartus II software or other synthesis tools can also select the most efficient register operation automatically when synthesizing HDL designs.

Each programmable register can be clocked by one of two ESB-wide clocks. The ESB-wide clocks can be generated from device dedicated clock pins, global signals, or local interconnect. Each clock also has an associated clock enable, generated from the local interconnect. The clock and clock enable signals are related for a particular ESB; any macrocell using a clock also uses the associated clock enable.

If both the rising and falling edges of a clock are used in an ESB, both ESB-wide clock signals are used.

The programmable register also supports an asynchronous clear function. Within the ESB, two asynchronous clears are generated from global signals and the local interconnect. Each macrocell can either choose between the two asynchronous clear signals or choose to not be cleared. Either of the two clear signals can be inverted within the ESB. Figure 15 shows the ESB control logic when implementing product-terms.

*Figure 15. ESB Product-Term Mode Control Logic*



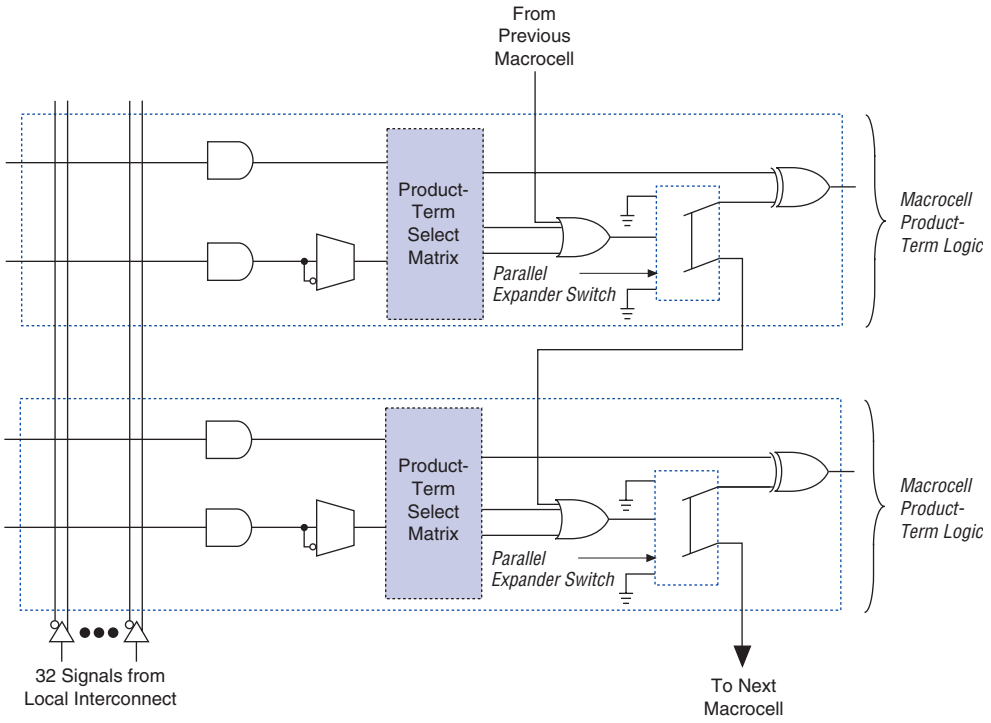

*Note to Figure 15:*
(1) APEX 20KE devices have four dedicated clocks.

### *Parallel Expanders*

Parallel expanders are unused product terms that can be allocated to a neighboring macrocell to implement fast, complex logic functions. Parallel expanders allow up to 32 product terms to feed the macrocell OR logic directly, with two product terms provided by the macrocell and 30 parallel expanders provided by the neighboring macrocells in the ESB.

The Quartus II software Compiler can allocate up to 15 sets of up to two parallel expanders per set to the macrocells automatically. Each set of two parallel expanders incurs a small, incremental timing delay. Figure 16 shows the APEX 20K parallel expanders.

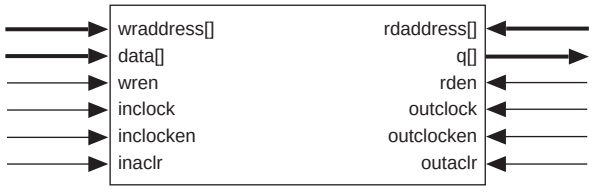
*Figure 16. APEX 20K Parallel Expanders*




## Embedded System Block

The ESB can implement various types of memory blocks, including dual-port RAM, ROM, FIFO, and CAM blocks. The ESB includes input and output registers; the input registers synchronize writes, and the output registers can pipeline designs to improve system performance. The ESB offers a dual-port mode, which supports simultaneous reads and writes at two different clock frequencies. Figure 17 shows the ESB block diagram.

*Figure 17. ESB Block Diagram*



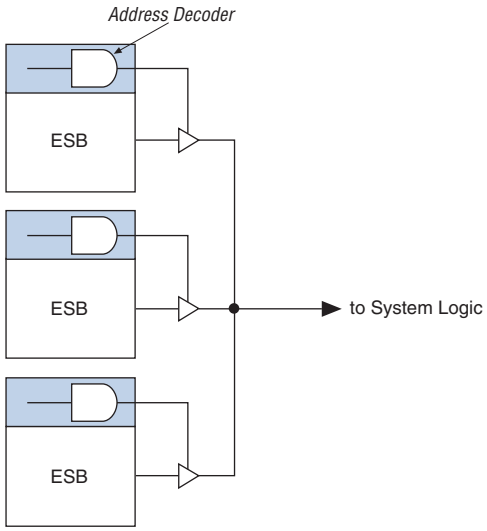
ESBs can implement synchronous RAM, which is easier to use than asynchronous RAM. A circuit using asynchronous RAM must generate the RAM write enable (WE) signal, while ensuring that its data and address signals meet setup and hold time specifications relative to the WE signal. In contrast, the ESB's synchronous RAM generates its own WE signal and is self-timed with respect to the global clock. Circuits using the ESB's self-timed RAM must only meet the setup and hold time specifications of the global clock.

ESB inputs are driven by the adjacent local interconnect, which in turn can be driven by the MegaLAB or FastTrack Interconnect. Because the ESB can be driven by the local interconnect, an adjacent LE can drive it directly for fast memory access. ESB outputs drive the MegaLAB and FastTrack Interconnect. In addition, ten ESB outputs, nine of which are unique output lines, drive the local interconnect for fast connection to adjacent LEs or for fast feedback product-term logic.

When implementing memory, each ESB can be configured in any of the following sizes: 128 × 16, 256 × 8, 512 × 4, 1,024 × 2, or 2,048 × 1. By combining multiple ESBs, the Quartus II software implements larger memory blocks automatically. For example, two 128 × 16 RAM blocks can be combined to form a 128 × 32 RAM block, and two 512 × 4 RAM blocks can be combined to form a 512 × 8 RAM block. Memory performance does not degrade for memory blocks up to 2,048 words deep. Each ESB can implement a 2,048-word-deep memory; the ESBs are used in parallel, eliminating the need for any external control logic and its associated delays.

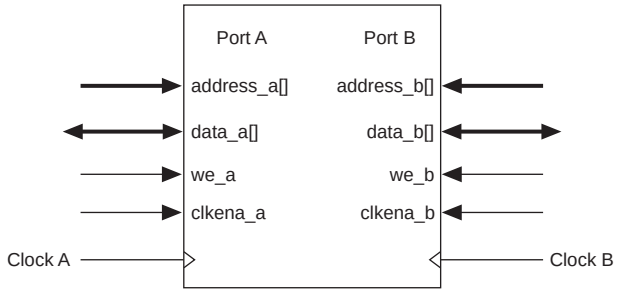
To create a high-speed memory block that is more than 2,048 words deep, ESBs drive tri-state lines. Each tri-state line connects all ESBs in a column of MegaLAB structures, and drives the MegaLAB interconnect and row and column FastTrack Interconnect throughout the column. Each ESB incorporates a programmable decoder to activate the tri-state driver appropriately. For instance, to implement 8,192-word-deep memory, four ESBs are used. Eleven address lines drive the ESB memory, and two more drive the tri-state decoder. Depending on which 2,048-word memory page is selected, the appropriate ESB driver is turned on, driving the output to the tri-state line. The Quartus II software automatically combines ESBs with tri-state lines to form deeper memory blocks. The internal tri-state control logic is designed to avoid internal contention and floating lines. See Figure 18.

*Figure 18. Deep Memory Block Implemented with Multiple ESBs*




The ESB implements two forms of dual-port memory: read/write clock mode and input/output clock mode. The ESB can also be used for bidirectional, dual-port memory applications in which two ports read or write simultaneously. To implement this type of dual-port memory, two or four ESBs are used to support two simultaneous reads or writes. This functionality is shown in Figure 19.

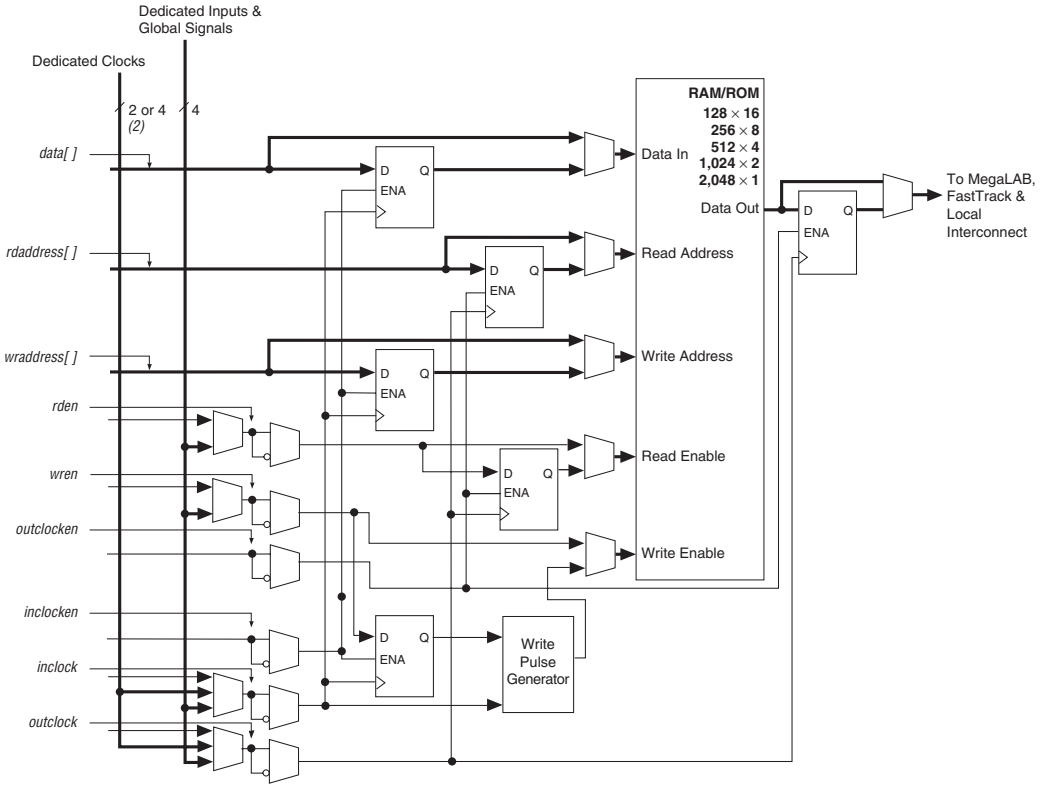
*Figure 19. APEX 20K ESB Implementing Dual-Port RAM*



## Read/Write Clock Mode

The read/write clock mode contains two clocks. One clock controls all registers associated with writing: data input, WE, and write address. The other clock controls all registers associated with reading: read enable (RE), read address, and data output. The ESB also supports clock enable and asynchronous clear signals; these signals also control the read and write registers independently. Read/write clock mode is commonly used for applications where reads and writes occur at different system frequencies. Figure 20 shows the ESB in read/write clock mode.

***Figure 20. ESB in Read/Write Clock Mode*** *Note (1)*

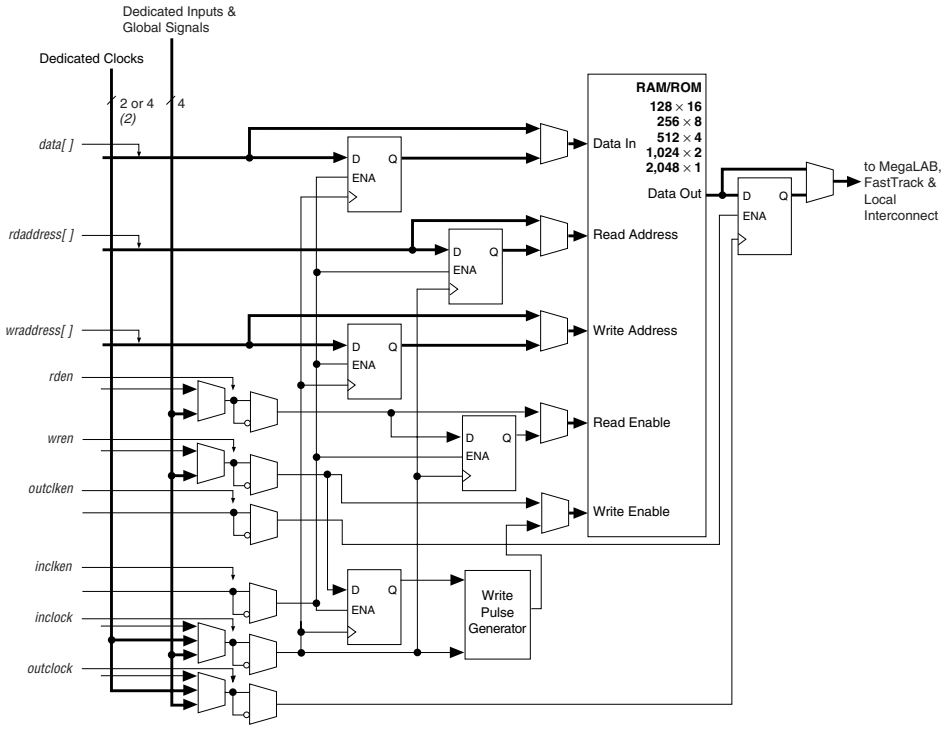



*Notes to Figure 20:*
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Input/Output Clock Mode

The input/output clock mode contains two clocks. One clock controls all registers for inputs into the ESB: data input, WE, RE, read address, and write address. The other clock controls the ESB data output registers. The ESB also supports clock enable and asynchronous clear signals; these signals also control the reading and writing of registers independently. Input/output clock mode is commonly used for applications where the reads and writes occur at the same system frequency, but require different clock enable signals for the input and output registers. Figure 21 shows the ESB in input/output clock mode.

***Figure 21. ESB in Input/Output Clock Mode*** *Note (1)*

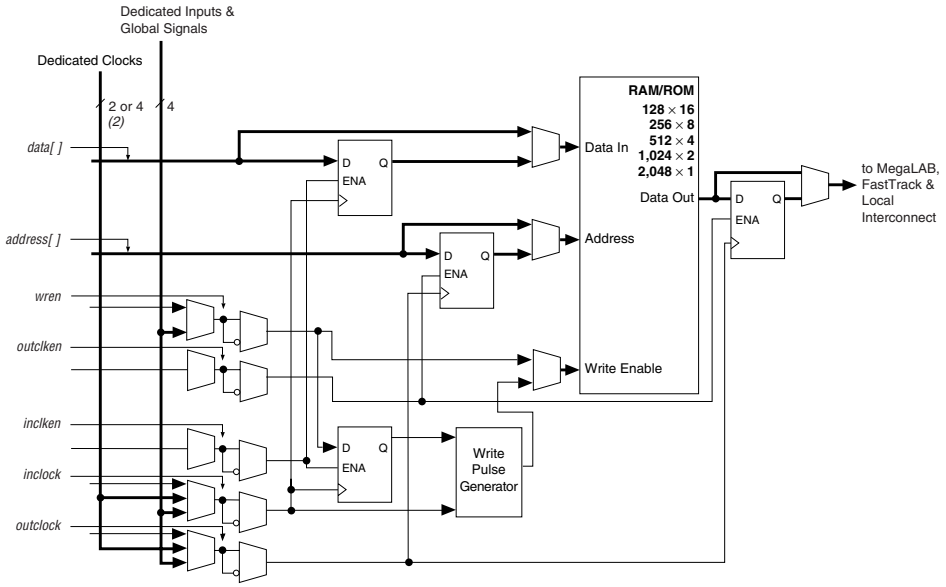



*Notes to Figure 21:*
(1) All registers can be cleared asynchronously by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Single-Port Mode

The APEX 20K ESB also supports a single-port mode, which is used when simultaneous reads and writes are not required. See Figure 22.

***Figure 22. ESB in Single-Port Mode*** *Note (1)*




*Notes to Figure 22:*

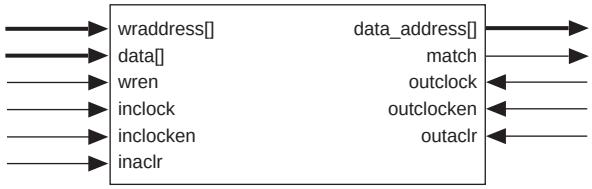
(1) All registers can be asynchronously cleared by ESB local interconnect signals, global signals, or the chip-wide reset.
(2) APEX 20KE devices have four dedicated clocks.

## Content-Addressable Memory

In APEX 20KE devices, the ESB can implement CAM. CAM can be thought of as the inverse of RAM. When read, RAM outputs the data for a given address. Conversely, CAM outputs an address for a given data word. For example, if the data `FA12` is stored in address `14`, the CAM outputs `14` when `FA12` is driven into it.

CAM is used for high-speed search operations. When searching for data within a RAM block, the search is performed serially. Thus, finding a particular data word can take many cycles. CAM searches all addresses in parallel and outputs the address storing a particular word. When a match is found, a match flag is set high. Figure 23 shows the CAM block diagram.

*Figure 23. APEX 20KE CAM Block Diagram*




CAM can be used in any application requiring high-speed searches, such as networking, communications, data compression, and cache management.

The APEX 20KE on-chip CAM provides faster system performance than traditional discrete CAM. Integrating CAM and logic into the APEX 20KE device eliminates off-chip and on-chip delays, improving system performance.

When in CAM mode, the ESB implements 32-word, 32-bit CAM. Wider or deeper CAM can be implemented by combining multiple CAMs with some ancillary logic implemented in LEs. The Quartus II software combines ESBs and LEs automatically to create larger CAMs.

CAM supports writing "don't care" bits into words of the memory. The "don't-care" bit can be used as a mask for CAM comparisons; any bit set to "don't-care" has no effect on matches.

The output of the CAM can be encoded or unencoded. When encoded, the ESB outputs an encoded address of the data's location. For instance, if the data is located in address `12`, the ESB output is `12`. When unencoded, the ESB uses its 16 outputs to show the location of the data over two clock cycles. In this case, if the data is located in address `12`, the 12th output line goes high. When using unencoded outputs, two clock cycles are required to read the output because a 16-bit output bus is used to show the status of 32 words.

The encoded output is better suited for designs that ensure duplicate data is not written into the CAM. If duplicate data is written into two locations, the CAM's output will be incorrect. If the CAM may contain duplicate data, the unencoded output is a better solution; CAM with unencoded outputs can distinguish multiple data locations.

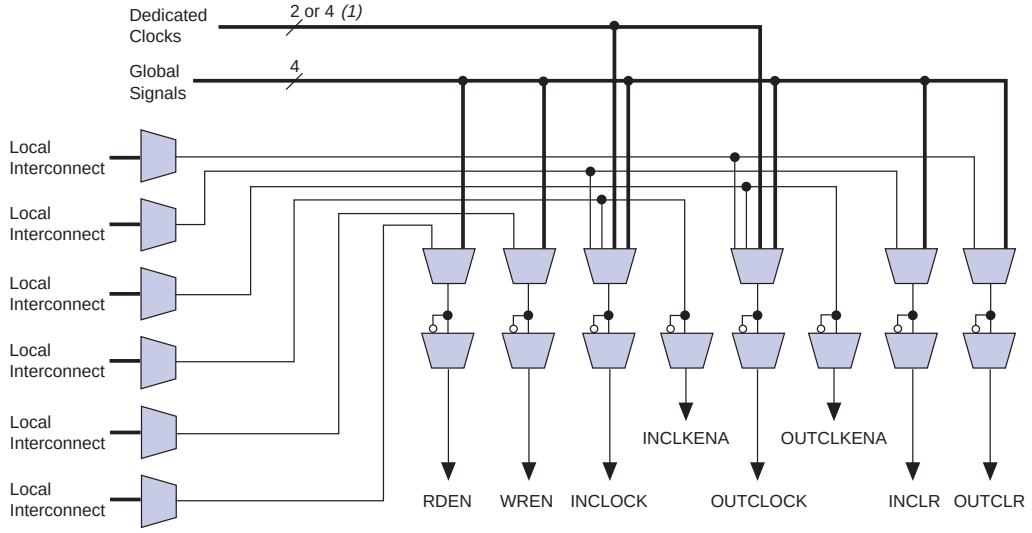
CAM can be pre-loaded with data during configuration, or it can be written during system operation. In most cases, two clock cycles are required to write each word into CAM. When "don't-care" bits are used, a third clock cycle is required.

For more information on APEX 20KE devices and CAM, see *Application Note 119 (Implementing High-Speed Search Applications with APEX CAM).*

## Driving Signals to the ESB

ESBs provide flexible options for driving control signals. Different clocks can be used for the ESB inputs and outputs. Registers can be inserted independently on the data input, data output, read address, write address, WE, and RE signals. The global signals and the local interconnect can drive the WE and RE signals. The global signals, dedicated clock pins, and local interconnect can drive the ESB clock signals. Because the LEs drive the local interconnect, the LEs can control the WE and RE signals and the ESB clock, clock enable, and asynchronous clear signals. Figure 24 shows the ESB control signal generation logic.

***Figure 24. ESB Control Signal Generation***




***Note to Figure 24:***
(1) APEX 20KE devices have four dedicated clocks.

An ESB is fed by the local interconnect, which is driven by adjacent LEs (for high-speed connection to the ESB) or the MegaLAB interconnect. The ESB can drive the local, MegaLAB, or FastTrack Interconnect routing structure to drive LEs and IOEs in the same MegaLAB structure or anywhere in the device.

### Implementing Logic in ROM

In addition to implementing logic with product terms, the ESB can implement logic functions when it is programmed with a read-only pattern during configuration, creating a large LUT. With LUTs, combinatorial functions are implemented by looking up the results, rather than by computing them. This implementation of combinatorial functions can be faster than using algorithms implemented in general logic, a performance advantage that is further enhanced by the fast access times of ESBs. The large capacity of ESBs enables designers to implement complex functions in one logic level without the routing delays associated with linked LEs or distributed RAM blocks. Parameterized functions such as LPM functions can take advantage of the ESB automatically. Further, the Quartus II software can implement portions of a design with ESBs where appropriate.

### Programmable Speed/Power Control

APEX 20K ESBs offer a high-speed mode that supports very fast operation on an ESB-by-ESB basis. When high speed is not required, this feature can be turned off to reduce the ESB's power dissipation by up to 50%. ESBs that run at low power incur a nominal timing delay adder. This Turbo Bit™ option is available for ESBs that implement product-term logic or memory functions. An ESB that is not used will be powered down so that it does not consume DC current.

Designers can program each ESB in the APEX 20K device for either high-speed or low-power operation. As a result, speed-critical paths in the design can run at high speed, while the remaining paths operate at reduced power.

## I/O Structure

The APEX 20K IOE contains a bidirectional I/O buffer and a register that can be used either as an input register for external data requiring fast setup times, or as an output register for data requiring fast clock-to-output performance. IOEs can be used as input, output, or bidirectional pins. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The Quartus II software Compiler uses the programmable inversion option to invert signals from the row and column interconnect automatically where appropriate. Because the APEX 20K IOE offers one output enable per pin, the Quartus II software Compiler can emulate open-drain operation efficiently.

The APEX 20K IOE includes programmable delays that can be activated to ensure zero hold times, minimum clock-to-output times, input IOE register-to-core register transfers, or core-to-output IOE register transfers. A path in which a pin directly drives a register may require the delay to ensure zero hold time, whereas a path in which a pin drives a register through combinatorial logic may not require the delay.

Table 10 describes the APEX 20K programmable delays and their logic options in the Quartus II software.

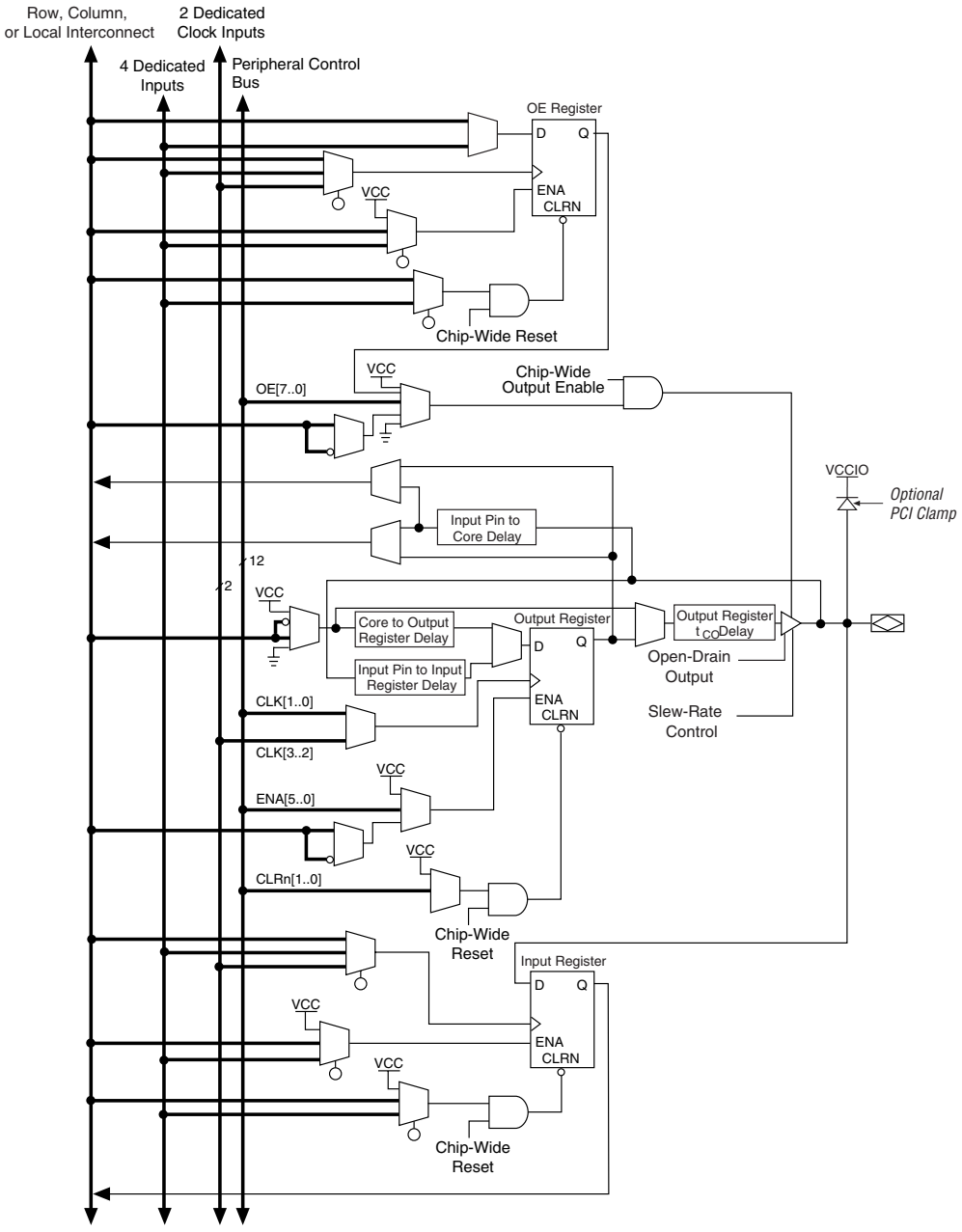
*Table 10. APEX 20K Programmable Delay Chains*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input pin to core delay | Decrease input delay to internal cells |
| Input pin to input register delay | Decrease input delay to input register |
| Core to output register delay | Decrease input delay to output register |
| Output register $t_{CO}$ delay | Increase delay to output pin |

The Quartus II software compiler can program these delays automatically to minimize setup time while providing a zero hold time. Figure 25 shows how fast bidirectional I/Os are implemented in APEX 20K devices.

The register in the APEX 20K IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, the register cannot be asynchronously cleared or preset. This feature is useful for cases where the APEX 20K device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

***Figure 25. APEX 20K Bidirectional I/O Registers*** *Note (1)*




*Note to Figure 25:*

(1) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

APEX 20KE devices include an enhanced IOE, which drives the FastRow interconnect. The FastRow interconnect connects a column I/O pin directly to the LAB local interconnect within two MegaLAB structures. This feature provides fast setup times for pins that drive high fan-outs with complex logic, such as PCI designs. For fast bidirectional I/O timing, LE registers using local routing can improve setup times and OE timing. The APEX 20KE IOE also includes direct support for open-drain operation, giving faster clock-to-output for open-drain signals. Some programmable delays in the APEX 20KE IOE offer multiple levels of delay to fine-tune setup and hold time requirements. The Quartus II software compiler can set these delays automatically to minimize setup time while providing a zero hold time.

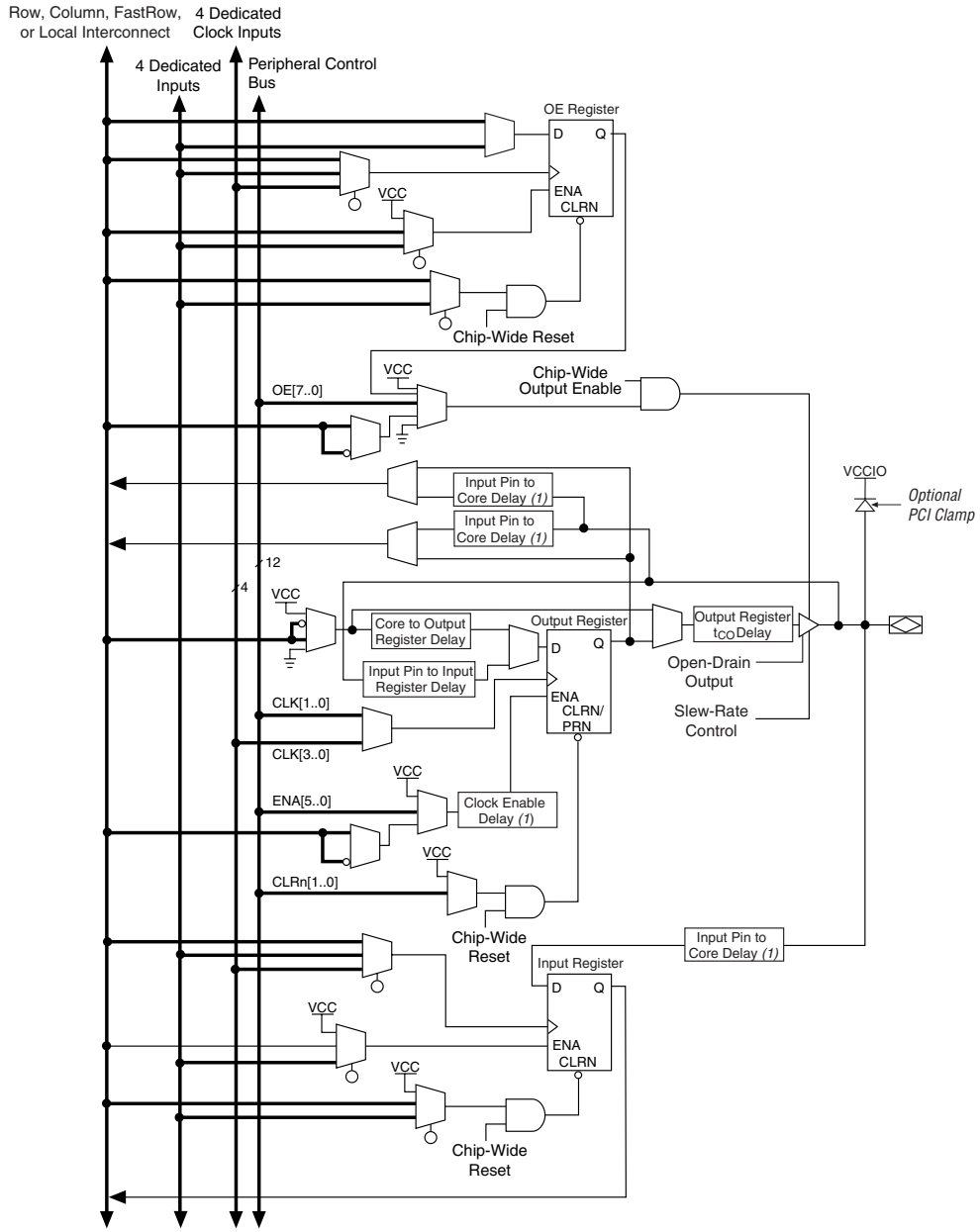
Table 11 describes the APEX 20KE programmable delays and their logic options in the Quartus II software.

*Table 11. APEX 20KE Programmable Delay Chains*

| Programmable Delays | Quartus II Logic Option |
|---|---|
| Input Pin to Core Delay | Decrease input delay to internal cells |
| Input Pin to Input Register Delay | Decrease input delay to input registers |
| Core to Output Register Delay | Decrease input delay to output register |
| Output Register $t_{CO}$ Delay | Increase delay to output pin |
| Clock Enable Delay | Increase clock enable delay |

The register in the APEX 20KE IOE can be programmed to power-up high or low after configuration is complete. If it is programmed to power-up low, an asynchronous clear can control the register. If it is programmed to power-up high, an asynchronous preset can control the register. Figure 26 shows how fast bidirectional I/O pins are implemented in APEX 20KE devices. This feature is useful for cases where the APEX 20KE device controls an active-low input or another device; it prevents inadvertent activation of the input upon power-up.

***Figure 26. APEX 20KE Bidirectional I/O Registers*** *Notes (1), (2)*




*Notes to Figure 26:*

(1) This programmable delay has four settings: off and three levels of delay.

(2) The output enable and input registers are LE registers in the LAB adjacent to the bidirectional pin.

Each IOE drives a row, column, MegaLAB, or local interconnect when used as an input or bidirectional pin. A row IOE can drive a local, MegaLAB, row, and column interconnect; a column IOE can drive the column interconnect. Figure 27 shows how a row IOE connects to the interconnect.

*Figure 27. Row IOE Connection to the Interconnect*

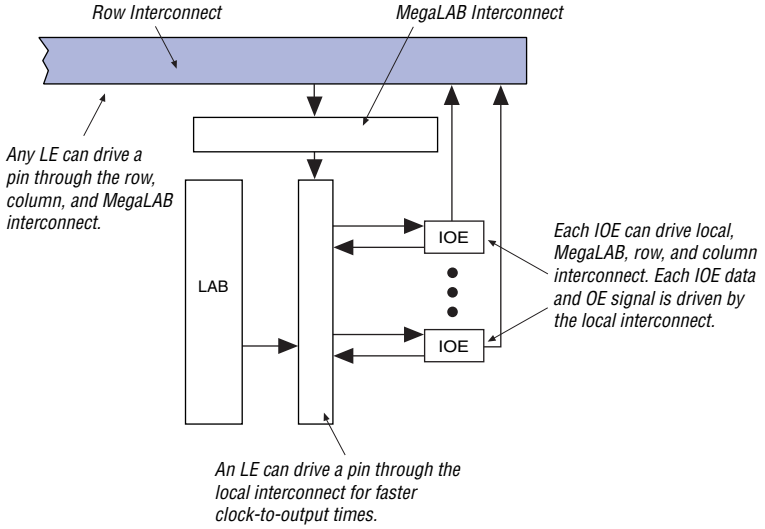
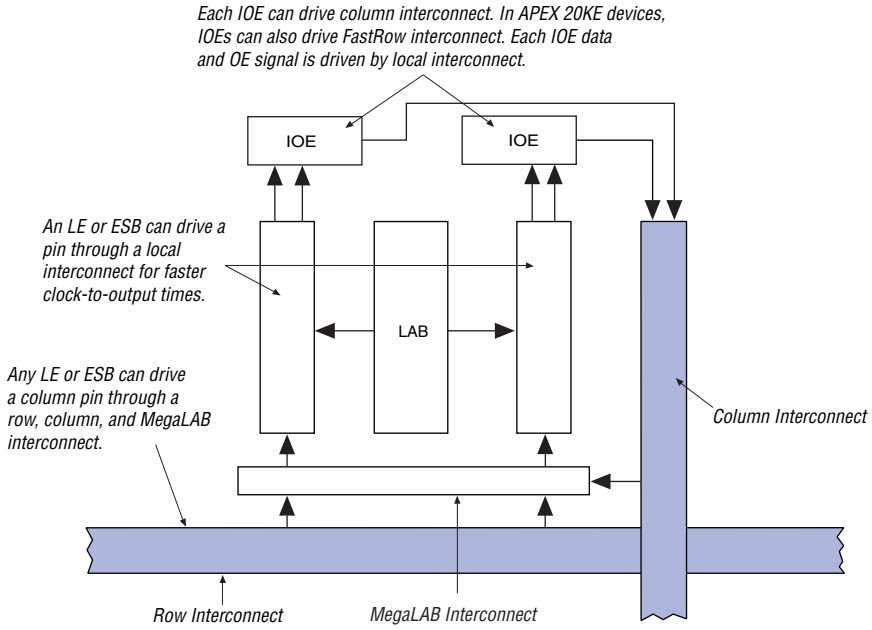


Figure 28 shows how a column IOE connects to the interconnect.

*Figure 28. Column IOE Connection to the Interconnect*




## Dedicated Fast I/O Pins

APEX 20KE devices incorporate an enhancement to support bidirectional pins with high internal fanout such as PCI control signals. These pins are called Dedicated Fast I/O pins (`FAST1`, `FAST2`, `FAST3`, and `FAST4`) and replace dedicated inputs. These pins can be used for fast clock, clear, or high fanout logic signal distribution. They also can drive out. The Dedicated Fast I/O pin data output and tri-state control are driven by local interconnect from the adjacent MegaLAB for high speed.

## Advanced I/O Standard Support

APEX 20KE IOEs support the following I/O standards: LVTTL, LVCMOS, 1.8-V I/O, 2.5-V I/O, 3.3-V PCI, PCI-X, 3.3-V AGP, LVDS, LVPECL, GTL+, CTT, HSTL Class I, SSTL-3 Class I and II, and SSTL-2 Class I and II.

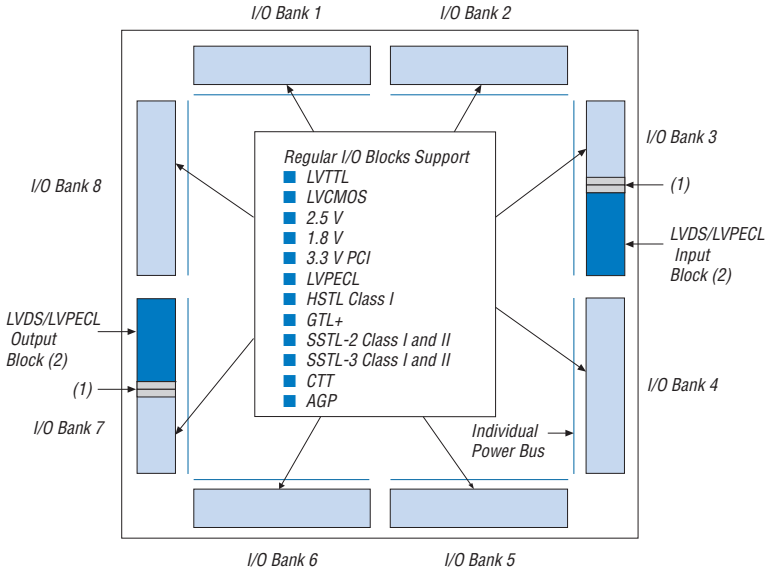
For more information on I/O standards supported by APEX 20KE devices, see *Application Note 117 (Using Selectable I/O Standards in Altera Devices)*.

The APEX 20KE device contains eight I/O banks. In QFP packages, the banks are linked to form four I/O banks. The I/O banks directly support all standards except LVDS and LVPECL. All I/O banks can support LVDS and LVPECL with the addition of external resistors. In addition, one block within a bank contains circuitry to support high-speed True-LVDS and LVPECL inputs, and another block within a particular bank supports high-speed True-LVDS and LVPECL outputs. The LVDS blocks support all of the I/O standards. Each I/O bank has its own VCCIO pins. A single device can support 1.8-V, 2.5-V, and 3.3-V interfaces; each bank can support a different standard independently. Each bank can also use a separate $V_{REF}$ level so that each bank can support any of the terminated standards (such as SSTL-3) independently. Within a bank, any one of the terminated standards can be supported. EP20K300E and larger APEX 20KE devices support the LVDS interface for data pins (smaller devices support LVDS clock pins, but not data pins). All EP20K300E and larger devices support the LVDS interface for data pins up to 155 Mbit per channel; EP20K400E devices and larger with an X-suffix on the ordering code add a serializer/deserializer circuit and PLL for higher-speed support.

Each bank can support multiple standards with the same VCCIO for output pins. Each bank can support one voltage-referenced I/O standard, but it can support multiple I/O standards with the same VCCIO voltage level. For example, when VCCIO is 3.3 V, a bank can support LVTTL, LVCMOS, 3.3-V PCI, and SSTL-3 for inputs and outputs.

When the LVDS banks are not used as LVDS I/O banks, they support all of the other I/O standards. Figure 29 shows the arrangement of the APEX 20KE I/O banks.

*Figure 29. APEX 20KE I/O Banks*




*Notes to Figure 29:*

(1) For more information on placing I/O pins in LVDS blocks, refer to the *Guidelines for Using LVDS Blocks* section in *Application Note 120 (Using LVDS in APEX 20KE Devices*).

(2) If the LVDS input and output blocks are not used for LVDS, they can support all of the I/O standards and can be used as input, output, or bidirectional pins with $V_{CCIO}$ set to 3.3 V, 2.5 V, or 1.8 V.

## Power Sequencing & Hot Socketing

Because APEX 20K and APEX 20KE devices can be used in a mixed-voltage environment, they have been designed specifically to tolerate any possible power-up sequence. Therefore, the $V_{CCIO}$ and $V_{CCINT}$ power supplies may be powered in any order.

For more information, please refer to the "Power Sequencing Considerations" section in the *Configuring APEX 20KE & APEX 20KC Devices* chapter of the *Configuration Devices Handbook*.

Signals can be driven into APEX 20K devices before and during power-up without damaging the device. In addition, APEX 20K devices do not drive out during power-up. Once operating conditions are reached and the device is configured, APEX 20K and APEX 20KE devices operate as specified by the user.

Under hot socketing conditions, APEX 20KE devices will not sustain any damage, but the I/O pins will drive out.

## MultiVolt I/O Interface

The APEX device architecture supports the MultiVolt I/O interface feature, which allows APEX devices in all packages to interface with systems of different supply voltages. The devices have one set of VCC pins for internal operation and input buffers (VCCINT), and another set for I/O output drivers (VCCIO).

The APEX 20K VCCINT pins must always be connected to a 2.5 V power supply. With a 2.5-V $V_{CCINT}$ level, input pins are 2.5-V, 3.3-V, and 5.0-V tolerant. The VCCIO pins can be connected to either a 2.5-V or 3.3-V power supply, depending on the output requirements. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When the VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and is compatible with 3.3-V or 5.0-V systems.

Table 12 summarizes 5.0-V tolerant APEX 20K MultiVolt I/O support.

*Table 12. 5.0-V Tolerant APEX 20K MultiVolt I/O Support*

| $V_{CCIO}$ (V) | Input Signals (V) | | | Output Signals (V) | | |
|---|---|---|---|---|---|---|
| | 2.5 | 3.3 | 5.0 | 2.5 | 3.3 | 5.0 |
| 2.5 | ✓ | ✓(1) | ✓(1) | ✓ | | |
| 3.3 | ✓ | ✓ | ✓(1) | ✓(2) | ✓ | ✓ |

*Notes to Table 12:*

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$.

(2) When $V_{CCIO}$ = 3.3 V, an APEX 20K device can drive a 2.5-V device with 3.3-V tolerant inputs.

Open-drain output pins on 5.0-V tolerant APEX 20K devices (with a pull-up resistor to the 5.0-V supply) can drive 5.0-V CMOS input pins that require a $V_{IH}$ of 3.5 V. When the pin is inactive, the trace will be pulled up to 5.0 V by the resistor. The open-drain pin will only drive low or tri-state; it will never drive high. The rise time is dependent on the value of the pull-up resistor and load impedance. The $I_{OL}$ current specification should be considered when selecting a pull-up resistor.

APEX 20KE devices also support the MultiVolt I/O interface feature. The APEX 20KE VCCINT pins must always be connected to a 1.8-V power supply. With a 1.8-V $V_{CCINT}$ level, input pins are 1.8-V, 2.5-V, and 3.3-V tolerant. The VCCIO pins can be connected to either a 1.8-V, 2.5-V, or 3.3-V power supply, depending on the I/O standard requirements. When the VCCIO pins are connected to a 1.8-V power supply, the output levels are compatible with 1.8-V systems. When VCCIO pins are connected to a 2.5-V power supply, the output levels are compatible with 2.5-V systems. When VCCIO pins are connected to a 3.3-V power supply, the output high is 3.3 V and compatible with 3.3-V or 5.0-V systems. An APEX 20KE device is 5.0-V tolerant with the addition of a resistor.

Table 13 summarizes APEX 20KE MultiVolt I/O support.

*Table 13. APEX 20KE MultiVolt I/O Support* *Note (1)*

| $V_{CCIO}$ (V) | Input Signals (V) | | | | Output Signals (V) | | | |
|---|---|---|---|---|---|---|---|---|
| | 1.8 | 2.5 | 3.3 | 5.0 | 1.8 | 2.5 | 3.3 | 5.0 |
| 1.8 | ✓ | ✓ | ✓ | | ✓ | | | |
| 2.5 | ✓ | ✓ | ✓ | | | ✓ | | |
| 3.3 | ✓ | ✓ | ✓ | *(2)* | | | ✓*(3)* | |

***Notes to Table 13:***

(1) The PCI clamping diode must be disabled to drive an input with voltages higher than $V_{CCIO}$, except for the 5.0-V input case.

(2) An APEX 20KE device can be made 5.0-V tolerant with the addition of an external resistor. You also need a PCI clamp and series resistor.

(3) When $V_{CCIO}$ = 3.3 V, an APEX 20KE device can drive a 2.5-V device with 3.3-V tolerant inputs.

## ClockLock & ClockBoost Features

APEX 20K devices support the ClockLock and ClockBoost clock management features, which are implemented with PLLs. The ClockLock circuitry uses a synchronizing PLL that reduces the clock delay and skew within a device. This reduction minimizes clock-to-output and setup times while maintaining zero hold times. The ClockBoost circuitry, which provides a clock multiplier, allows the designer to enhance device area efficiency by sharing resources within the device. The ClockBoost circuitry allows the designer to distribute a low-speed clock and multiply that clock on-device. APEX 20K devices include a high-speed clock tree; unlike ASICs, the user does not have to design and optimize the clock tree. The ClockLock and ClockBoost features work in conjunction with the APEX 20K device's high-speed clock to provide significant improvements in system performance and band-width. Devices with an X-suffix on the ordering code include the ClockLock circuit.

The ClockLock and ClockBoost features in APEX 20K devices are enabled through the Quartus II software. External devices are not required to use these features.

For designs that require both a multiplied and non-multiplied clock, the clock trace on the board can be connected to CLK2p. Table 14 shows the combinations supported by the ClockLock and ClockBoost circuitry. The CLK2p pin can feed both the ClockLock and ClockBoost circuitry in the APEX 20K device. However, when both circuits are used, the other clock pin (CLK1p) cannot be used.

*Table 14. Multiplication Factor Combinations*

| Clock 1 | Clock 2 |
|---|---|
| ×1 | ×1 |
| ×1, ×2 | ×2 |
| ×1, ×2, ×4 | ×4 |

## APEX 20KE ClockLock Feature

APEX 20KE devices include an enhanced ClockLock feature set. These devices include up to four PLLs, which can be used independently. Two PLLs are designed for either general-purpose use or LVDS use (on devices that support LVDS I/O pins). The remaining two PLLs are designed for general-purpose use. The EP20K200E and smaller devices have two PLLs; the EP20K300E and larger devices have four PLLs.

The following sections describe some of the features offered by the APEX 20KE PLLs.

### *External PLL Feedback*

The ClockLock circuit's output can be driven off-chip to clock other devices in the system; further, the feedback loop of the PLL can be routed off-chip. This feature allows the designer to exercise fine control over the I/O interface between the APEX 20KE device and another high-speed device, such as SDRAM.

### *Clock Multiplication*

The APEX 20KE ClockBoost circuit can multiply or divide clocks by a programmable number. The clock can be multiplied by $m/(n \times k)$ or $m/(n \times v)$, where $m$ and $k$ range from 2 to 160, and $n$ and $v$ range from 1 to 16. Clock multiplication and division can be used for time-domain multiplexing and other functions, which can reduce design LE requirements.

### *Clock Phase & Delay Adjustment*

The APEX 20KE ClockShift feature allows the clock phase and delay to be adjusted. The clock phase can be adjusted by 90° steps. The clock delay can be adjusted to increase or decrease the clock delay by an arbitrary amount, up to one clock period.

### *LVDS Support*

Two PLLs are designed to support the LVDS interface. When using LVDS, the I/O clock runs at a slower rate than the data transfer rate. Thus, PLLs are used to multiply the I/O clock internally to capture the LVDS data. For example, an I/O clock may run at 105 MHz to support 840 megabits per second (Mbps) LVDS data transfer. In this example, the PLL multiplies the incoming clock by eight to support the high-speed data transfer. You can use PLLs in EP20K400E and larger devices for high-speed LVDS interfacing.

### *Lock Signals*

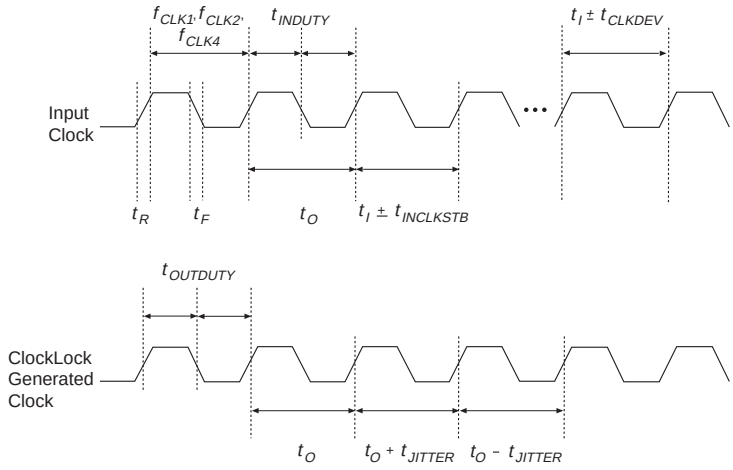
The APEX 20KE ClockLock circuitry supports individual `LOCK` signals. The `LOCK` signal drives high when the ClockLock circuit has locked onto the input clock. The `LOCK` signals are optional for each ClockLock circuit; when not used, they are I/O pins.

## ClockLock & ClockBoost Timing Parameters

For the ClockLock and ClockBoost circuitry to function properly, the incoming clock must meet certain requirements. If these specifications are not met, the circuitry may not lock onto the incoming clock, which generates an erroneous clock within the device. The clock generated by the ClockLock and ClockBoost circuitry must also meet certain specifications. If the incoming clock meets these requirements during configuration, the APEX 20K ClockLock and ClockBoost circuitry will lock onto the clock during configuration. The circuit will be ready for use immediately after configuration. In APEX 20KE devices, the clock input standard is programmable, so the PLL cannot respond to the clock until the device is configured. The PLL locks onto the input clock as soon as configuration is complete. Figure 30 shows the incoming and generated clock specifications.

For more information on ClockLock and ClockBoost circuitry, see *Application Note 115: Using the ClockLock and ClockBoost PLL Features in APEX Devices*.

*Figure 30. Specifications for the Incoming & Generated Clocks* *Note (1)*




*Note to Figure 30:*

(1) The tI parameter refers to the nominal input clock period; the tO parameter refers to the nominal output clock period.

Table 15 summarizes the APEX 20K ClockLock and ClockBoost parameters for -1 speed-grade devices.

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 1 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 180 | MHz |
| $f_{CLK1}$ *(1)* | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 180 *(1)* | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 90 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 48 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals 1) *(2)* | | 25,000 *(3)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ClockBoost to acquire lock *(4)* | | 10 | µs |

*Table 15. APEX 20K ClockLock & ClockBoost Parameters for -1 Speed-Grade Devices (Part 2 of 2)*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{SKEW}$ | Skew delay between related ClockLock/ClockBoost-generated clocks | | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ClockBoost-generated clock *(5)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

***Notes to Table 15:***

(1) The PLL input frequency range for the EP20K100-1X device for 1x multiplication is 25 MHz to 175 MHz.
(2) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(3) During device configuration, the ClockLock and ClockBoost circuitry is configured first. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration, because the lock time is less than the configuration time.
(4) The jitter specification is measured under long-term observation.
(5) If the input clock stability is 100 ps, $t_{JITTER}$ is 250 ps.

Table 16 summarizes the APEX 20K ClockLock and ClockBoost parameters for -2 speed grade devices.

*Table 16. APEX 20K ClockLock & ClockBoost Parameters for -2 Speed Grade Devices*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $f_{OUT}$ | Output frequency | 25 | 170 | MHz |
| $f_{CLK1}$ | Input clock frequency (ClockBoost clock multiplication factor equals 1) | 25 | 170 | MHz |
| $f_{CLK2}$ | Input clock frequency (ClockBoost clock multiplication factor equals 2) | 16 | 80 | MHz |
| $f_{CLK4}$ | Input clock frequency (ClockBoost clock multiplication factor equals 4) | 10 | 34 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock/ClockBoost-generated clock | 40 | 60 | % |
| $f_{CLKDEV}$ | Input deviation from user specification in the Quartus II software (ClockBoost clock multiplication factor equals one) *(1)* | | 25,000 *(2)* | PPM |
| $t_R$ | Input rise time | | 5 | ns |
| $t_F$ | Input fall time | | 5 | ns |
| $t_{LOCK}$ | Time required for ClockLock/ ClockBoost to acquire lock *(3)* | | 10 | µs |
| $t_{SKEW}$ | Skew delay between related ClockLock/ ClockBoost-generated clock | 500 | 500 | ps |
| $t_{JITTER}$ | Jitter on ClockLock/ ClockBoost-generated clock *(4)* | | 200 | ps |
| $t_{INCLKSTB}$ | Input clock stability (measured between adjacent clocks) | | 50 | ps |

*Notes to Table 16:*

(1) To implement the ClockLock and ClockBoost circuitry with the Quartus II software, designers must specify the input frequency. The Quartus II software tunes the PLL in the ClockLock and ClockBoost circuitry to this frequency. The $f_{CLKDEV}$ parameter specifies how much the incoming clock can differ from the specified frequency during device operation. Simulation does not reflect this parameter.

(2) Twenty-five thousand parts per million (PPM) equates to 2.5% of input clock period.

(3) During device configuration, the ClockLock and ClockBoost circuitry is configured before the rest of the device. If the incoming clock is supplied during configuration, the ClockLock and ClockBoost circuitry locks during configuration because the $t_{LOCK}$ value is less than the time required for configuration.

(4) The $t_{JITTER}$ specification is measured under long-term observation.

Tables 17 and 18 summarize the ClockLock and ClockBoost parameters for APEX 20KE devices.

*Table 17. APEX 20KE ClockLock & ClockBoost Parameters* *Note (1)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $t_R$ | Input rise time | | | | 5 | ns |
| $t_F$ | Input fall time | | | | 5 | ns |
| $t_{INDUTY}$ | Input duty cycle | | 40 | | 60 | % |
| $t_{INJITTER}$ | Input jitter peak-to-peak | | | | 2% of input period | peak-to-peak |
| $t_{OUTJITTER}$ | Jitter on ClockLock or ClockBoost-generated clock | | | | 0.35% of output period | RMS |
| $t_{OUTDUTY}$ | Duty cycle for ClockLock or ClockBoost-generated clock | | 45 | | 55 | % |
| $t_{LOCK}$ *(2)*, *(3)* | Time required for ClockLock or ClockBoost to acquire lock | | | | 40 | µs |

*Table 18. APEX 20KE Clock Input & Output Parameters (Part 1 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -1X Speed Grade | | -2X Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{VCO}$ *(4)* | Voltage controlled oscillator operating range | | 200 | 500 | 200 | 500 | MHz |
| $f_{CLOCK0}$ | `Clock0` PLL output frequency for internal use | | 1.5 | 335 | 1.5 | 200 | MHz |
| $f_{CLOCK1}$ | `Clock1` PLL output frequency for internal use | | 20 | 335 | 20 | 200 | MHz |
| $f_{CLOCK0_EXT}$ | Output clock frequency for external `clock0` output | 3.3-V LVTTL | 1.5 | 245 | 1.5 | 226 | MHz |
| | | 2.5-V LVTTL | 1.5 | 234 | 1.5 | 221 | MHz |
| | | 1.8-V LVTTL | 1.5 | 223 | 1.5 | 216 | MHz |
| | | GTL+ | 1.5 | 205 | 1.5 | 193 | MHz |
| | | SSTL-2 Class I | 1.5 | 158 | 1.5 | 157 | MHz |
| | | SSTL-2 Class II | 1.5 | 142 | 1.5 | 142 | MHz |
| | | SSTL-3 Class I | 1.5 | 166 | 1.5 | 162 | MHz |
| | | SSTL-3 Class II | 1.5 | 149 | 1.5 | 146 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |
| $f_{CLOCK1_EXT}$ | Output clock frequency for external `clock1` output | 3.3-V LVTTL | 20 | 245 | 20 | 226 | MHz |
| | | 2.5-V LVTTL | 20 | 234 | 20 | 221 | MHz |
| | | 1.8-V LVTTL | 20 | 223 | 20 | 216 | MHz |
| | | GTL+ | 20 | 205 | 20 | 193 | MHz |
| | | SSTL-2 Class I | 20 | 158 | 20 | 157 | MHz |
| | | SSTL-2 Class II | 20 | 142 | 20 | 142 | MHz |
| | | SSTL-3 Class I | 20 | 166 | 20 | 162 | MHz |
| | | SSTL-3 Class II | 20 | 149 | 20 | 146 | MHz |
| | | LVDS | 20 | 420 | 20 | 350 | MHz |

*Table 18. APEX 20KE Clock Input & Output Parameters (Part 2 of 2)* *Note (1)*

| Symbol | Parameter | I/O Standard | -1X Speed Grade | | -2X Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | | | Min | Max | Min | Max | |
| $f_{IN}$ | Input clock frequency | 3.3-V LVTTL | 1.5 | 290 | 1.5 | 257 | MHz |
| | | 2.5-V LVTTL | 1.5 | 281 | 1.5 | 250 | MHz |
| | | 1.8-V LVTTL | 1.5 | 272 | 1.5 | 243 | MHz |
| | | GTL+ | 1.5 | 303 | 1.5 | 261 | MHz |
| | | SSTL-2 Class I | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-2 Class II | 1.5 | 291 | 1.5 | 253 | MHz |
| | | SSTL-3 Class I | 1.5 | 300 | 1.5 | 260 | MHz |
| | | SSTL-3 Class II | 1.5 | 300 | 1.5 | 260 | MHz |
| | | LVDS | 1.5 | 420 | 1.5 | 350 | MHz |

*Notes to Tables 17 and 18:*

(1) All input clock specifications must be met. The PLL may not lock onto an incoming clock if the clock specifications are not met, creating an erroneous clock within the device.
(2) The maximum lock time is 40 µs or 2000 input clock cycles, whichever occurs first.
(3) Before configuration, the PLL circuits are disable and powered down. During configuration, the PLLs are still disabled. The PLLs begin to lock once the device is in the user mode. If the clock enable feature is used, lock begins once the `CLKLK_ENA` pin goes high in user mode.
(4) The PLL VCO operating range is 200 MHz ð $f_{VCO}$ ð 840 MHz for LVDS mode.

## SignalTap Embedded Logic Analyzer

APEX 20K devices include device enhancements to support the SignalTap embedded logic analyzer. By including this circuitry, the APEX 20K device provides the ability to monitor design operation over a period of time through the IEEE Std. 1149.1 (JTAG) circuitry; a designer can analyze internal logic at speed without bringing internal signals to the I/O pins. This feature is particularly important for advanced packages such as FineLine BGA packages because adding a connection to a pin during the debugging process can be difficult after a board is designed and manufactured.

## IEEE Std. 1149.1 (JTAG) Boundary-Scan Support

All APEX 20K devices provide JTAG BST circuitry that complies with the IEEE Std. 1149.1-1990 specification. JTAG boundary-scan testing can be performed before or after configuration, but not during configuration. APEX 20K devices can also use the JTAG port for configuration with the Quartus II software or with hardware using either Jam Files (**.jam**) or Jam Byte-Code Files (**.jbc**). Finally, APEX 20K devices use the JTAG port to monitor the logic operation of the device with the SignalTap embedded logic analyzer. APEX 20K devices support the JTAG instructions shown in Table 19. Although EP20K1500E devices support the JTAG BYPASS and SignalTap instructions, they do not support boundary-scan testing or the use of the JTAG port for configuration.

*Table 19. APEX 20K JTAG Instructions*

| JTAG Instruction | Description |
|---|---|
| SAMPLE/PRELOAD | Allows a snapshot of signals at the device pins to be captured and examined during normal device operation, and permits an initial data pattern to be output at the device pins. Also used by the SignalTap embedded logic analyzer. |
| EXTEST | Allows the external circuitry and board-level interconnections to be tested by forcing a test pattern at the output pins and capturing test results at the input pins. |
| BYPASS *(1)* | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation. |
| USERCODE | Selects the 32-bit USERCODE register and places it between the TDI and TDO pins, allowing the USERCODE to be serially shifted out of TDO. |
| IDCODE | Selects the IDCODE register and places it between TDI and TDO, allowing the IDCODE to be serially shifted out of TDO. |
| ICR Instructions | Used when configuring an APEX 20K device via the JTAG port with a MasterBlaster™ or ByteBlasterMV™ download cable, or when using a Jam File or Jam Byte-Code File via an embedded processor. |
| SignalTap Instructions *(1)* | Monitors internal device operation with the SignalTap embedded logic analyzer. |

*Note to Table 19:*
(1) The EP20K1500E device supports the JTAG BYPASS instruction and the SignalTap instructions.

The APEX 20K device instruction register length is 10 bits. The APEX 20K device USERCODE register length is 32 bits. Tables 20 and 21 show the boundary-scan register length and device IDCODE information for APEX 20K devices.

*Table 20. APEX 20K Boundary-Scan Register Length*

| Device | Boundary-Scan Register Length |
|---|---|
| EP20K30E | 420 |
| EP20K60E | 624 |
| EP20K100 | 786 |
| EP20K100E | 774 |
| EP20K160E | 984 |
| EP20K200 | 1,176 |
| EP20K200E | 1,164 |
| EP20K300E | 1,266 |
| EP20K400 | 1,536 |
| EP20K400E | 1,506 |
| EP20K600E | 1,806 |
| EP20K1000E | 2,190 |
| EP20K1500E | 1 *(1)* |

***Note to Table 20:***
(1) This device does not support JTAG boundary scan testing.

*Table 21. 32-Bit APEX 20K Device IDCODE*

| Device | IDCODE (32 Bits) *(1)* | | | |
|---|---|---|---|---|
| | Version (4 Bits) | Part Number (16 Bits) | Manufacturer Identity (11 Bits) | 1 (1 Bit) *(2)* |
| EP20K30E | 0000 | 1000 0000 0011 0000 | 000 0110 1110 | 1 |
| EP20K60E | 0000 | 1000 0000 0110 0000 | 000 0110 1110 | 1 |
| EP20K100 | 0000 | 0000 0100 0001 0110 | 000 0110 1110 | 1 |
| EP20K100E | 0000 | 1000 0001 0000 0000 | 000 0110 1110 | 1 |
| EP20K160E | 0000 | 1000 0001 0110 0000 | 000 0110 1110 | 1 |
| EP20K200 | 0000 | 0000 1000 0011 0010 | 000 0110 1110 | 1 |
| EP20K200E | 0000 | 1000 0010 0000 0000 | 000 0110 1110 | 1 |
| EP20K300E | 0000 | 1000 0011 0000 0000 | 000 0110 1110 | 1 |
| EP20K400 | 0000 | 0001 0110 0110 0100 | 000 0110 1110 | 1 |
| EP20K400E | 0000 | 1000 0100 0000 0000 | 000 0110 1110 | 1 |
| EP20K600E | 0000 | 1000 0110 0000 0000 | 000 0110 1110 | 1 |
| EP20K1000E | 0000 | 1001 0000 0000 0000 | 000 0110 1110 | 1 |

*Notes to Table 21:*
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 31 shows the timing requirements for the JTAG signals.

*Figure 31. APEX 20K JTAG Waveforms*

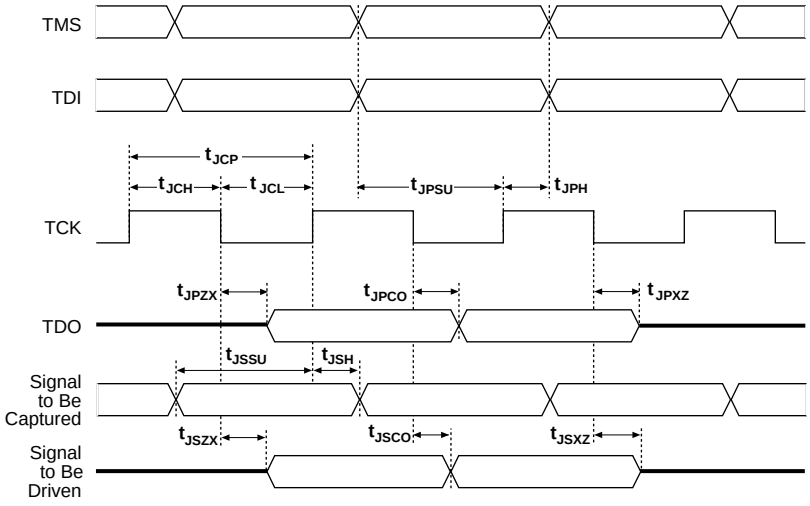


Table 22 shows the JTAG timing parameters and values for APEX 20K devices.

*Table 22. APEX 20K JTAG Timing Parameters & Values*

| Symbol | Parameter | Min | Max | Unit |
|---|---|---|---|---|
| $t_{JCP}$ | TCK clock period | 100 | | ns |
| $t_{JCH}$ | TCK clock high time | 50 | | ns |
| $t_{JCL}$ | TCK clock low time | 50 | | ns |
| $t_{JPSU}$ | JTAG port setup time | 20 | | ns |
| $t_{JPH}$ | JTAG port hold time | 45 | | ns |
| $t_{JPCO}$ | JTAG port clock to output | | 25 | ns |
| $t_{JPZX}$ | JTAG port high impedance to valid output | | 25 | ns |
| $t_{JPXZ}$ | JTAG port valid output to high impedance | | 25 | ns |
| $t_{JSSU}$ | Capture register setup time | 20 | | ns |
| $t_{JSH}$ | Capture register hold time | 45 | | ns |
| $t_{JSCO}$ | Update register clock to output | | 35 | ns |
| $t_{JSZX}$ | Update register high impedance to valid output | | 35 | ns |
| $t_{JSXZ}$ | Update register valid output to high impedance | | 35 | ns |

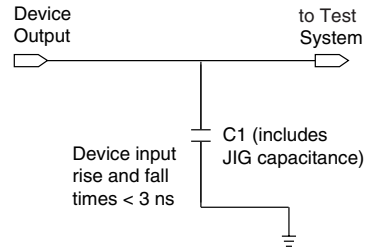
For more information, see the following documents:

- *Application Note 39 (IEEE Std. 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices)*
- *Jam Programming & Test Language Specification*

## Generic Testing

Each APEX 20K device is functionally tested. Complete testing of each configurable static random access memory (SRAM) bit and all logic functionality ensures 100% yield. AC test measurements for APEX 20K devices are made under conditions equivalent to those shown in Figure 32. Multiple test patterns can be used to configure devices during all stages of the production flow.

*Figure 32. APEX 20K AC Test Conditions* *Note (1)*




*Note to Figure 32:*

(1) Power supply transients can affect AC measurements. Simultaneous transitions of multiple outputs should be avoided for accurate measurement. Threshold tests must not be performed under AC conditions. Large-amplitude, fast-ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, significant reductions in observable noise immunity can result.

## Operating Conditions

Tables 23 through 26 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 2.5-V APEX 20K devices.

*Table 23. APEX 20K 5.0-V Tolerant Device Absolute Maximum Ratings* *Notes (1), (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage | With respect to ground *(3)* | –0.5 | 3.6 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –2.0 | 5.75 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 24. APEX 20K 5.0-V Tolerant Device Recommended Operating Conditions* *Note (2)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(4)*, *(5)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(4)*, *(5)* | 2.375 (2.375) | 2.625 (2.625) | V |
| $V_I$ | Input voltage | *(3)*, *(6)* | –0.5 | 5.75 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 1 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(9)* | | 5.75 | V |
| $V_{IL}$ | Low-level input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(9)* | V |
| $V_{OH}$ | 3.3-V high-level TTL output voltage | $I_{OH}$ = –8 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | 2.4 | | | V |
| | 3.3-V high-level CMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(10)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(10)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(10)* | 1.7 | | | V |

*Table 25. APEX 20K 5.0-V Tolerant Device DC Operating Conditions (Part 2 of 2)* *Notes (2), (7), (8)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{OL}$ | 3.3-V low-level TTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.45 | V |
| | 3.3-V low-level CMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | | | $0.1 \times V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 5.75 to –0.5 V | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade *(12)* | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades *(12)* | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(13)* | 20 | | 50 | W |
| | | $V_{CCIO}$ = 2.375 V *(13)* | 30 | | 80 | W |

| Table 26. APEX 20K 5.0-V Tolerant Device Capacitance Notes (2), (14) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

*Notes to Tables 23 through 26:*

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) All APEX 20K devices are 5.0-V tolerant.
(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(4) Numbers in parentheses are for industrial-temperature-range devices.
(5) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(6) All pins, including dedicated inputs, clock I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 2.5 V, and $V_{CCIO}$ = 2.5 or 3.3 V.
(8) These values are specified in the APEX 20K device recommended operating conditions, shown in Table 26 on page 62.
(9) The APEX 20K input buffers are compatible with 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant when $V_{CCIO}$ and $V_{CCINT}$ meet the relationship shown in Figure 33 on page 68.
(10) The $I_{OH}$ parameter refers to high-level TTL, PCI or CMOS output current.
(11) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(12) This value is specified for normal device operation. The value may vary during power-up.
(13) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(14) Capacitance is sample-tested only.

Tables 27 through 30 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.8-V APEX 20KE devices.

| Table 27. APEX 20KE Device Absolute Maximum Ratings Note (1) | | | | | |
|---|---|---|---|---|---|
| **Symbol** | **Parameter** | **Conditions** | **Min** | **Max** | **Unit** |
| $V_{CCINT}$ | Supply voltage | With respect to ground (2) | –0.5 | 2.5 | V |
| $V_{CCIO}$ | | | –0.5 | 4.6 | V |
| $V_I$ | DC input voltage | | –0.5 | 4.6 | V |
| $I_{OUT}$ | DC output current, per pin | | –25 | 25 | mA |
| $T_{STG}$ | Storage temperature | No bias | –65 | 150 | ° C |
| $T_{AMB}$ | Ambient temperature | Under bias | –65 | 135 | ° C |
| $T_J$ | Junction temperature | PQFP, RQFP, TQFP, and BGA packages, under bias | | 135 | ° C |
| | | Ceramic PGA packages, under bias | | 150 | ° C |

*Table 28. APEX 20KE Device Recommended Operating Conditions*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{CCINT}$ | Supply voltage for internal logic and input buffers | *(3), (4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_{CCIO}$ | Supply voltage for output buffers, 3.3-V operation | *(3), (4)* | 3.00 (3.00) | 3.60 (3.60) | V |
| | Supply voltage for output buffers, 2.5-V operation | *(3), (4)* | 2.375 (2.375) | 2.625 (2.625) | V |
| | Supply voltage for output buffers, 1.8-V operation | *(3), (4)* | 1.71 (1.71) | 1.89 (1.89) | V |
| $V_I$ | Input voltage | *(5), (6)* | –0.5 | 4.0 | V |
| $V_O$ | Output voltage | | 0 | $V_{CCIO}$ | V |
| $T_J$ | Junction temperature | For commercial use | 0 | 85 | ° C |
| | | For industrial use | –40 | 100 | ° C |
| $t_R$ | Input rise time | | | 40 | ns |
| $t_F$ | Input fall time | | | 40 | ns |

**Table 29. APEX 20KE Device DC Operating Conditions** *Notes (7), (8), (9)*

| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level LVTTL, CMOS, or 3.3-V PCI input voltage | | 1.7, 0.5 × $V_{CCIO}$ *(10)* | | 4.1 | V |
| $V_{IL}$ | Low-level LVTTL, CMOS, or 3.3-V PCI input voltage | | –0.5 | | 0.8, 0.3 × $V_{CCIO}$ *(10)* | V |
| $V_{OH}$ | 3.3-V high-level LVTTL output voltage | $I_{OH}$ = –12 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | 2.4 | | | V |
| | 3.3-V high-level LVCMOS output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 3.00 V *(11)* | $V_{CCIO}$ – 0.2 | | | V |
| | 3.3-V high-level PCI output voltage | $I_{OH}$ = –0.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(11)* | 0.9 × $V_{CCIO}$ | | | V |
| | 2.5-V high-level output voltage | $I_{OH}$ = –0.1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.1 | | | V |
| | | $I_{OH}$ = –1 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 2.0 | | | V |
| | | $I_{OH}$ = –2 mA DC, $V_{CCIO}$ = 2.30 V *(11)* | 1.7 | | | V |
| $V_{OL}$ | 3.3-V low-level LVTTL output voltage | $I_{OL}$ = 12 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.4 | V |
| | 3.3-V low-level LVCMOS output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 3.00 V *(12)* | | | 0.2 | V |
| | 3.3-V low-level PCI output voltage | $I_{OL}$ = 1.5 mA DC, $V_{CCIO}$ = 3.00 to 3.60 V *(12)* | | | 0.1 × $V_{CCIO}$ | V |
| | 2.5-V low-level output voltage | $I_{OL}$ = 0.1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.2 | V |
| | | $I_{OL}$ = 1 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.4 | V |
| | | $I_{OL}$ = 2 mA DC, $V_{CCIO}$ = 2.30 V *(12)* | | | 0.7 | V |
| $I_I$ | Input pin leakage current | $V_I$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O$ = 4.1 to –0.5 V *(13)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All ESBs in power-down mode) | $V_I$ = ground, no load, no toggling inputs, -1 speed grade | | 10 | | mA |
| | | $V_I$ = ground, no load, no toggling inputs, -2, -3 speed grades | | 5 | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | $V_{CCIO}$ = 3.0 V *(14)* | 20 | | 50 | kΩ |
| | | $V_{CCIO}$ = 2.375 V *(14)* | 30 | | 80 | kΩ |
| | | $V_{CCIO}$ = 1.71 V *(14)* | 60 | | 150 | kΩ |

For DC Operating Specifications on APEX 20KE I/O standards, please refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices).*

**Table 30. APEX 20KE Device Capacitance** *Note (15)*

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $C_{IN}$ | Input capacitance | $V_{IN}$ = 0 V, f = 1.0 MHz | | 8 | pF |
| $C_{INCLK}$ | Input capacitance on dedicated clock pin | $V_{IN}$ = 0 V, f = 1.0 MHz | | 12 | pF |
| $C_{OUT}$ | Output capacitance | $V_{OUT}$ = 0 V, f = 1.0 MHz | | 8 | pF |

***Notes to Tables 27 through 30:***

(1) See the *Operating Requirements for Altera Devices Data Sheet*.
(2) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 5.75 V for input currents less than 100 mA and periods shorter than 20 ns.
(3) Numbers in parentheses are for industrial-temperature-range devices.
(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.
(5) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to the voltage shown in the following table based on input duty cycle for input currents less than 100 mA. The overshoot is dependent upon duty cycle of the signal. The DC case is equivalent to 100% duty cycle.

| Vin | Max. Duty Cycle |
|---|---|
| 4.0V | 100% (DC) |
| 4.1 | 90% |
| 4.2 | 50% |
| 4.3 | 30% |
| 4.4 | 17% |
| 4.5 | 10% |

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.
(7) Typical values are for $T_A$ = 25° C, $V_{CCINT}$ = 1.8 V, and $V_{CCIO}$ = 1.8 V, 2.5 V or 3.3 V.
(8) These values are specified under the APEX 20KE device recommended operating conditions, shown in Table 24 on page 60.
(9) Refer to *Application Note 117 (Using Selectable I/O Standards in Altera Devices)* for the $V_{IH}$, $V_{IL}$, $V_{OH}$, $V_{OL}$, and $I_I$ parameters when VCCIO = 1.8 V.
(10) The APEX 20KE input buffers are compatible with 1.8-V, 2.5-V and 3.3-V (LVTTL and LVCMOS) signals. Additionally, the input buffers are 3.3-V PCI compliant. Input buffers also meet specifications for GTL+, CTT, AGP, SSTL-2, SSTL-3, and HSTL.
(11) The $I_{OH}$ parameter refers to high-level TTL, PCI, or CMOS output current.
(12) The $I_{OL}$ parameter refers to low-level TTL, PCI, or CMOS output current. This parameter applies to open-drain pins as well as output pins.
(13) This value is specified for normal device operation. The value may vary during power-up.
(14) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.
(15) Capacitance is sample-tested only.

Figure 33 shows the relationship between $V_{CCIO}$ and $V_{CCINT}$ for 3.3-V PCI compliance on APEX 20K devices.

*Figure 33. Relationship between $V_{CCIO}$ & $V_{CCINT}$ for 3.3-V PCI Compliance*

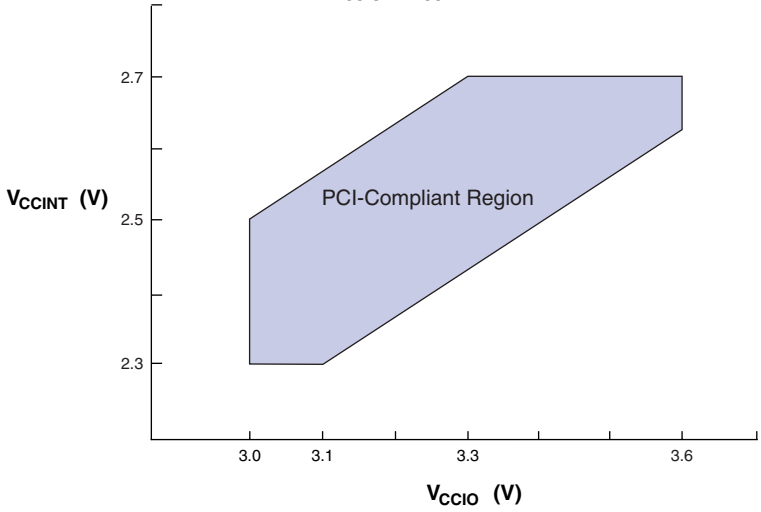
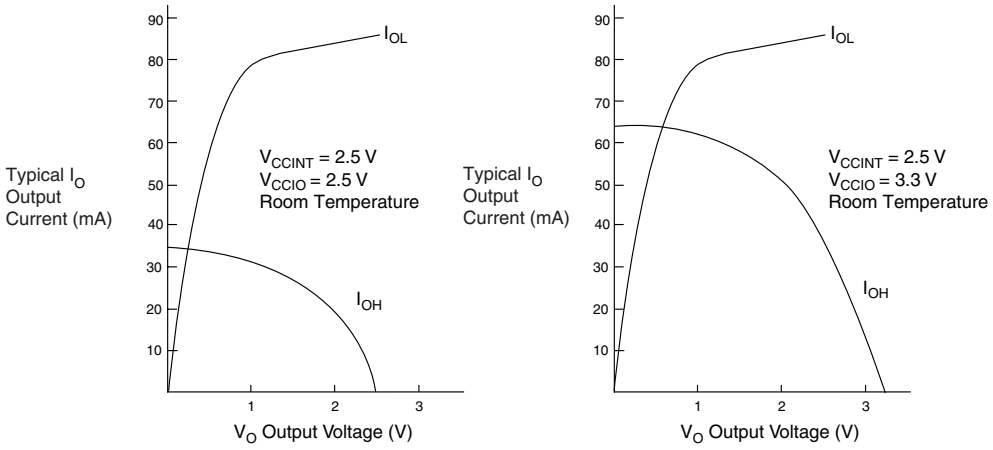



Figure 34 shows the typical output drive characteristics of APEX 20K devices with 3.3-V and 2.5-V $V_{CCIO}$. The output driver is compatible with the 3.3-V ***PCI Local Bus Specification, Revision 2.2*** (when `VCCIO` pins are connected to 3.3 V). 5-V tolerant APEX 20K devices in the -1 speed grade are 5-V PCI compliant over all operating conditions.

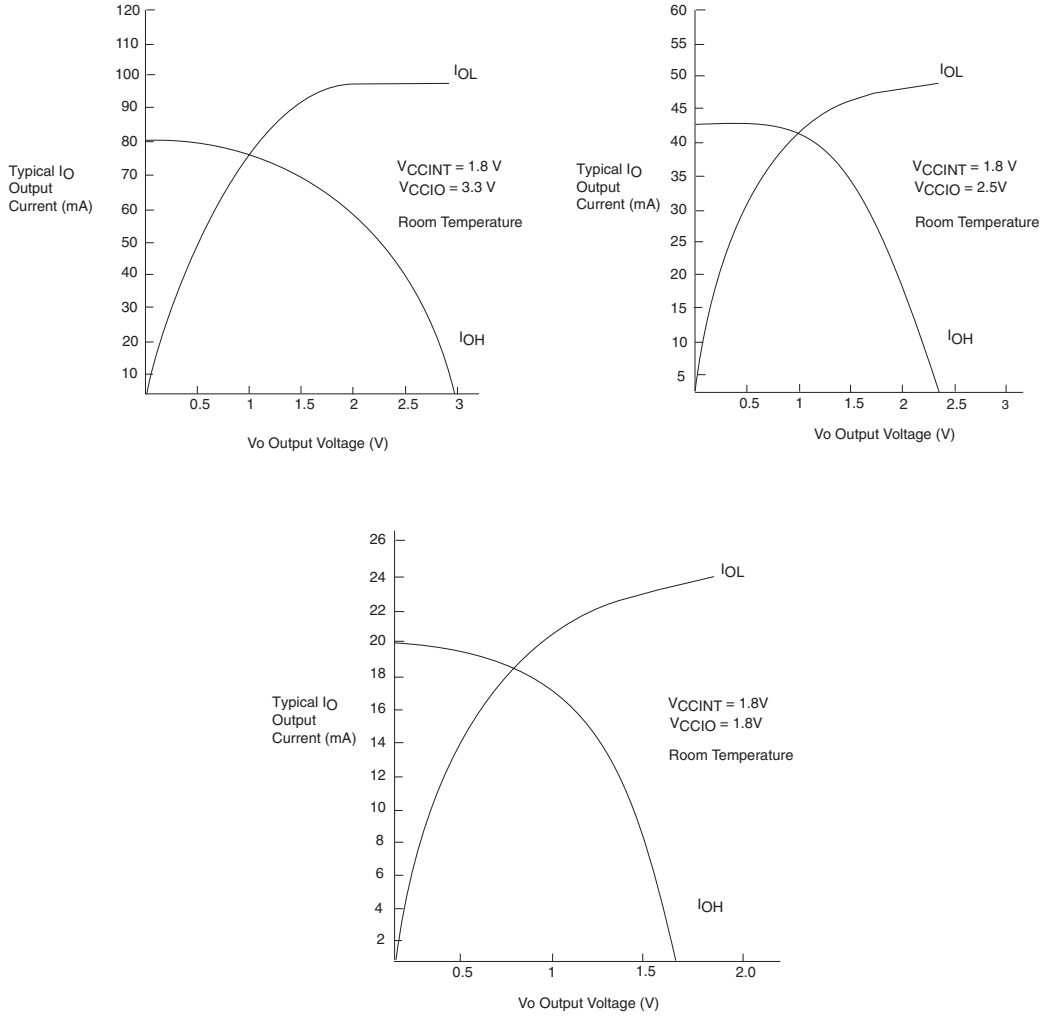
*Figure 34. Output Drive Characteristics of APEX 20K Device* *Note (1)*




***Note to Figure 34:***
(1) These are transient (AC) currents.

Figure 35 shows the output drive characteristics of APEX 20KE devices.

***Figure 35. Output Drive Characteristics of APEX 20KE Devices*** *Note (1)*




***Note to Figure 35:***
(1) These are transient (AC) currents.

# Timing Model

The high-performance FastTrack and MegaLAB interconnect routing resources ensure predictable performance, accurate simulation, and accurate timing analysis. This predictable performance contrasts with that of FPGAs, which use a segmented connection scheme and therefore have unpredictable performance.

All specifications are always representative of worst-case supply voltage and junction temperature conditions. All output-pin-timing specifications are reported for maximum driver strength.

Figure 36 shows the $f_{MAX}$ timing model for APEX 20K devices.

*Figure 36. APEX 20K $f_{MAX}$ Timing Model*

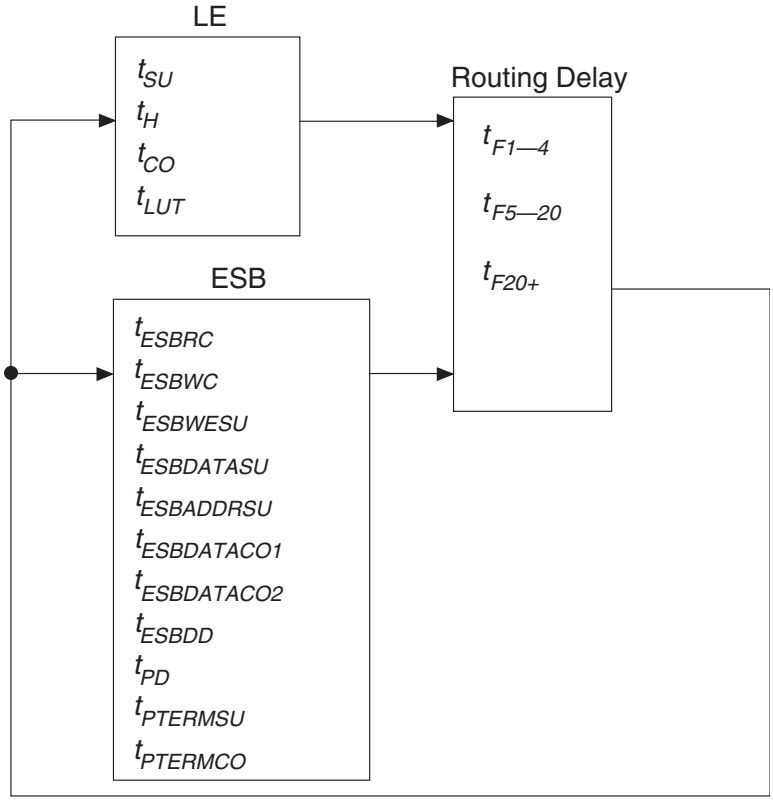
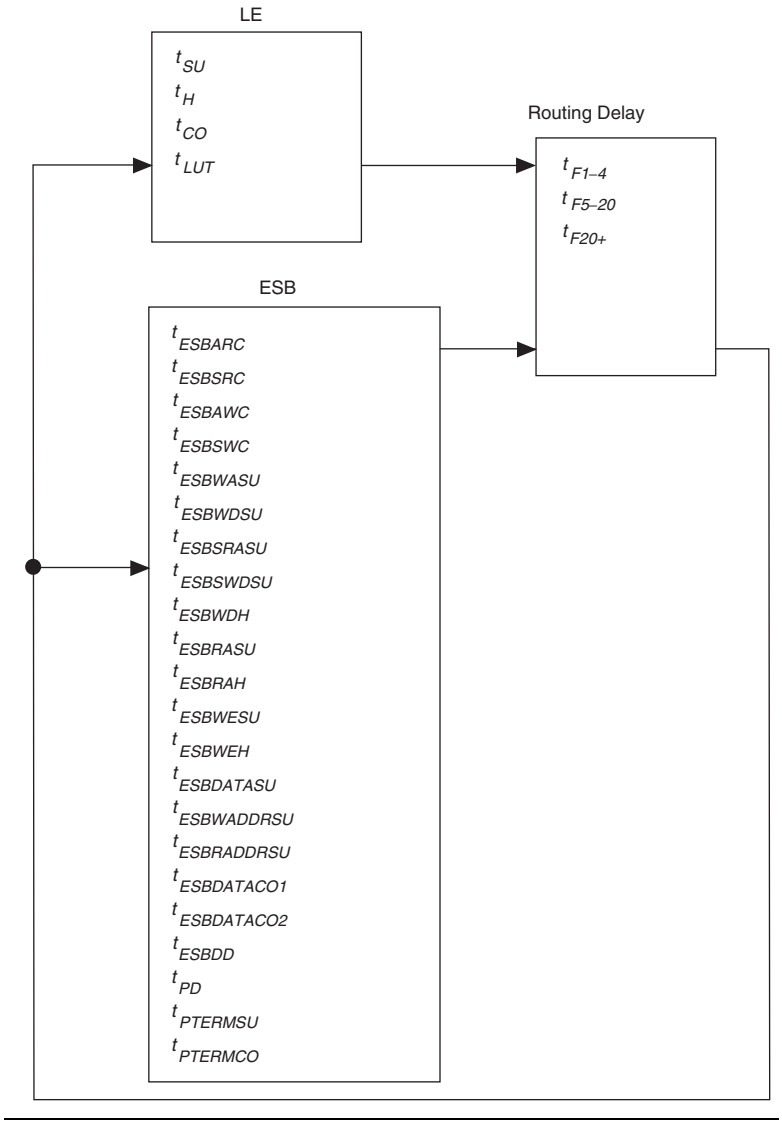



Figure 37 shows the $f_{MAX}$ timing model for APEX 20KE devices. These parameters can be used to estimate $f_{MAX}$ for multiple levels of logic. Quartus II software timing analysis should be used for more accurate timing information.

*Figure 37. APEX 20KE $f_{MAX}$ Timing Model*



Figures 38 and 39 show the asynchronous and synchronous timing waveforms, respectively, for the ESB macroparameters in Table 31.

*Figure 38. ESB Asynchronous Timing Waveforms*

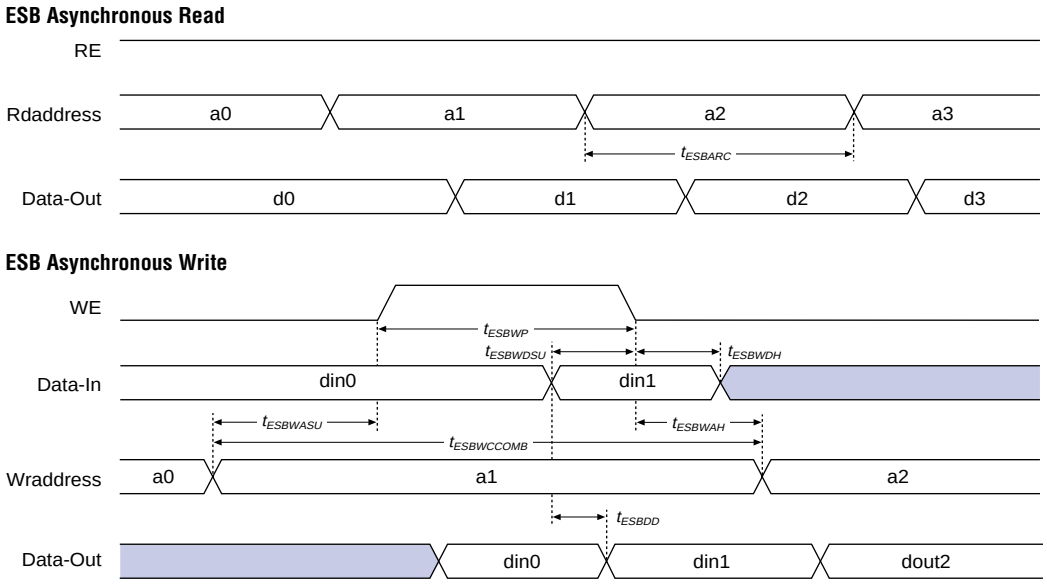


*Figure 39. ESB Synchronous Timing Waveforms*

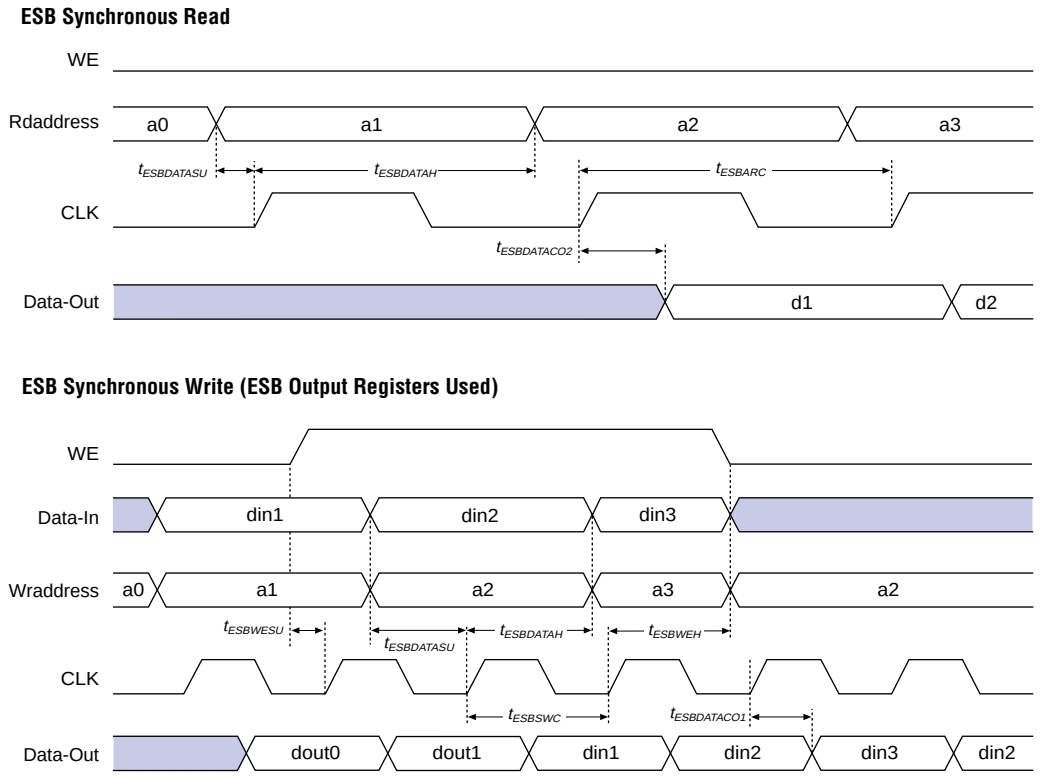
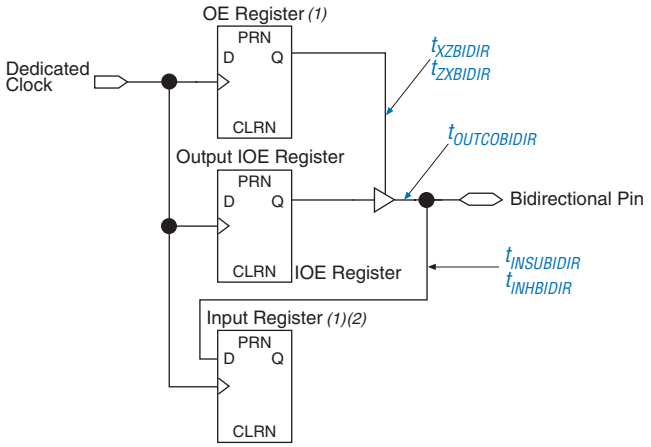



Figure 40 shows the timing model for bidirectional I/O pin timing.

*Figure 40. Synchronous Bidirectional Pin External Timing*




*Notes to Figure 40:*

(1) The output enable and input registers are LE registers in the LAB adjacent to a bidirectional row pin. The output enable register is set with "Output Enable Routing= Signal-Pin" option in the Quartus II software.

(2) The LAB adjacent input register is set with "Decrease Input Delay to Internal Cells= Off". This maintains a zero hold time for lab adjacent registers while giving a fast, position independent setup time. A faster setup time with zero hold time is possible by setting "Decrease Input Delay to Internal Cells= ON" and moving the input register farther away from the bidirectional pin. The exact position where zero hold occurs with the minimum setup time, varies with device density and speed grade.

Table 31 describes the $f_{MAX}$ timing parameters shown in Figure 36 on page 68.

*Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 1 of 2)*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in |
| $t_{ESBRC}$ | ESB Asynchronous read cycle time |
| $t_{ESBWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBADDRSU}$ | ESB address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |

| *Table 31. APEX 20K $f_{MAX}$ Timing Parameters (Part 2 of 2)* | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB macrocell register clock-to-output delay |
| $t_{F1-4}$ | Fanout delay using local interconnect |
| $t_{F5-20}$ | Fanout delay using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay using FastTrack Interconnect |
| $t_{CH}$ | Minimum clock high time from clock pin |
| $t_{CL}$ | Minimum clock low time from clock pin |
| $t_{CLRP}$ | LE clear pulse width |
| $t_{PREP}$ | LE preset pulse width |
| $t_{ESBCH}$ | Clock high time |
| $t_{ESBCL}$ | Clock low time |
| $t_{ESBWP}$ | Write pulse width |
| $t_{ESBRP}$ | Read pulse width |

Tables 32 and 33 describe APEX 20K external timing parameters.

| *Table 32. APEX 20K External Timing Parameters* *Note (1)* | |
|---|---|
| **Symbol** | **Clock Parameter** |
| $t_{INSU}$ | Setup time with global clock at IOE register |
| $t_{INH}$ | Hold time with global clock at IOE register |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE register |

| *Table 33. APEX 20K External Bidirectional Timing Parameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at same-row or same-column LE register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous IOE output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous IOE output buffer enable delay, slow slew rate = off | C1 = 10 pF |

*Note to Tables 32 and 33:*
(1) These timing parameters are sample-tested only.

Tables 34 through 37 show APEX 20KE LE, ESB, routing, and functional timing microparameters for the $f_{MAX}$ timing model.

*Table 34. APEX 20KE LE Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{SU}$ | LE register setup time before clock |
| $t_{H}$ | LE register hold time after clock |
| $t_{CO}$ | LE register clock-to-output delay |
| $t_{LUT}$ | LUT delay for data-in to data-out |

*Table 35. APEX 20KE ESB Timing Microparameters*

| Symbol | Parameter |
|---|---|
| $t_{ESBARC}$ | ESB Asynchronous read cycle time |
| $t_{ESBSRC}$ | ESB Synchronous read cycle time |
| $t_{ESBAWC}$ | ESB Asynchronous write cycle time |
| $t_{ESBSWC}$ | ESB Synchronous write cycle time |
| $t_{ESBWASU}$ | ESB write address setup time with respect to WE |
| $t_{ESBWAH}$ | ESB write address hold time with respect to WE |
| $t_{ESBWDSU}$ | ESB data setup time with respect to WE |
| $t_{ESBWDH}$ | ESB data hold time with respect to WE |
| $t_{ESBRASU}$ | ESB read address setup time with respect to RE |
| $t_{ESBRAH}$ | ESB read address hold time with respect to RE |
| $t_{ESBWESU}$ | ESB WE setup time before clock when using input register |
| $t_{ESBWEH}$ | ESB WE hold time after clock when using input register |
| $t_{ESBDATASU}$ | ESB data setup time before clock when using input register |
| $t_{ESBDATAH}$ | ESB data hold time after clock when using input register |
| $t_{ESBWADDRSU}$ | ESB write address setup time before clock when using input registers |
| $t_{ESBRADDRSU}$ | ESB read address setup time before clock when using input registers |
| $t_{ESBDATACO1}$ | ESB clock-to-output delay when using output registers |
| $t_{ESBDATACO2}$ | ESB clock-to-output delay without output registers |
| $t_{ESBDD}$ | ESB data-in to data-out delay for RAM mode |
| $t_{PD}$ | ESB Macrocell input to non-registered output |
| $t_{PTERMSU}$ | ESB Macrocell register setup time before clock |
| $t_{PTERMCO}$ | ESB Macrocell register clock-to-output delay |

| Table 36. APEX 20KE Routing Timing Microparameters Note (1) | |
|---|---|
| **Symbol** | **Parameter** |
| $t_{F1-4}$ | Fanout delay using Local Interconnect |
| $t_{F5-20}$ | Fanout delay estimate using MegaLab Interconnect |
| $t_{F20+}$ | Fanout delay estimate using FastTrack Interconnect |

*Note to Table 36:*

(1) These parameters are worst-case values for typical applications. Post-compilation timing simulation and timing analysis are required to determine actual worst-case performance.

| Table 37. APEX 20KE Functional Timing Microparameters | |
|---|---|
| **Symbol** | **Parameter** |
| TCH | Minimum clock high time from clock pin |
| TCL | Minimum clock low time from clock pin |
| TCLRP | LE clear Pulse Width |
| TPREP | LE preset pulse width |
| TESBCH | Clock high time for ESB |
| TESBCL | Clock low time for ESB |
| TESBWP | Write pulse width |
| TESBRP | Read pulse width |

Tables 38 and 39 describe the APEX 20KE external timing parameters.

| Table 38. APEX 20KE External Timing Parameters Note (1) | | |
|---|---|---|
| **Symbol** | **Clock Parameter** | **Conditions** |
| $t_{INSU}$ | Setup time with global clock at IOE input register | |
| $t_{INH}$ | Hold time with global clock at IOE input register | |
| $t_{OUTCO}$ | Clock-to-output delay with global clock at IOE output register | C1 = 10 pF |
| $t_{INSUPLL}$ | Setup time with PLL clock at IOE input register | |
| $t_{INHPLL}$ | Hold time with PLL clock at IOE input register | |
| $t_{OUTCOPLL}$ | Clock-to-output delay with PLL clock at IOE output register | C1 = 10 pF |

| *Table 39. APEX 20KE External Bidirectional Timing Parameters* *Note (1)* | | |
|---|---|---|
| **Symbol** | **Parameter** | **Conditions** |
| $t_{INSUBIDIR}$ | Setup time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{INHBIDIR}$ | Hold time for bidirectional pins with global clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIR}$ | Clock-to-output delay for bidirectional pins with global clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIR}$ | Synchronous Output Enable Register to output buffer disable delay | C1 = 10 pF |
| $t_{ZXBIDIR}$ | Synchronous Output Enable Register output buffer enable delay | C1 = 10 pF |
| $t_{INSUBIDIRPLL}$ | Setup time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{INHBIDIRPLL}$ | Hold time for bidirectional pins with PLL clock at LAB adjacent Input Register | |
| $t_{OUTCOBIDIRPLL}$ | Clock-to-output delay for bidirectional pins with PLL clock at IOE output register | C1 = 10 pF |
| $t_{XZBIDIRPLL}$ | Synchronous Output Enable Register to output buffer disable delay with PLL | C1 = 10 pF |
| $t_{ZXBIDIRPLL}$ | Synchronous Output Enable Register output buffer enable delay with PLL | C1 = 10 pF |

***Note to Tables 38 and 39:***
(1) These timing parameters are sample-tested only.

Tables 40 through 42 show the $f_{MAX}$ timing parameters for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 40. EP20K100 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.6 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 41. EP20K200 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{H}$ | 0.7 | | 0.8 | | 1.0 | | ns |
| $t_{CO}$ | | 0.3 | | 0.4 | | 0.5 | ns |
| $t_{LUT}$ | | 0.8 | | 1.0 | | 1.3 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.6 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.0 | | 3.6 | ns |
| $t_{PTERMSU}$ | 2.3 | | 2.7 | | 3.2 | | ns |
| $t_{PTERMCO}$ | | 1.5 | | 1.8 | | 2.1 | ns |
| $t_{F1-4}$ | | 0.5 | | 0.6 | | 0.7 | ns |
| $t_{F5-20}$ | | 1.6 | | 1.7 | | 1.8 | ns |
| $t_{F20+}$ | | 2.2 | | 2.2 | | 2.3 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.3 | | 0.4 | | 0.4 | | ns |
| $t_{PREP}$ | 0.4 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.6 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.3 | | 1.4 | | ns |

*Table 42. EP20K400 $f_{MAX}$ Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Units |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.1 | | 0.3 | | 0.6 | | ns |
| $t_{H}$ | 0.5 | | 0.8 | | 0.9 | | ns |
| $t_{CO}$ | | 0.1 | | 0.4 | | 0.6 | ns |
| $t_{LUT}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{ESBRC}$ | | 1.7 | | 2.1 | | 2.4 | ns |
| $t_{ESBWC}$ | | 5.7 | | 6.9 | | 8.1 | ns |
| $t_{ESBWESU}$ | 3.3 | | 3.9 | | 4.6 | | ns |
| $t_{ESBDATASU}$ | 2.2 | | 2.7 | | 3.1 | | ns |
| $t_{ESBDATAH}$ | 0.6 | | 0.8 | | 0.9 | | ns |
| $t_{ESBADDRSU}$ | 2.4 | | 2.9 | | 3.3 | | ns |
| $t_{ESBDATACO1}$ | | 1.3 | | 1.6 | | 1.8 | ns |
| $t_{ESBDATACO2}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{ESBDD}$ | | 2.5 | | 3.3 | | 3.6 | ns |
| $t_{PD}$ | | 2.5 | | 3.1 | | 3.6 | ns |
| $t_{PTERMSU}$ | 1.7 | | 2.1 | | 2.4 | | ns |
| $t_{PTERMCO}$ | | 1.0 | | 1.2 | | 1.4 | ns |
| $t_{F1-4}$ | | 0.4 | | 0.5 | | 0.6 | ns |
| $t_{F5-20}$ | | 2.6 | | 2.8 | | 2.9 | ns |
| $t_{F20+}$ | | 3.7 | | 3.8 | | 3.9 | ns |
| $t_{CH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{CLRP}$ | 0.5 | | 0.6 | | 0.8 | | ns |
| $t_{PREP}$ | 0.5 | | 0.5 | | 0.5 | | ns |
| $t_{ESBCH}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBCL}$ | 2.0 | | 2.5 | | 3.0 | | ns |
| $t_{ESBWP}$ | 1.5 | | 1.9 | | 2.2 | | ns |
| $t_{ESBRP}$ | 1.0 | | 1.2 | | 1.4 | | ns |

Tables 43 through 48 show the I/O external and external bidirectional timing parameter values for EP20K100, EP20K200, and EP20K400 APEX 20K devices.

*Table 43. EP20K100 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ (1) | 2.3 | | 2.8 | | 3.2 | | ns |
| $t_{INH}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ (1) | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| $t_{INSU}$ (2) | 1.1 | | 1.2 | | – | | ns |
| $t_{INH}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ (2) | 0.5 | 2.7 | 0.5 | 3.1 | – | 4.8 | ns |

*Table 44. EP20K100 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (1) | 2.3 | | 2.8 | | 3.2 | | ns |
| $t_{INHBIDIR}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ (1) | 2.0 | 4.5 | 2.0 | 4.9 | 2.0 | 6.6 | ns |
| $t_{XZBIDIR}$ (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{ZXBIDIR}$ (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{INSUBIDIR}$ (2) | 1.0 | | 1.2 | | – | | ns |
| $t_{INHBIDIR}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (2) | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |
| $t_{XZBIDIR}$ (2) | | 4.3 | | 5.0 | | – | ns |
| $t_{ZXBIDIR}$ (2) | | 4.3 | | 5.0 | | – | ns |

*Table 45. EP20K200 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ (1) | 1.9 | | 2.3 | | 2.6 | | ns |
| $t_{INH}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ (1) | 2.0 | 4.6 | 2.0 | 5.6 | 2.0 | 6.8 | ns |
| $t_{INSU}$ (2) | 1.1 | | 1.2 | | – | | ns |
| $t_{INH}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ (2) | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |

*Table 46. EP20K200 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (1) | 1.9 | | 2.3 | | 2.6 | | ns |
| $t_{INHBIDIR}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ (1) | 2.0 | 4.6 | 2.0 | 5.6 | 2.0 | 6.8 | ns |
| $t_{XZBIDIR}$ (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{ZXBIDIR}$ (1) | | 5.0 | | 5.9 | | 6.9 | ns |
| $t_{INSUBIDIR}$ (2) | 1.1 | | 1.2 | | – | | ns |
| $t_{INHBIDIR}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (2) | 0.5 | 2.7 | 0.5 | 3.1 | – | – | ns |
| $t_{XZBIDIR}$ (2) | | 4.3 | | 5.0 | | – | ns |
| $t_{ZXBIDIR}$ (2) | | 4.3 | | 5.0 | | – | ns |

*Table 47. EP20K400 External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ (1) | 1.4 | | 1.8 | | 2.0 | | ns |
| $t_{INH}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCO}$ (1) | 2.0 | 4.9 | 2.0 | 6.1 | 2.0 | 7.0 | ns |
| $t_{INSU}$ (2) | 0.4 | | 1.0 | | – | | ns |
| $t_{INH}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCO}$ (2) | 0.5 | 3.1 | 0.5 | 4.1 | – | – | ns |

*Table 48. EP20K400 External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ (1) | 1.4 | | 1.8 | | 2.0 | | ns |
| $t_{INHBIDIR}$ (1) | 0.0 | | 0.0 | | 0.0 | | ns |
| $t_{OUTCOBIDIR}$ (1) | 2.0 | 4.9 | 2.0 | 6.1 | 2.0 | 7.0 | ns |
| $t_{XZBIDIR}$ (1) | | 7.3 | | 8.9 | | 10.3 | ns |
| $t_{ZXBIDIR}$ (1) | | 7.3 | | 8.9 | | 10.3 | ns |
| $t_{INSUBIDIR}$ (2) | 0.5 | | 1.0 | | – | | ns |
| $t_{INHBIDIR}$ (2) | 0.0 | | 0.0 | | – | | ns |
| $t_{OUTCOBIDIR}$ (2) | 0.5 | 3.1 | 0.5 | 4.1 | – | – | ns |
| $t_{XZBIDIR}$ (2) | | 6.2 | | 7.6 | | – | ns |
| $t_{ZXBIDIR}$ (2) | | 6.2 | | 7.6 | | – | ns |

*Notes to Tables 43 through 48:*
(1) This parameter is measured without using ClockLock or ClockBoost circuits.
(2) This parameter is measured using ClockLock or ClockBoost circuits.

Tables 49 through 54 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K30E APEX 20KE devices.

*Table 49. EP20K30E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.01 | | 0.02 | | 0.02 | | ns |
| $t_{H}$ | 0.11 | | 0.16 | | 0.23 | | ns |
| $t_{CO}$ | | 0.32 | | 0.45 | | 0.67 | ns |
| $t_{LUT}$ | | 0.85 | | 1.20 | | 1.77 | ns |

*Table 50. EP20K30E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 2.03 | | 2.86 | | 4.24 | ns |
| $t_{ESBSRC}$ | | 2.58 | | 3.49 | | 5.02 | ns |
| $t_{ESBAWC}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{ESBSWC}$ | | 4.08 | | 5.35 | | 7.48 | ns |
| $t_{ESBWASU}$ | 1.77 | | 2.49 | | 3.68 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.95 | | 2.74 | | 4.05 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.96 | | 2.75 | | 4.07 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.80 | | 2.73 | | 4.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.48 | | 1.17 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.30 | | 0.80 | | 1.64 | | ns |
| $t_{ESBRADDRSU}$ | 0.37 | | 0.90 | | 1.78 | | ns |
| $t_{ESBDATACO1}$ | | 1.11 | | 1.32 | | 1.67 | ns |
| $t_{ESBDATACO2}$ | | 2.65 | | 3.73 | | 5.53 | ns |
| $t_{ESBDD}$ | | 3.88 | | 5.45 | | 8.08 | ns |
| $t_{PD}$ | | 1.91 | | 2.69 | | 3.98 | ns |
| $t_{PTERMSU}$ | 1.04 | | 1.71 | | 2.82 | | ns |
| $t_{PTERMCO}$ | | 1.13 | | 1.34 | | 1.69 | ns |

*Table 51. EP20K30E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.31 | ns |
| $t_{F5-20}$ | | 1.03 | | 1.14 | | 1.30 | ns |
| $t_{F20+}$ | | 1.42 | | 1.54 | | 1.77 | ns |

*Table 52. EP20K30E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{CLRP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{PREP}$ | 0.22 | | 0.31 | | 0.46 | | ns |
| $t_{ESBCH}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBCL}$ | 0.55 | | 0.78 | | 1.15 | | ns |
| $t_{ESBWP}$ | 1.43 | | 2.01 | | 2.97 | | ns |
| $t_{ESBRP}$ | 1.15 | | 1.62 | | 2.39 | | ns |

*Table 53. EP20K30E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.02 | | 2.13 | | 2.24 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{INSUPLL}$ | 2.11 | | 2.23 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |

*Table 54. EP20K30E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 1.85 | | 1.77 | | 1.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.88 | 2.00 | 5.36 | 2.00 | 5.88 | ns |
| $t_{XZBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{ZXBIDIR}$ | | 7.48 | | 8.46 | | 9.83 | ns |
| $t_{INSUBIDIRPLL}$ | 4.12 | | 4.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.60 | 0.50 | 2.88 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.21 | | 5.99 | | - | ns |

Tables 55 through 60 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K60E APEX 20KE devices.

*Table 55. EP20K60E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.17 | | 0.15 | | 0.16 | | ns |
| $t_{H}$ | 0.32 | | 0.33 | | 0.39 | | ns |
| $t_{CO}$ | | 0.29 | | 0.40 | | 0.60 | ns |
| $t_{LUT}$ | | 0.77 | | 1.07 | | 1.59 | ns |

*Table 56. EP20K60E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.83 | | 2.57 | | 3.79 | ns |
| $t_{ESBSRC}$ | | 2.46 | | 3.26 | | 4.61 | ns |
| $t_{ESBAWC}$ | | 3.50 | | 4.90 | | 7.23 | ns |
| $t_{ESBSWC}$ | | 3.77 | | 4.90 | | 6.79 | ns |
| $t_{ESBWASU}$ | 1.59 | | 2.23 | | 3.29 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.75 | | 2.46 | | 3.62 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.76 | | 2.47 | | 3.64 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.68 | | 2.49 | | 3.87 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.08 | | 0.43 | | 1.04 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.29 | | 0.72 | | 1.46 | | ns |
| $t_{ESBRADDRSU}$ | 0.36 | | 0.81 | | 1.58 | | ns |
| $t_{ESBDATACO1}$ | | 1.06 | | 1.24 | | 1.55 | ns |
| $t_{ESBDATACO2}$ | | 2.39 | | 3.35 | | 4.94 | ns |
| $t_{ESBDD}$ | | 3.50 | | 4.90 | | 7.23 | ns |
| $t_{PD}$ | | 1.72 | | 2.41 | | 3.56 | ns |
| $t_{PTERMSU}$ | 0.99 | | 1.56 | | 2.55 | | ns |
| $t_{PTERMCO}$ | | 1.07 | | 1.26 | | 1.08 | ns |

*Table 57. EP20K60E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.26 | | 0.30 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.58 | | 1.79 | ns |
| $t_{F20+}$ | | 1.96 | | 2.14 | | 2.45 | ns |

*Table 58. EP20K60E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{PREP}$ | 0.20 | | 0.28 | | 0.41 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.80 | | 2.66 | | ns |
| $t_{ESBRP}$ | 1.04 | | 1.45 | | 2.14 | | ns |

*Table 59. EP20K60E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.03 | | 2.12 | | 2.23 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{INSUPLL}$ | 1.12 | | 1.15 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |

*Table 60. EP20K60E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.91 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.84 | 2.00 | 5.31 | 2.00 | 5.81 | ns |
| $t_{XZBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{ZXBIDIR}$ | | 6.47 | | 7.44 | | 8.65 | ns |
| $t_{INSUBIDIRPLL}$ | 3.44 | | 3.24 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.37 | 0.50 | 3.69 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.82 | | - | ns |

Tables 61 through 66 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K100E APEX 20KE devices.

*Table 61. EP20K100E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.28 | | 0.34 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

*Table 62. EP20K100E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.61 | | 1.84 | | 1.97 | ns |
| $t_{ESBSRC}$ | | 2.57 | | 2.97 | | 3.20 | ns |
| $t_{ESBAWC}$ | | 0.52 | | 4.09 | | 4.39 | ns |
| $t_{ESBSWC}$ | | 3.17 | | 3.78 | | 4.09 | ns |
| $t_{ESBWASU}$ | 0.56 | | 6.41 | | 0.63 | | ns |
| $t_{ESBWAH}$ | 0.48 | | 0.54 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.71 | | 0.80 | | 0.81 | | ns |
| $t_{ESBWDH}$ | .048 | | 0.54 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.57 | | 1.75 | | 1.87 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.20 | | ns |
| $t_{ESBWESU}$ | 1.54 | | 1.72 | | 1.80 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.16 | | -0.20 | | -0.20 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.12 | | 0.08 | | 0.13 | | ns |
| $t_{ESBRADDRSU}$ | 0.17 | | 0.15 | | 0.19 | | ns |
| $t_{ESBDATACO1}$ | | 1.20 | | 1.39 | | 1.52 | ns |
| $t_{ESBDATACO2}$ | | 2.54 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.06 | | 3.56 | | 3.85 | ns |
| $t_{PD}$ | | 1.73 | | 2.02 | | 2.20 | ns |
| $t_{PTERMSU}$ | 1.11 | | 1.26 | | 1.38 | | ns |
| $t_{PTERMCO}$ | | 1.19 | | 1.40 | | 1.08 | ns |

*Table 63. EP20K100E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.24 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.04 | | 1.26 | | 1.52 | ns |
| $t_{F20+}$ | | 1.12 | | 1.36 | | 1.86 | ns |

*Table 64. EP20K100E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.00 | | 2.00 | | ns |
| $t_{ESBWP}$ | 1.29 | | 1.53 | | 1.66 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 65. EP20K100E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.23 | | 2.32 | | 2.43 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{INSUPLL}$ | 1.58 | | 1.66 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |

*Table 66. EP20K100E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.74 | | 2.96 | | 3.19 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 4.86 | 2.00 | 5.35 | 2.00 | 5.84 | ns |
| $t_{XZBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{ZXBIDIR}$ | | 5.00 | | 5.48 | | 5.89 | ns |
| $t_{INSUBIDIRPLL}$ | 4.64 | | 5.03 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.96 | 0.50 | 3.29 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 3.10 | | 3.42 | | - | ns |

Tables 67 through 72 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K160E APEX 20KE devices.

*Table 67. EP20K160E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.22 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.25 | | 0.31 | | 0.35 | ns |
| $t_{LUT}$ | | 0.69 | | 0.88 | | 1.12 | ns |

*Table 68. EP20K160E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.65 | | 2.02 | | 2.11 | ns |
| $t_{ESBSRC}$ | | 2.21 | | 2.70 | | 3.11 | ns |
| $t_{ESBAWC}$ | | 3.04 | | 3.79 | | 4.42 | ns |
| $t_{ESBSWC}$ | | 2.81 | | 3.56 | | 4.10 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.66 | | 0.73 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBWDSU}$ | 0.68 | | 0.81 | | 0.94 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.45 | | 0.47 | | ns |
| $t_{ESBRASU}$ | 1.58 | | 1.87 | | 2.06 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.41 | | 1.71 | | 2.00 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.02 | | -0.03 | | 0.09 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.14 | | 0.17 | | 0.35 | | ns |
| $t_{ESBRADDRSU}$ | 0.21 | | 0.27 | | 0.43 | | ns |
| $t_{ESBDATACO1}$ | | 1.04 | | 1.30 | | 1.46 | ns |
| $t_{ESBDATACO2}$ | | 2.15 | | 2.70 | | 3.16 | ns |
| $t_{ESBDD}$ | | 2.69 | | 3.35 | | 3.97 | ns |
| $t_{PD}$ | | 1.55 | | 1.93 | | 2.29 | ns |
| $t_{PTERMSU}$ | 1.01 | | 1.23 | | 1.52 | | ns |
| $t_{PTERMCO}$ | | 1.06 | | 1.32 | | 1.04 | ns |

*Table 69. EP20K160E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.26 | | 0.28 | ns |
| $t_{F5-20}$ | | 1.00 | | 1.18 | | 1.35 | ns |
| $t_{F20+}$ | | 1.95 | | 2.19 | | 2.30 | ns |

*Table 70. EP20K160E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{CL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{PREP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{ESBCH}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{ESBCL}$ | 1.34 | | 1.43 | | 1.55 | | ns |
| $t_{ESBWP}$ | 1.15 | | 1.45 | | 1.73 | | ns |
| $t_{ESBRP}$ | 0.93 | | 1.15 | | 1.38 | | ns |

*Table 71. EP20K160E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.23 | | 2.34 | | 2.47 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{INSUPLL}$ | 2.12 | | 2.07 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |

*Table 72. EP20K160E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.86 | | 3.24 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.07 | 2.00 | 5.59 | 2.00 | 6.13 | ns |
| $t_{XZBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{ZXBIDIR}$ | | 7.43 | | 8.23 | | 8.58 | ns |
| $t_{INSUBIDIRPLL}$ | 4.93 | | 5.48 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.00 | 0.50 | 3.35 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.36 | | 5.99 | | - | ns |

Tables 73 through 78 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K200E APEX 20KE devices.

*Table 73. EP20K200E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{H}$ | 0.23 | | 0.24 | | 0.26 | | ns |
| $t_{CO}$ | | 0.26 | | 0.31 | | 0.36 | ns |
| $t_{LUT}$ | | 0.70 | | 0.90 | | 1.14 | ns |

*Table 74. EP20K200E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.68 | | 2.06 | | 2.24 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 2.77 | | 3.18 | ns |
| $t_{ESBAWC}$ | | 3.10 | | 3.86 | | 4.50 | ns |
| $t_{ESBSWC}$ | | 2.90 | | 3.67 | | 4.21 | ns |
| $t_{ESBWASU}$ | 0.55 | | 0.67 | | 0.74 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.83 | | 0.95 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.46 | | 0.48 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.90 | | 2.09 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.42 | | 1.71 | | 2.01 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.06 | | -0.07 | | 0.05 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.13 | | 0.31 | | ns |
| $t_{ESBRADDRSU}$ | 0.18 | | 0.23 | | 0.39 | | ns |
| $t_{ESBDATACO1}$ | | 1.09 | | 1.35 | | 1.51 | ns |
| $t_{ESBDATACO2}$ | | 2.19 | | 2.75 | | 3.22 | ns |
| $t_{ESBDD}$ | | 2.75 | | 3.41 | | 4.03 | ns |
| $t_{PD}$ | | 1.58 | | 1.97 | | 2.33 | ns |
| $t_{PTERMSU}$ | 1.00 | | 1.22 | | 1.51 | | ns |
| $t_{PTERMCO}$ | | 1.10 | | 1.37 | | 1.09 | ns |

*Table 75. EP20K200E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.27 | | 0.29 | ns |
| $t_{F5-20}$ | | 1.02 | | 1.20 | | 1.41 | ns |
| $t_{F20+}$ | | 1.99 | | 2.23 | | 2.53 | ns |

*Table 76. EP20K200E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{CL}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{PREP}$ | 0.18 | | 0.19 | | 0.21 | | ns |
| $t_{ESBCH}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{ESBCL}$ | 1.36 | | 2.44 | | 2.65 | | ns |
| $t_{ESBWP}$ | 1.18 | | 1.48 | | 1.76 | | ns |
| $t_{ESBRP}$ | 0.95 | | 1.17 | | 1.41 | | ns |

*Table 77. EP20K200E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.24 | | 2.35 | | 2.47 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{INSUPLL}$ | 2.13 | | 2.07 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |

*Table 78. EP20K200E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.81 | | 3.19 | | 3.54 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.12 | 2.00 | 5.62 | 2.00 | 6.11 | ns |
| $t_{XZBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{ZXBIDIR}$ | | 7.51 | | 8.32 | | 8.67 | ns |
| $t_{INSUBIDIRPLL}$ | 3.30 | | 3.64 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 3.01 | 0.50 | 3.36 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.40 | | 6.05 | | - | ns |

Tables 79 through 84 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K300E APEX 20KE devices.

*Table 79. EP20K300E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.17 | | 0.18 | | ns |
| $t_{H}$ | 0.31 | | 0.33 | | 0.38 | | ns |
| $t_{CO}$ | | 0.28 | | 0.38 | | 0.51 | ns |
| $t_{LUT}$ | | 0.79 | | 1.07 | | 1.43 | ns |

*Table 80. EP20K300E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.79 | | 2.44 | | 3.25 | ns |
| $t_{ESBSRC}$ | | 2.40 | | 3.12 | | 4.01 | ns |
| $t_{ESBAWC}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{ESBSWC}$ | | 3.68 | | 4.68 | | 5.93 | ns |
| $t_{ESBWASU}$ | 1.55 | | 2.12 | | 2.83 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.71 | | 2.33 | | 3.11 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.72 | | 2.34 | | 3.13 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.63 | | 2.36 | | 3.28 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.07 | | 0.39 | | 0.80 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.27 | | 0.67 | | 1.17 | | ns |
| $t_{ESBRADDRSU}$ | 0.34 | | 0.75 | | 1.28 | | ns |
| $t_{ESBDATACO1}$ | | 1.03 | | 1.20 | | 1.40 | ns |
| $t_{ESBDATACO2}$ | | 2.33 | | 3.18 | | 4.24 | ns |
| $t_{ESBDD}$ | | 3.41 | | 4.65 | | 6.20 | ns |
| $t_{PD}$ | | 1.68 | | 2.29 | | 3.06 | ns |
| $t_{PTERMSU}$ | 0.96 | | 1.48 | | 2.14 | | ns |
| $t_{PTERMCO}$ | | 1.05 | | 1.22 | | 1.42 | ns |

*Table 81. EP20K300E $f_{MAX}$ Routing Delays*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.24 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.33 | | 1.43 | | 1.58 | ns |
| $t_{F20+}$ | | 3.63 | | 3.93 | | 4.35 | ns |

*Table 82. EP20K300E Minimum Pulse Width Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{PREP}$ | 0.19 | | 0.26 | | 0.35 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.25 | | 1.71 | | 2.28 | | ns |
| $t_{ESBRP}$ | 1.01 | | 1.38 | | 1.84 | | ns |

*Table 83. EP20K300E External Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.31 | | 2.44 | | 2.57 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{INSUPLL}$ | 1.76 | | 1.85 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |

*Table 84. EP20K300E External Bidirectional Timing Parameters*

| Symbol | -1 | | -2 | | -3 | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.77 | | 2.85 | | 3.11 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.29 | 2.00 | 5.82 | 2.00 | 6.24 | ns |
| $t_{XZBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{ZXBIDIR}$ | | 7.59 | | 8.30 | | 9.09 | ns |
| $t_{INSUBIDIRPLL}$ | 2.50 | | 2.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.65 | 0.50 | 2.95 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 5.00 | | 5.43 | | - | ns |

Tables 85 through 90 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K400E APEX 20KE devices.

*Table 85. EP20K400E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{H}$ | 0.23 | | 0.23 | | 0.23 | | ns |
| $t_{CO}$ | | 0.25 | | 0.29 | | 0.32 | ns |
| $t_{LUT}$ | | 0.70 | | 0.83 | | 1.01 | ns |

*Table 86. EP20K400E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 1.91 | | 1.99 | ns |
| $t_{ESBSRC}$ | | 2.30 | | 2.66 | | 2.93 | ns |
| $t_{ESBAWC}$ | | 3.09 | | 3.58 | | 3.99 | ns |
| $t_{ESBSWC}$ | | 3.01 | | 3.65 | | 4.05 | ns |
| $t_{ESBWASU}$ | 0.54 | | 0.63 | | 0.65 | | ns |
| $t_{ESBWAH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBWDSU}$ | 0.69 | | 0.77 | | 0.84 | | ns |
| $t_{ESBWDH}$ | 0.36 | | 0.43 | | 0.42 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 1.77 | | 1.86 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.01 | | ns |
| $t_{ESBWESU}$ | 1.35 | | 1.47 | | 1.61 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.18 | | -0.30 | | -0.27 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | -0.02 | | -0.11 | | -0.03 | | ns |
| $t_{ESBRADDRSU}$ | 0.06 | | -0.01 | | -0.05 | | ns |
| $t_{ESBDATACO1}$ | | 1.16 | | 1.40 | | 1.54 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 2.55 | | 2.85 | ns |
| $t_{ESBDD}$ | | 2.73 | | 3.17 | | 3.58 | ns |
| $t_{PD}$ | | 1.57 | | 1.83 | | 2.07 | ns |
| $t_{PTERMSU}$ | 0.92 | | 0.99 | | 1.18 | | ns |
| $t_{PTERMCO}$ | | 1.18 | | 1.43 | | 1.17 | ns |

*Table 87. EP20K400E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.25 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.01 | | 1.12 | | 1.25 | ns |
| $t_{F20+}$ | | 3.71 | | 3.92 | | 4.17 | ns |

*Table 88. EP20K400E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.36 | | 2.22 | | 2.35 | | ns |
| $t_{CL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{PREP}$ | 0.18 | | 0.18 | | 0.19 | | ns |
| $t_{ESBCH}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBCL}$ | 1.36 | | 2.26 | | 2.35 | | ns |
| $t_{ESBWP}$ | 1.17 | | 1.38 | | 1.56 | | ns |
| $t_{ESBRP}$ | 0.94 | | 1.09 | | 1.25 | | ns |

*Table 89. EP20K400E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.51 | | 2.64 | | 2.77 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{INSUPLL}$ | 3.221 | | 3.38 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |

*Table 90. EP20K400E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 2.93 | | 3.23 | | 3.44 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.25 | 2.00 | 5.79 | 2.00 | 6.32 | ns |
| $t_{XZBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{ZXBIDIR}$ | | 5.95 | | 6.77 | | 7.12 | ns |
| $t_{INSUBIDIRPLL}$ | 4.31 | | 4.76 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.45 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 2.94 | | 3.43 | | - | ns |

Tables 91 through 96 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K600E APEX 20KE devices.

*Table 91. EP20K600E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.16 | | 0.16 | | 0.17 | | ns |
| $t_{H}$ | 0.29 | | 0.33 | | 0.37 | | ns |
| $t_{CO}$ | | 0.65 | | 0.38 | | 0.49 | ns |
| $t_{LUT}$ | | 0.70 | | 1.00 | | 1.30 | ns |

*Table 92. EP20K600E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.67 | | 2.39 | | 3.11 | ns |
| $t_{ESBSRC}$ | | 2.27 | | 3.07 | | 3.86 | ns |
| $t_{ESBAWC}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{ESBSWC}$ | | 3.51 | | 4.62 | | 5.72 | ns |
| $t_{ESBWASU}$ | 1.46 | | 2.08 | | 2.70 | | ns |
| $t_{ESBWAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWDSU}$ | 1.60 | | 2.29 | | 2.97 | | ns |
| $t_{ESBWDH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBRASU}$ | 1.61 | | 2.30 | | 2.99 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBWESU}$ | 1.49 | | 2.30 | | 3.11 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | -0.01 | | 0.35 | | 0.71 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.19 | | 0.62 | | 1.06 | | ns |
| $t_{ESBRADDRSU}$ | 0.25 | | 0.71 | | 1.17 | | ns |
| $t_{ESBDATACO1}$ | | 1.01 | | 1.19 | | 1.37 | ns |
| $t_{ESBDATACO2}$ | | 2.18 | | 3.12 | | 4.05 | ns |
| $t_{ESBDD}$ | | 3.19 | | 4.56 | | 5.93 | ns |
| $t_{PD}$ | | 1.57 | | 2.25 | | 2.92 | ns |
| $t_{PTERMSU}$ | 0.85 | | 1.43 | | 2.01 | | ns |
| $t_{PTERMCO}$ | | 1.03 | | 1.21 | | 1.39 | ns |

*Table 93. EP20K600E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.22 | | 0.25 | | 0.26 | ns |
| $t_{F5-20}$ | | 1.26 | | 1.39 | | 1.52 | ns |
| $t_{F20+}$ | | 3.51 | | 3.88 | | 4.26 | ns |

*Table 94. EP20K600E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{CLRP}$ | 0.18 | | 0.26 | | 0.34 | | ns |
| $t_{PREP}$ | 0.18 | | 0.26 | | 0.34 | | ns |
| $t_{ESBCH}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBCL}$ | 2.00 | | 2.50 | | 2.75 | | ns |
| $t_{ESBWP}$ | 1.17 | | 1.68 | | 2.18 | | ns |
| $t_{ESBRP}$ | 0.95 | | 1.35 | | 1.76 | | ns |

*Table 95. EP20K600E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.74 | | 2.74 | | 2.87 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| $t_{INSUPLL}$ | 1.86 | | 1.96 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |

*Table 96. EP20K600E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 0.64 | | 0.98 | | 1.08 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.51 | 2.00 | 6.06 | 2.00 | 6.61 | ns |
| $t_{XZBIDIR}$ | | 6.10 | | 6.74 | | 7.10 | ns |
| $t_{ZXBIDIR}$ | | 6.10 | | 6.74 | | 7.10 | ns |
| $t_{INSUBIDIRPLL}$ | 2.26 | | 2.68 | | - | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.62 | 0.50 | 2.91 | - | - | ns |
| $t_{XZBIDIRPLL}$ | | 3.21 | | 3.59 | | - | ns |
| $t_{ZXBIDIRPLL}$ | | 3.21 | | 3.59 | | - | ns |

Tables 97 through 102 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1000E APEX 20KE devices.

*Table 97. EP20K1000E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

*Table 98. EP20K1000E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |

*Table 99. EP20K1000E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.27 | | 0.27 | | 0.27 | ns |
| $t_{F5-20}$ | | 1.45 | | 1.63 | | 1.75 | ns |
| $t_{F20+}$ | | 4.15 | | 4.33 | | 4.97 | ns |

*Table 100. EP20K1000E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 101. EP20K1000E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 2.70 | | 2.84 | | 2.97 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{INSUPLL}$ | 1.64 | | 2.09 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | - | - | ns |

*Table 102. EP20K1000E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.22 | | 3.33 | | 3.51 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 5.75 | 2.00 | 6.33 | 2.00 | 6.90 | ns |
| $t_{XZBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{ZXBIDIR}$ | | 6.31 | | 7.09 | | 7.76 | ns |
| $t_{INSUBIDIRPLL}$ | 3.25 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.25 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 2.81 | | 3.80 | | | ns |

Tables 103 through 108 describe $f_{MAX}$ LE Timing Microparameters, $f_{MAX}$ ESB Timing Microparameters, $f_{MAX}$ Routing Delays, Minimum Pulse Width Timing Parameters, External Timing Parameters, and External Bidirectional Timing Parameters for EP20K1500E APEX 20KE devices.

*Table 103. EP20K1500E $f_{MAX}$ LE Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{SU}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{H}$ | 0.25 | | 0.25 | | 0.25 | | ns |
| $t_{CO}$ | | 0.28 | | 0.32 | | 0.33 | ns |
| $t_{LUT}$ | | 0.80 | | 0.95 | | 1.13 | ns |

*Table 104. EP20K1500E $f_{MAX}$ ESB Timing Microparameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{ESBARC}$ | | 1.78 | | 2.02 | | 1.95 | ns |
| $t_{ESBSRC}$ | | 2.52 | | 2.91 | | 3.14 | ns |
| $t_{ESBAWC}$ | | 3.52 | | 4.11 | | 4.40 | ns |
| $t_{ESBSWC}$ | | 3.23 | | 3.84 | | 4.16 | ns |
| $t_{ESBWASU}$ | 0.62 | | 0.67 | | 0.61 | | ns |
| $t_{ESBWAH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBWDSU}$ | 0.77 | | 0.79 | | 0.81 | | ns |
| $t_{ESBWDH}$ | 0.41 | | 0.55 | | 0.55 | | ns |
| $t_{ESBRASU}$ | 1.74 | | 1.92 | | 1.85 | | ns |
| $t_{ESBRAH}$ | 0.00 | | 0.01 | | 0.23 | | ns |
| $t_{ESBWESU}$ | 2.07 | | 2.28 | | 2.41 | | ns |
| $t_{ESBWEH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{ESBDATASU}$ | 0.25 | | 0.27 | | 0.29 | | ns |
| $t_{ESBDATAH}$ | 0.13 | | 0.13 | | 0.13 | | ns |
| $t_{ESBWADDRSU}$ | 0.11 | | 0.04 | | 0.11 | | ns |
| $t_{ESBRADDRSU}$ | 0.14 | | 0.11 | | 0.16 | | ns |
| $t_{ESBDATACO1}$ | | 1.29 | | 1.50 | | 1.63 | ns |
| $t_{ESBDATACO2}$ | | 2.55 | | 2.99 | | 3.22 | ns |
| $t_{ESBDD}$ | | 3.12 | | 3.57 | | 3.85 | ns |
| $t_{PD}$ | | 1.84 | | 2.13 | | 2.32 | ns |
| $t_{PTERMSU}$ | 1.08 | | 1.19 | | 1.32 | | ns |
| $t_{PTERMCO}$ | | 1.31 | | 1.53 | | 1.66 | ns |

*Table 105. EP20K1500E $f_{MAX}$ Routing Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{F1-4}$ | | 0.28 | | 0.28 | | 0.28 | ns |
| $t_{F5-20}$ | | 1.36 | | 1.50 | | 1.62 | ns |
| $t_{F20+}$ | | 4.43 | | 4.48 | | 5.07 | ns |

*Table 106. EP20K1500E Minimum Pulse Width Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{CH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{CLRP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{PREP}$ | 0.20 | | 0.20 | | 0.20 | | ns |
| $t_{ESBCH}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBCL}$ | 1.25 | | 1.43 | | 1.67 | | ns |
| $t_{ESBWP}$ | 1.28 | | 1.51 | | 1.65 | | ns |
| $t_{ESBRP}$ | 1.11 | | 1.29 | | 1.41 | | ns |

*Table 107. EP20K1500E External Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSU}$ | 3.09 | | 3.30 | | 3.58 | | ns |
| $t_{INH}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCO}$ | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| $t_{INSUPLL}$ | 1.94 | | 2.08 | | - | | ns |
| $t_{INHPLL}$ | 0.00 | | 0.00 | | - | | ns |
| $t_{OUTCOPLL}$ | 0.50 | 2.67 | 0.50 | 2.99 | - | - | ns |

*Table 108. EP20K1500E External Bidirectional Timing Parameters*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | |
| $t_{INSUBIDIR}$ | 3.47 | | 3.68 | | 3.99 | | ns |
| $t_{INHBIDIR}$ | 0.00 | | 0.00 | | 0.00 | | ns |
| $t_{OUTCOBIDIR}$ | 2.00 | 6.18 | 2.00 | 6.81 | 2.00 | 7.36 | ns |
| $t_{XZBIDIR}$ | | 6.91 | | 7.62 | | 8.38 | ns |
| $t_{ZXBIDIR}$ | | 6.91 | | 7.62 | | 8.38 | ns |
| $t_{INSUBIDIRPLL}$ | 3.05 | | 3.26 | | | | ns |
| $t_{INHBIDIRPLL}$ | 0.00 | | 0.00 | | | | ns |
| $t_{OUTCOBIDIRPLL}$ | 0.50 | 2.67 | 0.50 | 2.99 | | | ns |
| $t_{XZBIDIRPLL}$ | | 3.41 | | 3.80 | | | ns |
| $t_{ZXBIDIRPLL}$ | | 3.41 | | 3.80 | | | ns |

Tables 109 and 110 show selectable I/O standard input and output delays for APEX 20KE devices. If you select an I/O standard input or output delay other than LVCMOS, add or subtract the selected speed grade to or from the LVCMOS value.

*Table 109. Selectable I/O Standard Input Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.04 | | 0.05 | ns |
| 1.8 V | | –0.11 | | 0.03 | | 0.04 | ns |
| PCI | | 0.01 | | 0.09 | | 0.10 | ns |
| GTL+ | | –0.24 | | –0.23 | | –0.19 | ns |
| SSTL-3 Class I | | –0.32 | | –0.21 | | –0.47 | ns |
| SSTL-3 Class II | | –0.08 | | 0.03 | | –0.23 | ns |
| SSTL-2 Class I | | –0.17 | | –0.06 | | –0.32 | ns |
| SSTL-2 Class II | | –0.16 | | –0.05 | | –0.31 | ns |
| LVDS | | –0.12 | | –0.12 | | –0.12 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

*Table 110. Selectable I/O Standard Output Delays*

| Symbol | -1 Speed Grade | | -2 Speed Grade | | -3 Speed Grade | | Unit |
|---|---|---|---|---|---|---|---|
| | Min | Max | Min | Max | Min | Max | Min |
| LVCMOS | | 0.00 | | 0.00 | | 0.00 | ns |
| LVTTL | | 0.00 | | 0.00 | | 0.00 | ns |
| 2.5 V | | 0.00 | | 0.09 | | 0.10 | ns |
| 1.8 V | | 2.49 | | 2.98 | | 3.03 | ns |
| PCI | | –0.03 | | 0.17 | | 0.16 | ns |
| GTL+ | | 0.75 | | 0.75 | | 0.76 | ns |
| SSTL-3 Class I | | 1.39 | | 1.51 | | 1.50 | ns |
| SSTL-3 Class II | | 1.11 | | 1.23 | | 1.23 | ns |
| SSTL-2 Class I | | 1.35 | | 1.48 | | 1.47 | ns |
| SSTL-2 Class II | | 1.00 | | 1.12 | | 1.12 | ns |
| LVDS | | –0.48 | | –0.48 | | –0.48 | ns |
| CTT | | 0.00 | | 0.00 | | 0.00 | ns |
| AGP | | 0.00 | | 0.00 | | 0.00 | ns |

# Power Consumption

To estimate device power consumption, use the interactive power calculator on the Altera web site at **http://www.altera.com**.

# Configuration & Operation

The APEX 20K architecture supports several configuration schemes. This section summarizes the device operating modes and available device configuration schemes.

## Operating Modes

The APEX architecture uses SRAM configuration elements that require configuration data to be loaded each time the circuit powers up. The process of physically loading the SRAM data into the device is called configuration. During initialization, which occurs immediately after configuration, the device resets registers, enables I/O pins, and begins to operate as a logic device. The I/O pins are tri-stated during power-up, and before and during configuration. Together, the configuration and initialization processes are called *command mode*; normal device operation is called *user mode*.

Before and during device configuration, all I/O pins are pulled to $V_{CCIO}$ by a built-in weak pull-up resistor.

SRAM configuration elements allow APEX 20K devices to be reconfigured in-circuit by loading new configuration data into the device. Real-time reconfiguration is performed by forcing the device into command mode with a device pin, loading different configuration data, reinitializing the device, and resuming user-mode operation. In-field upgrades can be performed by distributing new configuration files.

### Configuration Schemes

The configuration data for an APEX 20K device can be loaded with one of five configuration schemes (see Table 111), chosen on the basis of the target application. An EPC2 or EPC16 configuration device, intelligent controller, or the JTAG port can be used to control the configuration of an APEX 20K device. When a configuration device is used, the system can configure automatically at system power-up.

Multiple APEX 20K devices can be configured in any of five configuration schemes by connecting the configuration enable (nCE) and configuration enable output (nCEO) pins on each device.

*Table 111. Data Sources for Configuration*

| Configuration Scheme | Data Source |
|---|---|
| Configuration device | EPC1, EPC2, EPC16 configuration devices |
| Passive serial (PS) | MasterBlaster or ByteBlasterMV download cable or serial data source |
| Passive parallel asynchronous (PPA) | Parallel data source |
| Passive parallel synchronous (PPS) | Parallel data source |
| JTAG | MasterBlaster or ByteBlasterMV download cable or a microprocessor with a Jam or JBC File |

For more information on configuration, see *Application Note 116 (Configuring APEX 20K, FLEX 10K, & FLEX 6000 Devices.)*

## Device Pin-Outs

See the Altera web site **(http://www.altera.com)** or the ***Altera Digital Library*** for pin-out information

# Revision History

The information contained in the *APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 supersedes information published in previous versions.

## Version 5.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.1 contains the following changes:

- In version 5.0, the VI input voltage spec was updated in Table 28 on page 63.
- In version 5.0, *Note (5)* to Tables 27 through 30 was revised.
- Added *Note (2)* to Figure 21 on page 33.

## Version 5.0

*APEX 20K Programmable Logic Device Family Data Sheet* version 5.0 contains the following changes:

- Updated Tables 23 through 26. Removed 2.5-V operating condition tables because all APEX 20K devices are now 5.0-V tolerant.
- Updated conditions in Tables 33, 38 and 39.
- Updated data for $t_{ESBDATAH}$ parameter.

## Version 4.3

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.3 contains the following changes:

- Updated Figure 20.
- Updated *Note (2)* to Table 13.
- Updated notes to Tables 27 through 30.

## Version 4.2

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.2 contains the following changes:

- Updated Figure 29.
- Updated *Note (1)* to Figure 29.

## Version 4.1

*APEX 20K Programmable Logic Device Family Data Sheet* version 4.1 contains the following changes:

- $t_{ESBWEH}$ added to Figure 37 and Tables 35, 50, 56, 62, 68, 74, 86, 92, 97, and 104.
- Updated EP20K300E device internal and external timing numbers in Tables 79 through 84.

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