

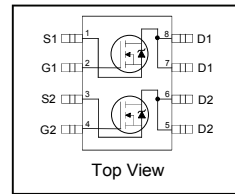


**THE DATASHEET OF
AUIRF7341QTR**



Features

- Advanced Planar Technology
- Ultra Low On-Resistance
- Logic Level Gate Drive
- Dual N Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 175°C Operating Temperature
- Lead-Free, RoHS Compliant
- Automotive Qualified *



| | | |
|--------------|------|---------------|
| V_{DS} | | 55V |
| $R_{DS(on)}$ | typ. | 0.043Ω |
| | max. | 0.050Ω |
| I_D | | 5.1A |



| | | |
|----------|----------|----------|
| G | D | S |
| Gate | Drain | Source |

Description

Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications. The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.

| Base part number | Package Type | Standard Pack | | Orderable Part Number |
|------------------|--------------|---------------|----------|-----------------------|
| | | Form | Quantity | |
| AUIRF7341Q | SO-8 | Tape and Reel | 4000 | AUIRF7341QTR |

Absolute Maximum Ratings

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

| Symbol | Parameter | Max. | Units |
|--------------------------|---|--------------------------|-------|
| V_{DS} | Drain-Source Voltage | 55 | V |
| $I_D @ T_A = 25^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 5.1 | A |
| $I_D @ T_A = 70^\circ C$ | Continuous Drain Current, $V_{GS} @ 10V$ | 4.2 | |
| I_{DM} | Pulsed Drain Current ① | 42 | |
| $P_D @ T_A = 25^\circ C$ | Maximum Power Dissipation ③ | 2.4 | W |
| $P_D @ T_A = 70^\circ C$ | Maximum Power Dissipation ③ | 1.7 | |
| | Linear Derating Factor | 16 | mW/°C |
| V_{GS} | Gate-to-Source Voltage | ± 20 | V |
| E_{AS} | Single Pulse Avalanche Energy (Thermally Limited) ② | 140 | mJ |
| I_{AR} | Avalanche Current | 5.1 | A |
| E_{AR} | Repetitive Avalanche Energy | See Fig.17, 18, 15a, 15b | mJ |
| T_J | Operating Junction and | -55 to + 175 | °C |
| T_{STG} | Storage Temperature Range | | |

Thermal Resistance

| Symbol | Parameter | Typ. | Max. | Units |
|-----------------|-----------------------|------|------|-------|
| $R_{\theta JA}$ | Junction-to-Ambient ④ | — | 62.5 | °C/W |

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*Qualification standards can be found at www.infineon.com

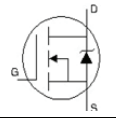
Static @ T_J = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|--|--------------------------------------|------|-------|-------|-------|---|
| V _{(BR)DSS} | Drain-to-Source Breakdown Voltage | 55 | — | — | V | V _{GS} = 0V, I _D = 250μA |
| ΔV _{(BR)DSS} /ΔT _J | Breakdown Voltage Temp. Coefficient | — | 0.052 | — | V/°C | Reference to 25°C, I _D = 1mA |
| R _{DS(on)} | Static Drain-to-Source On-Resistance | — | 0.043 | 0.050 | Ω | V _{GS} = 10V, I _D = 5.1A ③ |
| | | — | 0.056 | 0.065 | | V _{GS} = 4.5V, I _D = 4.42A ③ |
| V _{GS(th)} | Gate Threshold Voltage | 1.0 | — | 3.0 | V | V _{DS} = V _{GS} , I _D = 250μA |
| g _{fs} | Forward Trans conductance | 10.4 | — | — | S | V _{DS} = 10V, I _D = 5.2A |
| I _{DSS} | Drain-to-Source Leakage Current | — | — | 2.0 | μA | V _{DS} = 44V, V _{GS} = 0V |
| | | — | — | 25 | | V _{DS} = 44V, V _{GS} = 0V, T _J = 150°C |
| I _{GSS} | Gate-to-Source Forward Leakage | — | — | 100 | nA | V _{GS} = 20V |
| | Gate-to-Source Reverse Leakage | — | — | -100 | | V _{GS} = -20V |

Dynamic Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

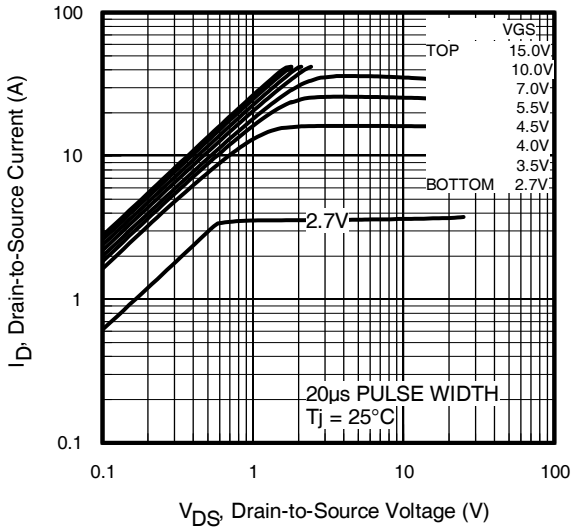
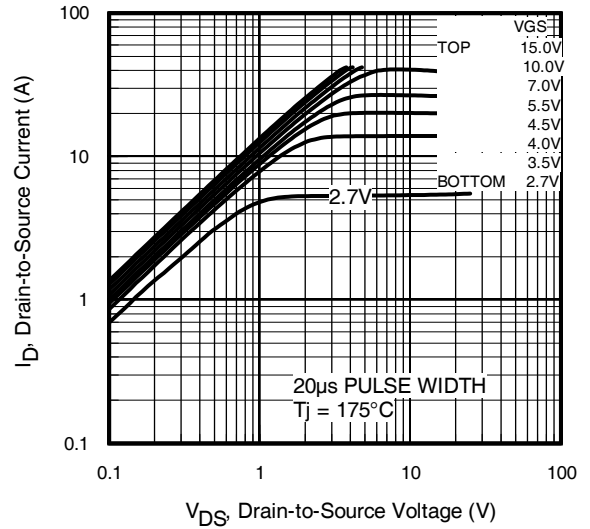
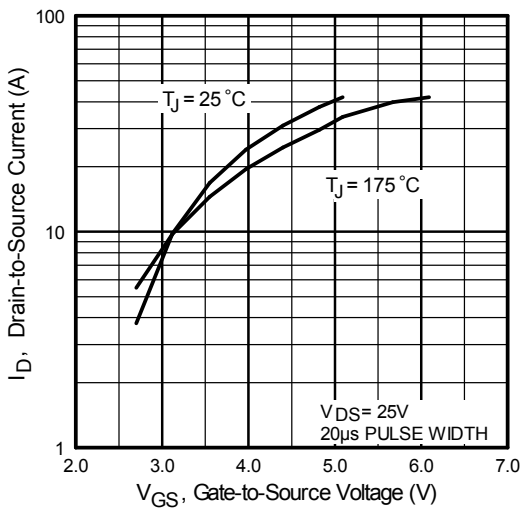
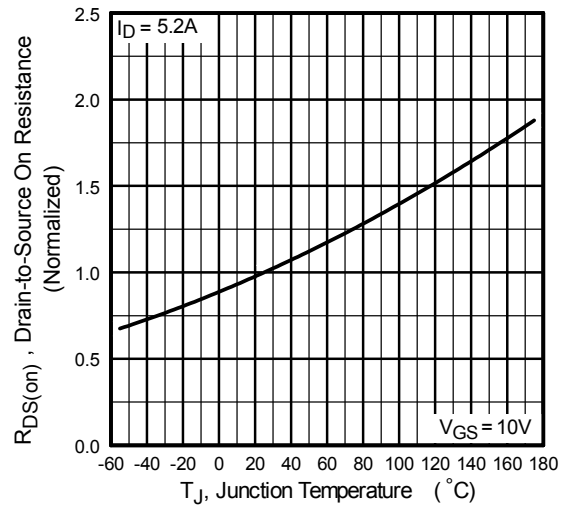
| | | | | | | |
|---------------------|------------------------------|---|------|-----|----|-------------------------|
| Q _g | Total Gate Charge | — | 29 | 44 | nC | I _D = 5.2A |
| Q _{gs} | Gate-to-Source Charge | — | 2.9 | 4.4 | | V _{DS} = 44V |
| Q _{gd} | Gate-to-Drain Charge | — | 7.3 | 11 | | V _{GS} = 10V |
| t _{d(on)} | Turn-On Delay Time | — | 9.2 | — | ns | V _{DD} = 28V |
| t _r | Rise Time | — | 7.7 | — | | I _D = 1.0A |
| t _{d(off)} | Turn-Off Delay Time | — | 31 | — | | R _G = 6.0Ω |
| t _f | Fall Time | — | 12.5 | — | | V _{GS} = 10V ③ |
| C _{iss} | Input Capacitance | — | 780 | — | pF | V _{GS} = 0V |
| C _{oss} | Output Capacitance | — | 190 | — | | V _{DS} = 25V |
| C _{rss} | Reverse Transfer Capacitance | — | 66 | — | | f = 1.0MHz |

Diode Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|-----------------|--|------|------|------|-------|--|
| I _S | Continuous Source Current (Body Diode) | — | — | 2.4 | A | MOSFET symbol showing the integral reverse p-n junction diode.  |
| I _{SM} | Pulsed Source Current (Body Diode) ① | — | — | 42 | | |
| V _{SD} | Diode Forward Voltage | — | — | 1.2 | V | T _J = 25°C, I _S = 2.6A, V _{GS} = 0V ② ③ |
| t _{rr} | Reverse Recovery Time | — | 51 | 77 | ns | T _J = 25°C, I _F = 2.6A, |
| Q _{rr} | Reverse Recovery Charge | — | 76 | 114 | nC | di/dt = 100A/μs ③ |

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② V_{DD} = 25V, Starting T_J = 25°C, L = 10.7mH, R_G = 25Ω, I_{AS} = 5.2A.
- ③ Pulse width ≤ 300μs; duty cycle ≤ 2%.
- ④ Surface mounted FR-4 board, t ≤ 10sec.


Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics

Fig. 3 Typical Transfer Characteristics

Fig. 4 Normalized On-Resistance vs. Temperature

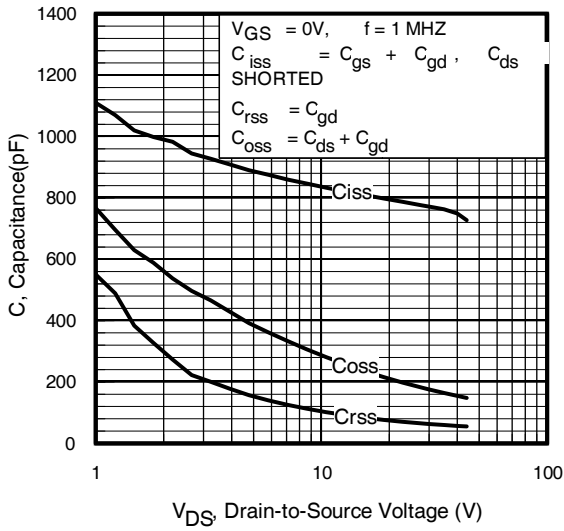


Fig 5. Typical Capacitance vs. Drain-to-Source Voltage

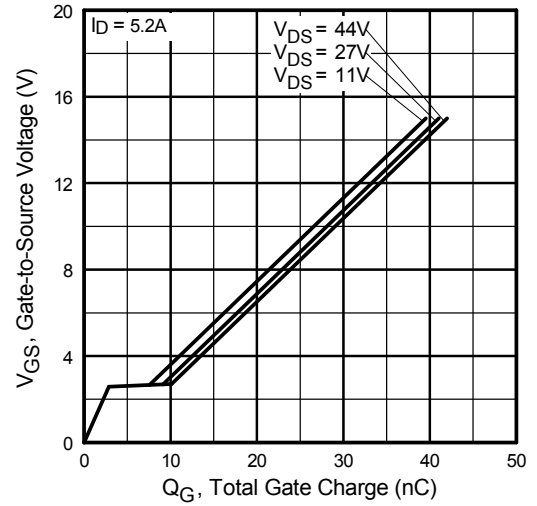


Fig 6. Typical Gate Charge vs. Gate-to-Source Voltage

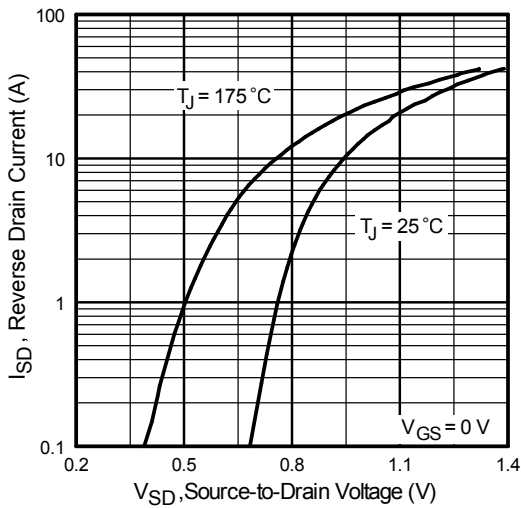


Fig 7. Typical Source-to-Drain Diode Forward Voltage

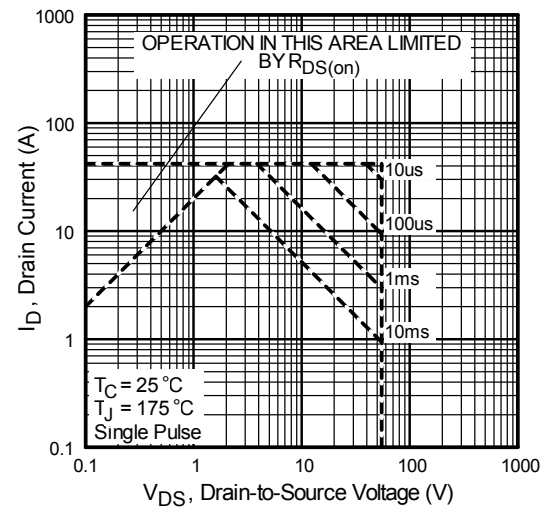
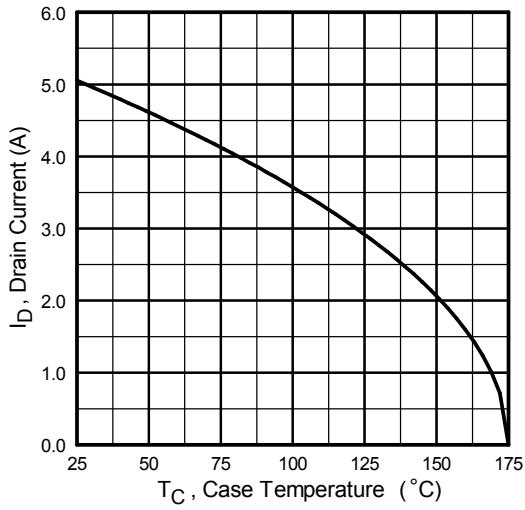
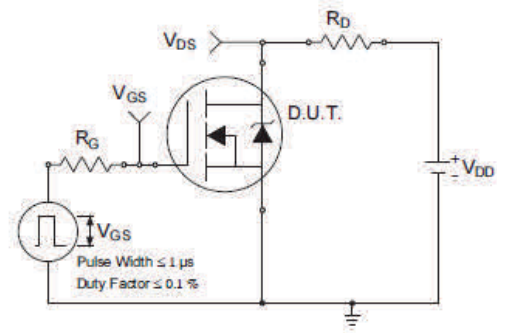
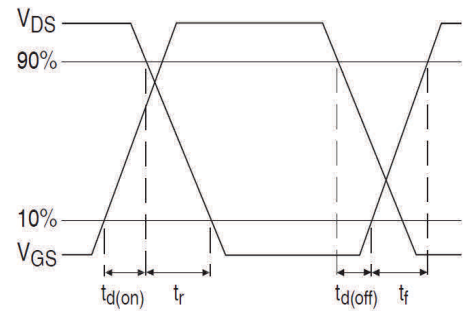
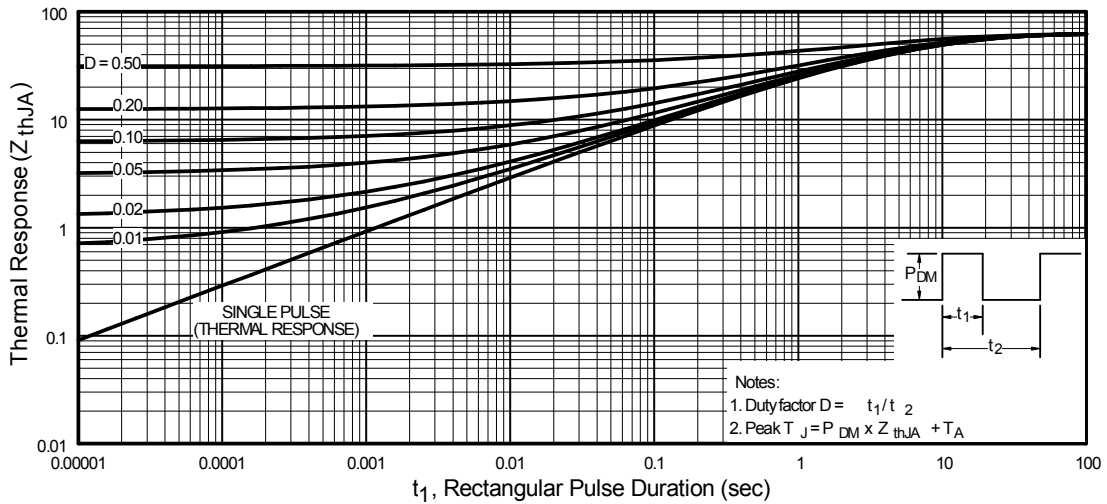
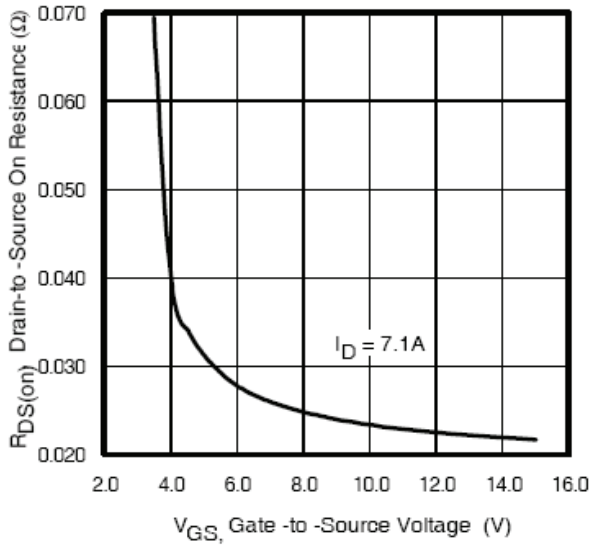
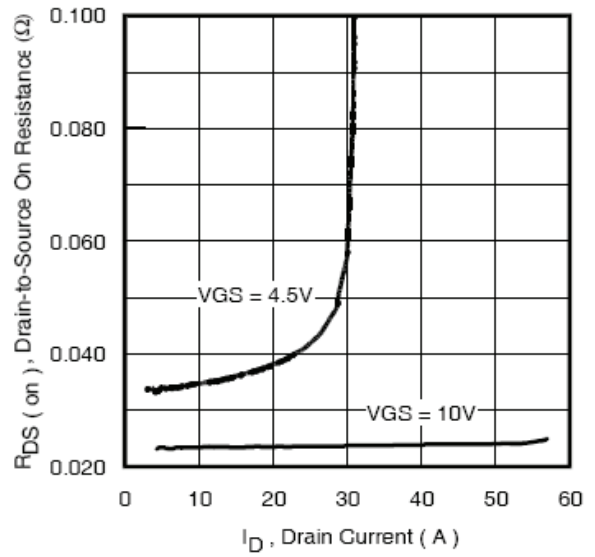
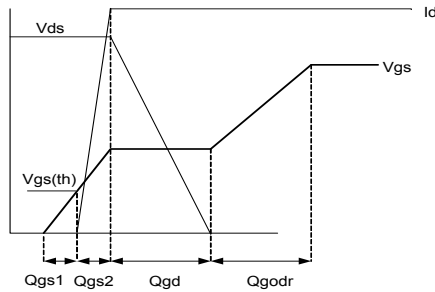
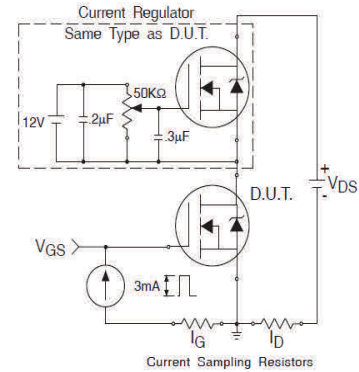
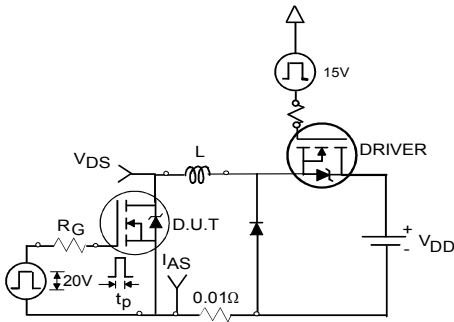
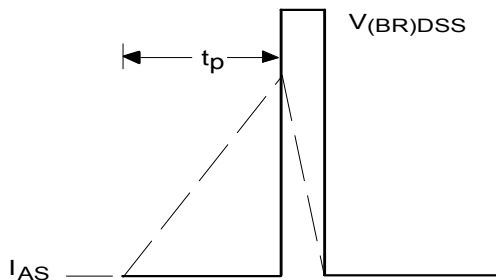
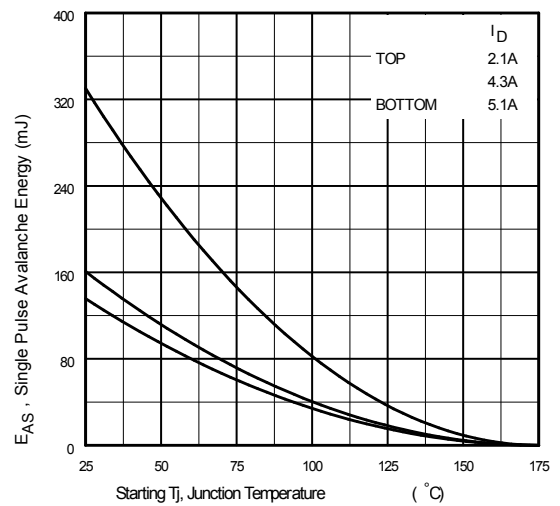
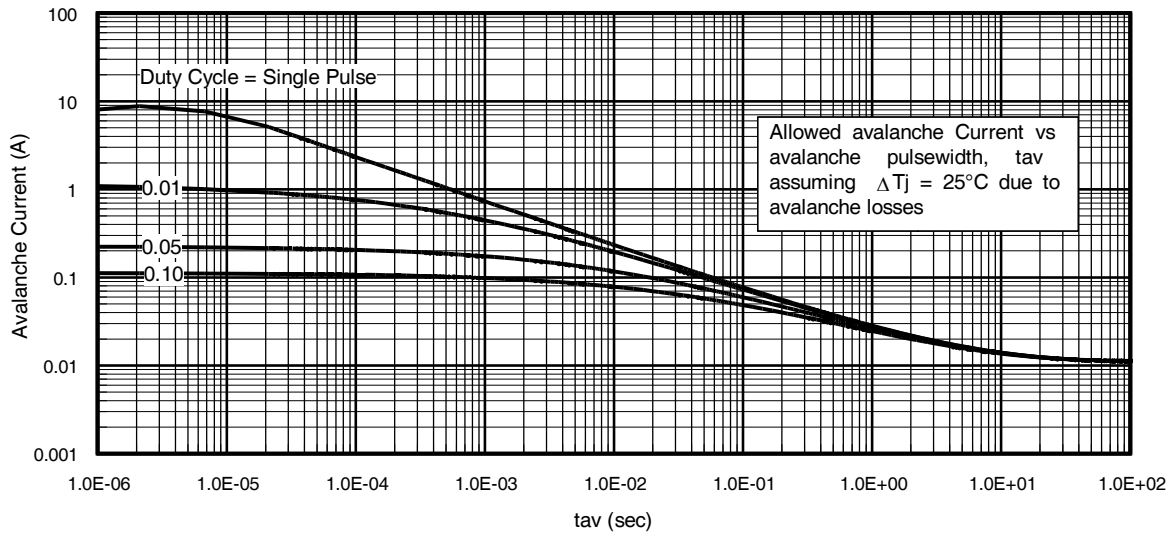
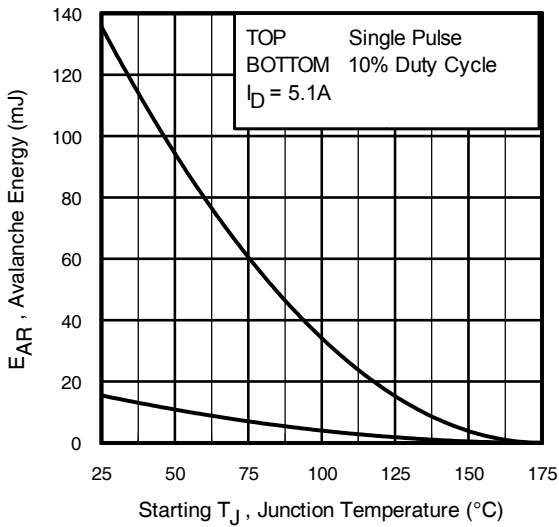


Fig 8. Maximum Safe Operating Area


Fig 9. Maximum Drain Current vs. Case Temperature

Fig 10a. Switching Time Test Circuit

Fig 10b. Switching Time Waveforms

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient


Fig 12. Typical On-Resistance Vs. Gate Voltage

Fig 13. Typical On-Resistance Vs. Drain Current

Fig 14a. Basic Gate Charge Waveform

Fig 14b. Gate Charge Test Circuit

Fig 15a. Unclamped Inductive Test Circuit

Fig 15b. Unclamped Inductive Waveforms

Fig 16. Maximum Avalanche Energy vs. Drain Current


Fig 17. Typical Avalanche Current vs. Pulse width

Fig 18. Maximum Avalanche Energy vs. Temperature
**Notes on Repetitive Avalanche Curves , Figures 17, 18:
(For further info, see AN-1005 at www.infineon.com)**

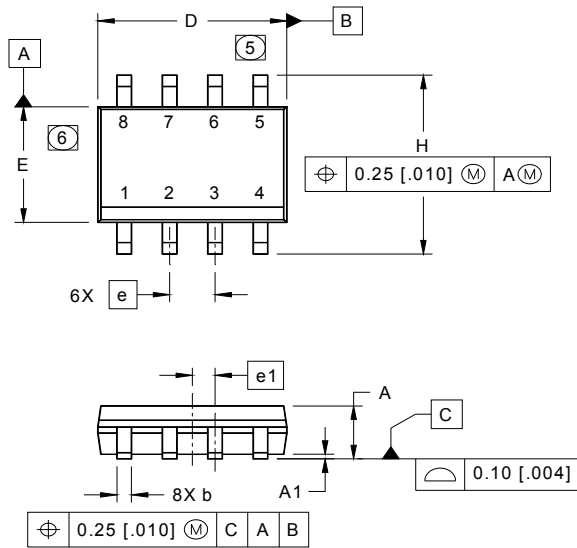
1. Avalanche failures assumption:
Purely a thermal phenomenon and failure occurs at a temperature far in excess of T_{jmax} . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as T_{jmax} is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 15a, 15b.
4. $P_{D(ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. I_{av} = Allowable avalanche current.
7. ΔT = Allowable rise in junction temperature, not to exceed T_{jmax} (assumed as 25°C in Figure 11, 17).
 t_{av} = Average time in avalanche.
 D = Duty cycle in avalanche = $t_{av} \cdot f$
 $Z_{thJC}(D, t_{av})$ = Transient thermal resistance, see Figures 11)

$$P_{D(ave)} = 1/2 (1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$

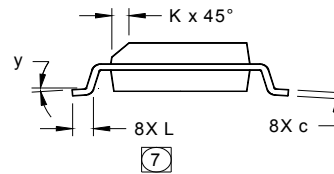
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{thJC}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$

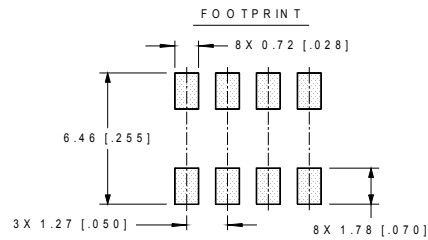
SO-8 Package Outline (Dimensions are shown in millimeters (inches))



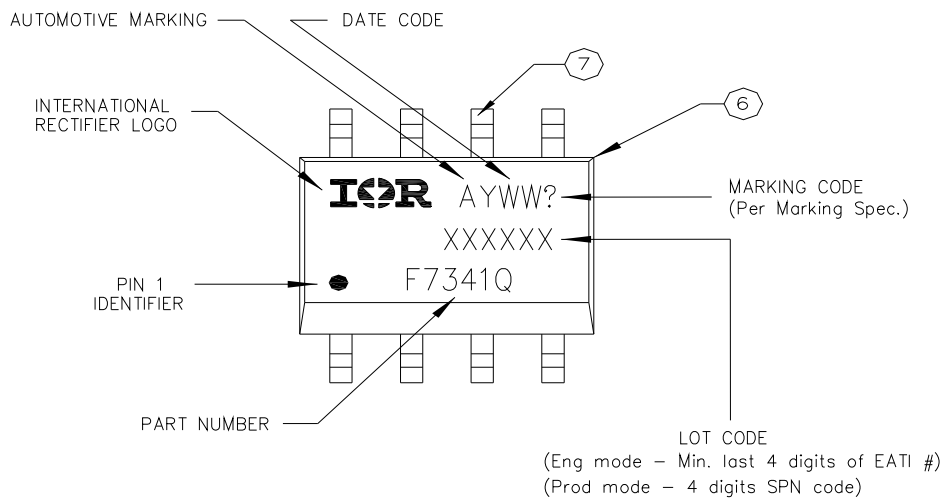
| DIM | INCHES | | MILLIMETERS | |
|-----|------------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | .0532 | .0688 | 1.35 | 1.75 |
| A1 | .0040 | .0098 | 0.10 | 0.25 |
| b | .013 | .020 | 0.33 | 0.51 |
| c | .0075 | .0098 | 0.19 | 0.25 |
| D | .189 | .1968 | 4.80 | 5.00 |
| E | .1497 | .1574 | 3.80 | 4.00 |
| e | .050 BASIC | | 1.27 BASIC | |
| e 1 | .025 BASIC | | 0.635 BASIC | |
| H | .2284 | .2440 | 5.80 | 6.20 |
| K | .0099 | .0196 | 0.25 | 0.50 |
| L | .016 | .050 | 0.40 | 1.27 |
| y | 0° | 8° | 0° | 8° |

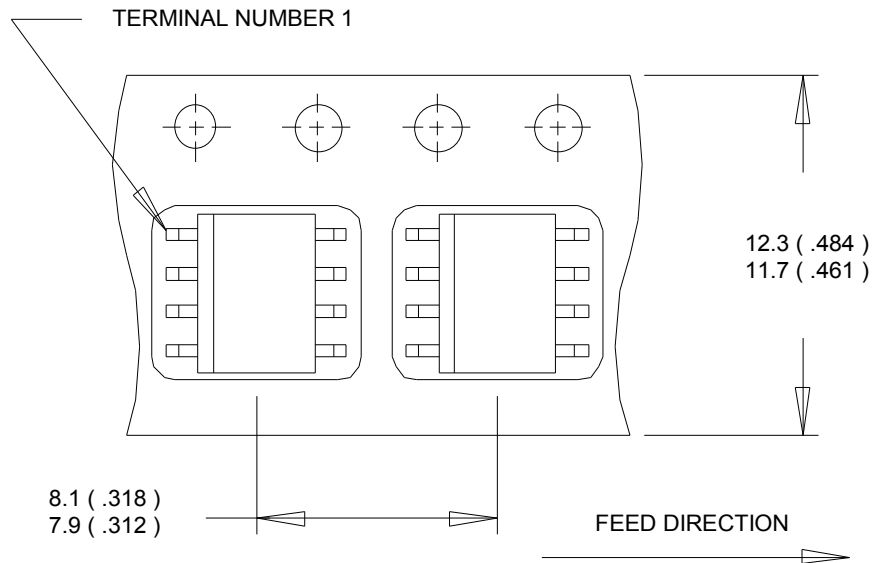


- NOTES:
1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 2. CONTROLLING DIMENSION: MILLIMETER
 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 4. OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.
 5. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
 6. DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
 7. DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

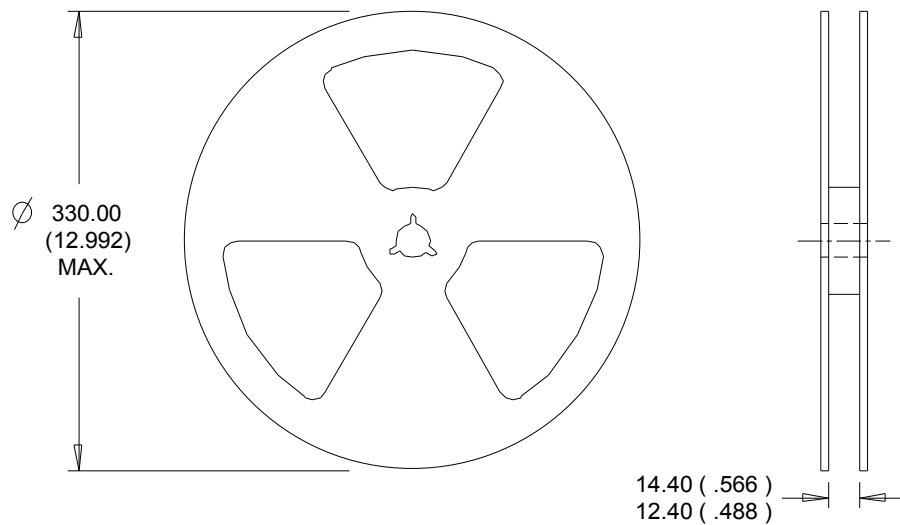


SO-8 Part Marking Information



SO-8 Tape and Reel (Dimensions are shown in millimeters (inches))

NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.


NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Qualification Information

| | | | |
|-----------------------------------|----------------------|---|------|
| Qualification Level | | Automotive (per AEC-Q101) | |
| | | Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level. | |
| Moisture Sensitivity Level | | SO-8 | MSL1 |
| ESD | Machine Model | Class M2 (+/- 200V) [†] AEC-Q101-002 | |
| | Human Body Model | Class H1A (+/- 500V) [†] AEC-Q101-001 | |
| | Charged Device Model | Class C5 (+/- 1125V) [†] AEC-Q101-005 | |
| RoHS Compliant | | Yes | |

† Highest passing voltage.

Revision History

| Date | Comments |
|-----------|--|
| 3/10/2014 | <ul style="list-style-type: none"> Added "Logic Level Gate Drive" bullet in the features section on page 1 Updated data sheet with new IR corporate template |
| 9/30/2015 | <ul style="list-style-type: none"> Updated datasheet with corporate template Corrected ordering table on page 1. |

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