



**THE DATASHEET OF
FSDL321L**



FSDH321, FSDL321

Green Mode Fairchild Power Switch (FPS™)

Features

- Internal Avalanche Rugged Sense FET
- Consumes only 0.65W at 240VAC & 0.3W load with Advanced Burst-Mode Operation
- Frequency Modulation for low EMI
- Precision Fixed Operating Frequency
- Internal Start-up Circuit
- Pulse by Pulse Current Limiting
- Abnormal Over Current Protection
- Over Voltage Protection
- Over Load Protection
- Internal Thermal Shutdown Function
- Auto-Restart Mode
- Under Voltage Lockout
- Low Operating Current (max 3mA)
- Adjustable Peak Current Limit
- Built-in Soft Start

Applications

- SMPS for STB, Low cost DVD
- Auxiliary Power for PC
- Adaptor for Charger

Description

The FSDx321(x stands for H, L) are integrated Pulse Width Modulators (PWM) and Sense FETs specifically designed for high performance offline Switch Mode Power Supplies (SMPS) with minimal external components. Both devices are integrated high voltage power switching regulators which combine an avalanche rugged Sense FET with a current mode PWM control block. The integrated PWM controller features include: a fixed oscillator with frequency modulation for reduced EMI, Under Voltage Lock Out (UVLO) protection, Leading Edge Blanking (LEB), optimized gate turn-on/turn-off driver, Thermal Shut Down (TSD) protection, Abnormal Over Current Protection (AOCP) and temperature compensated precision current sources for loop compensation and fault protection circuitry. When compared to a discrete MOSFET and controller or RCC switching converter solution, the FSDx321 reduce total component count, design size, weight and at the same time increase efficiency, productivity, and system reliability. Both devices are a basic platform well suited for cost effective designs of flyback converters.

OUTPUT POWER TABLE				
PRODUCT	230VAC ±15% ⁽³⁾		85-265VAC	
	Adapt-er ⁽¹⁾	Open Frame ⁽²⁾	Adapt-er ⁽¹⁾	Open Frame ⁽²⁾
FSDL321	11W	17W	8W	12W
FSDH321	11W	17W	8W	12W
FSDL0165RN	13W	23W	11W	17W
FSDM0265RN	16W	27W	13W	20W
FSDH0265RN	16W	27W	13W	20W
FSDL0365RN	19W	30W	16W	24W
FSDM0365RN	19W	30W	16W	24W
FSDL321L	11W	17W	8W	12W
FSDH321L	11W	17W	8W	12W
FSDL0165RL	13W	23W	11W	17W
FSDM0265RL	16W	27W	13W	20W
FSDH0265RL	16W	27W	13W	20W
FSDL0365RL	19W	30W	16W	24W
FSDM0365RL	19W	30W	16W	24W

Table 1. Notes: 1. Typical continuous power in a non-ventilated enclosed adapter with sufficient drain pattern or something as a heat sinker measured at 50°C ambient. 2. Maximum practical continuous power in an open frame design with sufficient drain pattern or something as a heat sinker at 50°C ambient. 3. 230 VAC or 100/115 VAC with doubler.

Typical Circuit

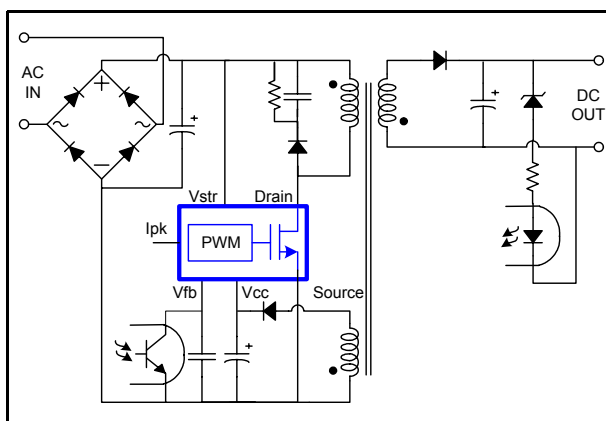


Figure 1. Typical Flyback Application

Internal Block Diagram

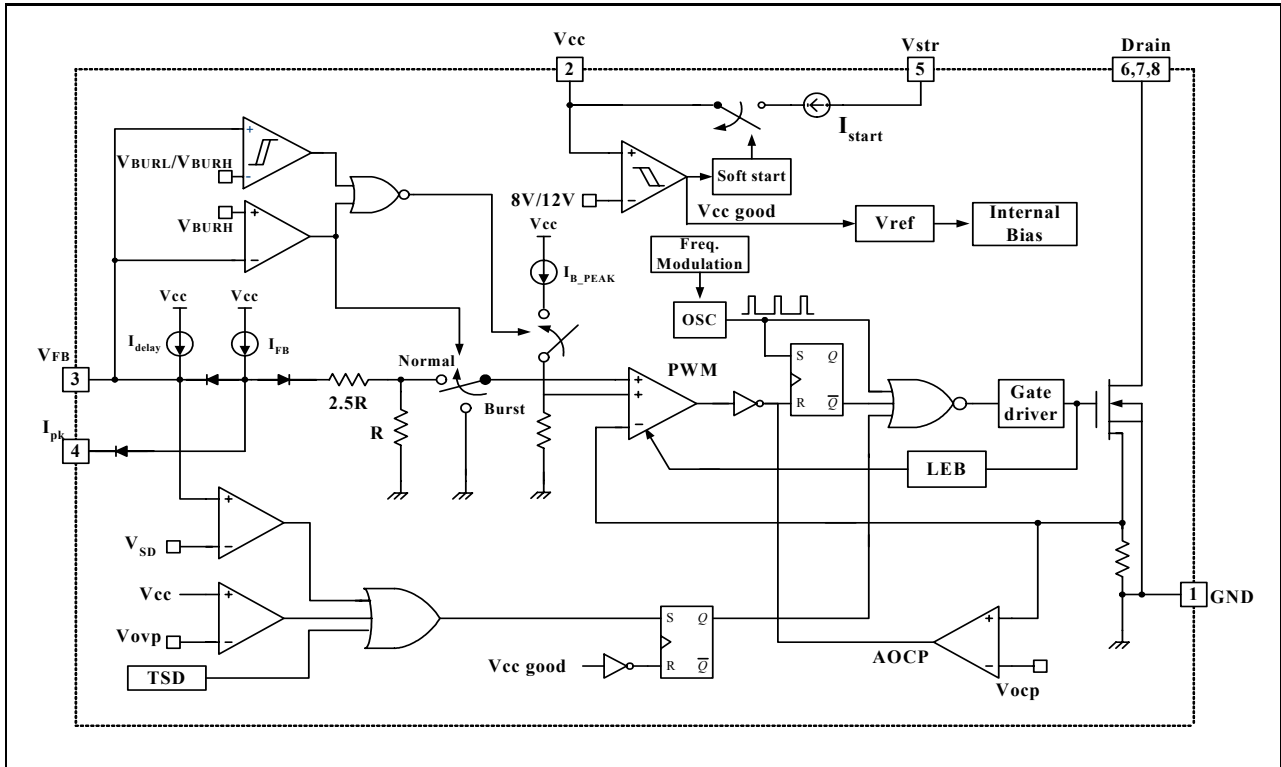


Figure 2. Functional Block Diagram of FSDx321

Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	GND	Sense FET source terminal on primary side and internal control ground.
2	Vcc	Positive supply voltage input. Although connected to an auxiliary transformer winding, current is supplied from pin 5 (Vstr) via an internal switch during startup (see Internal Block Diagram section). It is not until Vcc reaches the UVLO upper threshold (12V) that the internal start-up switch opens and device power is supplied via the auxiliary transformer winding.
3	Vfb	The feedback voltage pin is the non-inverting input to the PWM comparator. It has a 0.9mA current source connected internally while a capacitor and optocoupler are typically connected externally. A feedback voltage of 6V triggers over load protection (OLP). There is a time delay while charging between 3V and 6V using an internal 5uA current source, which prevents false triggering under transient conditions but still allows the protection mechanism to operate under true overload conditions.
4	l _{pk}	Pin to adjust the current limit of the Sense FET. The feedback 0.9mA current source is diverted to the parallel combination of an internal 2.8kΩ resistor and any external resistor to GND on this pin to determine the current limit. If this pin is tied to Vcc or left floating, the typical current limit will be 0.7A.
5	Vstr	This pin connects directly to the rectified AC line voltage source. At start up the internal switch supplies internal bias and charges an external storage capacitor placed between the Vcc pin and ground. Once the Vcc reaches 12V, the internal switch is disabled.
6, 7, 8	Drain	The Drain pin is designed to connect directly to the primary lead of the transformer and is capable of switching a maximum of 650V. Minimizing the length of the trace connecting this pin to the transformer will decrease leakage inductance.

Pin Configuration

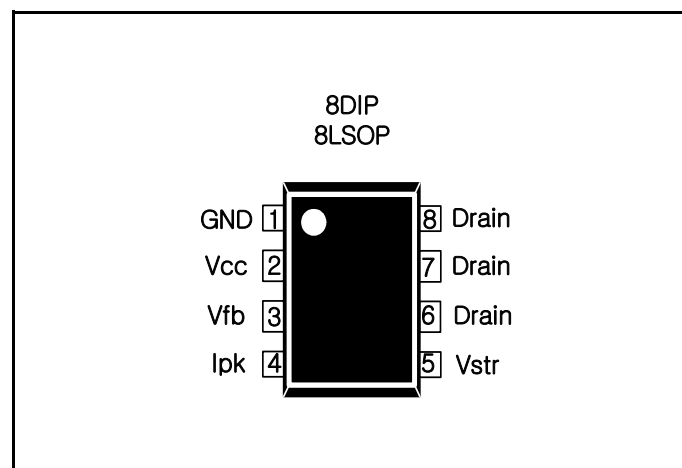


Figure 3. Pin Configuration (Top View)

Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Maximum Vstr Pin Voltage	VSTR,MAX	650	V
Maximum Drain Pin Voltage	VDRAIN,MAX	650	V
Drain-Gate Voltage (RGS=1MΩ)	VDGR	650	V
Gate-Source (GND) Voltage	VGS	±20	V
Drain Current Pulsed ⁽¹⁾	IDM	1.5	ADC
Continuous Drain Current (Tc=25°C)	ID	0.7	ADC
Continuous Drain Current (Tc=100°C)	ID	0.32	ADC
Single Pulsed Avalanche Energy ⁽²⁾	EAS	10	mJ
Maximum Supply Voltage	VCC,MAX	20	V
Input Voltage Range	VFB	-0.3 to VCC	V
Total Power Dissipation	PD	1.40	W
Operating Junction Temperature.	TJ	Internally limited	°C
Operating Ambient Temperature.	TA	-25 to +85	°C
Storage Temperature Range.	TSTG	-55 to +150	°C

Note:

1. Repetitive rating: Pulse width limited by maximum junction temperature
2. L = 24mH, starting Tj = 25°C

Thermal Impedance

Parameter	Symbol	Value	Unit
8DIP			
Junction-to-Ambient Thermal	$\theta_{JA}^{(1)}$	88.84 ⁽³⁾	°C/W
Junction-to-Case Thermal	$\theta_{JC}^{(2)}$	13.94	°C/W

Note:

1. Free standing without heatsink.
 2. Measured on the Drain pin close to plastic interface.
 3. Without copper clad.
- * - all items are tested with the standard JESD 51-10(DIP)

Electrical Characteristics (Sense FET Part)

(Ta = 25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Sense FET SECTION						
Zero Gate Voltage Drain Current	IDSS	VDS=Max. Rating, VGS=0V	-	-	25	μA
		VDS=0.8Max. Rating, VGS=0V, TC=125°C	-	-	200	μA
Static Drain-Source on Resistance (Note)	RDS(ON)	VGS=10V, ID=0.5A	-	14	19	Ω
Forward Trans conductance (Note)	gfs	VDS=50V, ID=0.5A	1.0	1.3	-	S
Input Capacitance	CISS	VGS=0V, VDS=25V, f=1MHz	-	162	-	pF
Output Capacitance	COSS		-	18	-	
Reverse Transfer Capacitance	CRSS		-	3.8	-	
Turn on Delay Time	td(on)	VDD=0.5B VDSS, ID=1.0A (MOSFET switching time is essentially independent of operating temperature)	-	9.5	-	ns
Rise Time	tr		-	19	-	
Turn Off Delay Time	td(off)		-	33	-	
Fall Time	tf		-	42	-	
Total Gate Charge (Gate-Source + Gate-Drain)	Qg	VGS=10V, ID=1.0A, VDS=0.5B VDSS (MOSFET switching time is essentially independent of operating temperature)	-	7.0	-	nC
Gate-Source Charge	Qgs		-	3.1	-	
Gate-Drain (Miller) Charge	Qgd		-	0.4	-	

Note:

1. Pulse test: Pulse width ≤ 300μS, duty ≤ 2%

2. $S = \frac{1}{R}$

Electrical Characteristics (Control Part) (Continued)

(Ta=25°C unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
UVLO SECTION						
Start Threshold Voltage	VSTART	VFB=GND	11	12	13	V
Stop Threshold Voltage	VSTOP	VFB=GND	7	8	9	V
OSCILLATOR SECTION						
Initial Accuracy	FOSC	FSDH321	90	100	110	kHz
Frequency Modulation	FMOD		±2.5	±3	±3.5	
Initial Accuracy	FOSC	FSDL321	45	50	55	kHz
Frequency Modulation	FMOD		±1.0	±1.5	±2.0	
Frequency Change With Temperature ⁽²⁾	ΔF/ΔT	-25°C ≤ Ta ≤ +85°C	-	±5	±10	%
Maximum Duty Cycle	Dmax	FSDH321	62	67	72	%
		FSDL321	71	77	83	%
FEEDBACK SECTION						
Feedback Source Current	IFB	Ta=25°C, Vfb = 0V	0.70	0.90	1.1	mA
Shutdown Feedback Voltage	VSD		5.5	6.0	6.5	V
Shutdown Delay Current	IDELAY	Ta=25°C, Vfb = 4V	3.5	5.0	6.5	μA
BURST MODE SECTION						
Burst Mode Voltage	VBURH	Tj = 25°C	0.4	0.5	0.6	V
	VBURL		0.25	0.35	0.45	V
	Hysteresis		-	150	-	mV
CURRENT LIMIT(SELF-PROTECTION)SECTION						
Peak Current Limit ⁽³⁾	ILIM	Tj = 25°C	0.60	0.70	0.80	A
Current Limit Delay ⁽¹⁾	TCLD	Tj = 25°C	-	600	-	ns
SOFT START SECTION						
Soft Start Time	TSS	Vfb = 4V	10	15	20	ms
PROTECTION SECTION						
Thermal Shutdown Temperature ⁽¹⁾	TSD	-	125	145	-	°C
Over Voltage Protection	VOVP		18	19	20	V
TOTAL STANDBY CURRENT SECTION						
Startup Charging Current	ICH	VCC=0V	0.7	0.85	1.0	mA
Operating Supply Current (Control Part Only)	IOP	VCC = 14V, Vfb = 0V	1	3	5	mA

Note:

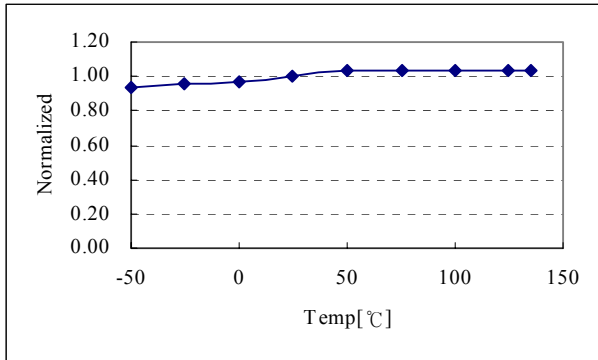
1. These parameters, although guaranteed, are not 100% tested in production
2. These parameters, although guaranteed, are tested in EDS (wafer test) process
3. di/dt = 250mA/μS

Comparison Between FSDM311 and FSDx321

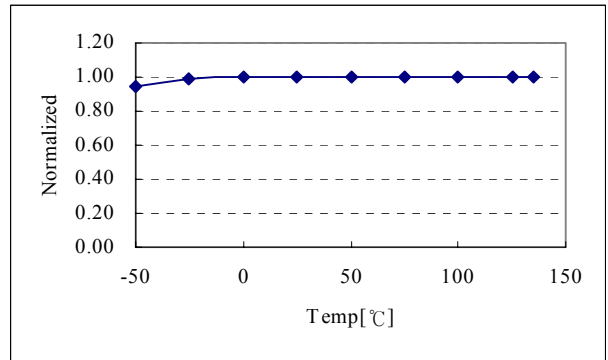
Function	FSDM311	FSDx321	FSDx321 Advantages
Soft-Start	15mS	15mS	<ul style="list-style-type: none"> • Gradually increasing current limit during soft-start further reduces peak current and voltage component stresses • Eliminates external components used for soft-start in most applications • Reduces or eliminates output overshoot
External Current Limit	not applicable	Programmable of default current limit	<ul style="list-style-type: none"> • Smaller transformer • Allows power limiting (constant over-load power) • Allows use of larger device for lower losses and higher efficiency.
Frequency Modulation	not applicable	$\pm 1.5\text{KHz @}50\text{KHz}$ $\pm 3.0\text{KHz @}100\text{KHz}$	<ul style="list-style-type: none"> • Reduced conducted EMI
Burst Mode Operation	Yes-built into controller	Yes-built into controller	<ul style="list-style-type: none"> • Improve light load efficiency • Reduces no-load consumption • Transformer audible noise reduction
Drain Creepage at Package	7.62mm	7.62mm	<ul style="list-style-type: none"> • Greater immunity to arcing as a result of build-up of dust, debris and other contaminants

Typical Performance Characteristics (Control Part)

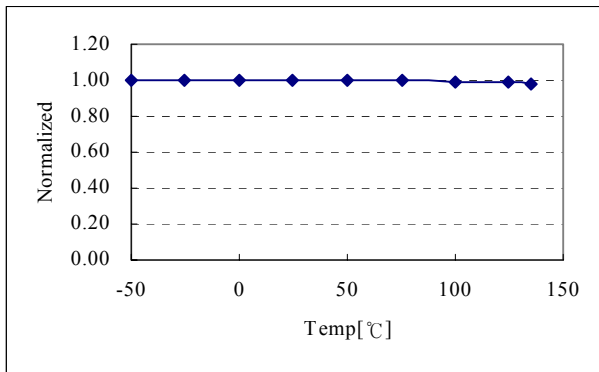
(These characteristic graphs are normalized at $T_a = 25^\circ\text{C}$)



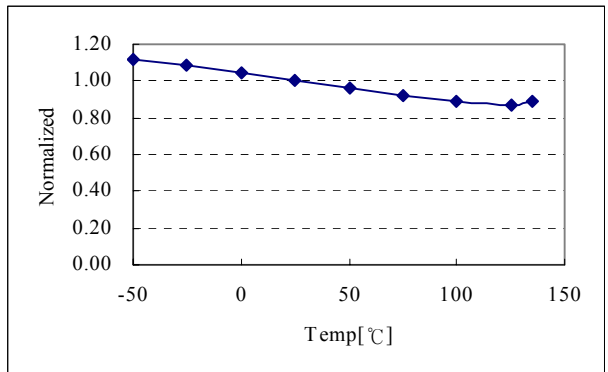
Operating Frequency (Fosc)



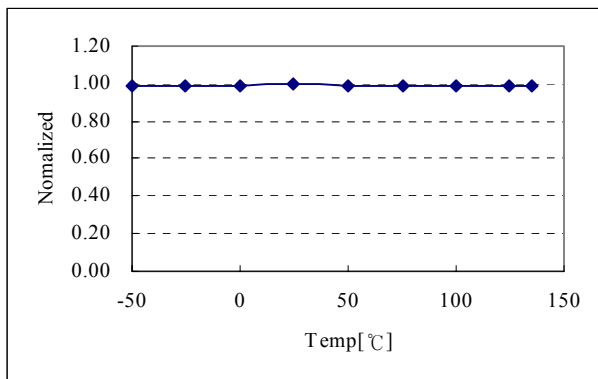
Frequency Modulation (Fmod)



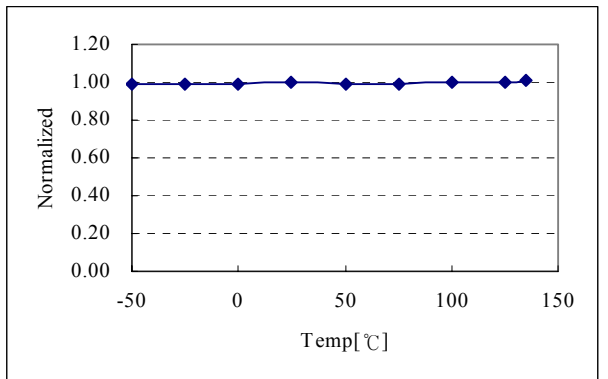
Maximum duty cycle (Dmax)



Operating supply current (Iop)

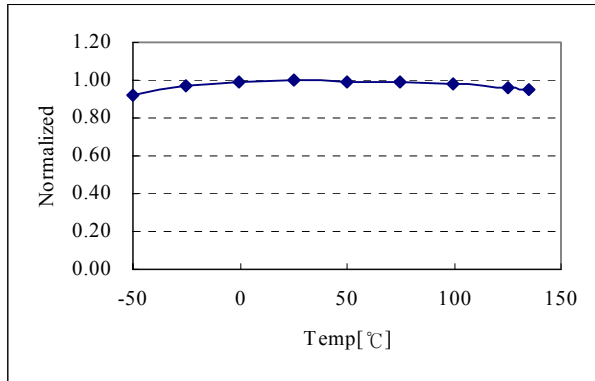


Start Threshold Voltage (Vstart)

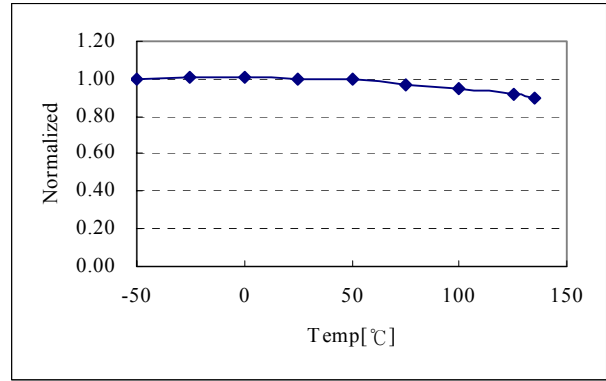


Stop Threshold Voltage (Vstop)

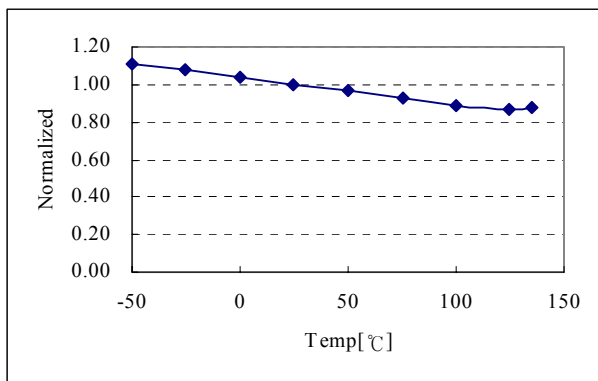
Typical Performance Characteristics (Continued)



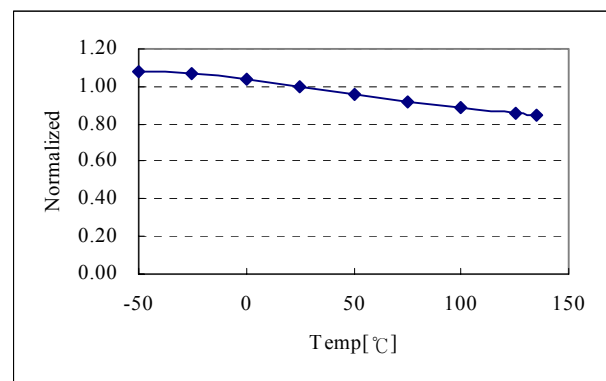
Feedback Source Current (I_{fb})



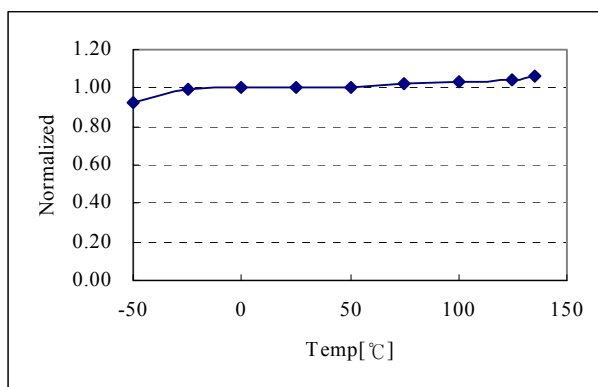
Peak current limit (I_{LIM})



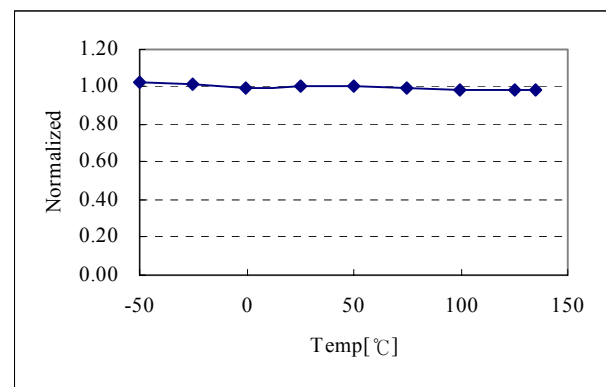
Start up Current (I_{start})



Startup Charging Current (I_{ch})



Burst peak current (I_{burst})



Over Voltage Protection (V_{ovp})

Cfb from 3V to 6V with 5uA.

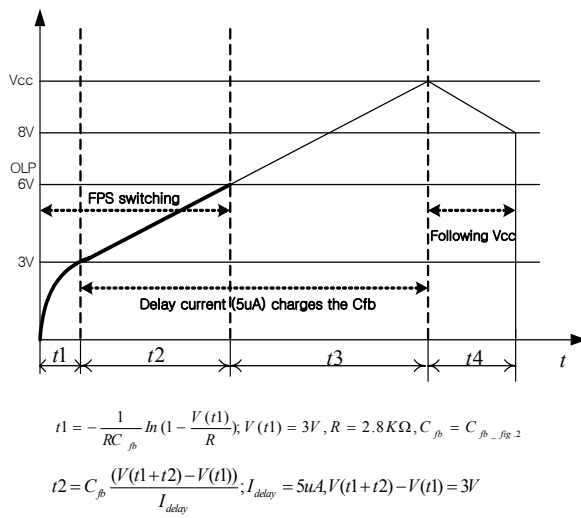


Figure 6. Over load protection

4.2 Thermal Shutdown (TSD) : The Sense FET and the control IC are integrated, making it easier for the control IC to detect the temperature of the Sense FET. When the temperature exceeds approximately 140°C, thermal shutdown is activated.

4.3 Abnormal Over Current Protection (AOCP) :

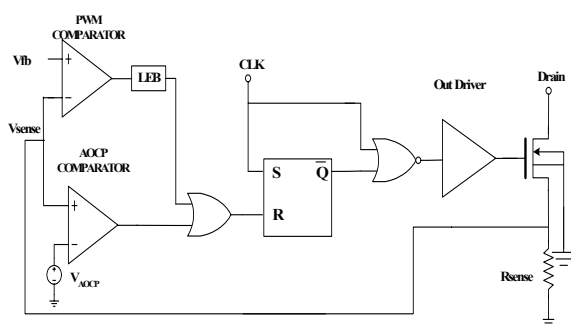


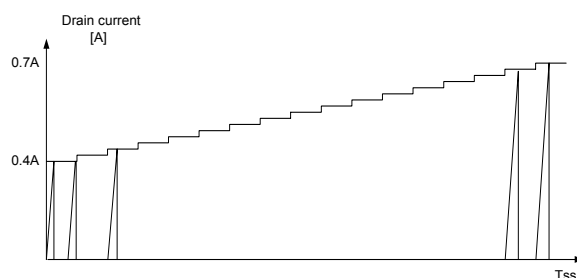
Figure 7. AOCP Function & Block

Even though the FPSTM has OLP (Over Load Protection) and current mode PWM feedback, these are not enough to protect the FPSTM when a secondary side diode short or a transformer pin short occurs. In addition to start-up, soft-start is also activated at each restart attempt during auto-restart and when restarting after latch mode is activated. The FPSTM has an internal AOCP (Abnormal Over Current Pro-

tection) circuit as shown in figure 7. When the gate turn-on signal is applied to the power Sense FET, the AOCP block is enabled and monitors the current through the sensing resistor. The voltage across the resistor is then compared with a preset AOCP level. If the sensing resistor voltage is greater than the AOCP level, pulse by pulse AOCP is triggered regardless of uncontrollable LEB time. Here, pulse by pulse AOCP stops Sense FET within 350ns after it is activated.

4.4 Over Voltage Protection (OVP) : In case of malfunction in the secondary side feedback circuit, or feedback loop open caused by a defect of solder, the current through the opto-coupler transistor becomes almost zero. Then, Vfb climbs up in a similar manner to the over load situation, forcing the preset maximum current to be supplied to the SMPS until the over load protection is activated. Because excess energy is provided to the output, the output voltage may exceed the rated voltage before the over load protection is activated, resulting in the breakdown of the devices in the secondary side. In order to prevent this situation, an over voltage protection (OVP) circuit is employed. In general, Vcc is proportional to the output voltage and the FPSTM uses Vcc instead of directly monitoring the output voltage. If Vcc exceeds 19V, OVP circuit is activated resulting in termination of the switching operation. In order to avoid undesired activation of OVP during normal operation, Vcc should be properly designed to be below 19V.

5. Soft Start : The FPSTM has an internal soft start circuit that increases the feedback voltage together with the Sense FET current slowly after it starts up. The typical soft start time is 15msec, as shown in figure 8, where progressive increments of Sense FET current are allowed during the start-up phase. The pulse width to the power switching device is progressively increased to establish the correct working conditions for transformers, inductors, and capacitors. The voltage on the output capacitors is progressively increased with the intention of smoothly establishing the required output voltage. It also helps to prevent transformer saturation and reduce the stress on the secondary diode.



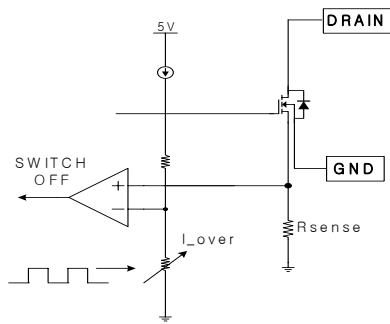


Figure 8. Soft Start Function

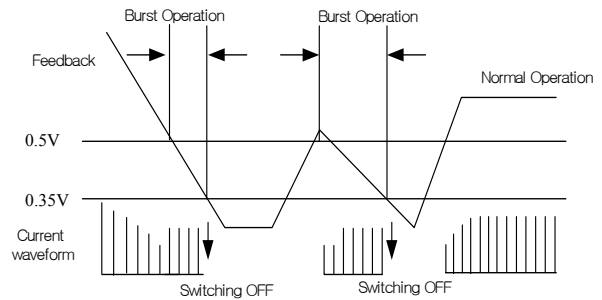


Figure 10. Circuit for Burst Operation

6. Burst operation : In order to minimize power dissipation in standby mode, the FPS™ enters burst mode operation.

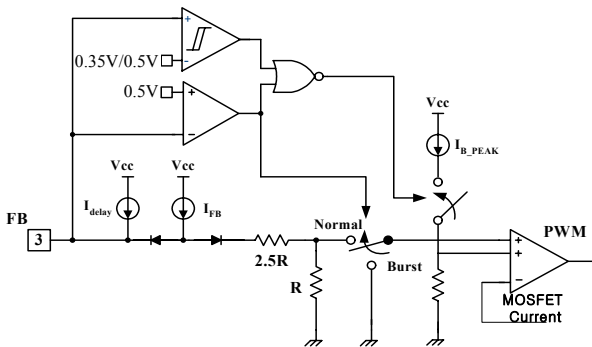


Figure 9. Circuit for Burst operation

As the load decreases, the feedback voltage decreases. As shown in figure 10, the device automatically enters burst mode when the feedback voltage drops below V_{BURH} (500mV). Switching still continues but the current limit is set to a fixed limit internally to minimize flux density in the transformer. The fixed current limit is larger than that defined by $V_{fb} = V_{BURH}$ and therefore, V_{fb} is driven down further. Switching continues until the feedback voltage drops below V_{BURL} (350mV). At this point switching stops and the output voltages start to drop at a rate dependent on the standby current load. This causes the feedback voltage to rise. Once it passes V_{BURH} (500mV) switching resumes. The feedback voltage then falls and the process repeats. Burst mode operation alternately enables and disables switching of the power Sense FET thereby reducing switching loss in Standby mode.

7. Frequency Modulation : EMI reduction can be accomplished by modulating the switching frequency of a switched power supply. Frequency modulation can reduce EMI by spreading the energy over a wider frequency range than the band width measured by the EMI test equipment. The amount of EMI reduction is directly related to the depth of the reference frequency. As can be seen in Figure 11, the frequency changes from 97KHz to 100KHz (from 48.5KHz to 51.5KHz for FSDL321)in 4mS for the FSDH321. Frequency modulation allows the use of a cost effective inductor instead of an AC input mode choke to satisfy the requirements of world wide EMI limits.

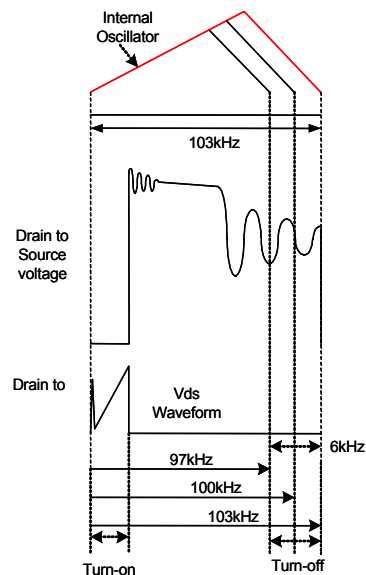


Figure 11. Frequency Modulation Waveform for FSDH321

8. Adjusting Current limit function: As shown in fig 12, a combined $2.8k\Omega$ internal resistance is connected into the non-inverting lead on the PWM comparator. A external resistance of A on the current limit pin forms a parallel resistance with the $2.8k\Omega$ when the internal diodes are biased by the main current source of $900\mu A$.

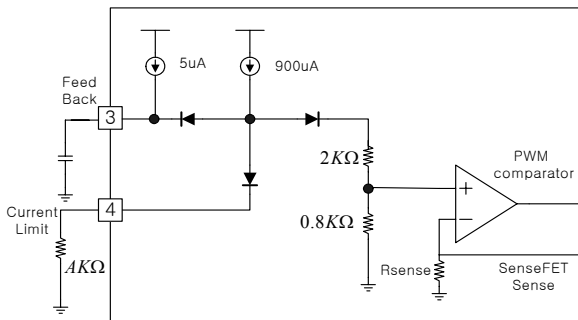


Figure 12. Peak current adjustment

For example, FSDH321 has a typical Sense FET current limit (I_{LIM}) of $0.7A$. The Sense FET current can be limited to 0.5 by inserting a $7k\Omega$ between the current limit pin and ground which is derived from the following equations:

$$0.7 : 0.5 = 2.8k\Omega : Xk\Omega ,$$

$$X = 2k\Omega$$

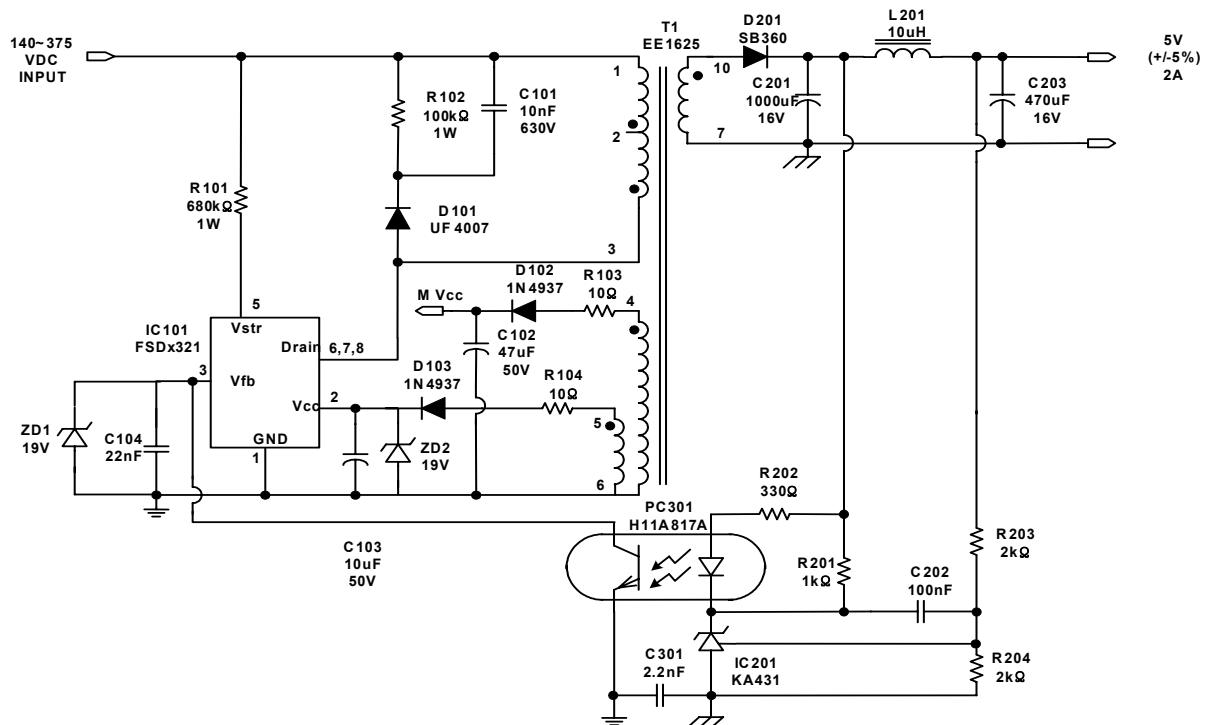
Since X represents the resistance of the parallel network, A can be calculated using the following equation:

$$A = X / (1 - (X/2.8k\Omega))$$

Layout Considerations

Typical application circuit

1. PC Auxiliary Power Circuit (10W Output Power)



10W PC Auxiliary Power Circuit

10W PC Auxiliary Power, 150~375VDC Input Power supply:

It shows an auxiliary power for PC. Efficiency at 10W, 150/375VDC is $\geq 70\%$.

The PC application has the standard of standby power consumption, under 1W at the output load 0.5W and input voltage 230VAC. For this the FSDH321 also has the burst operating function like other green mode FPS' such as FSDM0265RN or FSDM0365RN and so on. This skill reduces the MOSFET switching numbers and power MOSFET switching loss. This design takes advantage of self protection without external components and high switching frequency, 100kHz. The frequency makes using a small size transformer core possible. The EE16 or EE1625 can be used for 10W application.

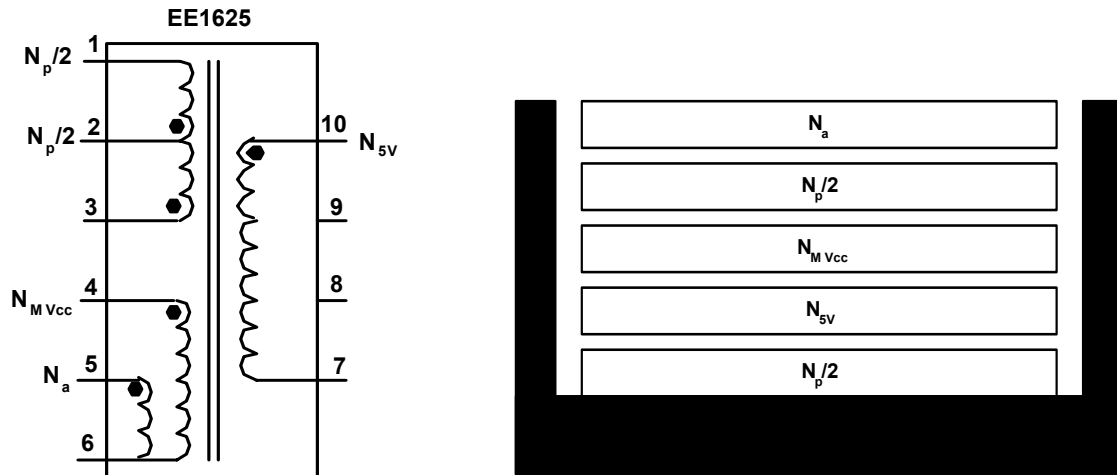
This is achieved by preventing the green FPS from switching when the input voltage goes below a level needed to maintain output regulation, and keeping it off until the input voltage goes above the under-voltage threshold, when the AC is turned on again. For example with the resistor, R101, 680kΩ, the threshold voltage is around 150VAC(210VDC) at the room temperature.

Surge voltages on the DRAIN pin due to the leakage induc-

tance is clamped by R102 and C101, keeping the DRAIN voltage below 650 V under all conditions. The frequency modulation feature of FSDH321 allows the circuit shown to meet CISPR2AB with simple EMI filtering. The secondary is rectified and smoothed by D201. Similarly D102 and D103 are also rectifiers for main power control IC and FSDH321 respectively. The 5V output voltage require two capacitors in parallel to meet the ripple current requirement. Switching noise filtering is provided by L201. The output is regulated by the reference (TL431) voltage in secondary. It is sensed via R203 and R204. Resistor R201 provides bias for TL431 and R202 sets the overall DC gain. R202, C202 and R203 provide loop compensation.

2. Transformer Specification (10W Output Power)

1. Schematic Diagram



2. Winding Specification

	Pin (S → F)	Wire	Turns	Winding Method
$N_p/2$	3 → 2	0.15 ϕ × 1	80	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
N_{5V}	10 → 7	0.55 ϕ × 1	12	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
N_{MVCC}	4 → 6	0.20 ϕ × 1	40	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
$N_p/2$	2 → 1	0.15 ϕ × 1	80	Solenoid winding
Insulation : Polyester Tape t = 0.050mm, 3Layers				
N_a	5 → 6	0.20 ϕ × 1	34	Solenoid winding
Outer Insulation : Polyester Tape t = 0.050mm, 3Layers				

3. Electric Specification and Core and Bobbin

	Pin	Spec.	Remark
Inductance	1 – 3	1.8 mH	1kHz, 1V
Leakage	1 – 3	100uH	2nd side all short
Core		EE1625	
Bobbin		EE1625	

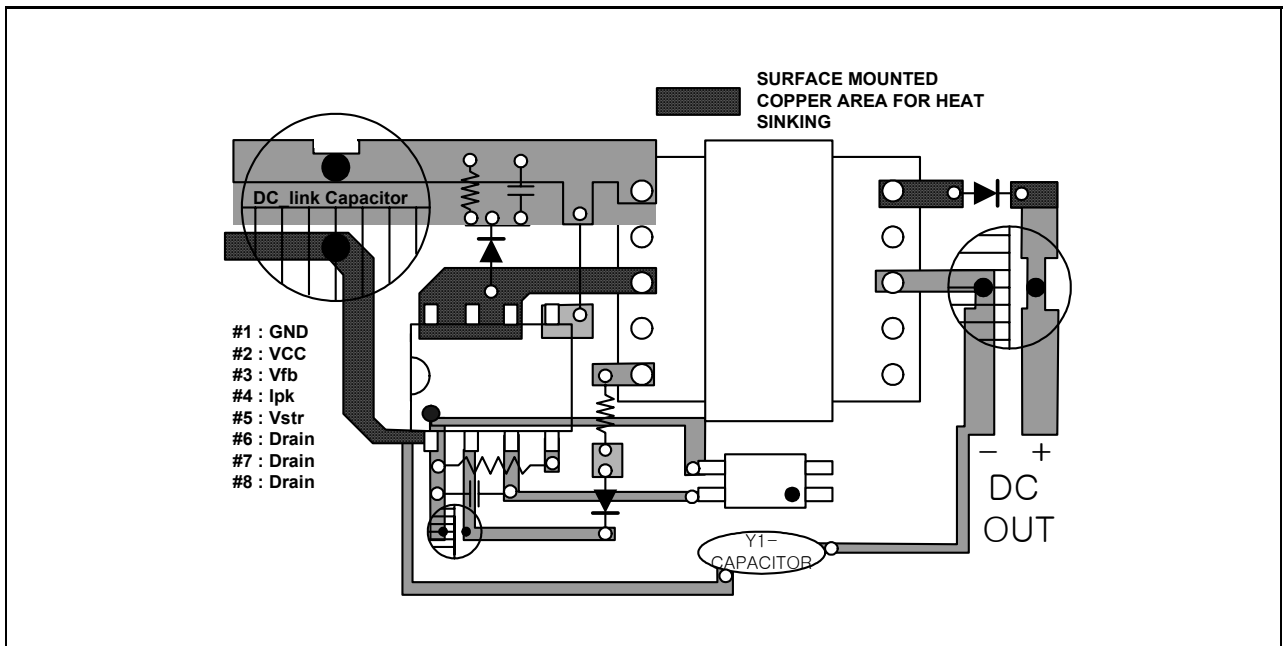
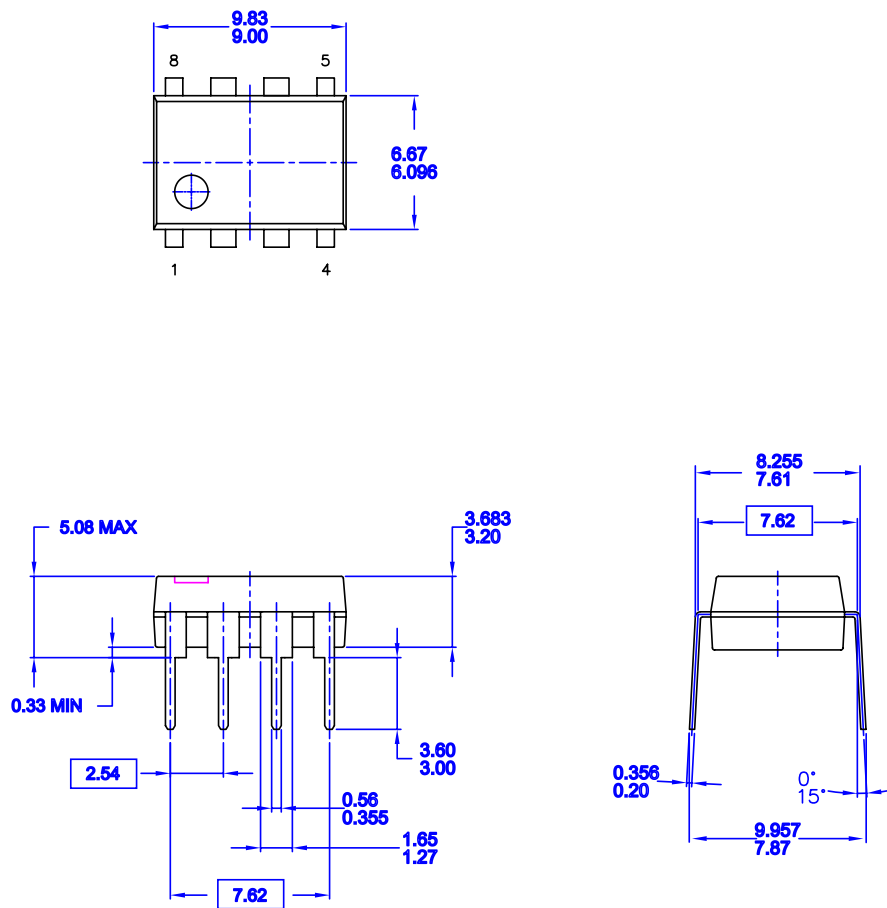


Figure 13. Layout Considerations for FSDx321 using 8DIP

Package Dimensions

8DIP

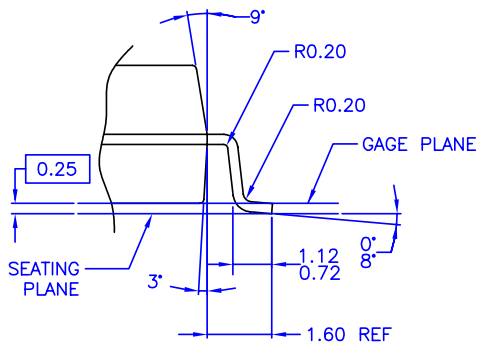
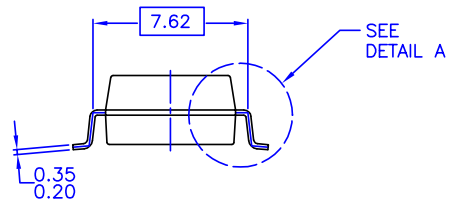
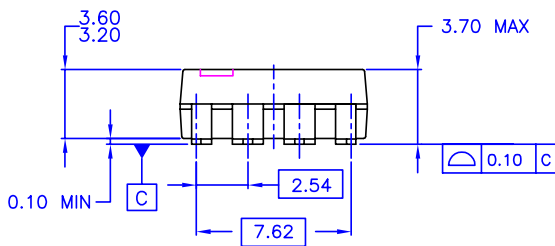
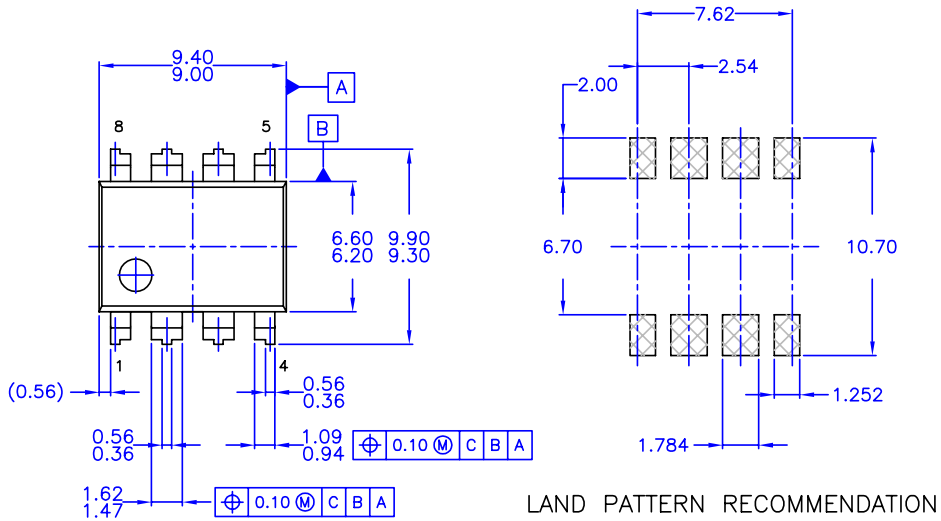


- NOTES: UNLESS OTHERWISE SPECIFIED**
- A) THIS PACKAGE CONFORMS TO JEDEC MS-001 VARIATION BA
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

MKT-N08FrevB

Package Dimensions (Continued)

8LSOP



DETAIL A
SCALE: 2X

- NOTES: UNLESS OTHERWISE SPECIFIED
- A) THIS PACKAGE DOESNOT CONFORM TO ANY CURRENT PACKAGE STANDARD
 - B) ALL DIMENSIONS ARE IN MILLIMETERS.
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
 - D) DIMENSIONS AND TOLERANCES PER ASME Y14.5M-1994

Ordering Information

Product Number	Package	Marking Code	BVDSS	FOSC	RDS(on)
FSDH321	8DIP	DH321	650V	100KHz	14Ω
FSDL321	8DIP	DL321	650V	50KHz	14Ω
FSDH321L	8LSOP	DH321	650V	100KHz	14Ω
FSDL321L	8LSOP	DL321	650V	50KHz	14Ω

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2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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