



# THE DATASHEET OF INA333SHKJ



# Micro-Power, Zero-Drift, Rail-to-Rail Out Instrumentation Amplifier

Check for Samples: [INA333-HT](#)

## FEATURES

- **Low Offset Voltage:** 25  $\mu\text{V}$  (max at 25°C),  $G \geq 100$
- **Low Drift:** 0.2  $\mu\text{V}/^\circ\text{C}$ ,  $G \geq 1000$
- **Low Noise:** 55  $\text{nV}/\sqrt{\text{Hz}}$ ,  $G \geq 100$
- **High CMRR:** 100 dB (min at 25°C),  $G \geq 10$
- **Supply Range:** +1.8 V to +5.5 V
- **Input Voltage:** (V–) +0.1 V to (V+) –0.1 V
- **Output Range:** (V–) +0.05 V to (V+) –0.05V
- **Low Quiescent Current:** 198  $\mu\text{A}$
- **RFI Filtered Inputs**

## APPLICATIONS

- **Down-Hole Drilling**
- **High Temperature Environments**

## DESCRIPTION

The INA333 is a low-power, precision instrumentation amplifier offering excellent accuracy. The versatile 3-op amp design, small size, and low power make it ideal for a wide range of portable applications.

A single external resistor sets any gain from 1 to 1000. The INA333 is designed to use an industry-standard gain equation:  $G = 1 + (100\text{k}\Omega/R_G)$ .

The INA333 provides very low offset voltage (25  $\mu\text{V}$  at 25°C,  $G \geq 100$ ), excellent offset voltage drift (0.2  $\mu\text{V}/^\circ\text{C}$ ,  $G \geq 100$ ), and high common-mode rejection (100 dB at 25°C,  $G \geq 10$ ). It operates with power supplies as low as 1.8 V ( $\pm 0.9\text{V}$ ), and quiescent current is only 50  $\mu\text{A}$ —ideal for battery-operated systems. Using autocalibration techniques to ensure excellent precision over the extended industrial temperature range, the INA333 also offers exceptionally low noise density (55  $\text{nV}/\sqrt{\text{Hz}}$ ) that extends down to dc.

The INA333 is specified over the  $T_A = -55^\circ\text{C}$  to  $+210^\circ\text{C}$  temperature range.

## SUPPORTS EXTREME TEMPERATURE APPLICATIONS

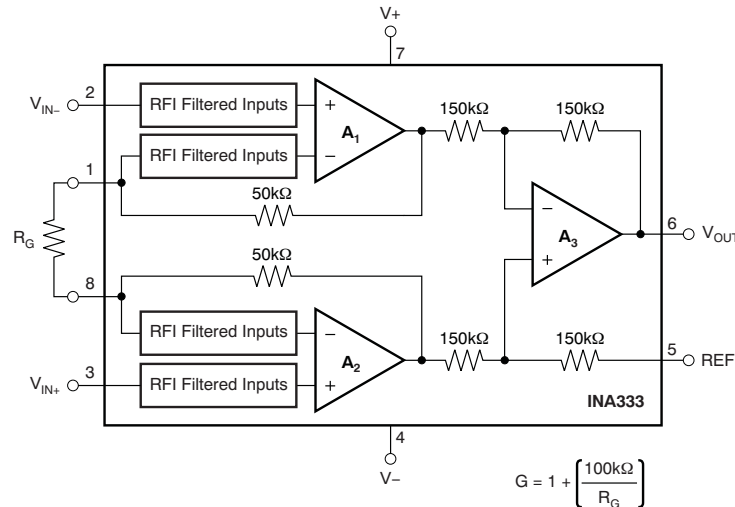
- **Controlled Baseline**
- **One Assembly/Test Site**
- **One Fabrication Site**
- **Available in Extreme ( $-55^\circ\text{C}/210^\circ\text{C}$ ) Temperature Range** <sup>(1)</sup>
- **Extended Product Life Cycle**
- **Extended Product-Change Notification**
- **Product Traceability**
- **Texas Instruments' high temperature products utilize highly optimized silicon (die) solutions with design and process enhancements to maximize performance over extended temperatures.**

(1) Custom temperature ranges available



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ORDERING INFORMATION<sup>(1)</sup>

T <sub>A</sub>	PACKAGE <sup>(2)</sup>	ORDERABLE PART NUMBER	TOP-SIDE MARKING	PACKAGE QTY   CARRIER
–55°C to 210°C	KGD	INA333SKGD1	NA	240   TRAY
		INA333SKGD2	NA	10   TRAY
	JD	INA333SJD	INA333SJD	1   TUBE
	HKJ	INA333SHKJ	INA333SHKJ	1   TUBE
	HKQ	INA333SHKQ	INA333SHKQ	1   TUBE

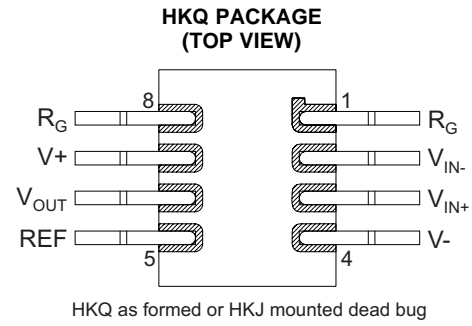
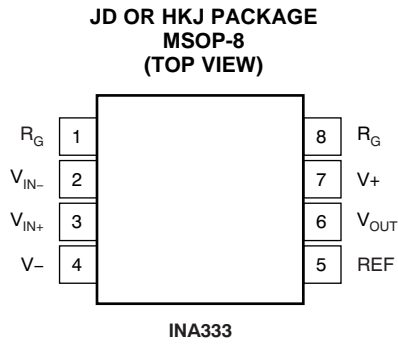
- (1) For the most current package and ordering information see the Package Option Addendum at the end of this document, or see the TI web site at [www.ti.com](http://www.ti.com).
- (2) Package drawings, standard packaging quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/packaging](http://www.ti.com/packaging).

## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

		INA333	UNIT
Supply voltage		+7	V
Analog input voltage range <sup>(2)</sup>		(V–) – 0.3 to (V+) + 0.3	V
Output short-circuit <sup>(3)</sup>		Continuous	
Operating temperature range, T <sub>A</sub>		–55 to +210	°C
Storage temperature range, T <sub>STG</sub>		–65 to +210	°C
Junction temperature, T <sub>J</sub>		+210	°C
ESD rating	Human body model (HBM)	4000	V
	Charged device model (CDM)	1000	V
	Machine model (MM)	200	V

- (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
- (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.3V beyond the supply rails should be current limited to 10mA or less.
- (3) Short-circuit to ground.

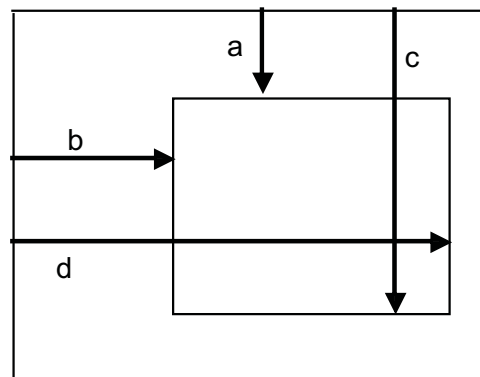
**PIN CONFIGURATIONS**



**BARE DIE INFORMATION**

DIE THICKNESS	BACKSIDE FINISH	BACKSIDE POTENTIAL	BOND PAD METALLIZATION COMPOSITION
15 mils.	Silicon with backgrind	V-	Al-Si-Cu (0.5%)

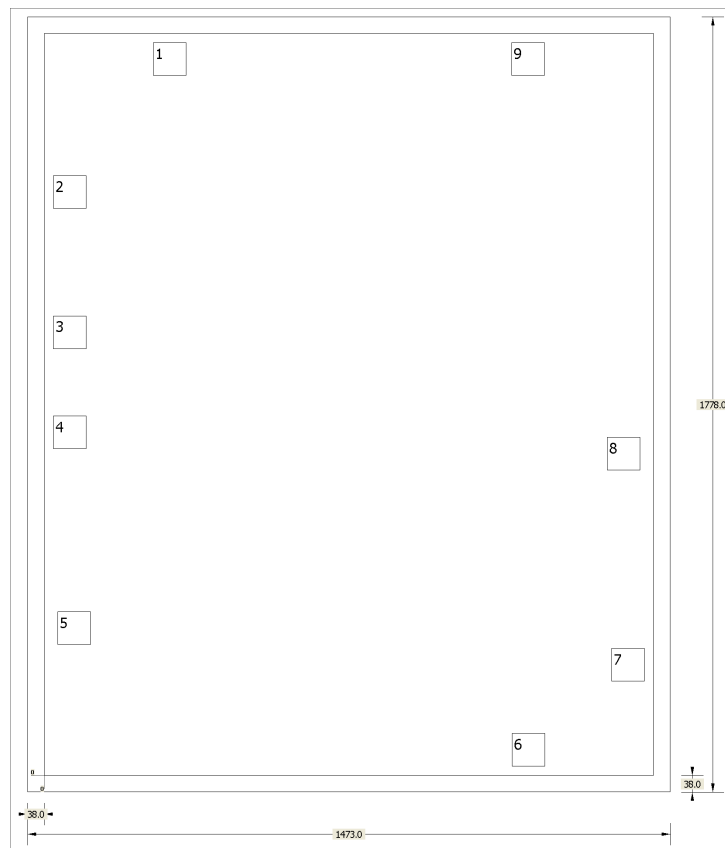
Origin



**Table 1. Bond Pad Coordinates in Microns<sup>(1)</sup>**

DESCRIPTION	PAD NUMBER	X MIN	Y MIN	X MAX	Y MAX
R <sub>G</sub>	1	250	1604.8	326	1680.8
V <sub>IN-</sub>	2	21.2	1300	97.2	1376
V <sub>IN+</sub>	3	21.2	978.5	97.2	1054.5
NC	4	21.2	748.65	97.2	824.65
V <sub>-</sub>	5	31.3	300	107.3	376
REF	6	1072.15	21.2	1148.15	97.2
V <sub>OUT</sub>	7	1299.8	216.2	1375.8	292.2
V <sub>+</sub>	8	1289.7	700	1365.7	776
R <sub>G</sub>	9	1071	1604.8	1147	1680.8

(1) Substrate is N/C



## THERMAL CHARACTERISTICS FOR JD PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JA}$	Junction-to-ambient thermal resistance <sup>(1)</sup>	High-K board <sup>(2)</sup> , no airflow		64.9		°C/W
		No airflow		83.4		
$\theta_{JB}$	Junction-to-board thermal resistance	High-K board without underfill		27.9		°C/W
$\theta_{JC}$	Junction-to-case thermal resistance			6.49		°C/W

- (1) The intent of  $\theta_{JA}$  specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.
- (2) JED51-7, high effective thermal conductivity test board for leaded surface mount packages.

## THERMAL CHARACTERISTICS FOR HKJ OR HKQ PACKAGE

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\theta_{JC}$	Junction-to-case thermal resistance	to ceramic side of case			5.7	°C/W
		to top of case lid (metal side of case)			13.7	

## ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V to }+5.5\text{ V}$

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S/2$ , and  $G = 1$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			$T_A = +210^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT<sup>(1)</sup></b>								
Offset voltage, $V_{OSI}$ RTI <sup>(2)</sup>			$\pm 10 \pm 25/G$	$\pm 25 \pm 75/G$		$\pm 15$		$\mu\text{V}$
<b>vs Temperature</b>				$\pm 0.1 \pm 0.5/G^{(3)}$		$0.2^{(4)(5)}$		$\mu\text{V}/^\circ\text{C}$
vs Power supply Long-term stability	$1.8\text{ V} \leq V_S \leq 5.5\text{ V}$		$\pm 1 \pm 5/G$ See note <sup>(6)</sup>	$\pm 5 \pm 15/G$		$2.5^{(4)}$		$\mu\text{V/V}$
Turn-on time to specified $V_{OSI}$		See Typical characteristics			See Typical characteristics			
Impedance								
Differential $Z_{IN}$			$100 \parallel 3$			$100 \parallel 3$		$\text{G}\Omega \parallel \text{pF}$
Common-mode $Z_{IN}$			$100 \parallel 3$			$100 \parallel 3$		$\text{G}\Omega \parallel \text{pF}$
Common-mode voltage range $V_{CM}$	$V_O = 0\text{ V}$	$(V-) + 0.1$		$(V+) - 0.1$	$(V-) + 0.1$		$(V+) - 0.1\text{ V}$	$\text{V}$
Common-mode rejection $\text{CMR}$	DC to 60 Hz							
$G = 1$	$V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	80	90					dB
$G = 10$	$V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	100	110					dB
$G = 100$	$V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	100	115			110		dB
$G = 1000$	$V_{CM} = (V-) + 0.1\text{ V to } (V+) - 0.1\text{ V}$	100	115			113		dB
<b>INPUT BIAS CURRENT</b>								
Input bias current $I_B$			$\pm 70$	$\pm 200$		$\pm 1260$	$\pm 2044$	$\mu\text{A}$
<b>vs Temperature</b>			See Typical Characteristic curve			See Typical Characteristic curve		$\mu\text{A}/^\circ\text{C}$
Input offset current $I_{OS}$			$\pm 50$	$\pm 200$				$\mu\text{A}$
<b>vs Temperature</b>			See Typical Characteristic curve			See Typical Characteristic curve		$\mu\text{A}/^\circ\text{C}$

- (1) Total  $V_{OS}$ , Referred-to-input =  $(V_{OSI}) + (V_{OSO}/G)$ .
- (2) RTI = Referred-to-input.
- (3) Temperature drift is measured from  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .
- (4)  $G = 1000$
- (5) Temperature drift is measured from  $125^\circ\text{C}$  to  $+210^\circ\text{C}$ .
- (6) 300-hour life test at  $+150^\circ\text{C}$  demonstrated randomly distributed variation of approximately  $1\ \mu\text{V}$ .

## ELECTRICAL CHARACTERISTICS: $V_S = +1.8\text{ V to }+5.5\text{ V}$ (continued)

 At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{ k}\Omega$ ,  $V_{REF} = V_S/2$ , and  $G = 1$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			$T_A = +210^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
<b>INPUT VOLTAGE NOISE</b>								
Input voltage noise	$e_{NI}$	$G = 100, R_S = 0\ \Omega$						
$f = 10\text{ Hz}$			42			63		$\text{nV}/\sqrt{\text{Hz}}$
$f = 100\text{ Hz}$			40			70		$\text{nV}/\sqrt{\text{Hz}}$
$f = 1\text{ kHz}$			50			55		$\text{nV}/\sqrt{\text{Hz}}$
$f = 0.1\text{ Hz to }10\text{ Hz}$			2			6		$\mu\text{V}_{PP}$
Input current noise	$i_N$							
$f = 10\text{ Hz}$			100					$\text{fA}/\sqrt{\text{Hz}}$
$f = 0.1\text{ Hz to }10\text{ Hz}$			2					$\text{pA}_{PP}$
<b>GAIN</b>								
Gain equation	$G$		$1 + (100\text{ k}\Omega/R_G)$			$1 + (100\text{ k}\Omega/R_G)$		$\text{V}/\text{V}$
Range of gain <sup>(7)</sup>		1		1000	100		1000	$\text{V}/\text{V}$
Gain error		$V_S = 5.5\text{ V},$ $(V^-) + 100\text{ mV} \leq V_O \leq$ $(V^+) - 100\text{ mV}$						
$G = 1$			$\pm 0.02$	$\pm 0.1$				%
$G = 10$			$\pm 0.05$	$\pm 0.5$				%
$G = 100$			$\pm 0.01$	$\pm 0.5$		$\pm 1.3$		%
$G = 1000$			$\pm 0.43$	$\pm 1.15$		$\pm 1.7$		%
<b>GAIN (continued)</b>								
<b>Gain vs Temperature</b>								
$G = 1$			$\pm 1$	$\pm 5$				$\text{ppm}/^\circ\text{C}$
$G > 1$ <sup>(8)</sup>			$\pm 15$	$\pm 50$				$\text{ppm}/^\circ\text{C}$
Gain nonlinearity		$V_S = 5.5\text{ V},$ $(V^-) + 100\text{ mV} \leq V_O \leq$ $(V^+) - 100\text{ mV}$						
$G = 1\text{ to }1000$		$R_L = 10\text{ k}\Omega$	10			10		ppm
<b>OUTPUT</b>								
Output voltage swing from rail <sup>(9)</sup>		$V_S = 5.5\text{ V}, R_L = 10\text{ k}\Omega$	See note <sup>(9)</sup>	50			185	mV
Capacitive load drive			500			500		pF
Short-circuit current	$I_{SC}$	Continuous to common	-55, +5			-36, +1		mA
<b>FREQUENCY RESPONSE</b>								
Bandwidth, -3dB								
Range of gain <sup>(7)</sup>								
$G = 1$			150					kHz
$G = 10$			35					kHz
$G = 100$			3.5			3.1		kHz
$G = 1000$			350			300		Hz
Slew rate	SR	$V_S = 5\text{ V}, V_O = 4\text{ V Step}$						
$G = 1$			0.16			0.25		$\text{V}/\mu\text{s}$
$G = 100$			0.06			0.04		$\text{V}/\mu\text{s}$
Settling time to 0.01%	$t_S$							
$G = 1$		$V_{STEP} = 4\text{ V}$	35			32		$\mu\text{s}$
$G = 100$		$V_{STEP} = 4\text{ V}$	240			326		$\mu\text{s}$
Settling time to 0.001%	$t_S$							

(7) Not recommend gain &lt; 100 for 210°C application.

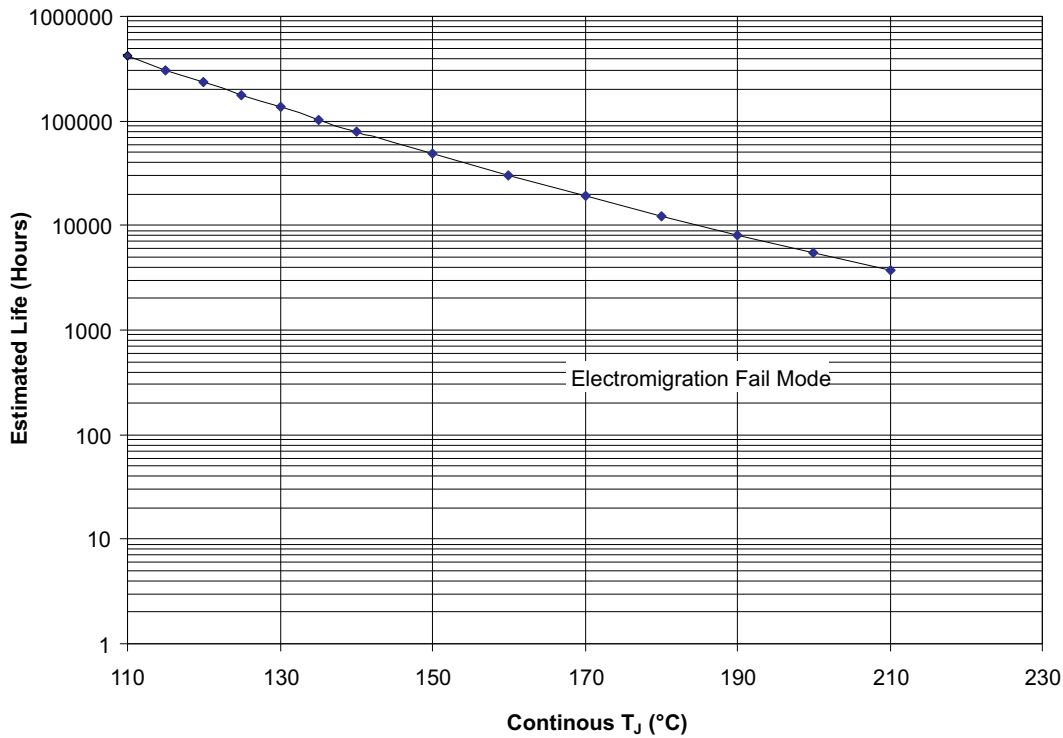
 (8) Does not include effects of external resistor  $R_G$ .

 (9) See Typical Characteristics curve, *Output Voltage Swing vs Output Current* (Figure 31).

**ELECTRICAL CHARACTERISTICS:  $V_S = +1.8\text{ V to }+5.5\text{ V}$  (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = V_S/2$ , and  $G = 1$ , unless otherwise noted.

PARAMETER	TEST CONDITIONS	$T_A = -55^\circ\text{C to }+125^\circ\text{C}$			$T_A = +210^\circ\text{C}$			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	
$G = 1$	$V_{STEP} = 4\text{ V}$		60			55		$\mu\text{s}$
$G = 100$	$V_{STEP} = 4\text{ V}$		500			530		$\mu\text{s}$
Overload recovery	50% overdrive		52			28		$\mu\text{s}$
<b>REFERENCE INPUT</b>								
$R_{IN}$			300			300		$\text{k}\Omega$
Voltage range		V-		V+	V-		V+	V
<b>POWER SUPPLY</b>								
Voltage range								
Single		+1.8		+5.5	+1.8		+5.5	V
Dual		$\pm 0.9$		$\pm 2.75$	$\pm 0.9$		$\pm 2.75$	V
Quiescent current $I_Q$	$V_{IN} = V_S/2$		50	75				$\mu\text{A}$
<b>vs Temperature</b>				<b>80</b>		<b>198</b>	<b>345</b>	<b><math>\mu\text{A}</math></b>
<b>TEMPERATURE RANGE</b>								
Specified temperature range		-55		+125	-55		+210	$^\circ\text{C}$
Operating temperature range		-55		+125	-55		+210	$^\circ\text{C}$



Notes

- See datasheet for absolute maximum and minimum recommended operating conditions.
- Silicon operating life design goal is 10 years at  $105^\circ\text{C}$  junction temperature (does not include package interconnect life).

**Figure 1. INA333SKGD1 Operating Life Derating Chart**

## TYPICAL CHARACTERISTICS

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

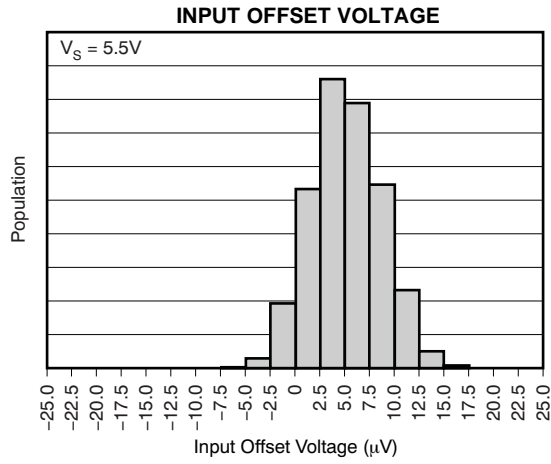


Figure 2.

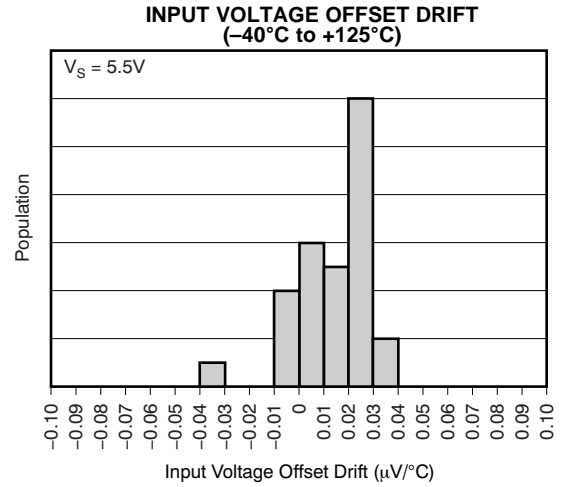


Figure 3.

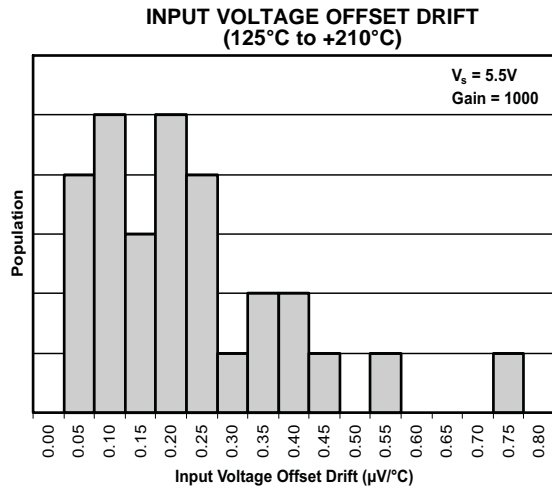


Figure 4.

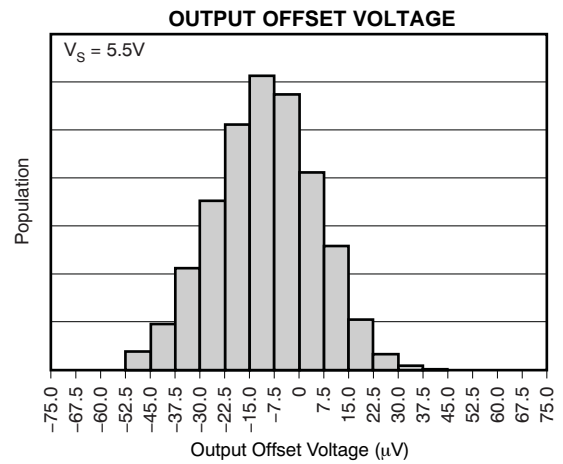


Figure 5.

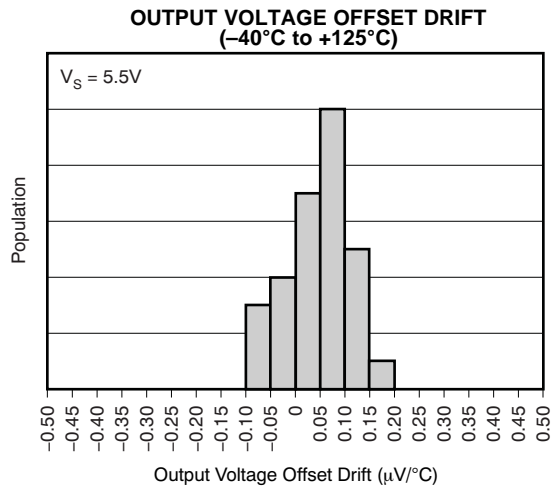


Figure 6.

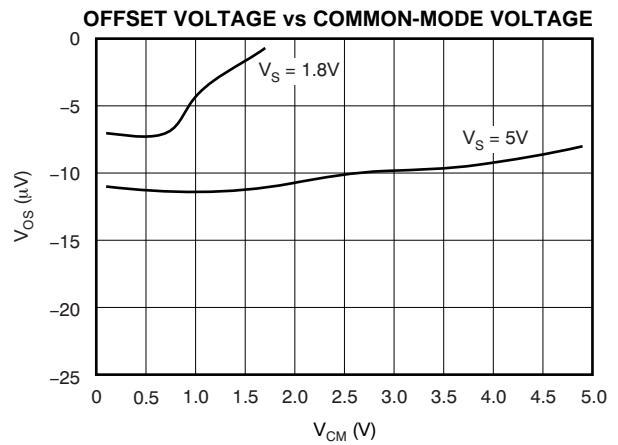


Figure 7.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

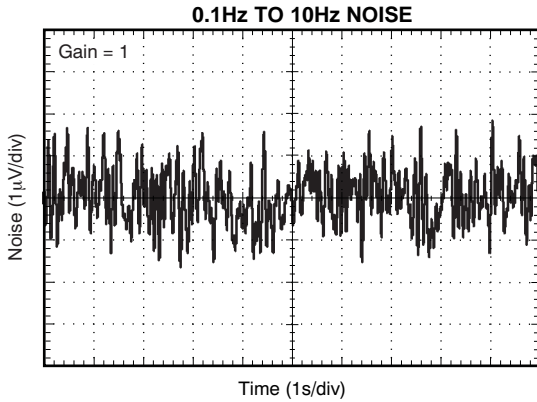


Figure 8.

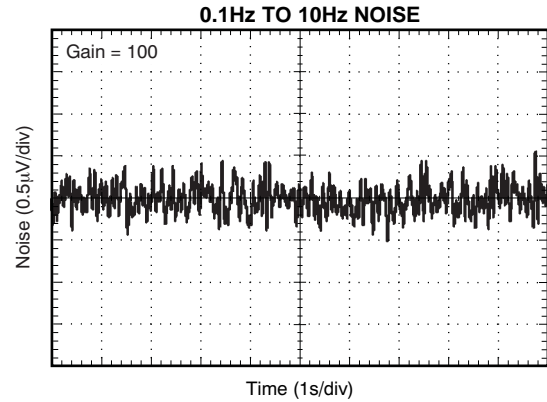


Figure 9.

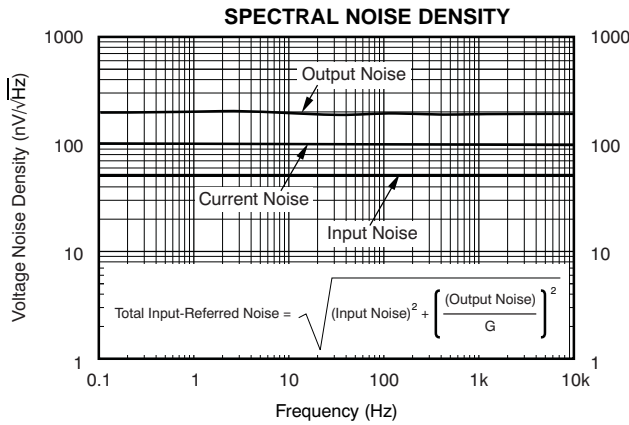


Figure 10.

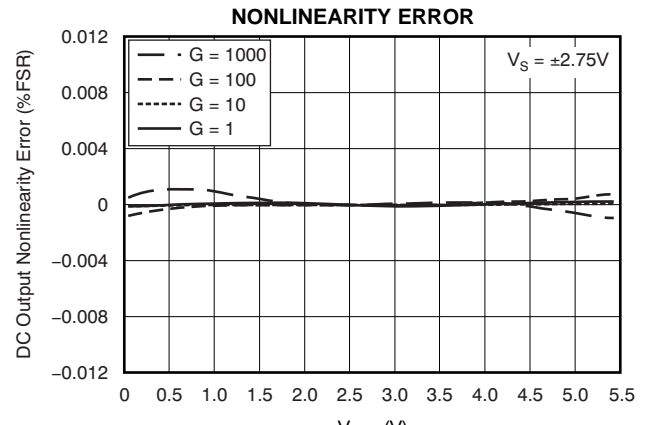


Figure 11.

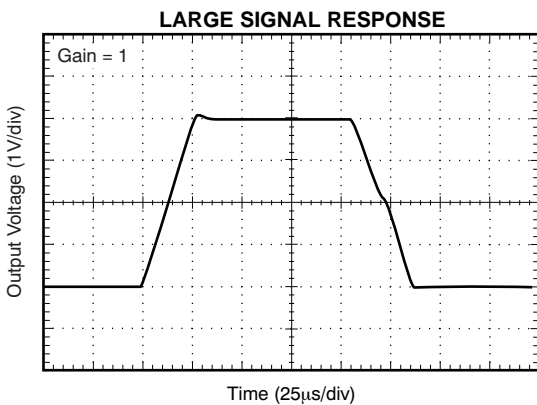


Figure 12.

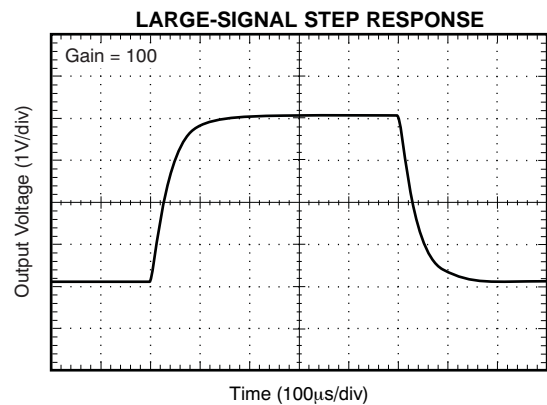


Figure 13.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

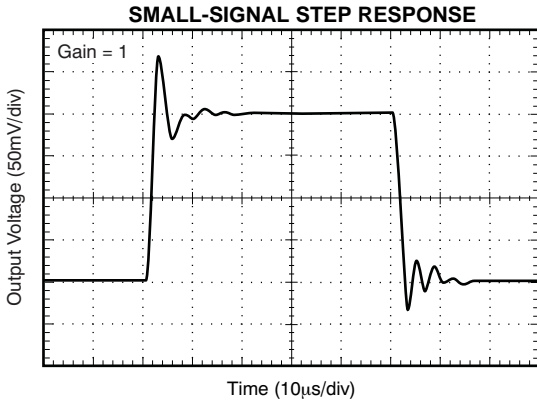


Figure 14.

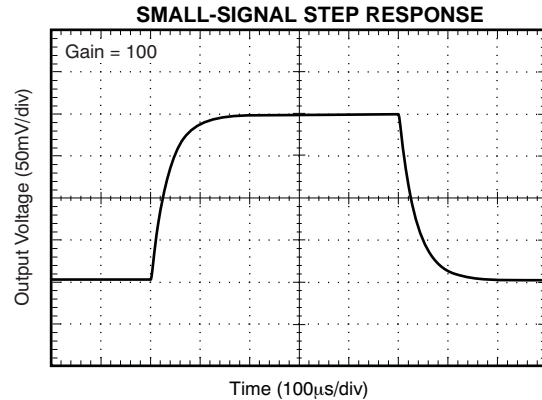


Figure 15.

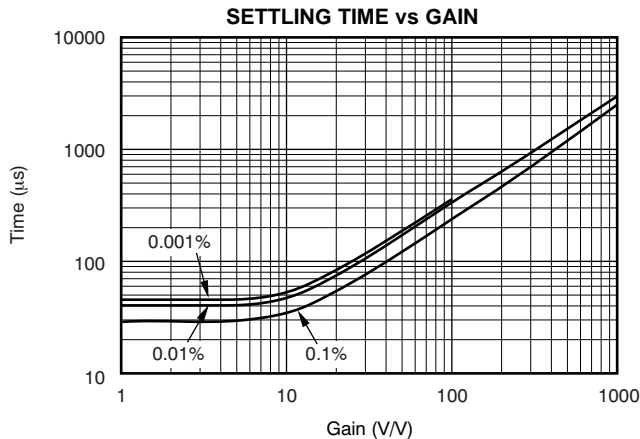


Figure 16.

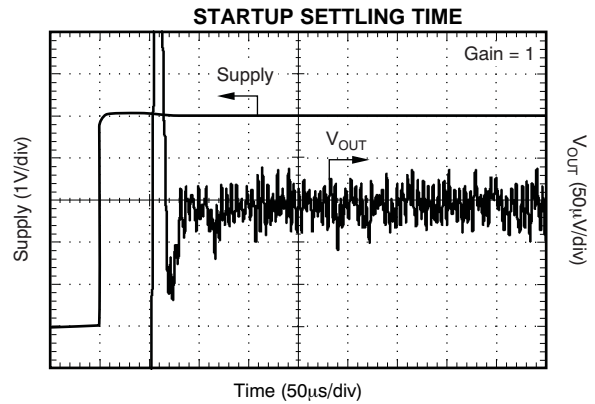


Figure 17.

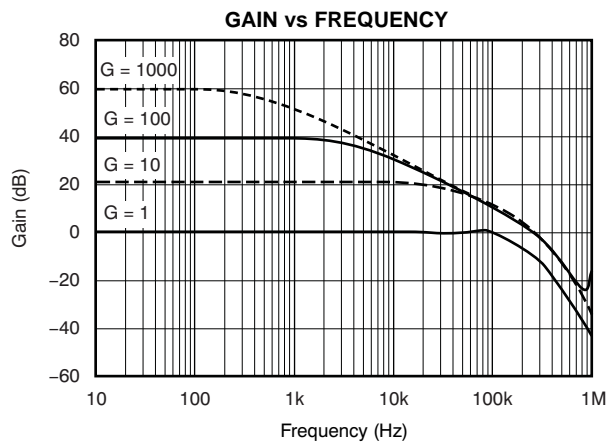


Figure 18.

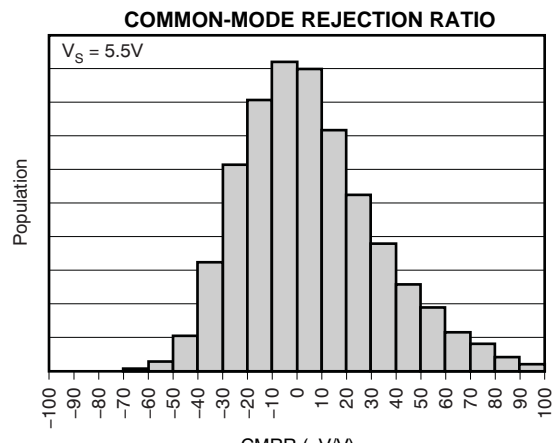


Figure 19.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

**COMMON-MODE REJECTION RATIO vs TEMPERATURE**

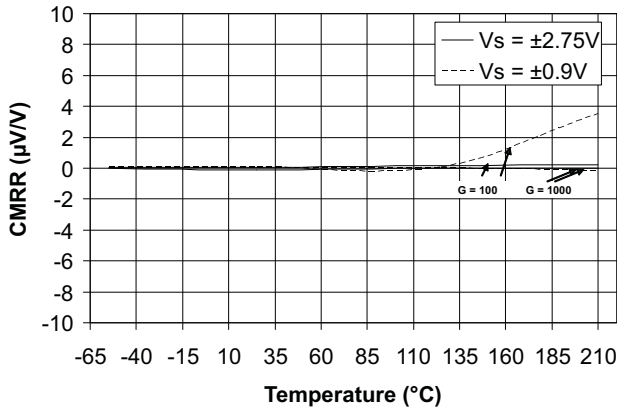


Figure 20.

**COMMON-MODE REJECTION RATIO vs FREQUENCY**

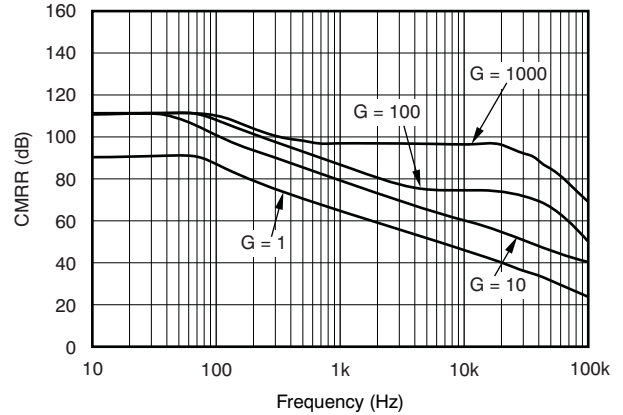


Figure 21.

**TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE**

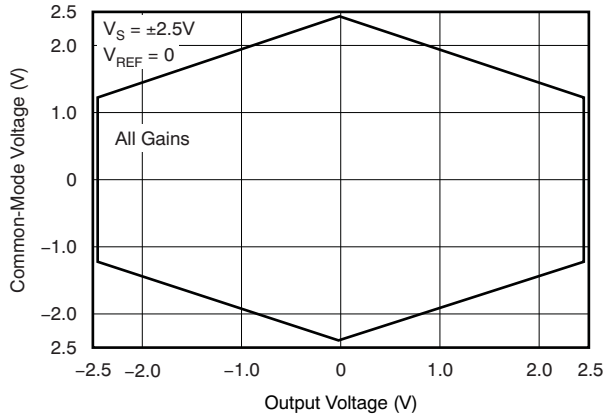


Figure 22.

**TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE**

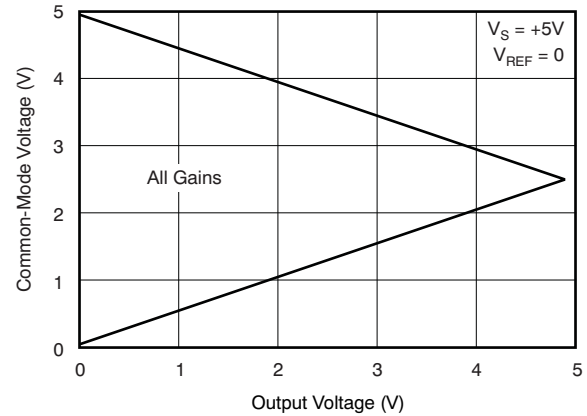


Figure 23.

**TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE**

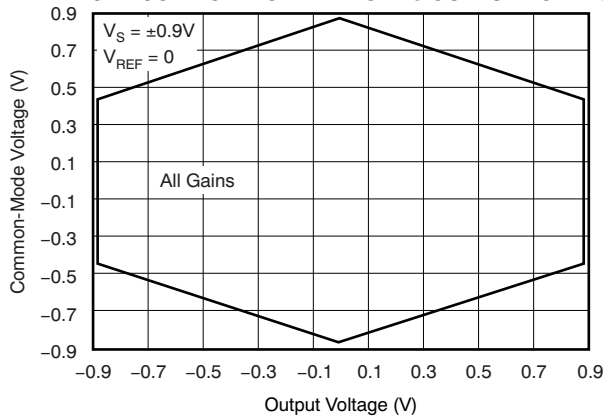


Figure 24.

**TYPICAL COMMON-MODE RANGE vs OUTPUT VOLTAGE**

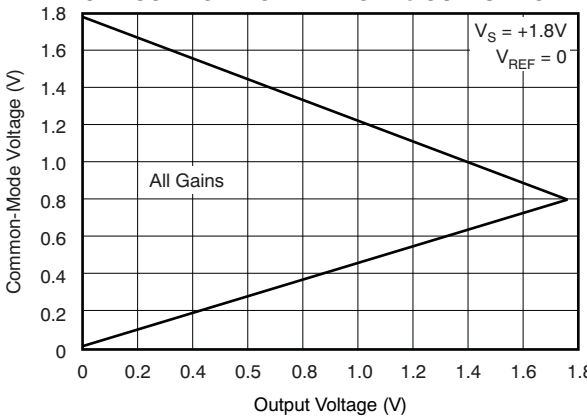


Figure 25.

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{REF} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

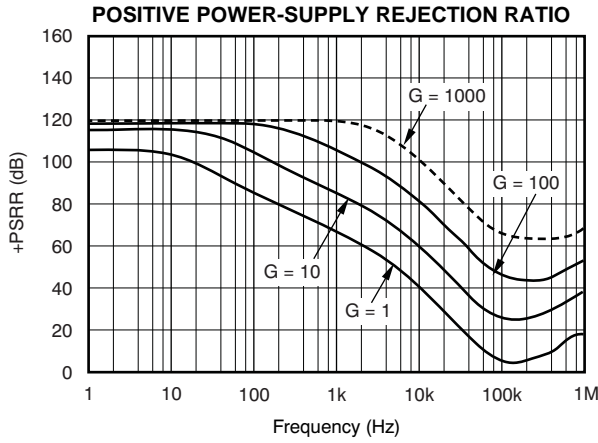


Figure 26.

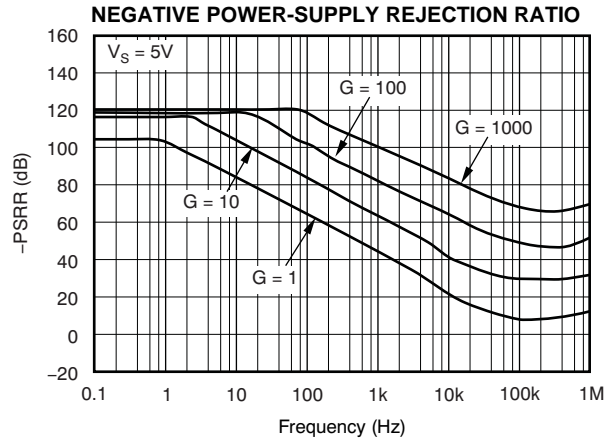


Figure 27.

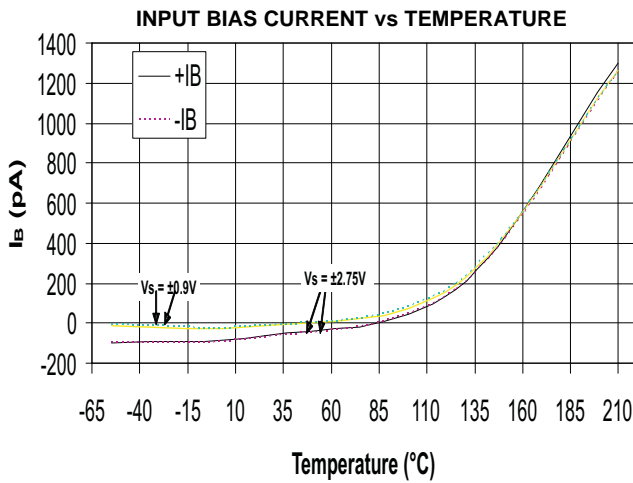


Figure 28.

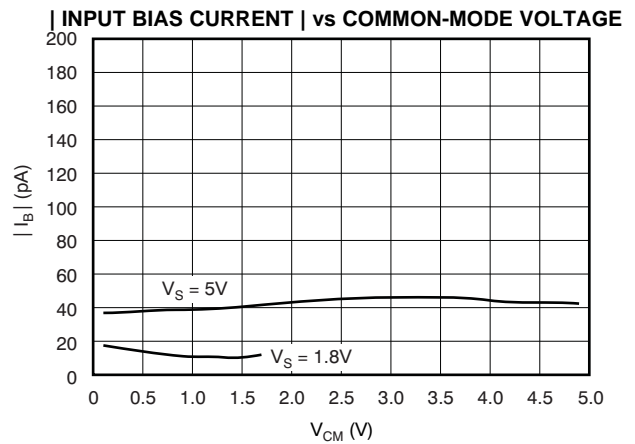


Figure 29.

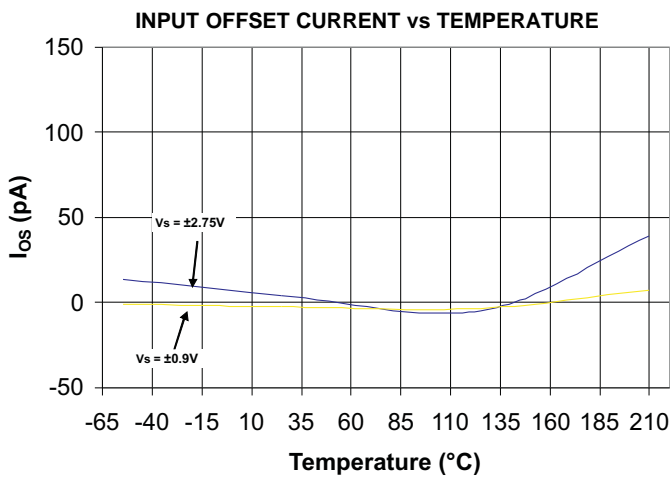


Figure 30.

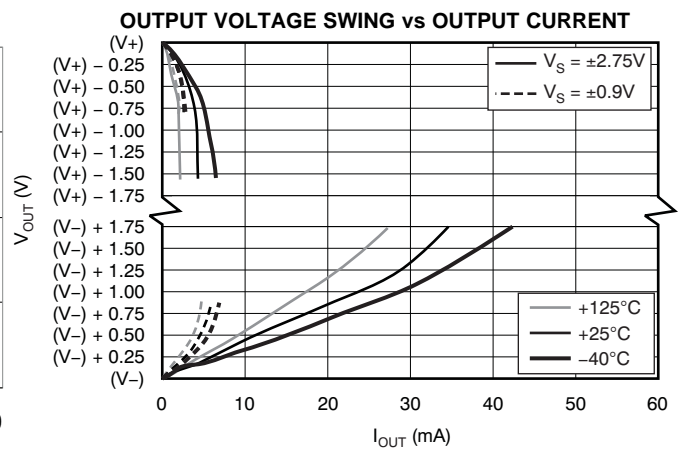


Figure 31.

**TYPICAL CHARACTERISTICS (continued)**

At  $T_A = +25^\circ\text{C}$ ,  $V_S = 5\text{V}$ ,  $R_L = 10\text{k}\Omega$ ,  $V_{\text{REF}} = \text{midsupply}$ , and  $G = 1$ , unless otherwise noted.

**QUIESCENT CURRENT vs TEMPERATURE**

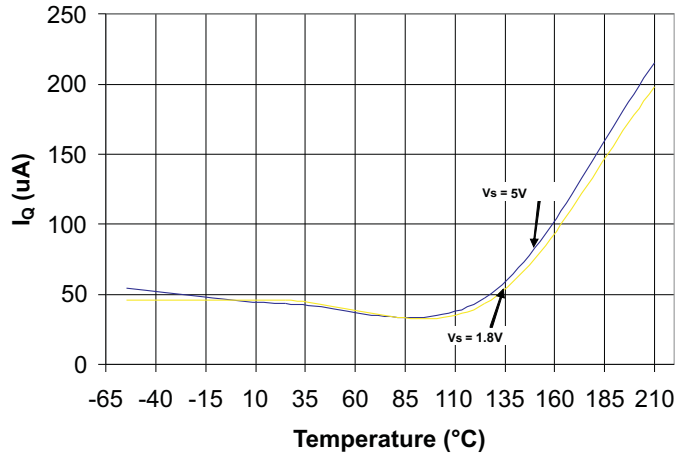


Figure 32.

**QUIESCENT CURRENT vs COMMON-MODE VOLTAGE**

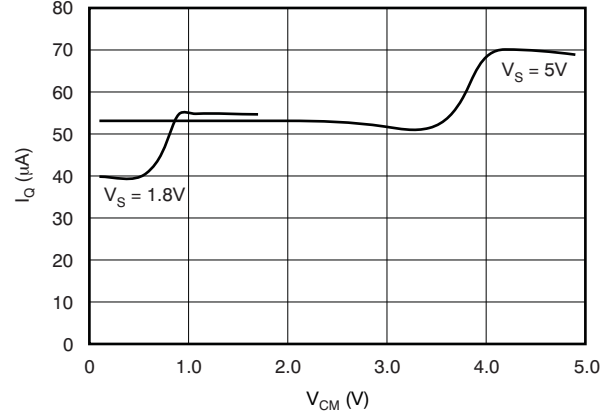


Figure 33.

## APPLICATION INFORMATION

Application information below is provided for commercial temperature as a reference and not for high temperature.

It is not recommended to use a gain < 100 for high temperature (210°C) applications. For gains > 100 in such applications, a compensation circuit is needed at pins 1 and 8. The circuit is needed at each pin and consists of a resistor in series with a capacitor referenced to ground. Recommended values for the resistor and capacitor are 3.5 kΩ and 10 nF respectively.

[Figure 34](#) shows the basic connections required for operation of the INA333. Good layout practice mandates the use of bypass capacitors placed close to the device pins as shown.

The output of the INA333 is referred to the output reference (REF) terminal, which is normally grounded. This connection must be low-impedance to assure good common-mode rejection. Although 15 Ω or less of stray resistance can be tolerated while maintaining specified CMRR, small stray resistances of tens of ohms in series with the REF pin can cause noticeable degradation in CMRR.

### SETTING THE GAIN

Gain of the INA333 is set by a single external resistor,  $R_G$ , connected between pins 1 and 8. The value of  $R_G$  is selected according to [Equation 1](#):

$$G = 1 + (100 \text{ k}\Omega / R_G) \quad (1) \quad (1)$$

[Table 2](#) lists several commonly-used gains and resistor values. The 100 kΩ term in [Equation 1](#) comes from the sum of the two internal feedback resistors of  $A_1$  and  $A_2$ . These on-chip resistors are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA333.

The stability and temperature drift of the external gain setting resistor,  $R_G$ , also affects gain. The contribution of  $R_G$  to gain accuracy and drift can be directly inferred from the gain [Equation 1](#). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance and contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater. To ensure stability, avoid parasitic capacitance of more than a few picofarads at the  $R_G$  connections. Careful matching of any parasitics on both  $R_G$  pins maintains optimal CMRR over frequency.

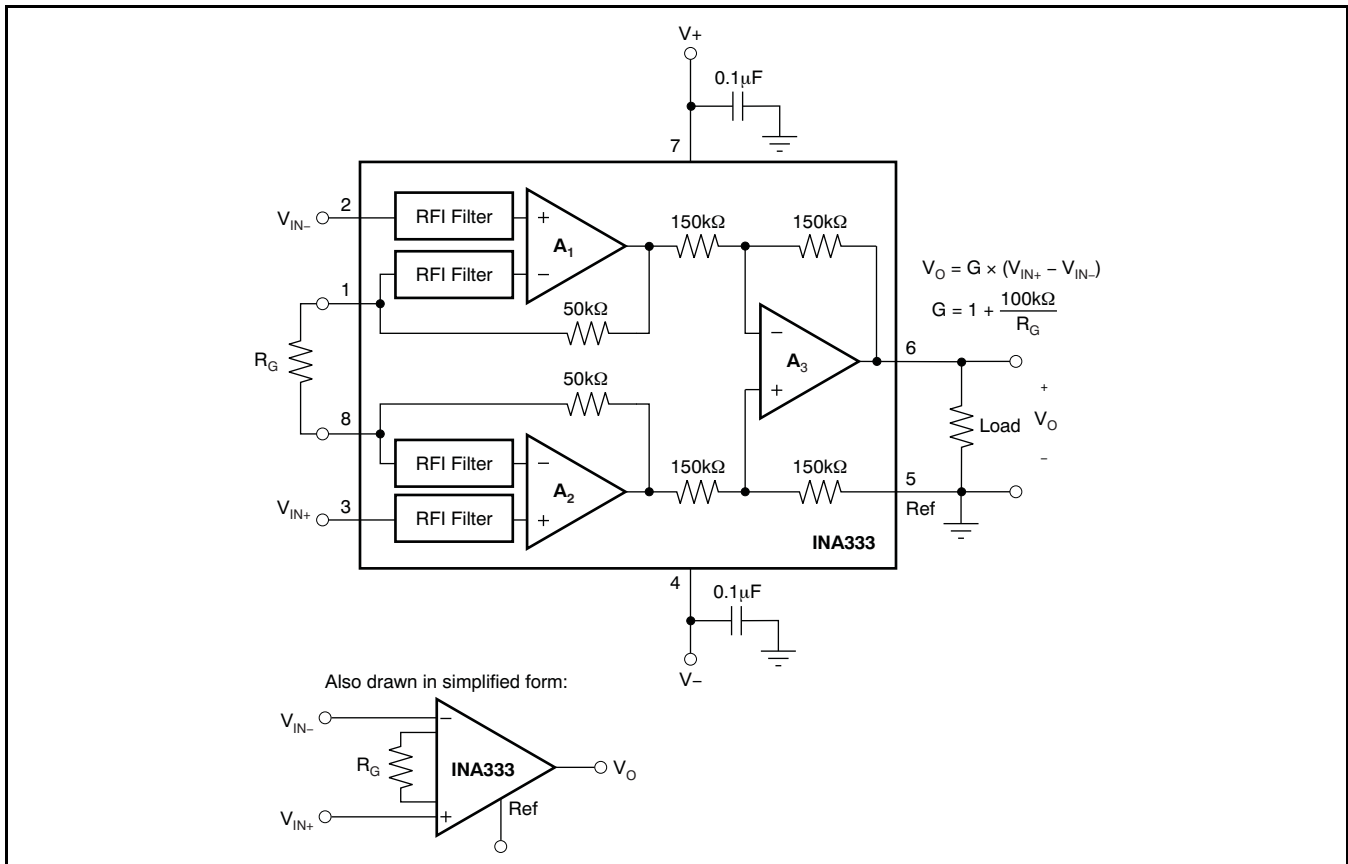


Figure 34. Basic Connections

Table 2. Commonly-Used Gains and Resistor Values

DESIRED GAIN	R <sub>G</sub> (Ω)	NEAREST 1% R <sub>G</sub> (Ω)
1	NC <sup>(1)</sup>	NC
2	100k	100k
5	25k	24.9k
10	11.1k	11k
20	5.26k	5.23k
50	2.04k	2.05
100	1.01k	1k
200	502.5	499
500	200.4	200
1000	100.1	100

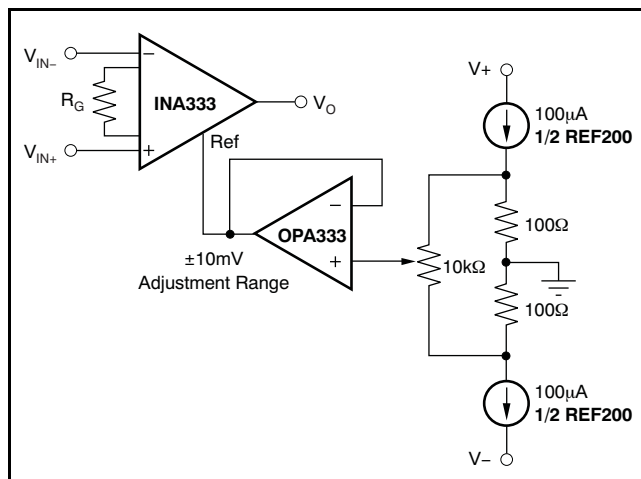
(1) NC denotes no connection. When using the SPICE model, the simulation will not converge unless a resistor is connected to the R<sub>G</sub> pins; use a very large resistor value.

## INTERNAL OFFSET CORRECTION

The INA333 internal op amps use an auto-calibration technique with a time-continuous 350-kHz op amp in the signal path. The amplifier is zero-corrected every 8  $\mu$ s using a proprietary technique. Upon power-up, the amplifier requires approximately 100  $\mu$ s to achieve specified  $V_{OS}$  accuracy. This design has no aliasing or flicker noise.

## OFFSET TRIMMING

Most applications require no external offset adjustment; however, if necessary, adjustments can be made by applying a voltage to the REF terminal. Figure 35 shows an optional circuit for trimming the output offset voltage. The voltage applied to REF terminal is summed at the output. The op amp buffer provides low impedance at the REF terminal to preserve good common-mode rejection.



(1) REF200 and OPA333 are not tested or characterized at 210°C.

**Figure 35. Optional Trimming of Output Offset Voltage**

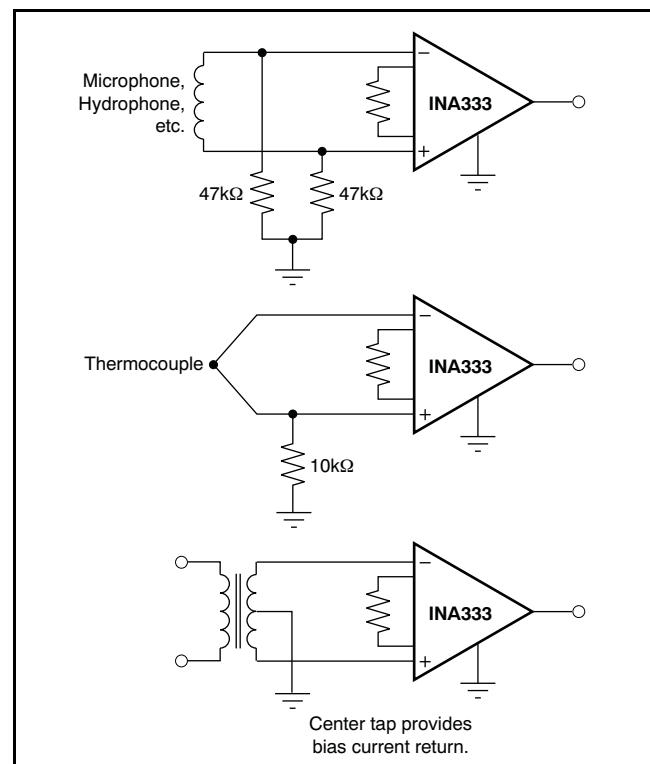
## NOISE PERFORMANCE

The auto-calibration technique used by the INA333 results in reduced low frequency noise, typically only 50 nV/ $\sqrt{\text{Hz}}$ , ( $G = 100$ ). The spectral noise density can be seen in detail in Figure 10. Low frequency noise of the INA333 is approximately 1  $\mu$ V<sub>PP</sub> measured from 0.1 Hz to 10 Hz, ( $G = 100$ ).

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA333 is extremely high—approximately 100 G $\Omega$ . However, a path must be provided for the input bias current of both inputs. This input bias current is typically  $\pm 70$  pA. High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current for proper operation. Figure 36 illustrates various provisions for an input bias current path. Without a bias current path, the inputs will float to a potential that exceeds the common-mode range of the INA333, and the input amplifiers will saturate. If the differential source resistance is low, the bias current return path can be connected to one input (see the thermocouple example in Figure 36). With higher source impedance, using two equal resistors provides a balanced input with possible advantages of lower input offset voltage as a result of bias current and better high-frequency common-mode rejection.



**Figure 36. Providing an Input Common-Mode Current Path**

## INPUT COMMON-MODE RANGE

The linear input voltage range of the input circuitry of the INA333 is from approximately 0.1 V below the positive supply voltage to 0.1 V above the negative supply. As a differential input voltage causes the output voltage to increase, however, the linear input range is limited by the output voltage swing of amplifiers  $A_1$  and  $A_2$ . Thus, the linear common-mode input range is related to the output voltage of the complete amplifier. This behavior also depends on supply voltage—see Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* (Figure 22 to Figure 25).

Input overload conditions can produce an output voltage that appears normal. For example, if an input overload condition drives both input amplifiers to the respective positive output swing limit, the difference voltage measured by the output amplifier is near zero. The output of the INA333 is near 0 V even though both inputs are overloaded.

## OPERATING VOLTAGE

The INA333 operates over a power-supply range of +1.8 V to +5.5 V ( $\pm 0.9$  V to  $\pm 2.75$  V). Supply voltages higher than +7 V (absolute maximum) can permanently damage the device. Parameters that vary over supply voltage or temperature are shown in the [Typical Characteristics](#) section of this data sheet.

## LOW VOLTAGE OPERATION

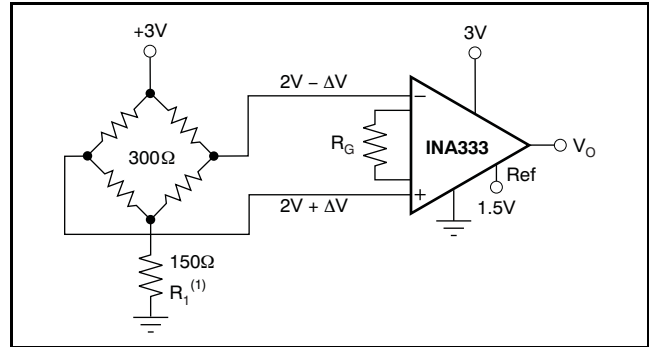
The INA333 can be operated on power supplies as low as  $\pm 0.9$  V. Most parameters vary only slightly throughout this supply voltage range—see the [Typical Characteristics](#) section. Operation at very low supply voltage requires careful attention to assure that the input voltages remain within the linear range. Voltage swing requirements of internal nodes limit the input common-mode range with low power-supply voltage. The Typical Characteristic curves *Typical Common-Mode Range vs Output Voltage* ([Figure 22](#) to [Figure 25](#)) show the range of linear operation for various supply voltages and gains.

## SINGLE-SUPPLY OPERATION

The INA333 can be used on single power supplies of +1.8 V to +5.5 V. [Figure 37](#) illustrates a basic single-supply circuit. The output REF terminal is connected to mid-supply. Zero differential input voltage demands an output voltage of mid-supply. Actual output voltage swing is limited to approximately 50 mV above ground, when the load is referred to ground as shown. The typical characteristic curve *Output Voltage Swing vs Output Current* ([Figure 31](#)) shows how the output voltage swing varies with output current.

With single-supply operation,  $V_{IN+}$  and  $V_{IN-}$  must both be 0.1V above ground for linear operation. For instance, the inverting input cannot be connected to ground to measure a voltage connected to the noninverting input.

To illustrate the issues affecting low voltage operation, consider the circuit in [Figure 37](#). It shows the INA333 operating from a single 3-V supply. A resistor in series with the low side of the bridge assures that the bridge output voltage is within the common-mode range of the amplifier inputs.



(1)  $R_1$  creates proper common-mode voltage, only for low-voltage operation—see the [Single-Supply Operation](#) section.

**Figure 37. Single-Supply Bridge Amplifier**

## INPUT PROTECTION

The input terminals of the INA333 are protected with internal diodes connected to the power-supply rails. These diodes clamp the applied signal to prevent it from damaging the input circuitry. If the input signal voltage can exceed the power supplies by more than 0.3 V, the input signal current should be limited to less than 10 mA to protect the internal clamp diodes. This current limiting can generally be done with a series input resistor. Some signal sources are inherently current-limited and do not require limiting resistors.

## GENERAL LAYOUT GUIDELINES

Attention to good layout practices is always recommended. Keep traces short and, when possible, use a printed circuit board (PCB) ground plane with surface-mount components placed as close to the device pins as possible. Place a 0.1- $\mu$ F bypass capacitor closely across the supply pins. These guidelines should be applied throughout the analog circuit to improve performance and provide benefits such as reducing the electromagnetic-interference (EMI) susceptibility.

Instrumentation amplifiers vary in the susceptibility to radio-frequency interference (RFI). RFI can generally be identified as a variation in offset voltage or dc signal levels with changes in the interfering RF signal. The INA333 has been specifically designed to minimize susceptibility to RFI by incorporating passive RC filters with an 8-MHz corner frequency at the  $V_{IN+}$  and  $V_{IN-}$  inputs. As a result, the INA333 demonstrates remarkably low sensitivity compared to previous generation devices. Strong RF fields may continue to cause varying offset levels, however, and may require additional shielding.

## APPLICATION IDEAS

Additional application ideas are shown in [Figure 38](#) to [Figure 41](#).

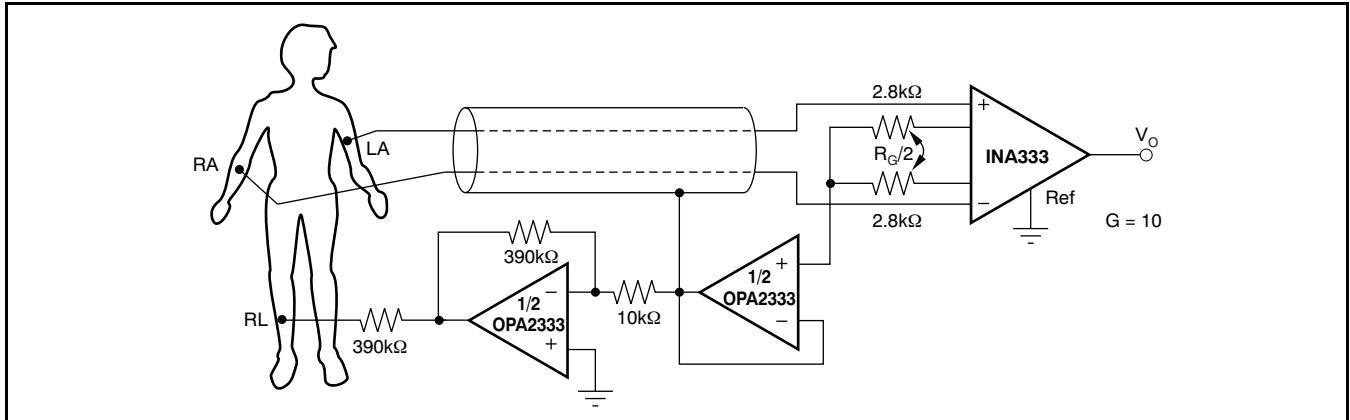
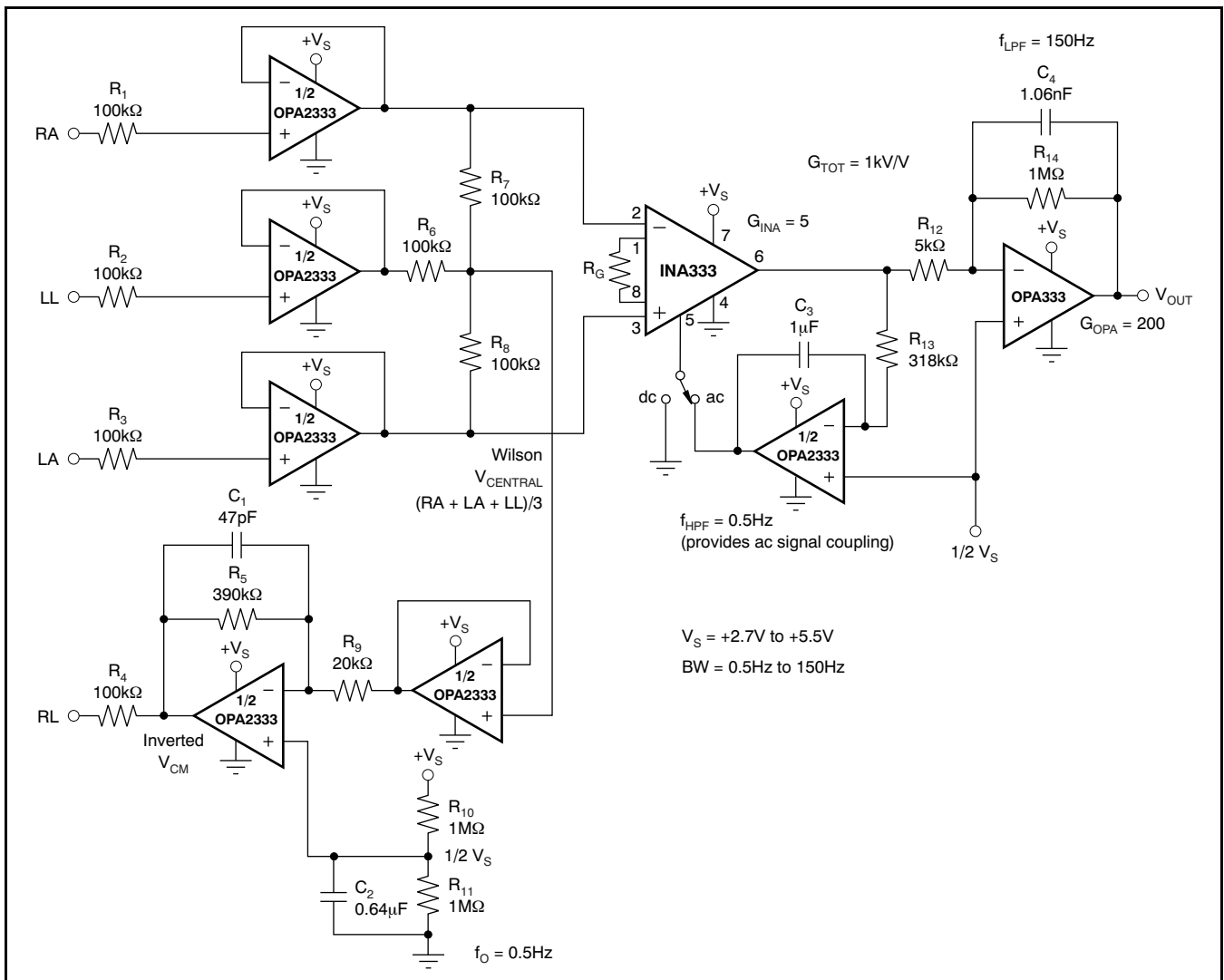


Figure 38. ECG Amplifier With Right-Leg Drive



(1) OPA333 is not tested or characterized at 210°C.

Figure 39. Single-Supply, Very Low Power, ECG Circuit

**TINA-TI  
(FREE DOWNLOAD SOFTWARE)**

**Using TINA-TI SPICE-Based Analog Simulation Program with the INA333**

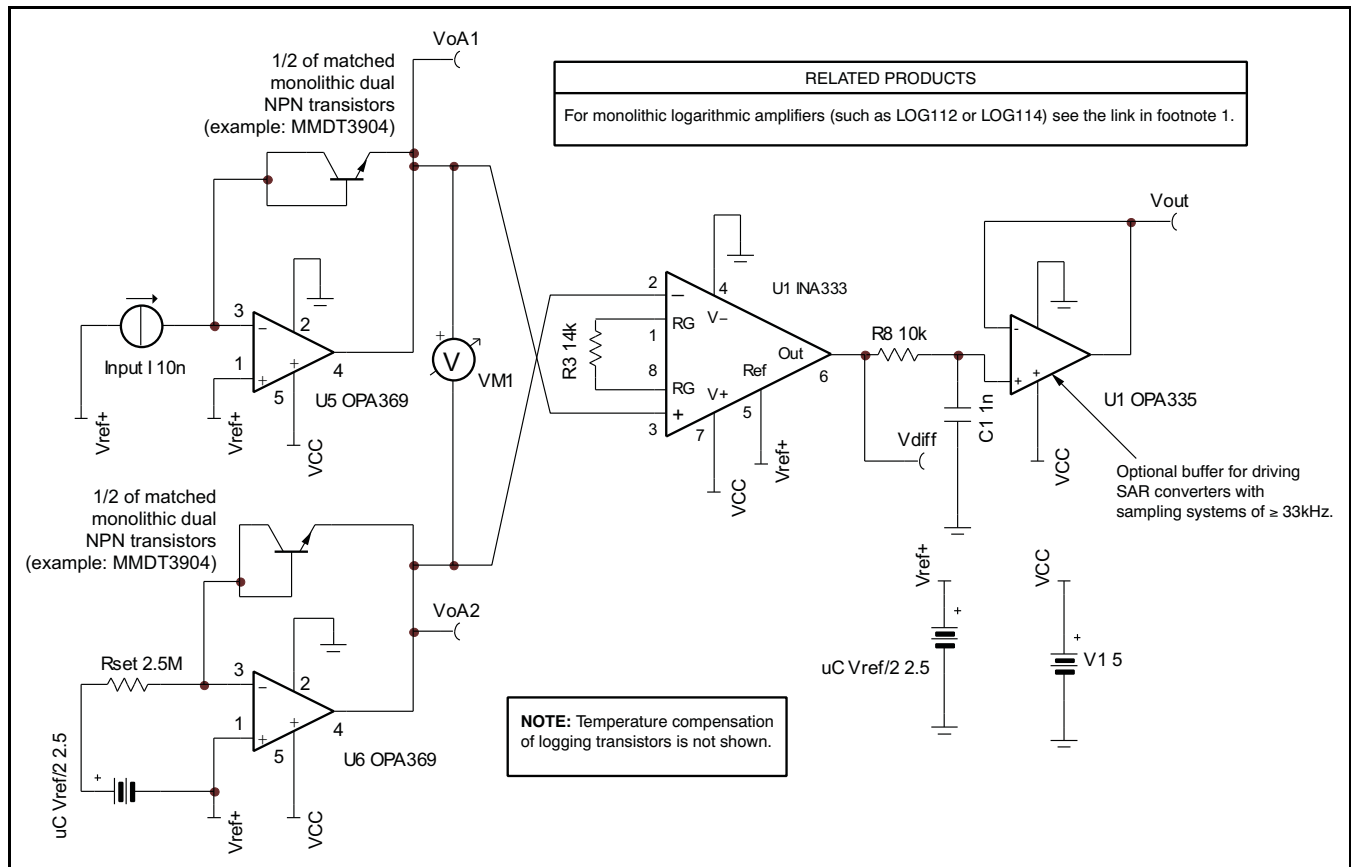
TINA is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully functional version of the TINA software, preloaded with a library of macromodels in addition to a range of both passive and active models. It provides all the conventional dc, transient, and frequency domain analysis of SPICE as well as additional design capabilities.

Available as a free download from the [Analog eLab Design Center](#), TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways.

Virtual instruments offer users the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

Figure 40 and Figure 41 show example TINA-TI circuits for the INA333 that can be used to develop, modify, and assess the circuit design for specific applications. Links to download these simulation files are given below.

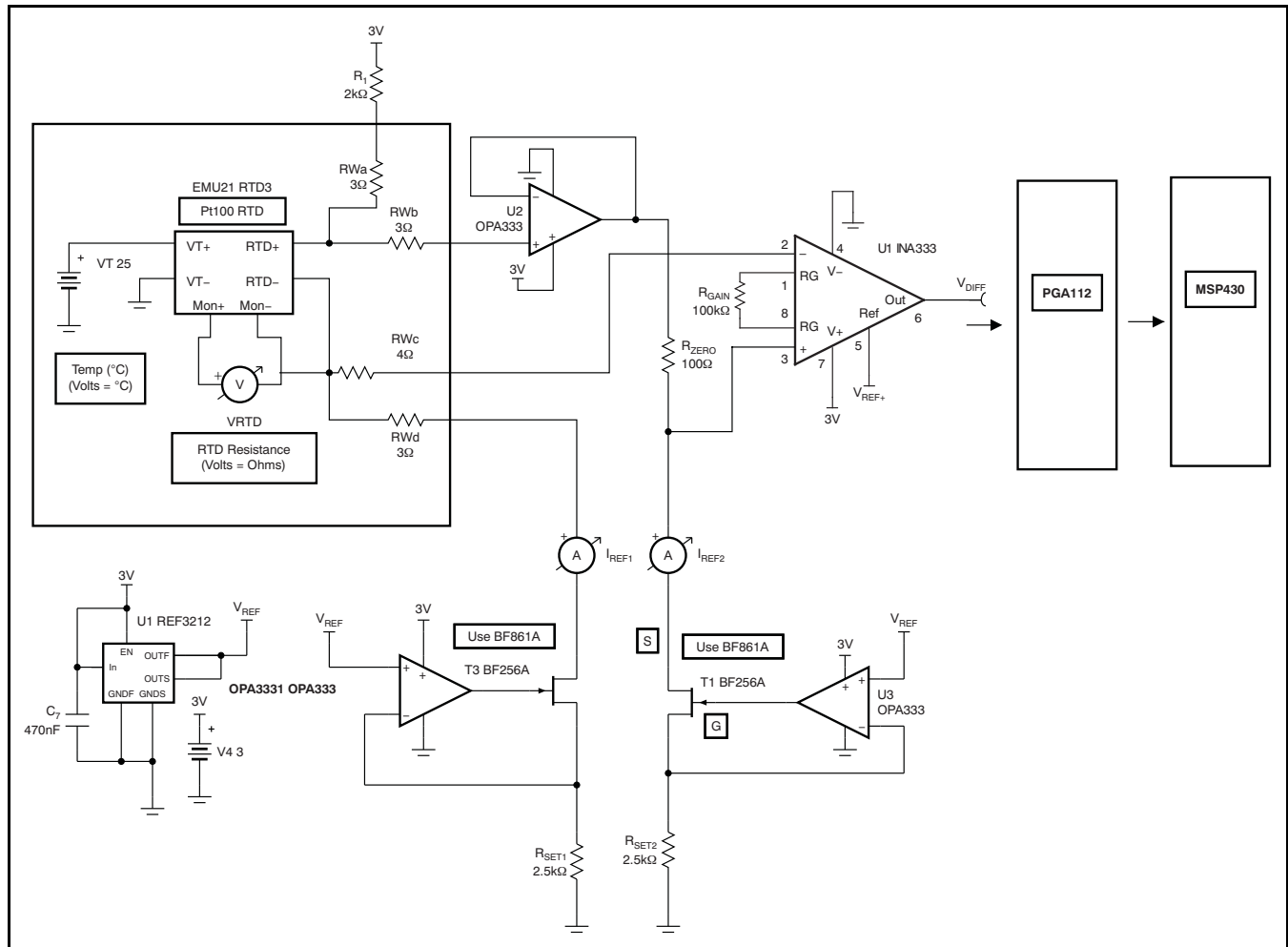
**NOTE:** these files require that either the TINA software (from DesignSoft) or TINA-TI software be installed. Download the free TINA-TI software from the [TINA-TI folder](#).



- (1) The following link launches the TI logarithmic amplifiers web page: [Logarithmic Amplifier Products Home Page](#)
- (2) OPA369 and OPA335 are not characterized at 210°C.

**Figure 40. Low-Power Log Function Circuit for Portable Battery-Powered Systems (Example Glucose Meter)**

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: [Log Circuit](#).



- (1) R<sub>Wa</sub>, R<sub>Wb</sub>, R<sub>Wc</sub>, and R<sub>Wd</sub> simulate wire resistance. These resistors are included to show the four-wire sense technique immunity to line mismatches. This method assumes the use of a four-wire RTD.
- (2) In this diagram, only INA333 is tested and characterized at 210°C.

**Figure 41. Four-Wire, 3V Conditioner for a PT100 RTD With Programmable Gain Acquisition System**

To download a compressed file that contains the TINA-TI simulation file for this circuit, click the following link: [PT100 RTD](#).

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
INA333SHKJ	ACTIVE	CFP	HKJ	8	1	TBD	Call TI	N / A for Pkg Type	-55 to 210	INA333S HKJ	<a href="#">Samples</a>
INA333SHKQ	ACTIVE	CFP	HKQ	8	1	TBD	AU	N / A for Pkg Type	-55 to 210	INA333S HKQ	<a href="#">Samples</a>
INA333SJD	ACTIVE	CDIP SB	JD	8	1	TBD	POST-PLATE	N / A for Pkg Type	-55 to 210	INA333SJD	<a href="#">Samples</a>
INA333SKGD1	ACTIVE	XCEPT	KGD	0	240	Green (RoHS & no Sb/Br)	Call TI	N / A for Pkg Type	-55 to 210		<a href="#">Samples</a>
INA333SKGD2	ACTIVE	XCEPT	KGD	0	10	TBD	Call TI	N / A for Pkg Type	-55 to 210		<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF INA333-HT :**

- Catalog: [INA333](#)

NOTE: Qualified Version Definitions:

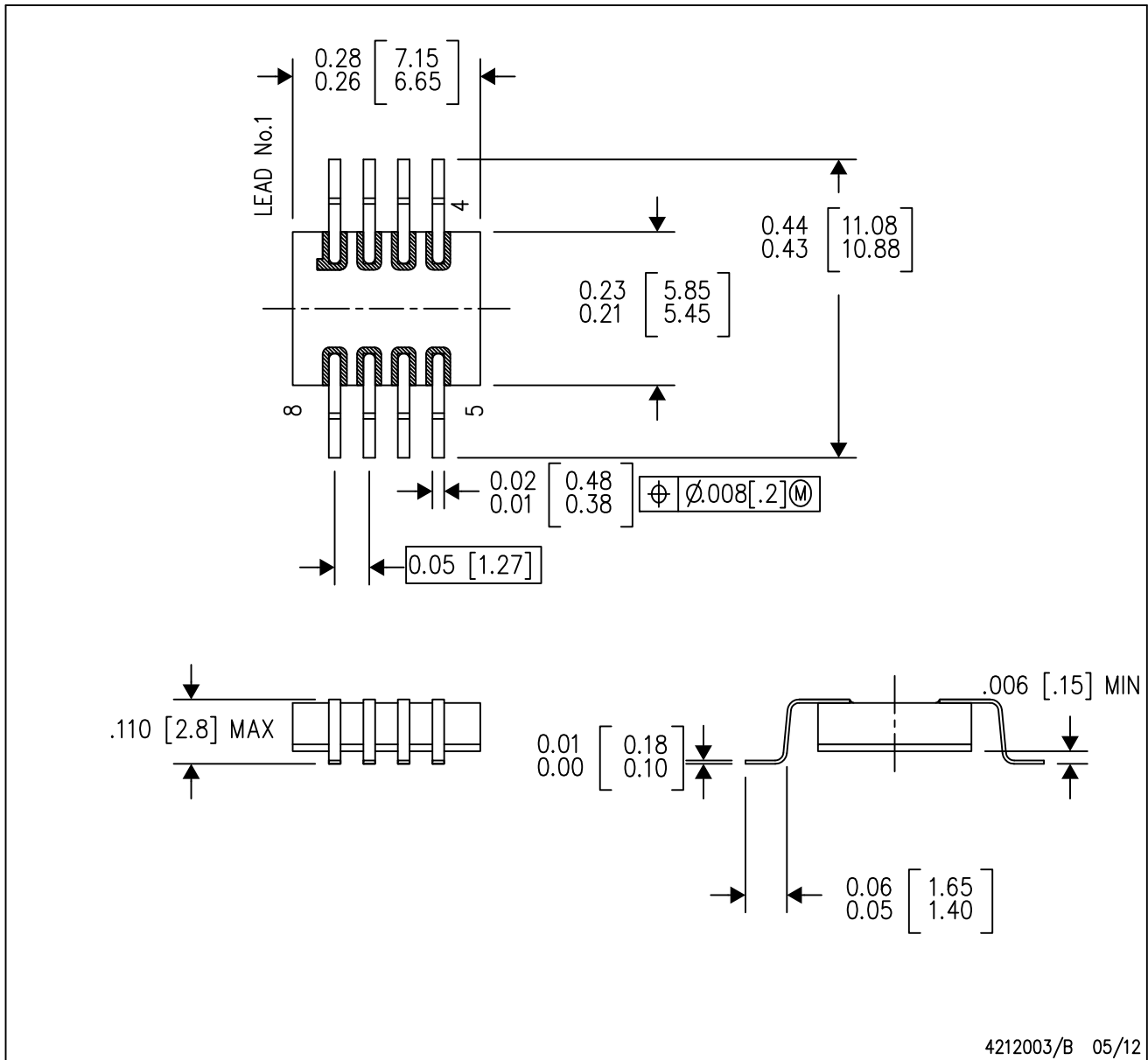
- Catalog - TI's standard catalog product



# MECHANICAL DATA

HKQ (R-CDFP-G8)

CERAMIC GULL WING

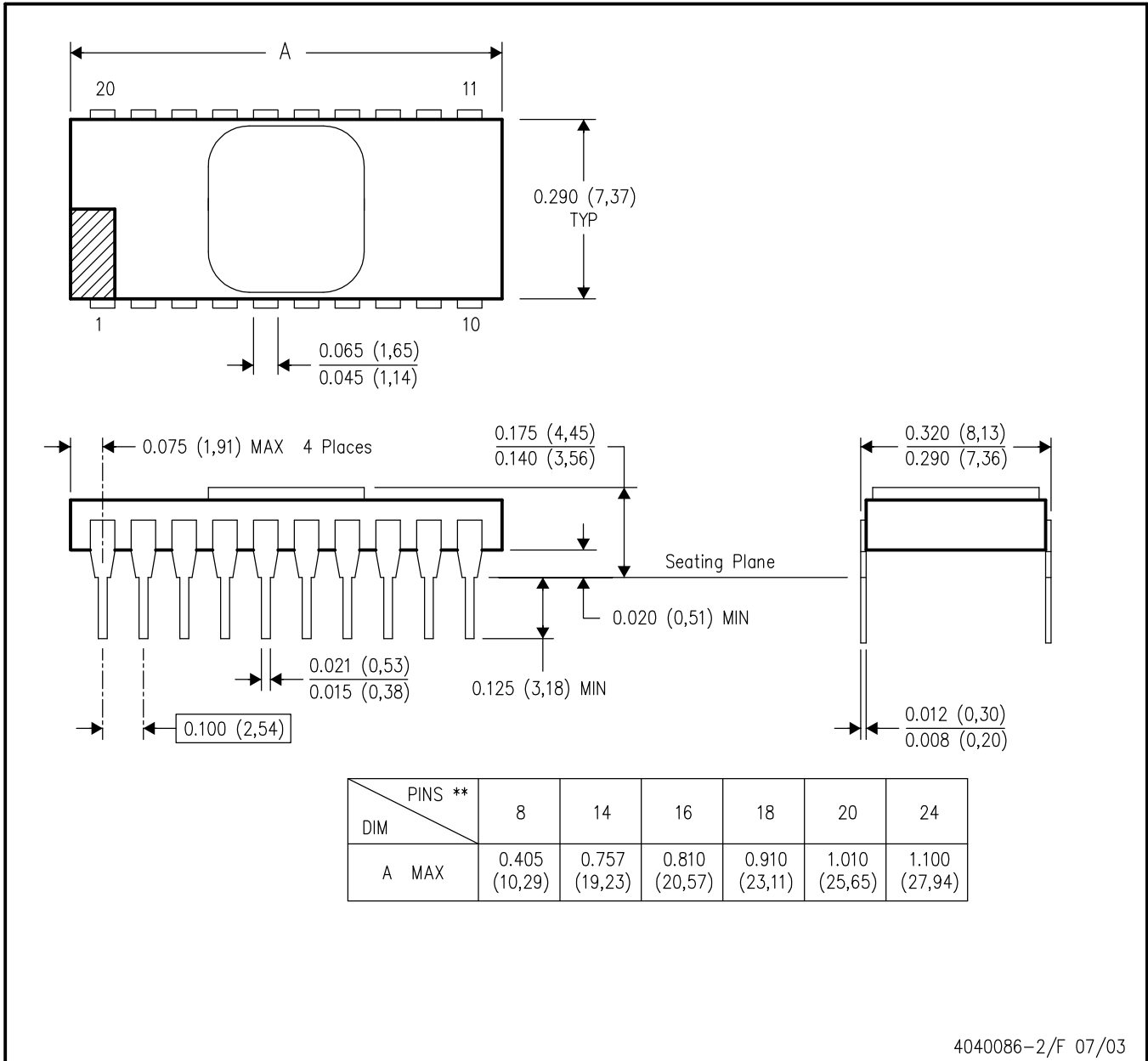


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals will be gold plated.
  - E. Lid is not connected to any lead.

JD (R-CDIP-T\*\*)

CERAMIC SIDE-BRAZE DUAL-IN-LINE PACKAGE

20 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within MIL STD 1835 CDIP2 - T8, T14, T16, T18, T20 and T24 respectively.

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2019, Texas Instruments Incorporated

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View INA333SHKJ on WIN SOURCE](#)

 [Texas Instruments](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management