THE DATASHEET OF

IP2005CPBF

iPOWIR™ TECHNOLOGY

Synchronous Buck
Optimized LGA Power Block

Features

- 40A Multiphase building block
- No derating up to T_{PCB} = 95ºC
- Optimized for low power loss
- Bias supply range of 4.5V to 7.0V
- Operation up to 1.5MHz
- Bi-directional current flow
- Under Voltage Lockout
- LGA interface
- 7.65mm x 7.65mm outline

Applications

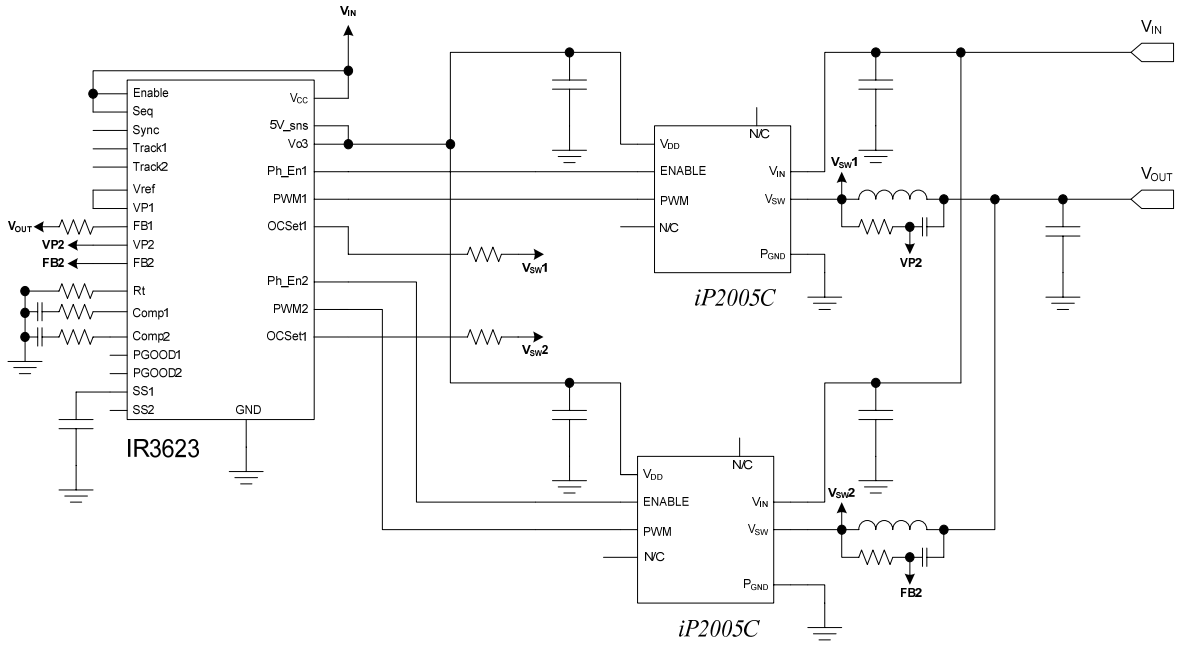
- Multi-phase Architectures
- Low Duty-Ratio, High Current
- Microprocessor Power Supplies
- High Frequency Low Profile DC-DC Converters

Description

The iP2005C is a fully optimized solution for high current synchronous buck multiphase applications. Board space and design time are greatly reduced because most of the components required for each phase of a typical discrete-based multiphase circuit are integrated into a single 7.65mm x 7.65mm x 1.66mm power block. The only additional components required for a complete multiphase converter are a PWM controller, the output inductors, and the input and output capacitors.

Package Description	Interface Connection	Standard Quantity
iP2005CPbF	LGA	10
iP2005CTRPbF	LGA	2000

Typical Application



Absolute Maximum Ratings

V_{IN} to PGND ……..……...-0.5V to 16.5V
V_{DD} to PGND ……..……...-0.5V to 7.5V
PWM to PGND ……-0.5V to V_{DD} + 0.5V (Note 1)
ENABLE to PGND …….. -0.5V to V_{DD} + 0.5V (Note 1)
Storage Temperature …… -60ºC to 150ºC
Block Temperature….. …… -40ºC to 135ºC (Note 2)
ESD Rating…….... JEDEC, JESD22-A114 (HBM[4KV], Class 3A)
……... JEDEC, JESD22-A115 (MM[400V], Class C)
MSL Rating…… 3
Reflow Temperature …..……..260ºC Peak

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied.

Recommended Operation Conditions

PARAMETER	Min	Typ	Max	Units	Conditions
Supply Voltage (V_{DD})	4.5	-	7.0	V	
Input Voltage (V_{IN})	2.5	-	13.2	V	
Output Voltage (V_{OUT})	-	-	5.5	V	
Output Current (I_{OUT})	-	-	40	A	
Switching Frequency (F_{SW})	250	-	1500	kHz	
On Time Duty Cycle	-	-	85	%	
Minimum On Time	50	-	-	ns	
Block Temperature	-40	-	125	ºC	

Electrical Specifications

These specifications apply for T_{BLK} = 0ºC to 125ºC and V_{DD} = 5.0V, unless otherwise specified.

PARAMETER	Min	Typ	Max	Units	Conditions
P_{Loss}					
Power Block Losses	-	7.8	9.4	W	V_{IN} = 12V, V_{DD} = 5.0V, V_{OUT} = 1.3V, I_{OUT} = 40A, F_{SW} = 1MHz, L_{OUT} = 0.3uH, T_{BLK} = 25ºC
V_{IN}					
Leakage Current	-	-	0.5	mA	VIN = 12V, ENABLE = 0V
V_{SW}					
Leakage Current	-30	-	-	µA	Iout=0, current pulled from VSW until VSW=0
VDD					

PARAMETER	Min	Typ	Max	Units	Conditions
Supply Current (Stand By)	-	3	4	mA	V_{DD} = 5.0V, ENABLE = 0V
Supply Current (Operating)	-	60	75	mA	V_{IN} = 12V, ENABLE = V_{DD} = 5.0V, F_{SW} = 1MHz, V_o = 1.3V
Power-On Reset (POR)					
V_{DD} Rising	3.8	4.15	4.5	V	
V_{DD} Falling	3.6	3.95	4.3	V	
Hysteresis	-	200	-	mV	V_{DD} Rising & Falling
ENABLE INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	V_{DD} = POR to 7.0V
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	40	-	ns	
Falling Propagation Delay (T_{PDL})	-	75	-	ns	
PWM INPUT					
Logic Level Low Threshold (V_{IL})	-	-	0.8	V	V_{DD} = POR to 7.0V
Logic Level High Threshold (V_{IH})	2.0	-	-	V	
Threshold Hysteresis	-	100	-	mV	
Weak Pull-down Impedance	-	100	-	kΩ	
Rising Propagation Delay (T_{PDH})	-	60	-	ns	
Falling Propagation Delay (T_{PDL})	-	30	-	ns	

Notes:

1. Must not exceed 7.5V.
2. Block temperature (T_{BLK}) is defined as the highest Junction temperature within the package

Power Loss Curve

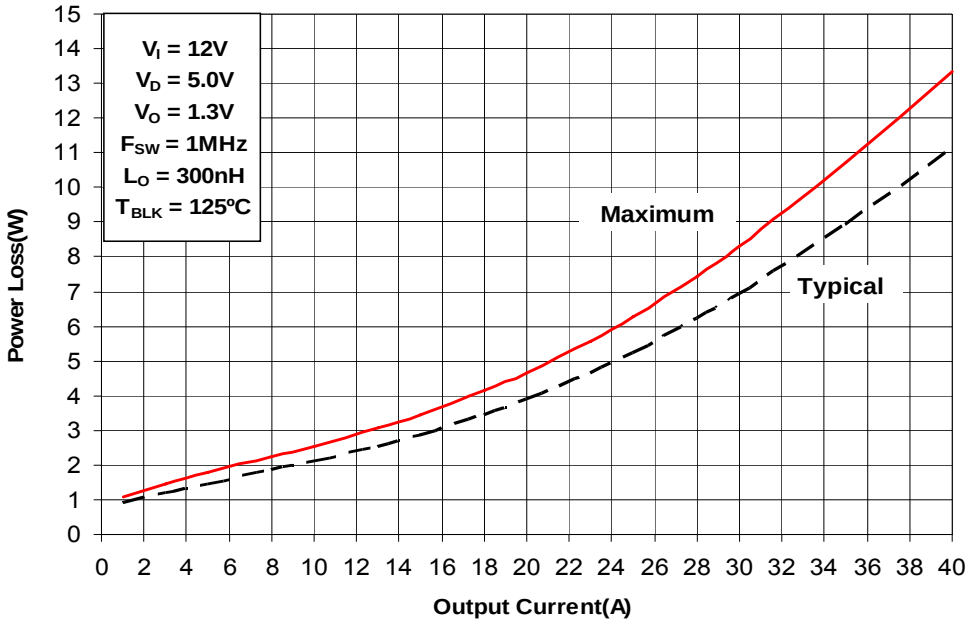


Figure 1 Power Loss Curve

SOA Curve

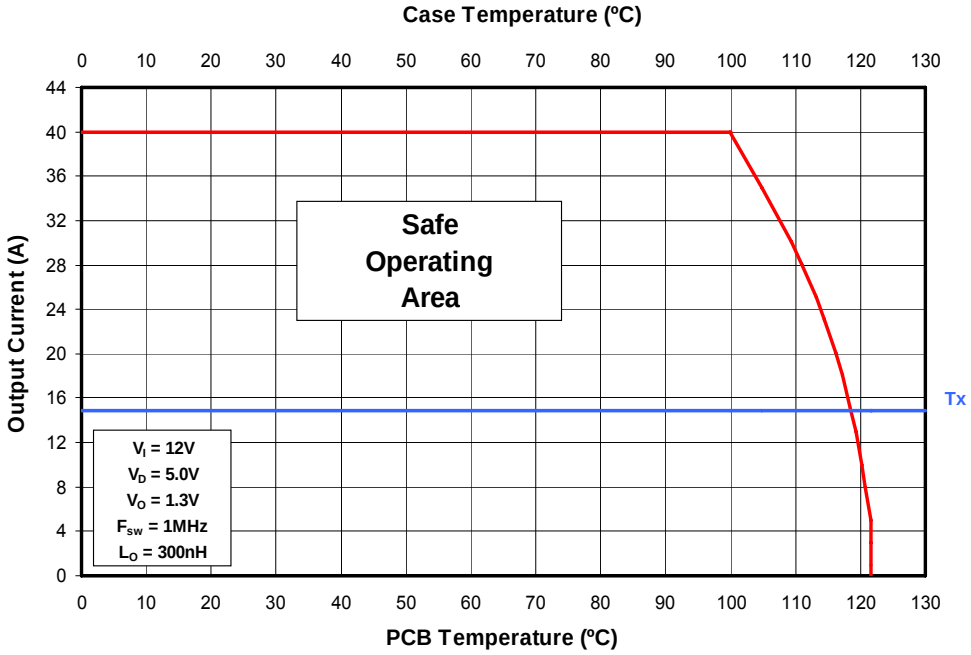


Figure 2 Safe Operating Area Curve

Typical Performance Curves

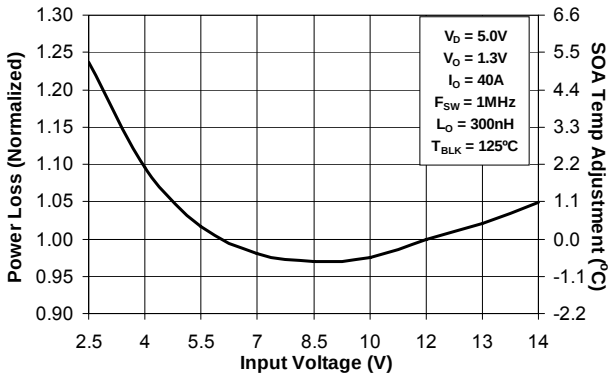


Figure 3 Normalized Power Loss vs. Input Voltage

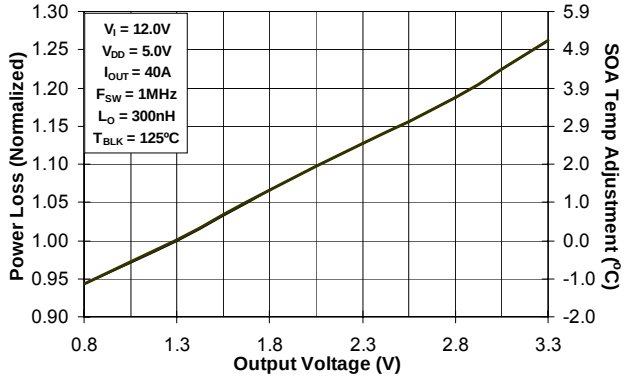


Figure 4 Normalized Power Loss vs. Output Voltage

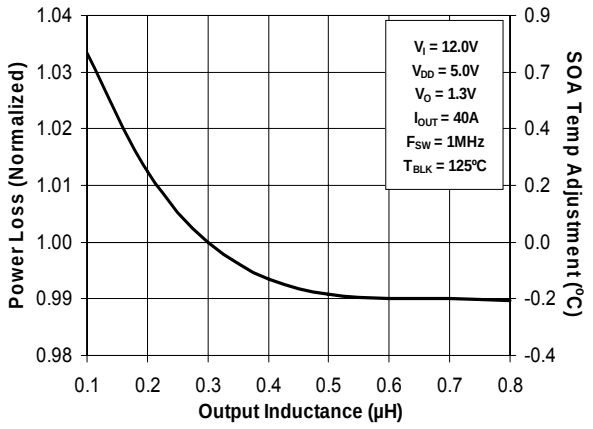


Figure 5 Normalized Power Loss vs. Inductance

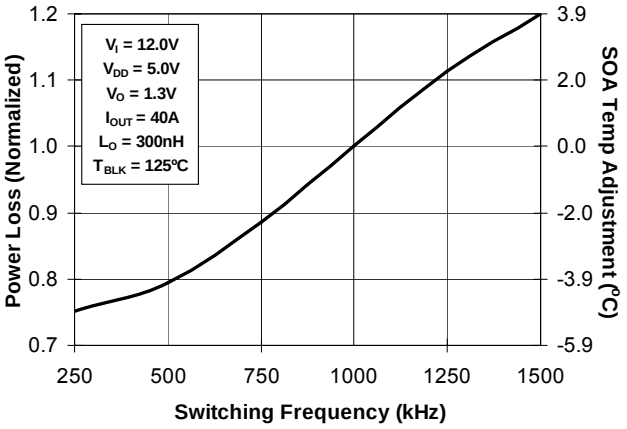


Figure 6 Normalized Power Loss vs. Switching Frequency

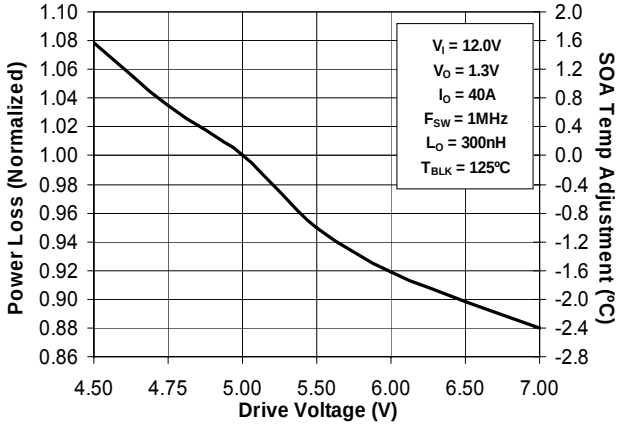


Figure 7 Normalized Power Loss vs. Drive Voltage

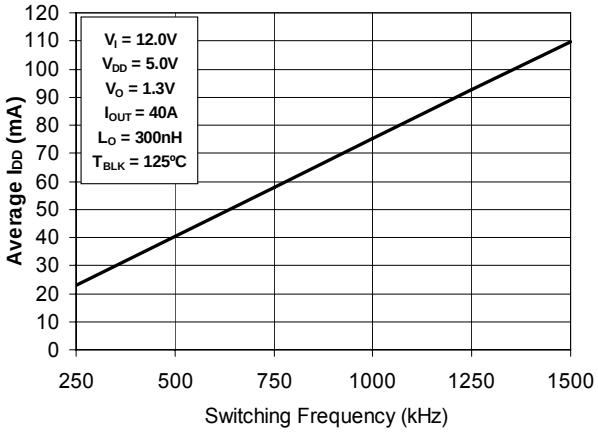


Figure 8 Max. Drive Current vs. Switching Frequency

$P_{IN} = V_{IN}$ Average **x** I_{IN} Average

$P_{DD} = V_{DD}$ Average **x** I_{DD} Average

$P_{OUT} = V_{OUT}$ Average **x** I_{OUT} Average

$P_{LOSS} = (P_{IN} + P_{DD}) - P_{OUT}$

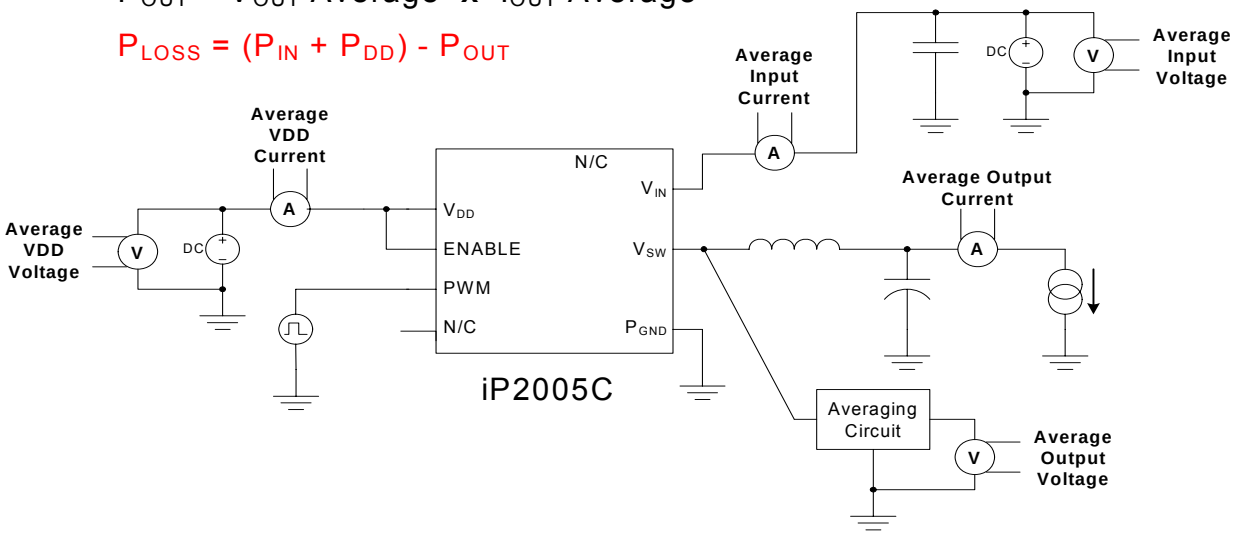


Figure 9 Power Loss Test Circuit

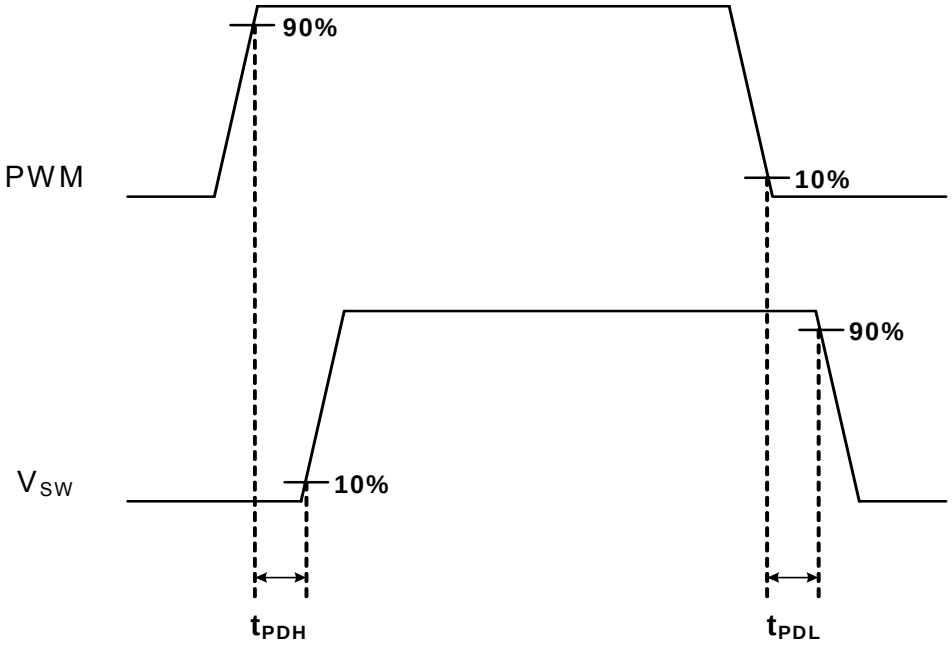


Figure 10 Timing Diagram

Applying the Safe Operating Area (SOA) Curve

The SOA graph incorporates power loss and thermal resistance information in a way that allows one to solve for maximum current capability in a simplified graphical manner. It incorporates the ability to solve thermal problems where heat is drawn out through the printed circuit board and the top of the case. Please refer to International Rectifier Application Note AN1047 for further details on using this SOA curve in your thermal environment.

Procedure

1. Calculate (based on estimated Power Loss) or measure the Case temperature on the device and the board temperature near the device (1mm from the edge).

2. Draw a line from Case Temperature axis to the PCB Temperature axis.

3. Draw a vertical line from the T_X axis intercept to the SOA curve.

4. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.

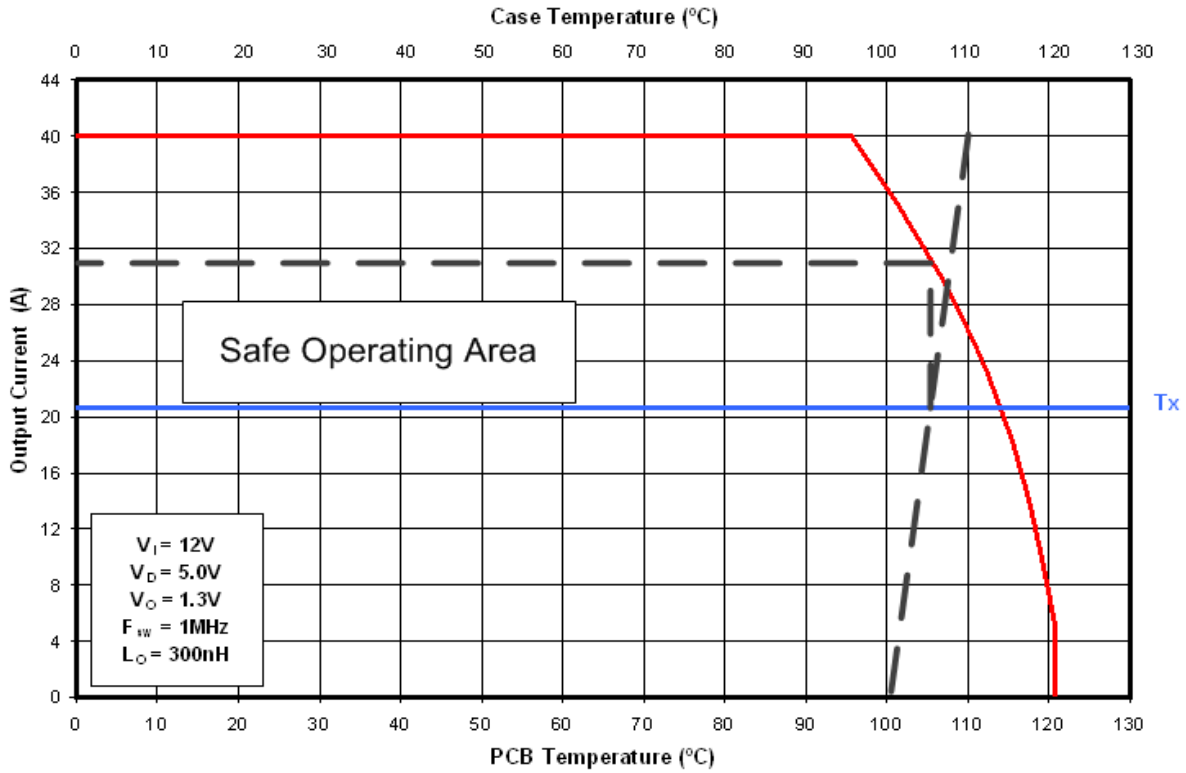


Figure 11 SOA Example, Continuous current ≈ 31A for TPCB = 100ºC & TCASE = 110ºC

Calculating Power Loss and SOA for Different Operating Conditions

To calculate Power Loss for a given set of operation conditions, the following procedure should be followed:

Power Loss Procedure

1. Determine the maximum current and obtain the maximum power loss from figure 1
2. Use the normalized curves to obtain power loss values that match the operating conditions in the application
3. The maximum power loss under the application conditions is then the product of the power loss from figure 1and the normalized values.

To calculate the Safe Operating Area (SOA) for a given set of operating conditions, the following procedure should be followed:

SOA Procedure

1. Determine the maximum PCB and CASE temperature at the maximum operating current for each iP2005C
2. Use the normalized curves to obtain SOA temperature adjustments that match the operating conditions in the application
3. Then, add the sum of the SOA temperature adjustments to the T_X axis intercept in figure 2

Design Example

Operating Conditions:

Output Current = 30A Input Voltage = 10V Output Voltage = 1.3V

Switching Freq = 750 kHz Inductor = 0.2µH Drive Voltage (VDD) = 5V

Calculating Maximum Power Loss:

(Figure 1) Maximum power loss = 7.0W

(Figure 3) Normalized power loss for input voltage ≈ 0.975

(Figure 5) Normalized power loss for output inductor ≈ 1.012

(Figure 6) Normalized power loss for switch frequency ≈ 0.88

Calculated Maximum Power Loss ≈ 7.0W x 0.975 x 1.0 x 1.012 x 0.88 ≈ 6.09W

Calculating SOA Temperature:

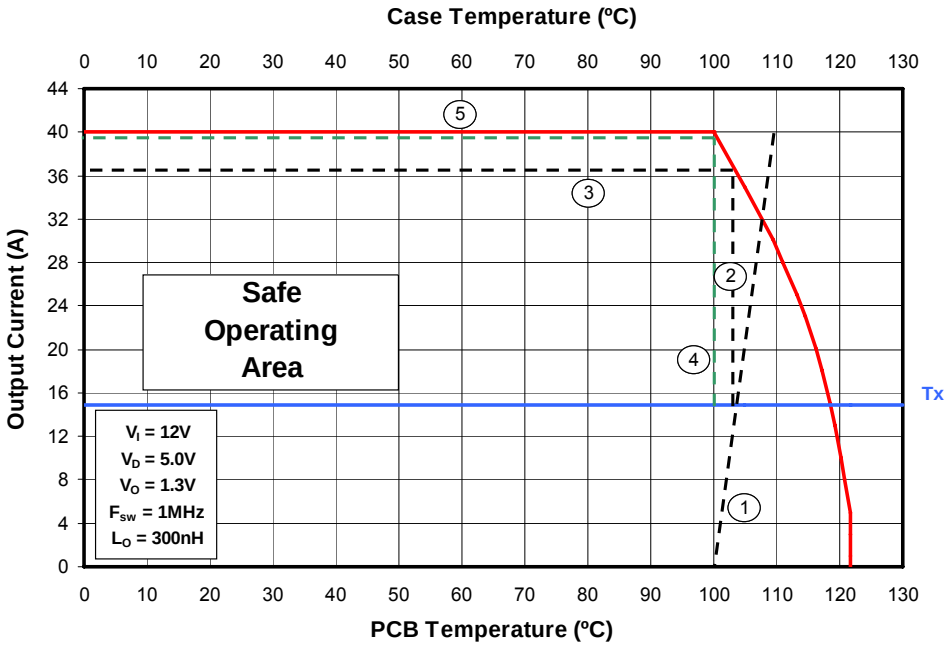
(Figure 3) SOA temperature adjustment for input voltage ≈ -0.6ºC

(Figure 5) SOA temperature adjustment for output inductor ≈ 0.25 ºC

(Figure 6) SOA temperature adjustment for switch frequency ≈ -2.5 ºC

T_X axis intercept adjustment ≈ -0.6 ºC + 0.25 ºC – 2.5 ºC ≈ -2.9 ºC

Assuming T_{PCB} = 100ºC & T_{CASE} = 110ºC, the following example shows how the SOA current is adjusted for T_X decrease of 2.8 ºC



1. Draw a line from Case Temperature axis to the PCB Temperature axis.
2. Draw a vertical line from the T_X axis intercept to the SOA curve.
3. Draw a horizontal line from the intersection of the vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the SOA continuous current.
4. Draw a new vertical line from the T_X axis by adding or subtracting the SOA adjustment temperature from the original T_X intercept point.
5. Draw a horizontal line from the intersection of the new vertical line with the SOA curve to the Y-axis (Output Current). The point at which the horizontal line meets the Y-axis is the new SOA continuous current.

The SOA adjustment indicates the part is still allowed to run at a continuous current of 39A.

Internal Block Diagram

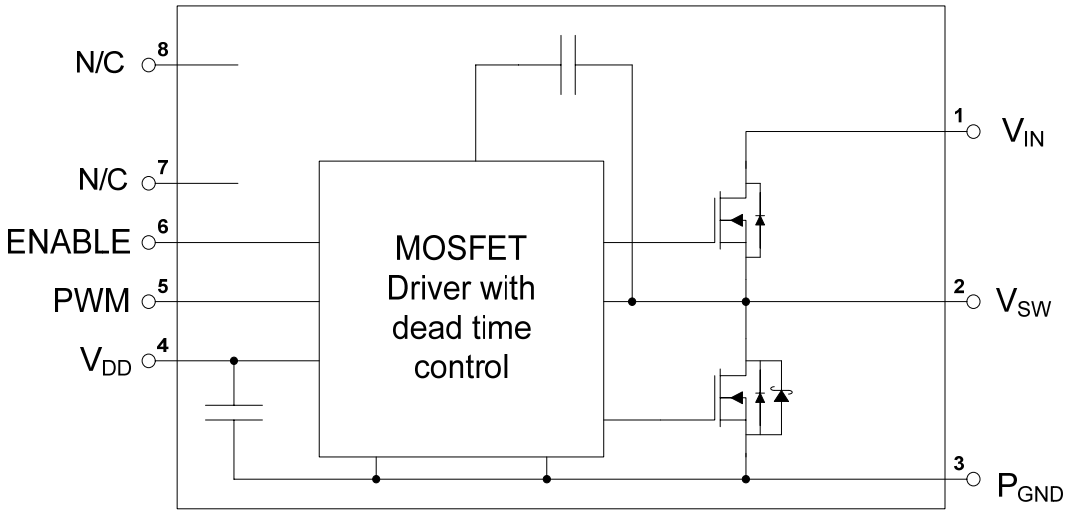


Figure 12 Internal Block Diagram

Pin Description

Pin Number	Pin Name	Description
1	V_{IN}	Input voltage pin. Connect input capacitors close to this pin.
2	V_{SW}	Voltage Switching Node – pin connection to the output inductor.
3	PGND	Power Ground
4	V_{DD}	Supply voltage to internal circuitry.
5	PWM	TTL level input to MOSFET drivers. When PWM is HIGH, the Control FET is on and the Sync FET is off. When PWM is LOW, the Sync FET is on and the Control FET is off.
6	ENABLE	When set to logic level high, internal circuitry of the device is enabled. When set to logic level low, the Control and Synchronous FETs are turned off.
7,8	N/C	No Connection, can be left floating. (Note A)

Notes:

A. It is recommended to connect PIN 7 and 8 to PIN 1 on PCB to reduce thermal resistance.

Recommended PCB Layout

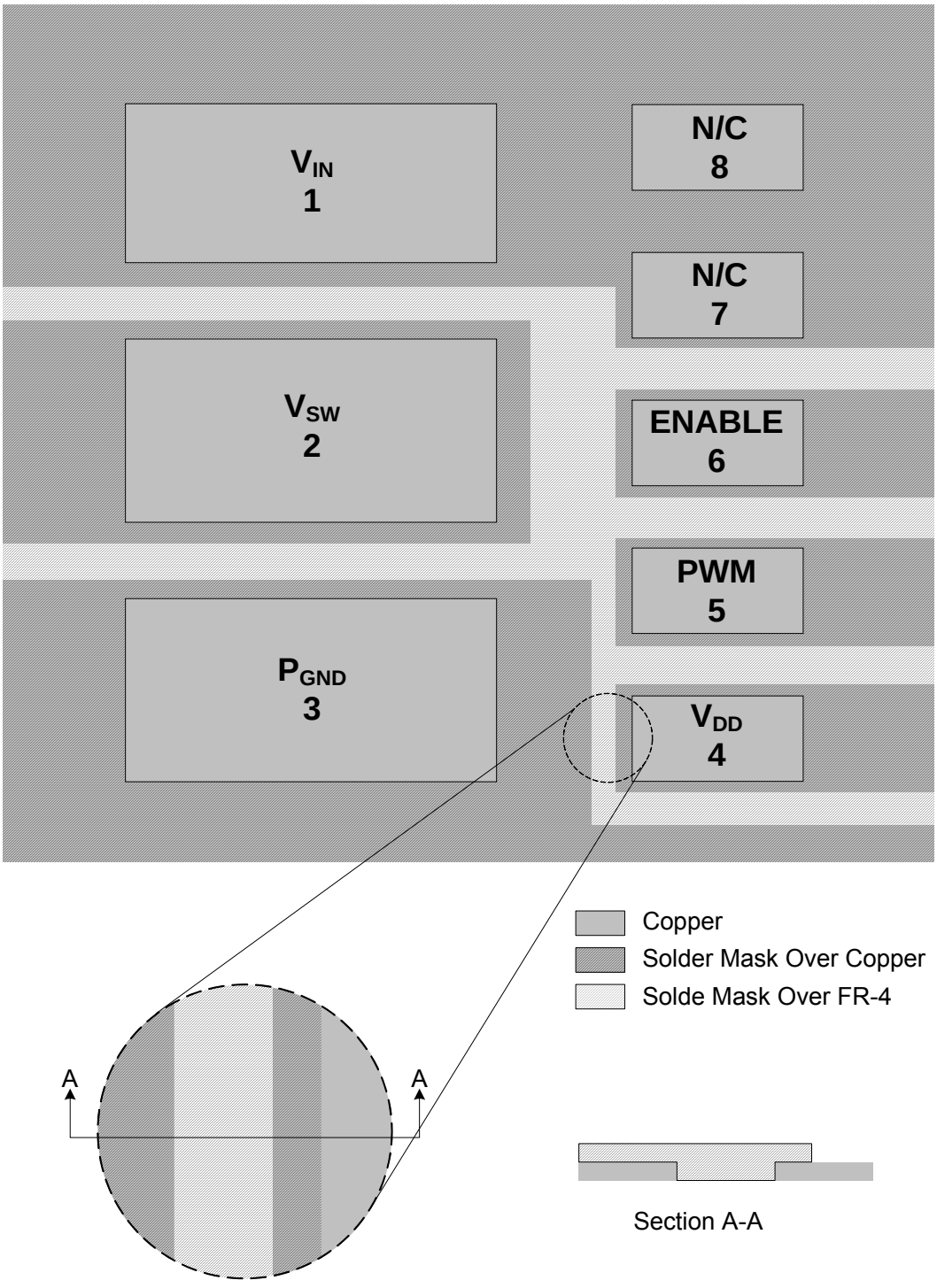


Figure 13 Top copper and Solder-mask layer of PCB layout

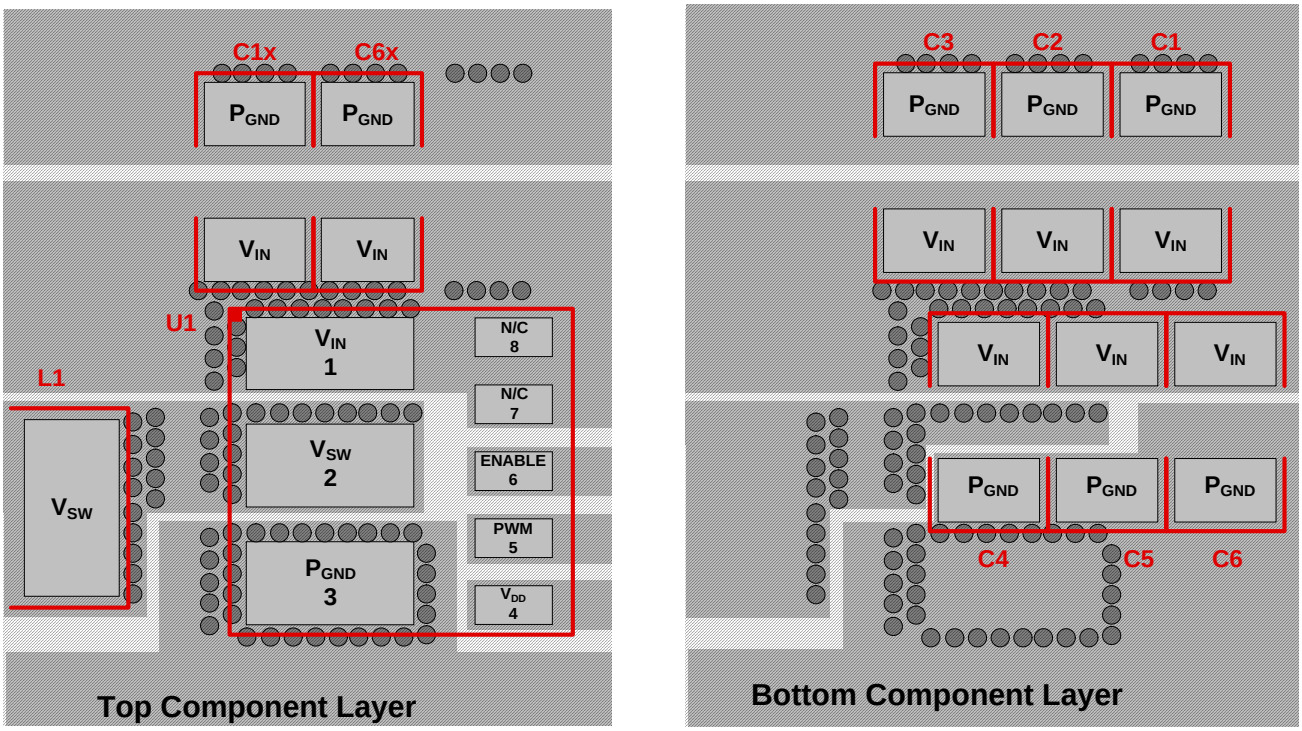


Figure 14 Top & Bottom Component and Via Placement (Topside, Transparent view down)

PCB Layout Guidelines

The following guidelines are recommended to reduce the parasitic values and optimize overall performance.

- All pads on the iP2005C footprint design need to be Solder-mask defined (see Figure 13). Also refer to International Rectifier application notes AN1028 and AN1029 for further footprint design guidance.
- Place as many vias around the Power pads (V_{IN}, V_{SW}, and P_{GND}) for both electrical and optimal thermal performance.
- A minimum of six 10µF, X5R, 16V ceramic capacitors per iP2005C are needed for greater than 30A operation at 1MHz switching frequency. This will result in the lowest loss due to input capacitor ESR.
- Placement of the ceramic input capacitors is critical to optimize switching performance. In cases where there is a heatsink on the case of iP2005C, place all six ceramic capacitors right underneath the iP2005C footprint (see Figure Bottom Component Layer). In cases where there is no heatsink, C1 and C6 on the bottom layer may be moved to the C1x and C6x locations (respectively) on the top component layer (see Figure Top Component Layer). In both cases, C2 – C5 need to be placed right underneath the iP2005C PCB footprint.
- Dedicate at least two layers to PGND.
- Duplicate the Power Nodes on multiple layers (refer to AN1029).

Mechanical Outline Drawing

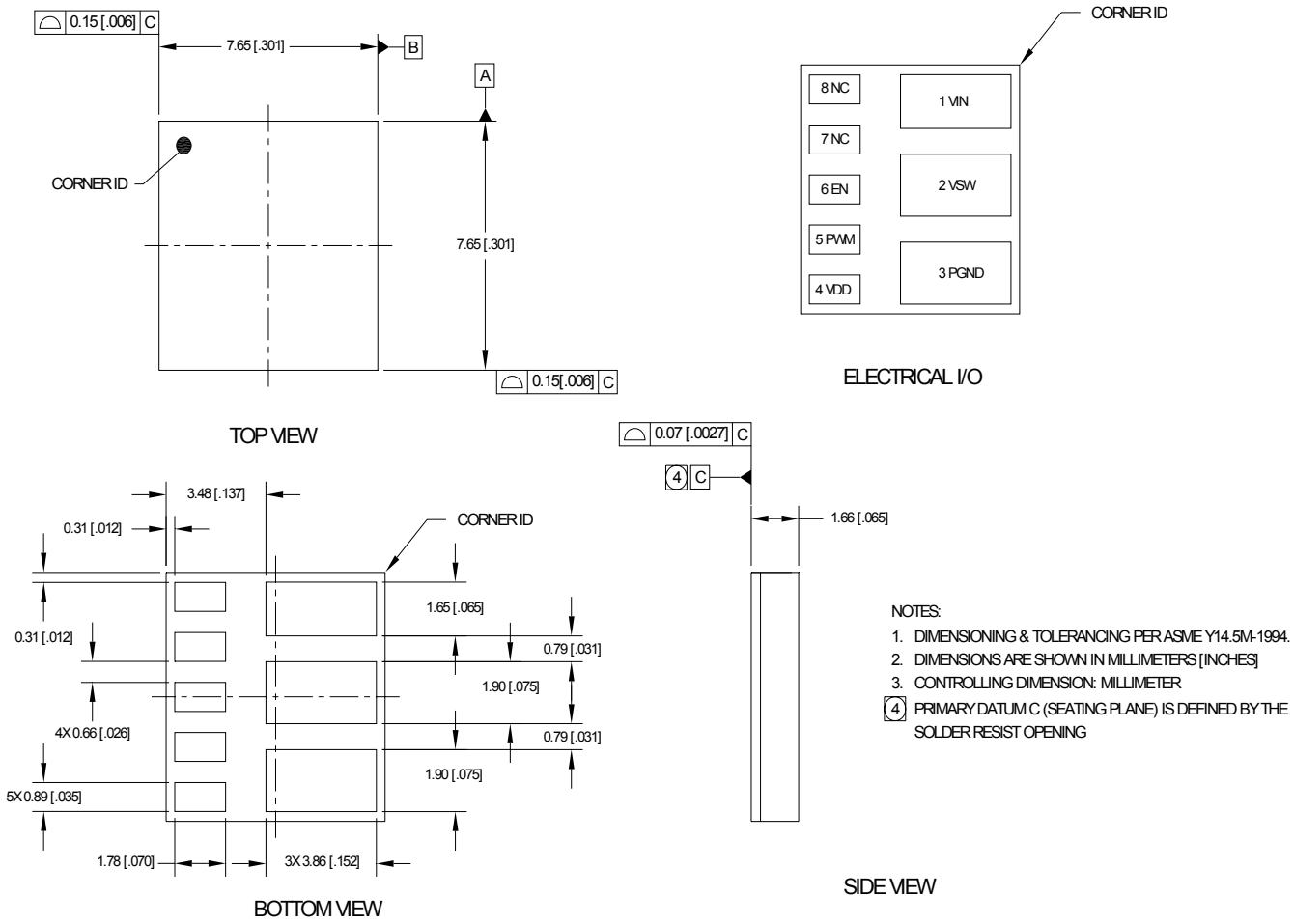
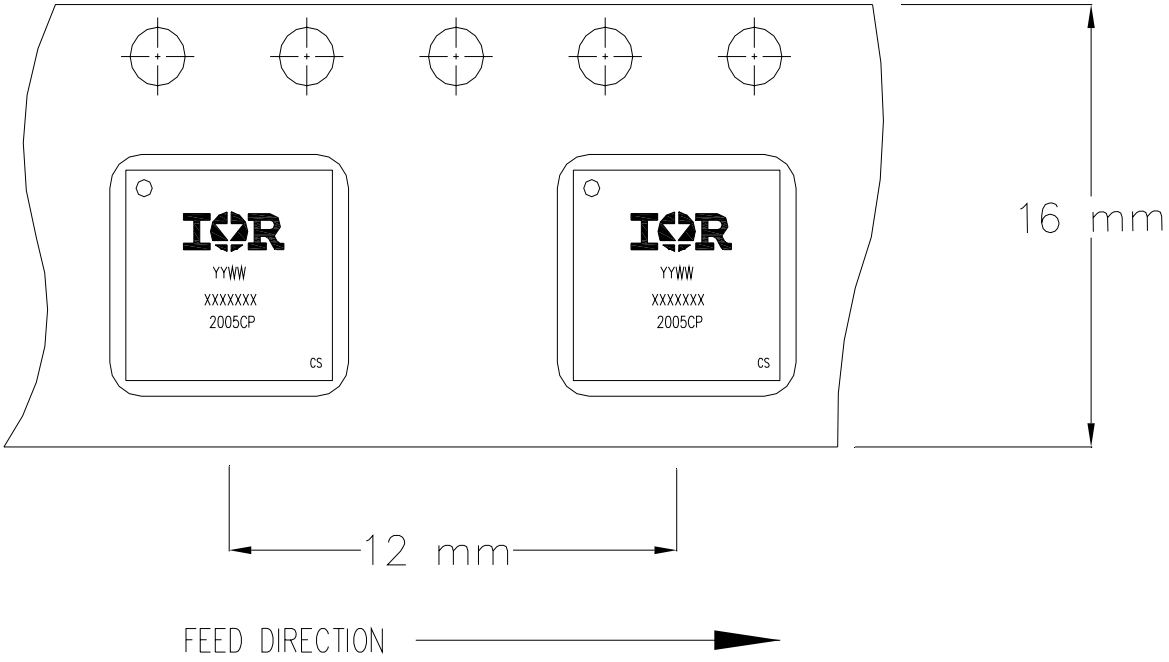
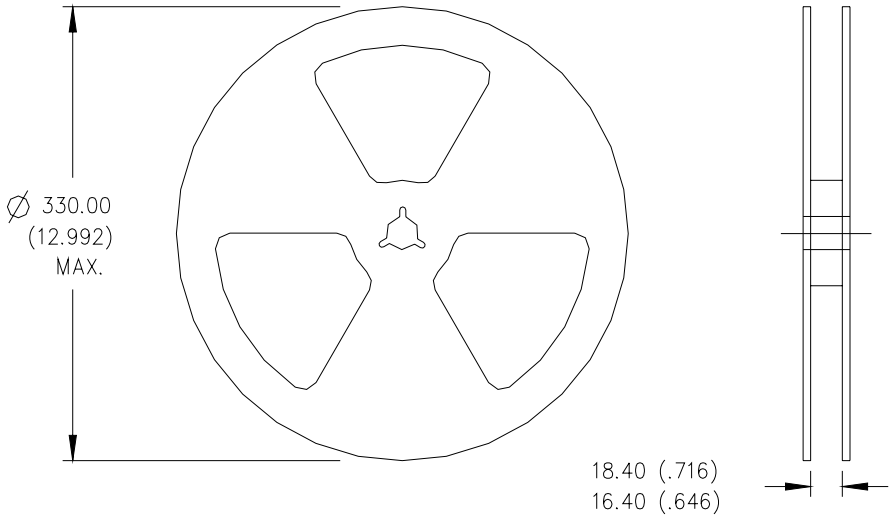


Figure 15 Mechanical Outline Drawing



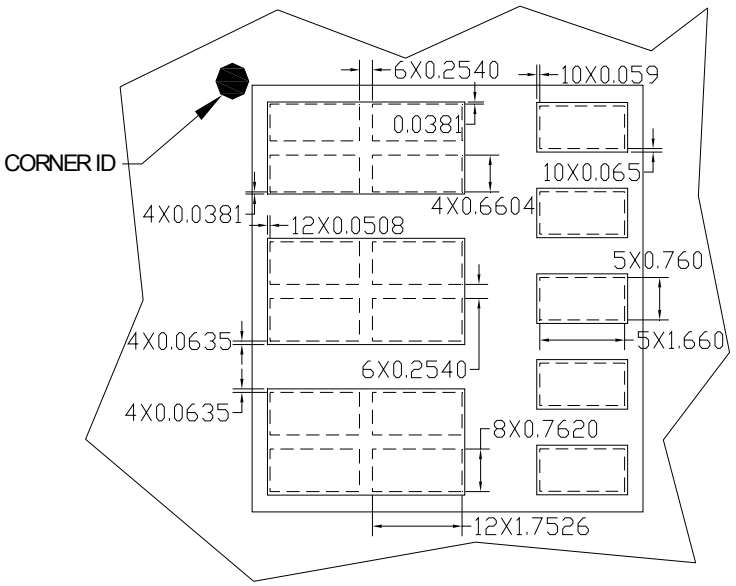


NOTES:

1. CONTROLLING DIMENSION: MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Figure 16 Tape and Reel Information

Recommended Solder Paste Stencil Design



Notes:
1. This view is stencil squeegee view.
2. Dimensions are shown in millimeters.
3. This opening is based on using 150 micron stencil. if using different thickness stencil this opening needs to be adjusted accordingly.
4. Dashed lines show stencil openings. Solid lines show pad openings.

Figure 17 Solder Paste Stencil Design

The recommended reflow peak temperature is 260°C. The total furnace time is approximately 5 minutes with approximately 10 seconds at peak temperature.

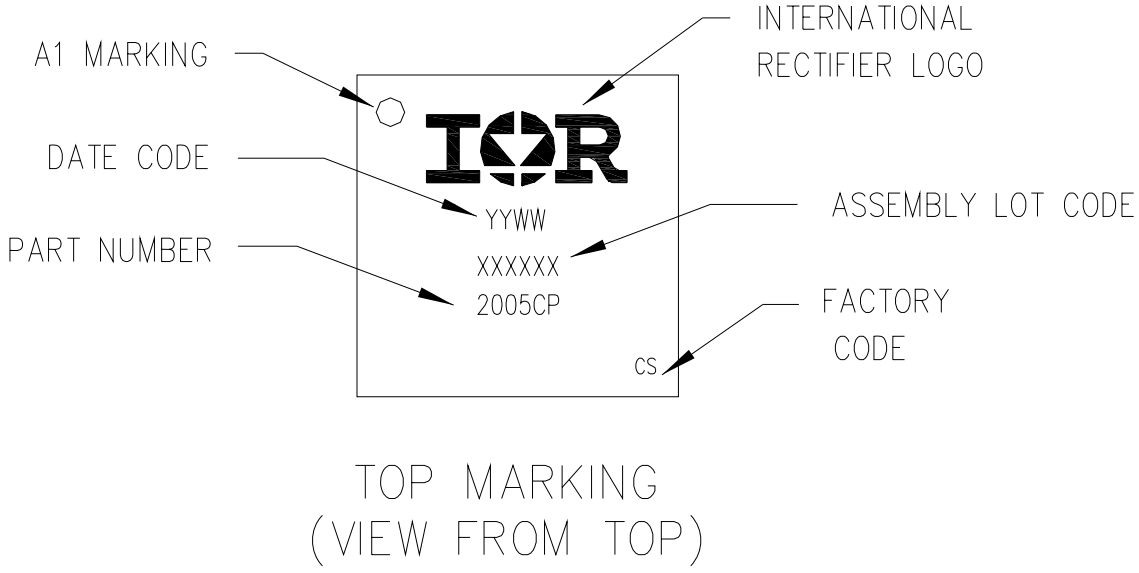


Figure 18 Part Marking

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