

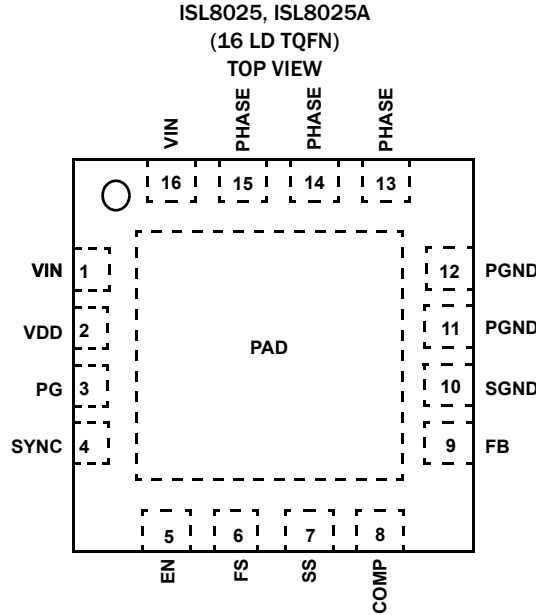




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## Pin Configuration



## Pin Descriptions

PIN NUMBER	SYMBOL	DESCRIPTION
1, 16	VIN	Input supply voltage. Place a minimum of two 22µF ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.
2	VDD	Input supply voltage for the logic. Connect VIN pin.
3	PG	Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms upon output reached within regulation.
4	SYNC	Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of SYNC pin float.
5	EN	Regulator enable pin. Enable the output when driven to high. Shutdown the chip and discharge output capacitor when driven to low.
6	FS	This pin sets the oscillator switching frequency, using a resistor, RFS, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 1MHz if FS is connected to VIN.
7	SS	SS is used to adjust the soft-start time. Set to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.
8, 9	COMP, FB	The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. COMP is the output of the amplifier if COMP is not tied to VDD. Otherwise, COMP is disconnected thru a MOSFET for internal compensation. Must connect COMP to VDD in internal compensation mode to meet a typical application. Additional external networks across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and under-voltage protection circuitry use FB to monitor the regulator output voltage.
10	SGND	Signal ground.
11, 12	PGND	Power ground.
13, 14, 15	PHASE	Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See “FUNCTIONAL BLOCK DIAGRAM” on page 5 for more detail.
Exposed Pad	-	The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to SGND plane for optimal thermal performance.

## Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	OPERATION FREQUENCY (MHz)	TEMP. RANGE (°C)	PACKAGE (Pb-Free)	PKG. DWG. #
ISL8025IRTAJZ	025A	1	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D
ISL8025AIRTAJZ	25AA	2	-40 to +85	16 Ld 3x3 TQFN	L16.3x3D

### NOTES:

1. Add "-T\*" suffix for tape and reel. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL8025](#), [ISL8025A](#). For more information on MSL please see techbrief [TB363](#).

TABLE 1. SUMMARY OF KEY DIFFERENCES

PART NUMBER	I <sub>OUT</sub> (MAX) (A)	F <sub>SW</sub> RANGE (MHz)	V <sub>IN</sub> RANGE (V)	V <sub>OUT</sub> RANGE (V)	PART SIZE (mm)
ISL8025	5	Programmable 0.5MHz to 4MHz	2.7 to 5.5	0.6 to 5.5	3x3
ISL8025A		Programmable 1MHz to 4MHz			

### NOTES:

4. The Evaluation Kit default configuration is V<sub>OUT</sub> = 1.8V, F<sub>SW</sub> = 1MHz.
5. V<sub>REF</sub> is 0.6V.

TABLE 2. ISL8025 COMPONENT SELECTION

V <sub>OUT</sub>	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	3.6V
C1	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF
C2	4 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF
C3	22pF	22pF	22pF	22pF	22pF	22pF	22pF
L1	0.47~1μH	0.47~1μH	0.47~1μH	0.68~1.5μH	0.68~1.5μH	1~2.2μH	1~2.2μH
R2	33kΩ	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ	500kΩ
R3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

TABLE 3. ISL8025A COMPONENT SELECTION

V <sub>OUT</sub>	0.8V	1.2V	1.5V	1.8V	2.5V	3.3V	3.6V
C1	22μF	22μF	22μF	22μF	22μF	22μF	22μF
C2	3 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF	2 x 22μF
C3	22pF	22pF	22pF	22pF	22pF	22pF	22pF
L1	0.22~0.47μH	0.22~0.47μH	0.22~0.47μH	0.33~0.68μH	0.33~0.68μH	0.47~1μH	0.47~1μH
R2	33kΩ	100kΩ	150kΩ	200kΩ	316kΩ	450kΩ	500kΩ
R3	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ	100kΩ

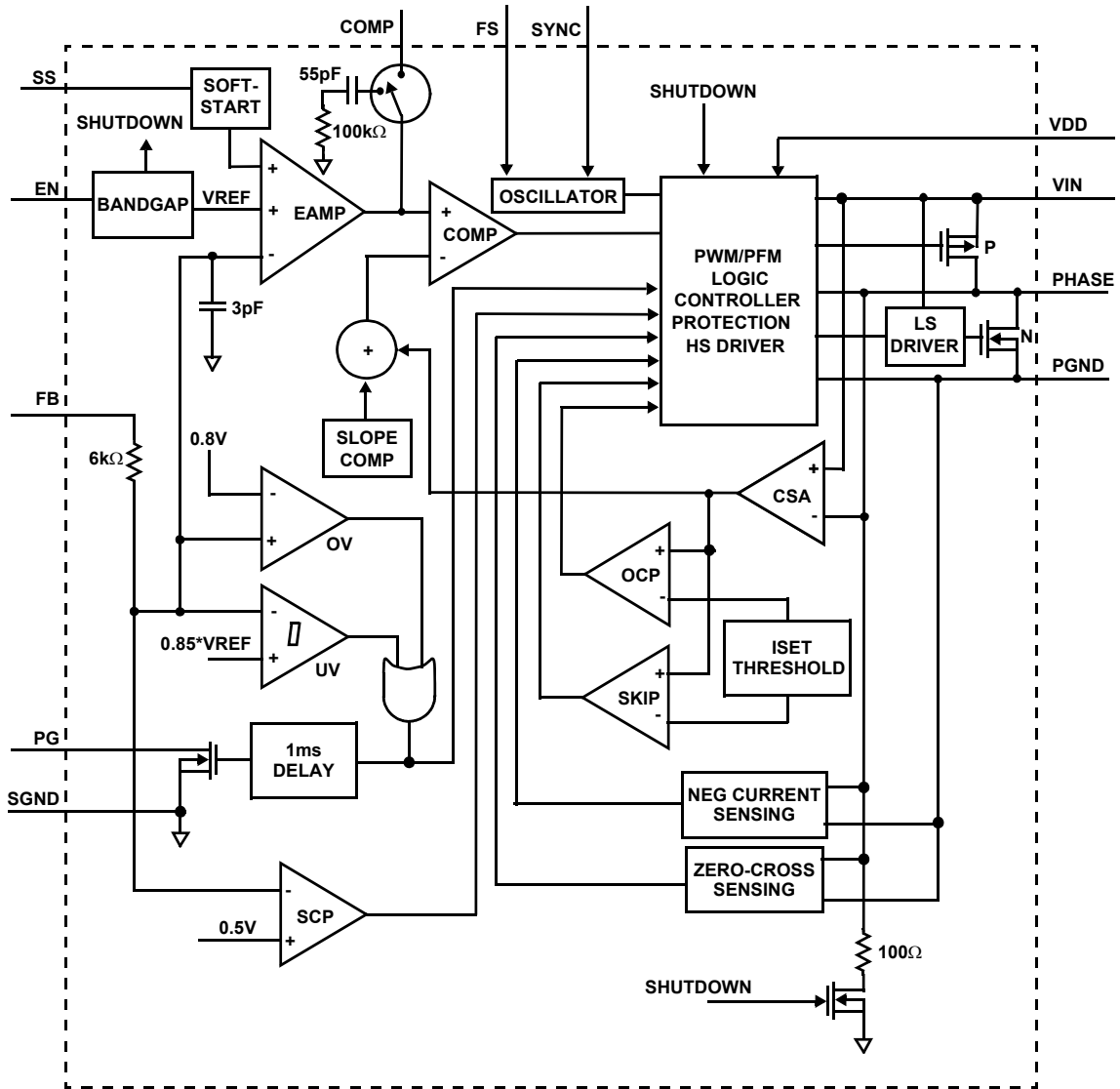


FIGURE 3. FUNCTIONAL BLOCK DIAGRAM

**Absolute Maximum Ratings** (Reference to GND)

VIN	-0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB	-0.3V to VIN + 0.3V
PHASE	-1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS	-0.3V to 2.7V
<b>ESD Ratings</b>	
Human Body Model (Tested per JESD22-A114)	3kV
Charged Device Model (Tested per JESD22-C101E)	2kV
Machine Model (Tested per JESD22-A115)	300V
Latch Up (Tested per JESD-78A; Class 2, Level A)	100mA @ +85°C

**Thermal Information**

Thermal Resistance	$\theta_{JA}$ (°C/W)	$\theta_{JC}$ (°C/W)
16 LD TQFN Package (Notes 6, 7)	47	6.5
Junction Temperature Range	-55°C to +125°C	
Storage Temperature Range	-65°C to +150°C	
Pb-Free Reflow Profile	see link below	
	<a href="http://www.intersil.com/pbfree/Pb-FreeReflow.asp">http://www.intersil.com/pbfree/Pb-FreeReflow.asp</a>	

**Recommended Operating Conditions**

VIN Supply Voltage Range	2.7V to 5.5V
Load Current Range	0A to 5A
Ambient Temperature Range	-40°C to +85°C

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**NOTES:**

- $\theta_{JA}$  is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief [TB379](#).
- $\theta_{JC}$ , “case temperature” location is at the center of the exposed metal pad on the package underside.

**Electrical Specifications** Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{IN} = 3.6\text{V}$ ,  $EN = V_{IN}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ . **Boldface limits apply over the operating temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
<b>INPUT SUPPLY</b>						
VIN Undervoltage Lockout Threshold	V <sub>UVLO</sub>	Rising, no load		2.5	<b>2.7</b>	V
		Falling, no load	<b>2.2</b>	2.4		V
Quiescent Supply Current	I <sub>VIN</sub>	SYNC = GND, no load at the output		50		μA
		SYNC = GND, no load at the output and no switches switching		50	<b>60</b>	μA
		SYNC = V <sub>IN</sub> , F <sub>SW</sub> = 1MHz, no load at the output		8	<b>15</b>	mA
		SYNC = V <sub>IN</sub> , F <sub>SW</sub> = 2MHz, no load at the output		16	<b>23</b>	mA
Shutdown Supply Current	I <sub>SD</sub>	SYNC = GND, V <sub>IN</sub> = 5.5V, EN = low		5	<b>7</b>	μA
<b>OUTPUT REGULATION</b>						
Reference Voltage	V <sub>REF</sub>		<b>0.595</b>	0.600	<b>0.605</b>	V
VFB Bias Current	I <sub>VFB</sub>	VFB = 0.75V		0.1		μA
Line Regulation		V <sub>IN</sub> = V <sub>O</sub> + 0.5V to 5.5V (minimal 2.7V)		0.2		%/V
Soft-Start Ramp Time Cycle		SS = SGND		1		ms
Soft-Start Charging Current	I <sub>SS</sub>	V <sub>SS</sub> = 0.1V	<b>1.45</b>	1.85	<b>2.25</b>	μA
<b>OVERCURRENT PROTECTION</b>						
Current Limit Blanking Time	t <sub>OCON</sub>			17		Clock pulses
Overcurrent and Auto Restart Period	t <sub>OCOFF</sub>			8		SS cycle
Positive Peak Current Limit	I <sub>PLIMIT</sub>	5A application	<b>6</b>	7.5	<b>9</b>	A
Peak Skip Limit	I <sub>SKIP</sub>	5A application (See “Application Information” on page 18 for more detail)	<b>0.8</b>	1	<b>1.2</b>	A
Zero Cross Threshold			<b>-200</b>		<b>200</b>	mA
Negative Current Limit	I <sub>NLIMIT</sub>		<b>-4.5</b>	-3	<b>-1.5</b>	A

**Electrical Specifications** Unless otherwise noted, all parameter limits are established over the recommended operating conditions and the typical specification are measured at the following conditions:  $T_A = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ ,  $V_{IN} = 3.6\text{V}$ ,  $EN = V_{IN}$ , unless otherwise noted. Typical values are at  $T_A = +25^\circ\text{C}$ . **Boldface limits apply over the operating temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .** (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 8)	TYP	MAX (Note 8)	UNITS
<b>COMPENSATION</b>						
Error Amplifier Trans-Conductance		Internal compensation		60		$\mu\text{A}/\text{V}$
		External compensation		120		$\mu\text{A}/\text{V}$
Trans-Resistance	RT	5A application (test at 3.6V)	<b>0.155</b>	0.175	<b>0.195</b>	$\Omega$
<b>PHASE</b>						
P-Channel MOSFET ON-Resistance		$V_{IN} = 5\text{V}$ , $I_O = 200\text{mA}$		36	<b>41</b>	m $\Omega$
		$V_{IN} = 2.7\text{V}$ , $I_O = 200\text{mA}$		52	<b>60</b>	m $\Omega$
N-Channel MOSFET ON-Resistance		$V_{IN} = 5\text{V}$ , $I_O = 200\text{mA}$		13	<b>16</b>	m $\Omega$
		$V_{IN} = 2.7\text{V}$ , $I_O = 200\text{mA}$		17	<b>21</b>	m $\Omega$
PHASE Maximum Duty Cycle				100		%
PHASE Minimum On-Time		SYNC = High			<b>140</b>	ns
<b>OSCILLATOR</b>						
Nominal Switching Frequency	$F_{SW}$	$F_{SW} = V_{IN}$ , ISL8025	<b>800</b>	1000	<b>1200</b>	kHz
		$F_{SW} = V_{IN}$ , ISL8025A	<b>1600</b>	2000	<b>2400</b>	kHz
		$F_{SW}$ with $R_S = 402\text{k}\Omega$		490		kHz
		$F_{SW}$ with $R_S = 42.2\text{k}\Omega$		4200		kHz
SYNC Logic Low-to-High Transition Range			<b>0.70</b>	0.75	<b>0.80</b>	V
SYNC Hysteresis				0.15		V
SYNC Logic Input Leakage Current		$V_{IN} = 3.6\text{V}$		3.6	<b>5</b>	$\mu\text{A}$
<b>PG</b>						
Output Low Voltage					<b>0.3</b>	V
Delay Time (Rising Edge)		Time from $V_{OUT}$ reached regulation	<b>0.5</b>	1	<b>2</b>	ms
PG Pin Leakage Current		$PG = V_{IN}$		0.01	<b>0.1</b>	$\mu\text{A}$
OVP PG Rising Threshold				0.80		V
UVP PG Rising Threshold			<b>0.48</b>	0.51	<b>0.54</b>	V
UVP PG Hysteresis				30		mV
PGOOD Delay Time (Falling Edge)				7.5		$\mu\text{s}$
<b>EN</b>						
Logic Input Low					<b>0.4</b>	V
Logic Input High			<b>0.9</b>			V
EN Logic Input Leakage Current		Pulled up to 5.5V		0.1	<b>1</b>	$\mu\text{A}$
Thermal Shutdown		Temperature Rising		150		$^\circ\text{C}$
Thermal Shutdown Hysteresis		Temperature Falling		25		$^\circ\text{C}$

## NOTE:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

# Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $E_N = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$ . Resistor load is used in the test

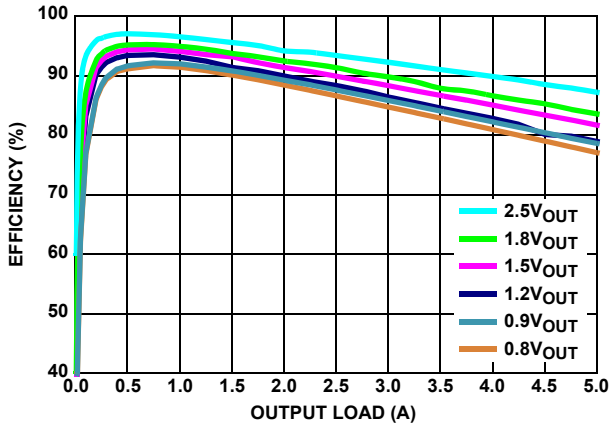


FIGURE 4. EFFICIENCY vs LOAD (1MHz 3.3  $V_{IN}$  PWM)

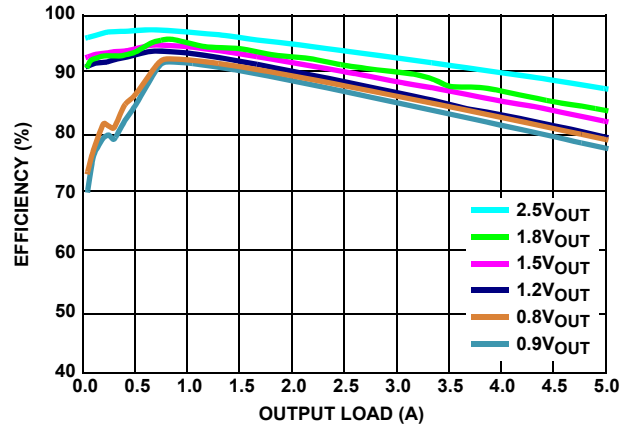


FIGURE 5. EFFICIENCY vs LOAD (1MHz 3.3  $V_{IN}$  PFM)

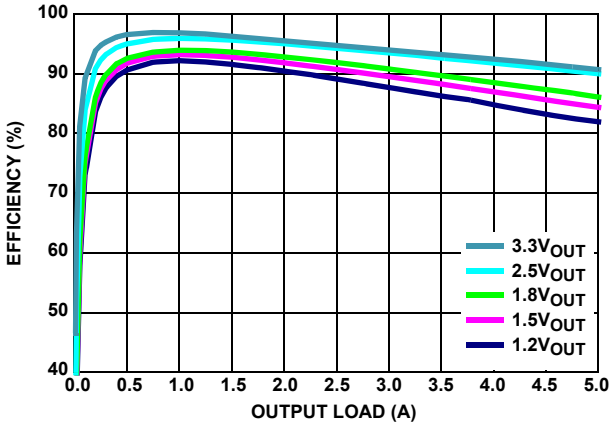


FIGURE 6. EFFICIENCY vs LOAD (1MHz 5 $V_{IN}$  PWM)

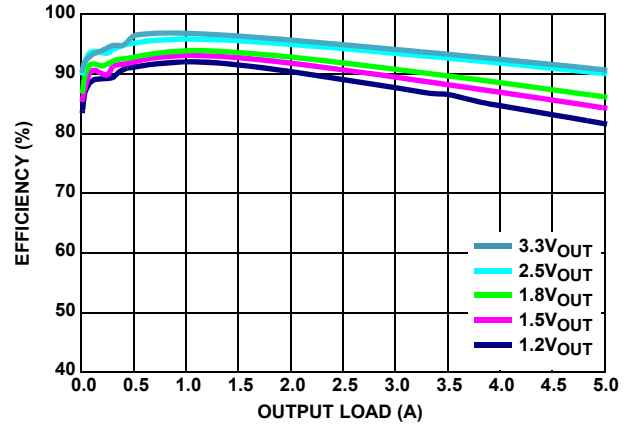


FIGURE 7. EFFICIENCY vs LOAD (1MHz 5 $V_{IN}$  PFM)

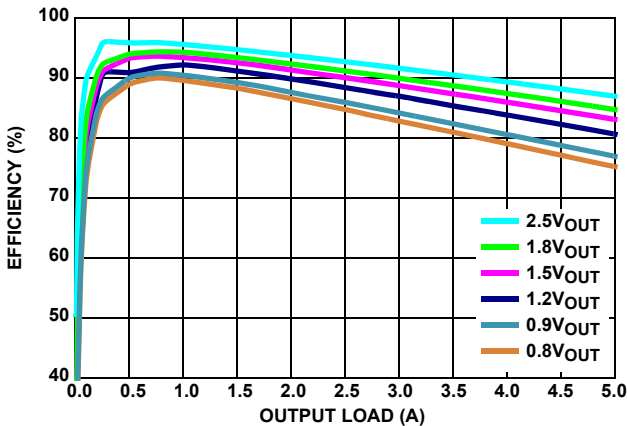


FIGURE 8. EFFICIENCY vs LOAD (2MHz 3.3 $V_{IN}$  PWM)

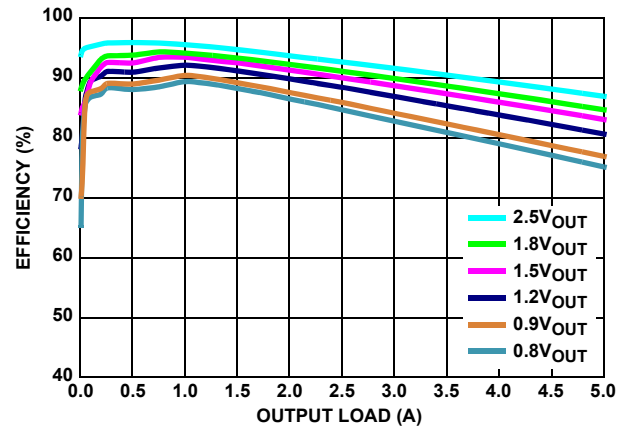


FIGURE 9. EFFICIENCY vs LOAD (2MHz 3.3 $V_{IN}$  PFM)

# Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A}$  to  $5\text{A}$ . Resistor load is used in the test (Continued)

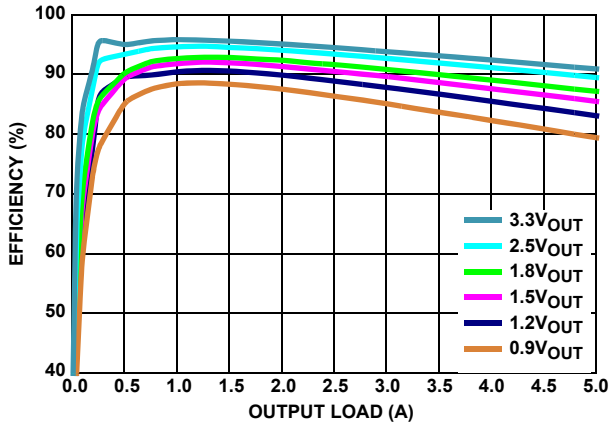


FIGURE 10. EFFICIENCY vs LOAD (2MHz 5VIN PWM)

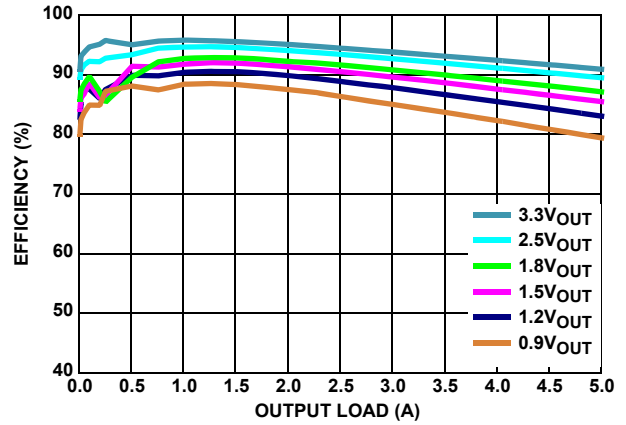


FIGURE 11. EFFICIENCY vs LOAD (2MHz 5VIN PFM)

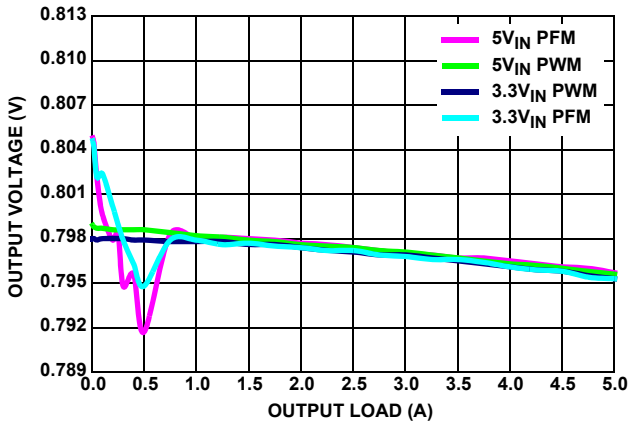


FIGURE 12.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 0.8\text{V}$ )

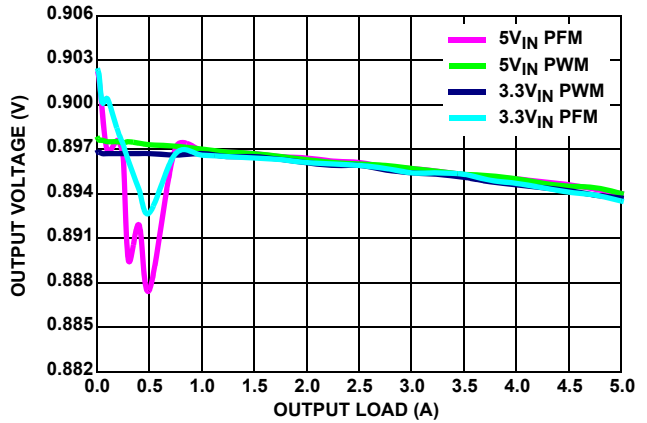


FIGURE 13.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 0.9\text{V}$ )

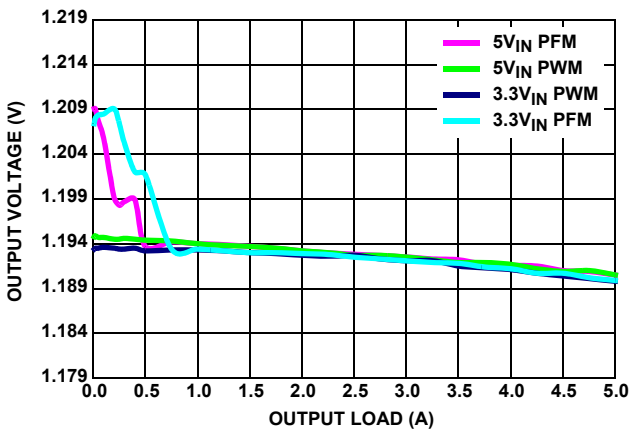


FIGURE 14.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 1.2\text{V}$ )

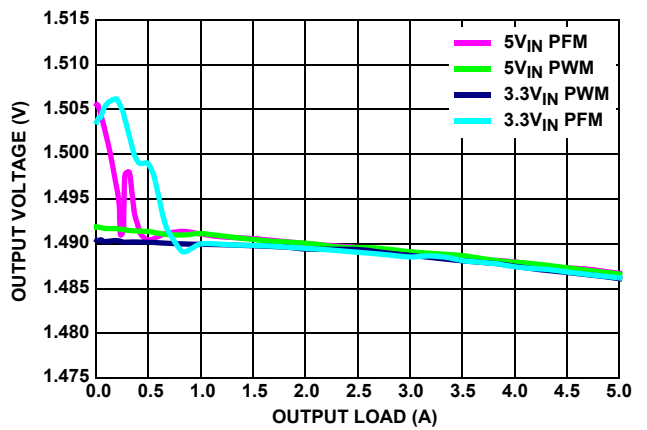


FIGURE 15.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 1.5\text{V}$ )

## Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A}$  to  $5\text{A}$ . Resistor load is used in the test (Continued)

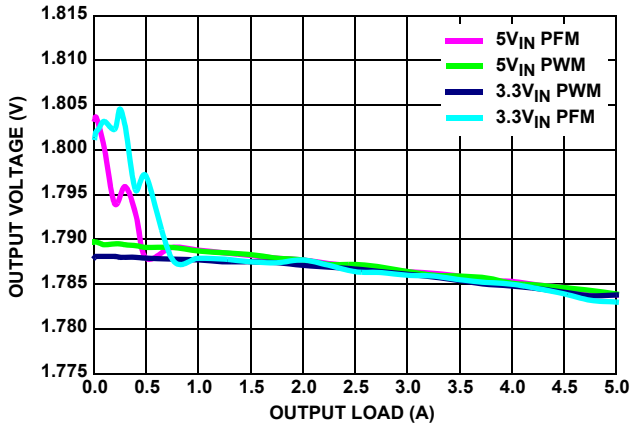


FIGURE 16.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 1.8\text{V}$ )

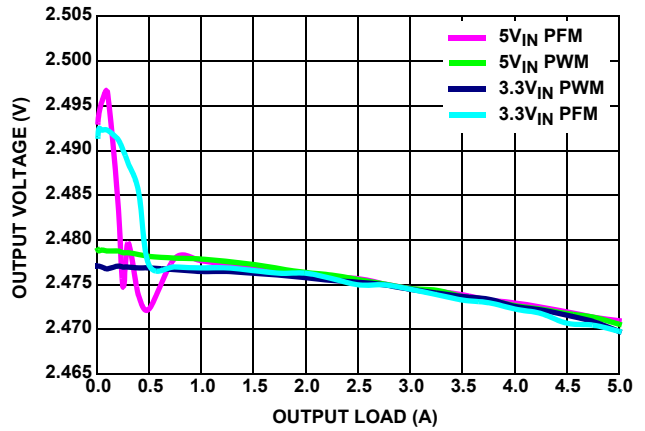


FIGURE 17.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 2.5\text{V}$ )

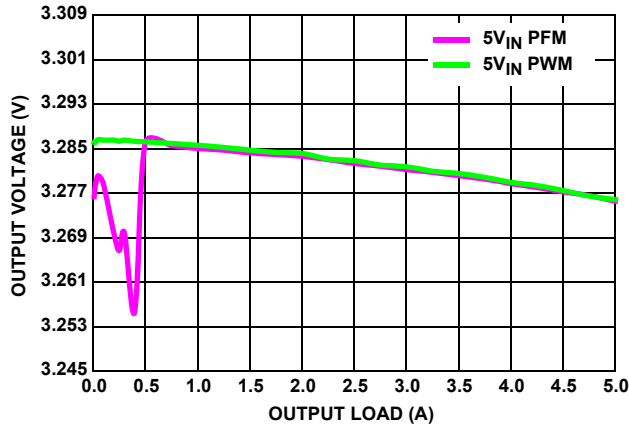


FIGURE 18.  $V_{OUT}$  REGULATION vs LOAD (1MHz,  $V_{OUT} = 3.3\text{V}$ )

## Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $\text{SYNC} = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$  Resistor load is used in the test.

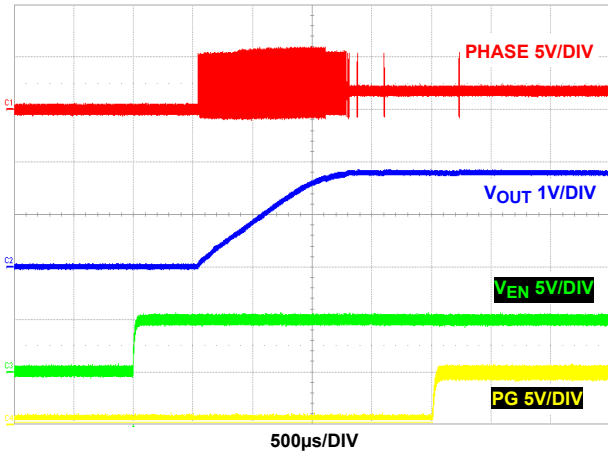


FIGURE 19. START-UP AT NO LOAD (PFM)

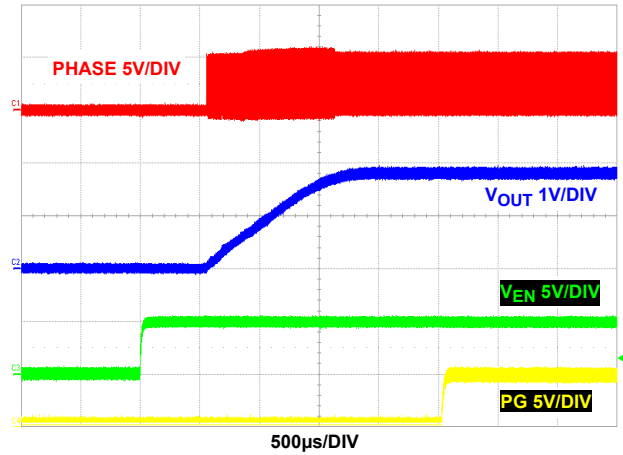


FIGURE 20. START-UP AT NO LOAD (PWM)

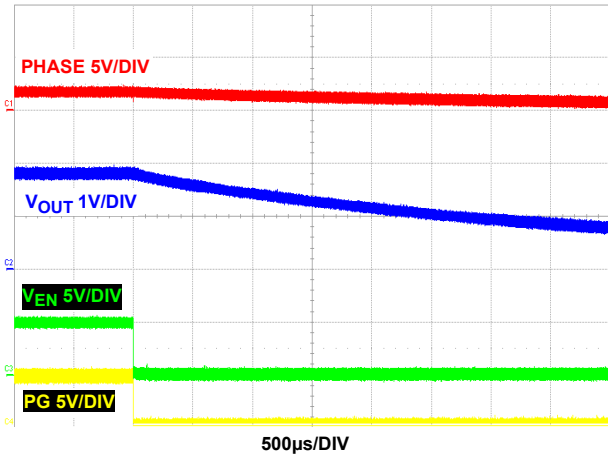


FIGURE 21. SHUTDOWN AT NO LOAD (PFM)

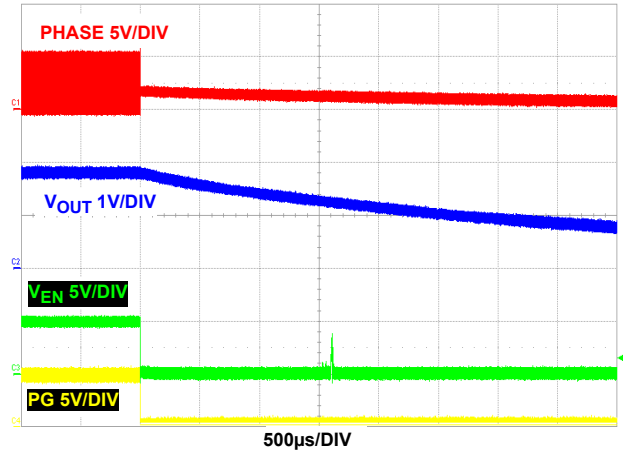


FIGURE 22. SHUTDOWN AT NO LOAD (PWM)

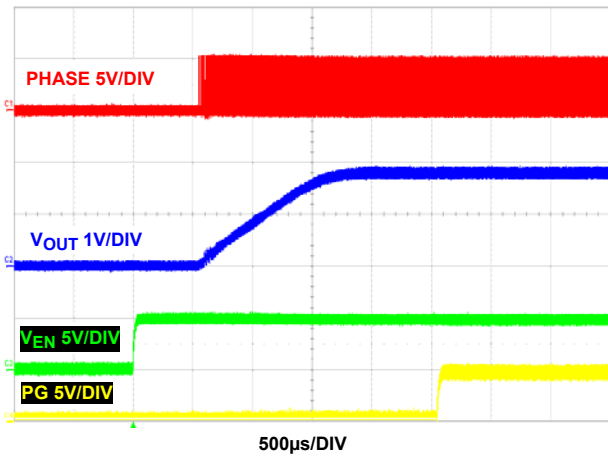


FIGURE 23. START-UP AT 5A LOAD (PWM)

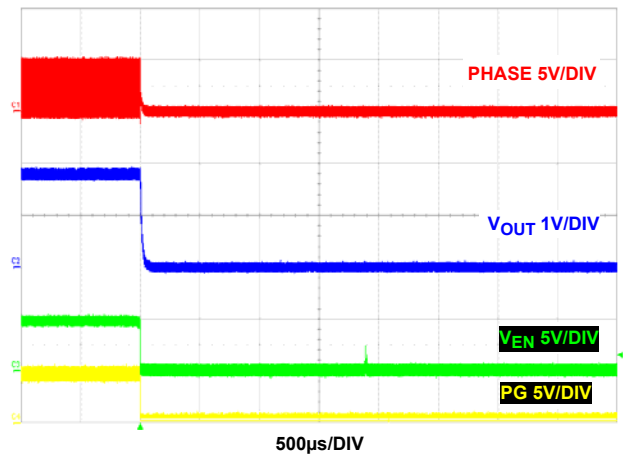


FIGURE 24. SHUTDOWN AT 5A LOAD (PWM)

## Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{VIN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$  Resistor load is used in the test. (Continued)

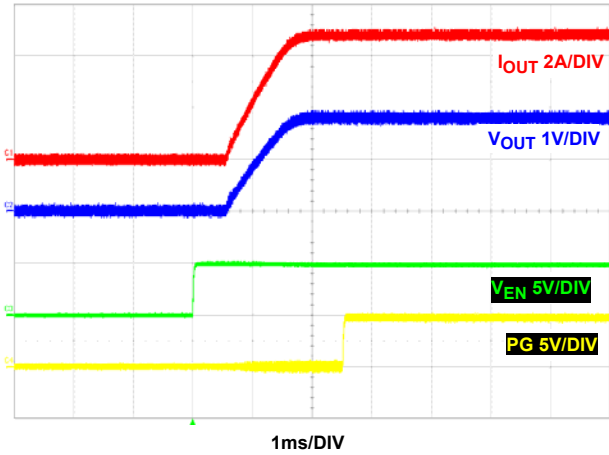


FIGURE 25. START-UP AT 5A LOAD (PFM)

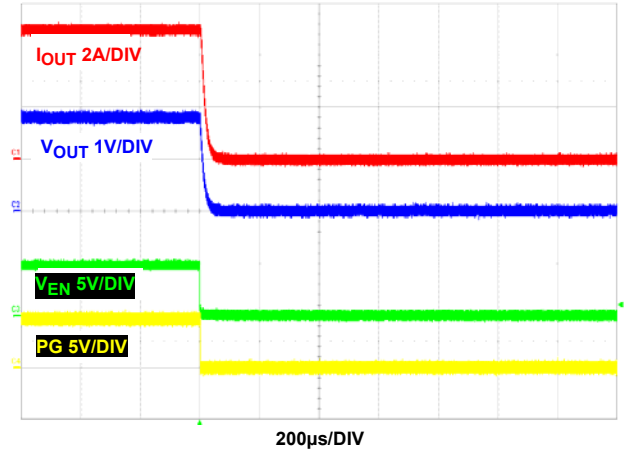


FIGURE 26. SHUTDOWN AT 5A LOAD (PFM)

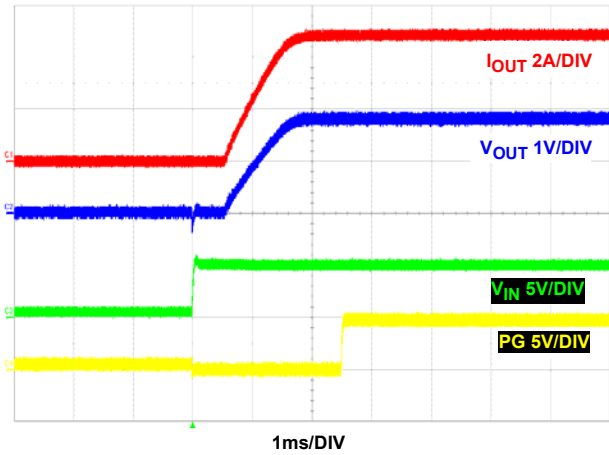


FIGURE 27. START-UP  $V_{IN}$  AT 5A LOAD (PFM)

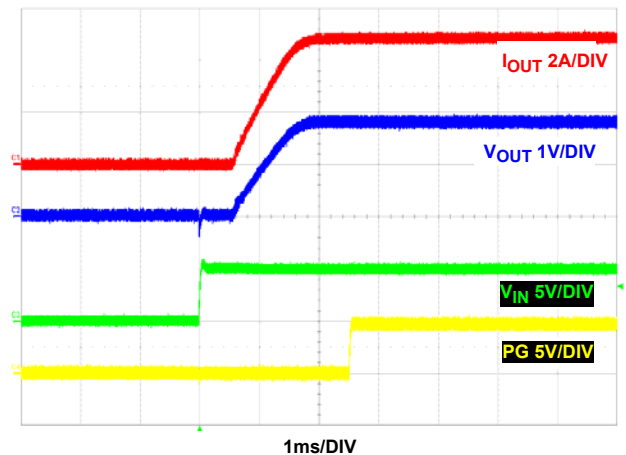


FIGURE 28. START-UP  $V_{IN}$  AT 5A LOAD (PWM)

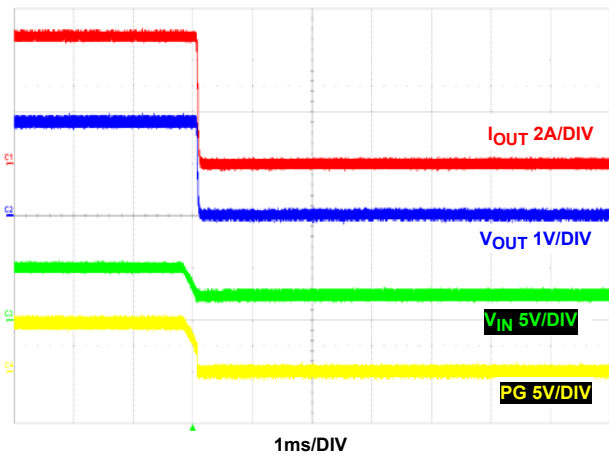


FIGURE 29. SHUTDOWN  $V_{IN}$  AT 5A LOAD (PFM)

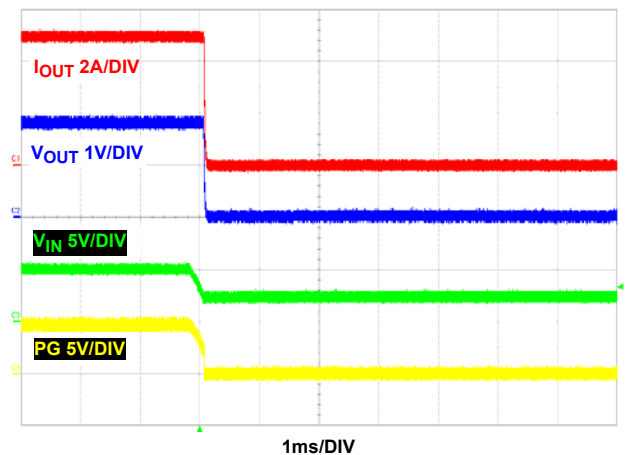


FIGURE 30. SHUTDOWN  $V_{IN}$  AT 5A LOAD (PWM)

## Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{VIN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$  Resistor load is used in the test. (Continued)

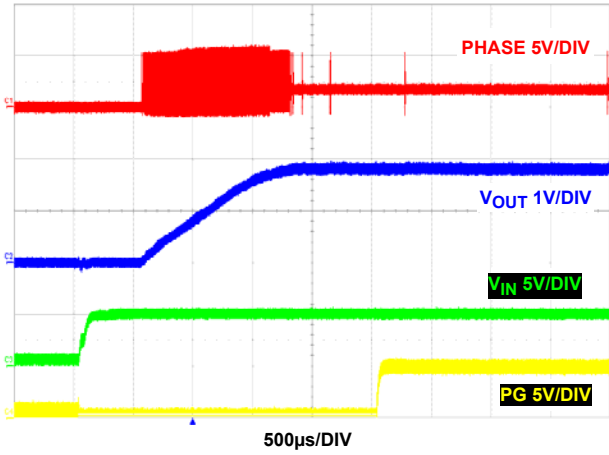


FIGURE 31. START-UP  $V_{IN}$  AT NO LOAD (PFM)

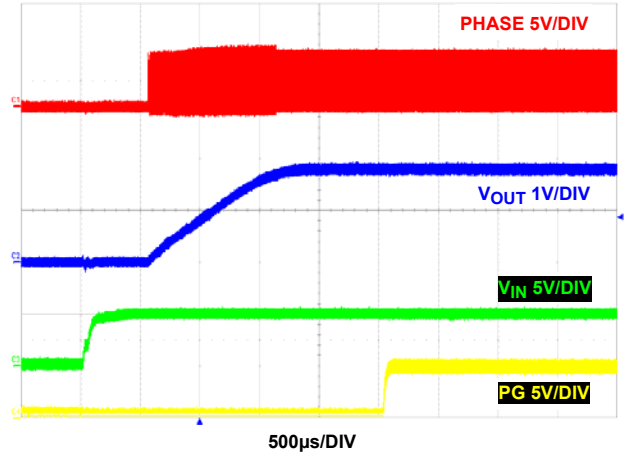


FIGURE 32. START-UP  $V_{IN}$  AT NO LOAD (PWM)

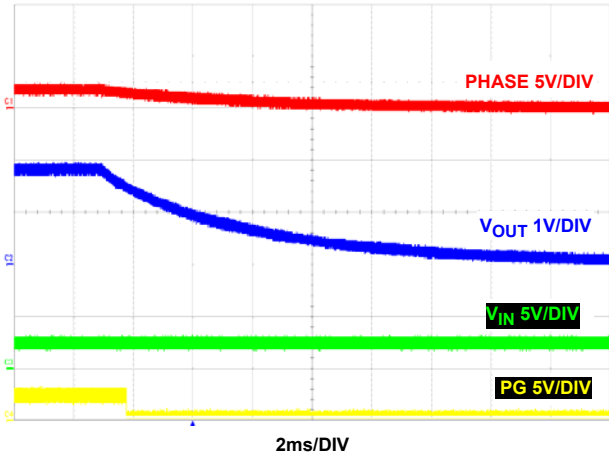


FIGURE 33. SHUTDOWN  $V_{IN}$  AT NO LOAD (PFM)

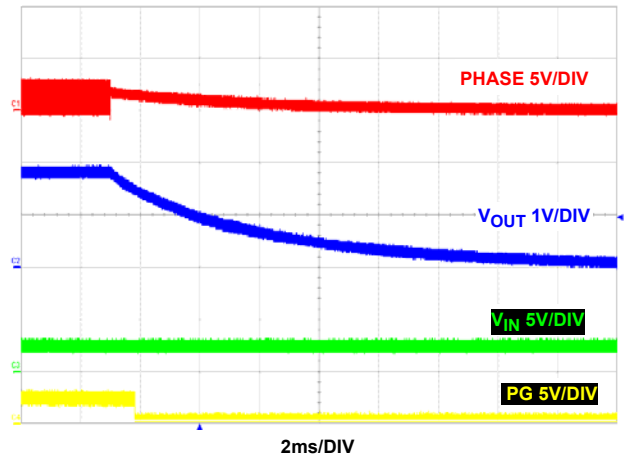


FIGURE 34. SHUTDOWN  $V_{IN}$  AT NO LOAD (PWM)

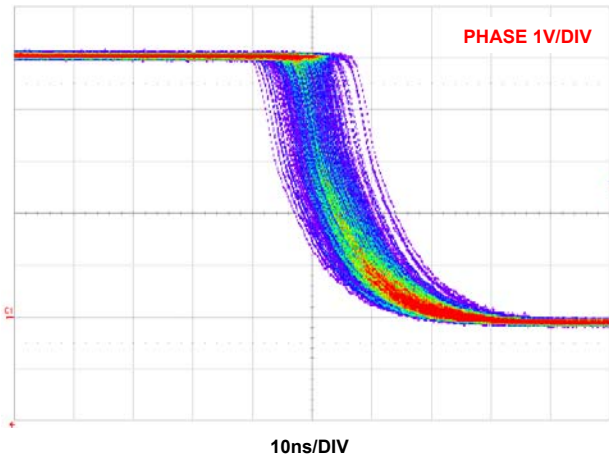


FIGURE 35. JITTER AT NO LOAD PWM

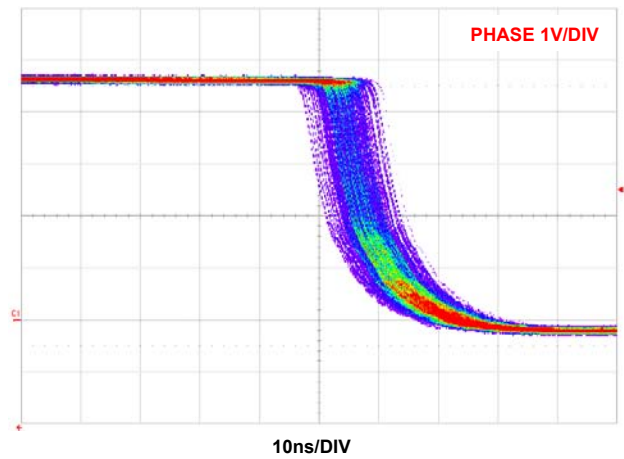


FIGURE 36. JITTER AT FULL LOAD PWM

## Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{IN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$  Resistor load is used in the test. (Continued)

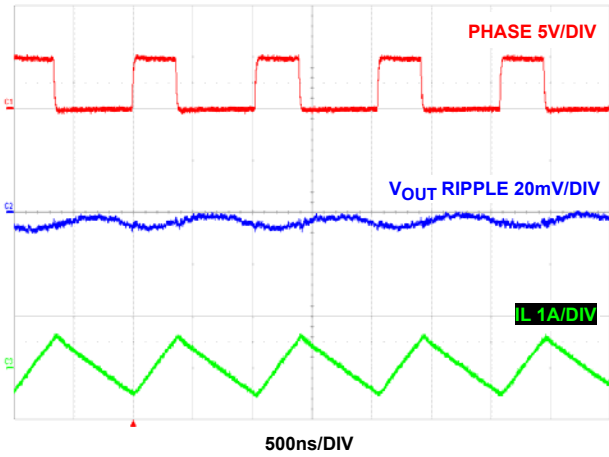


FIGURE 37. STEADY STATE AT NO LOAD PWM

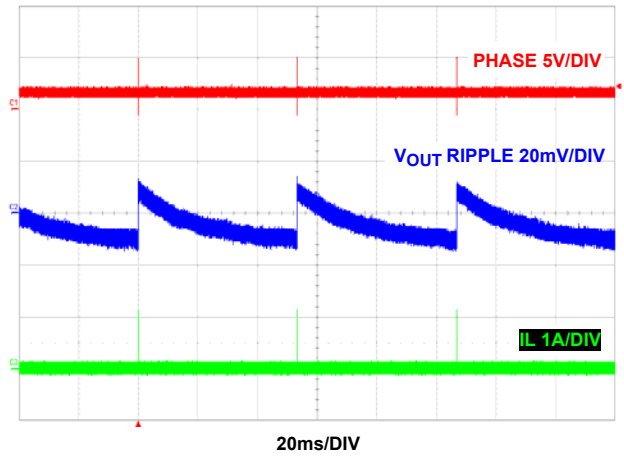


FIGURE 38. STEADY STATE AT NO LOAD PFM

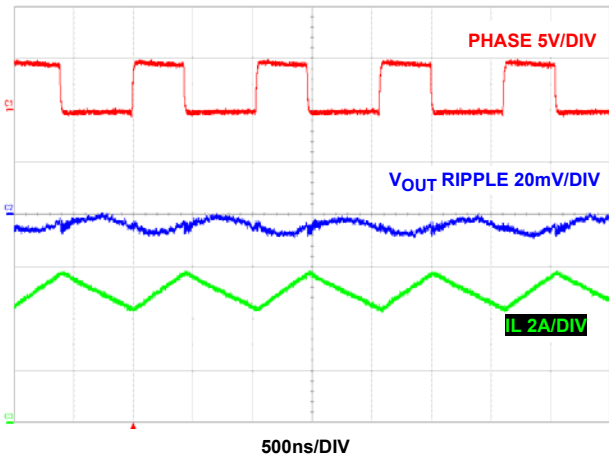


FIGURE 39. STEADY STATE AT 5A PWM

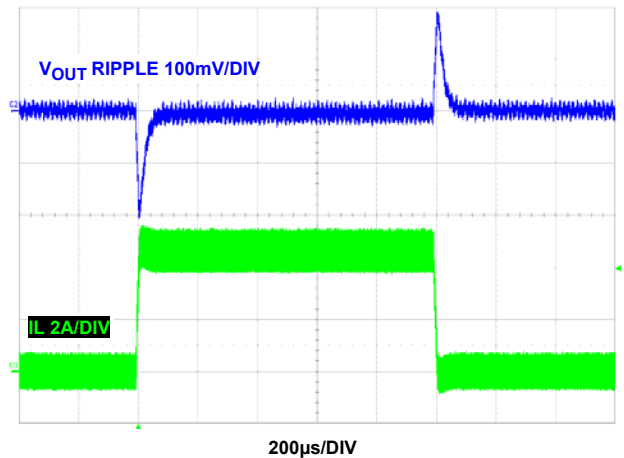


FIGURE 40. LOAD TRANSIENT (PWM)

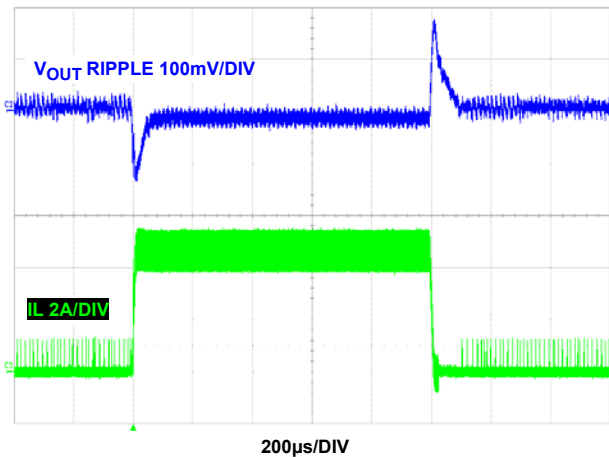


FIGURE 41. LOAD TRANSIENT (PFM)

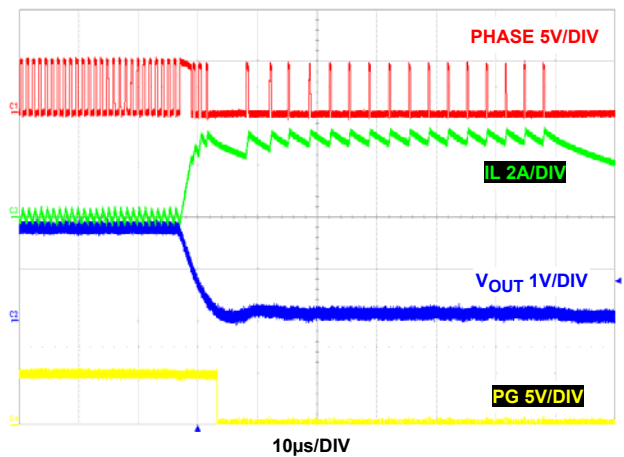


FIGURE 42. OUTPUT SHORT CIRCUIT

# Typical Operating Performance

Unless otherwise noted, operating conditions are:  $T_A = +25^\circ\text{C}$ ,  $V_{VIN} = 5\text{V}$ ,  $EN = V_{IN}$ ,  $SYNC = V_{IN}$ ,  $L = 1.0\mu\text{H}$ ,  $C_1 = 22\mu\text{F}$ ,  $C_2 = 2 \times 22\mu\text{F}$ ,  $I_{OUT} = 0\text{A to } 5\text{A}$  Resistor load is used in the test. (Continued)

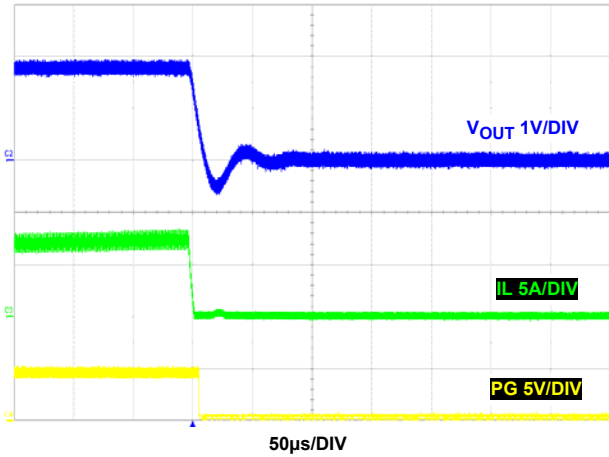


FIGURE 43. OVERCURRENT PROTECTION

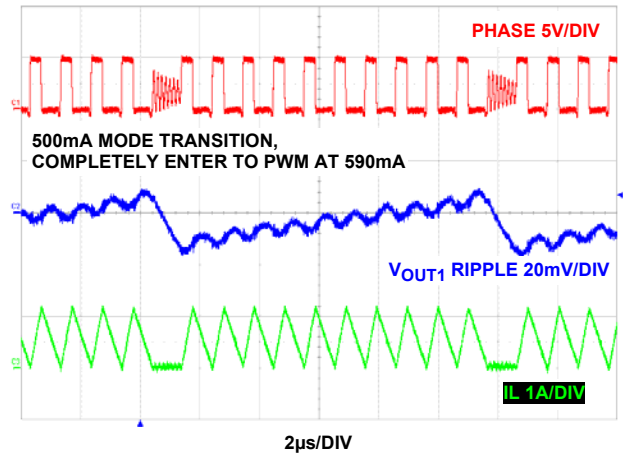


FIGURE 44. PFM TO PWM TRANSITION

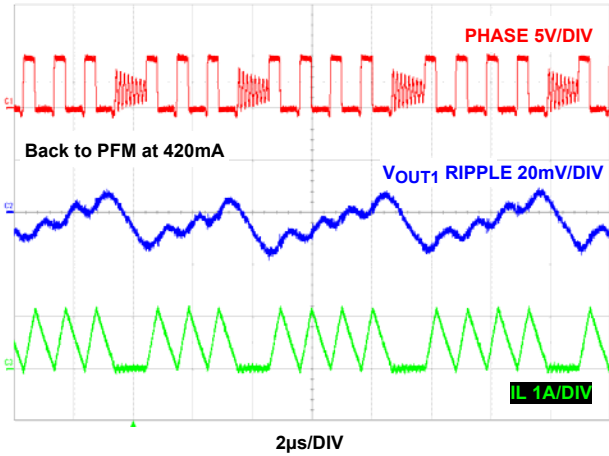


FIGURE 45. PWM TO PFM TRANSITION

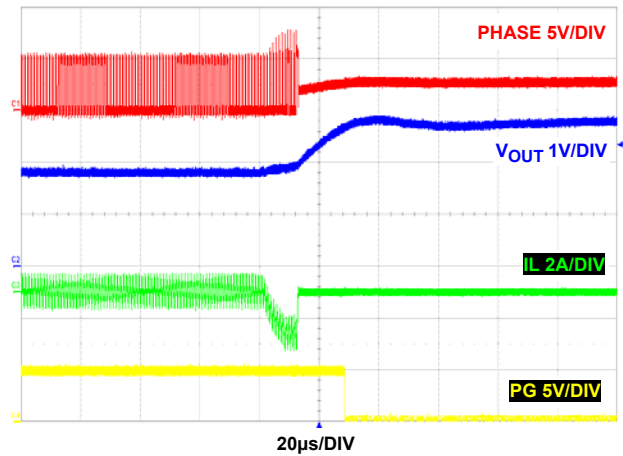


FIGURE 46. OVERVOLTAGE PROTECTION

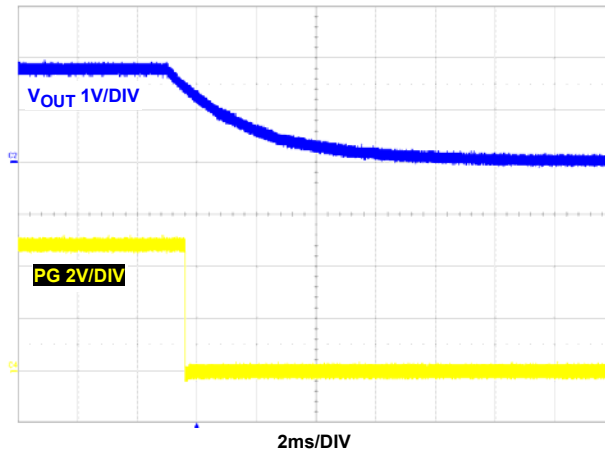


FIGURE 47. OVER-TEMPERATURE PROTECTION

## Theory of Operation

The ISL8025, ISL8025A are step-down switching regulators optimized for battery-powered applications. The regulators operate at 1MHz or 2MHz fixed default switching frequency for high efficiency and allow smaller form factor, when FS is connected to VIN. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 50µA. The supply current is typically only 5µA when the regulator is shut down.

### PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL8025, ISL8025A employs the current-mode pulse-width modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 5 shows the Functional Block Diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 200mV/A. The control reference for the current loops comes from the error amplifier's (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier CSA and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-Channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 48 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the current-sense amplifier's CSA output.

The output voltage is regulated by controlling the  $V_{EAMP}$  voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

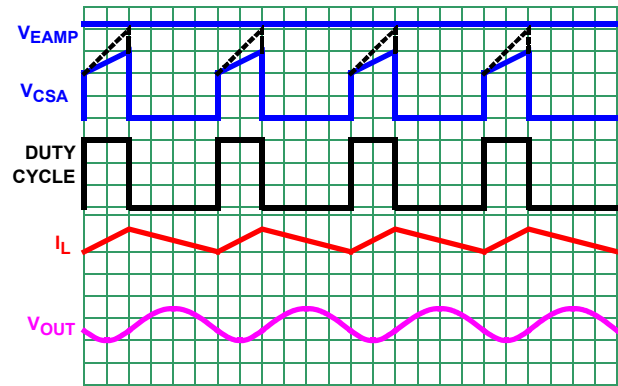


FIGURE 48. PWM OPERATION WAVEFORMS

### SKIP Mode

Pulling the SYNC pin LO (<0.4V) forces the converter into PFM mode. The ISL8025, ISL8025A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 49 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 3 on page 5 monitors the N-FET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters the skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the SKIP comparator shown in Figure 3 on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock's rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak Skip current limit value. Then, the inductor current is discharging to 0A and stays at zero (the internal clock is disabled), and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 2.5% (1.2% for 2MHz) below the nominal voltage.

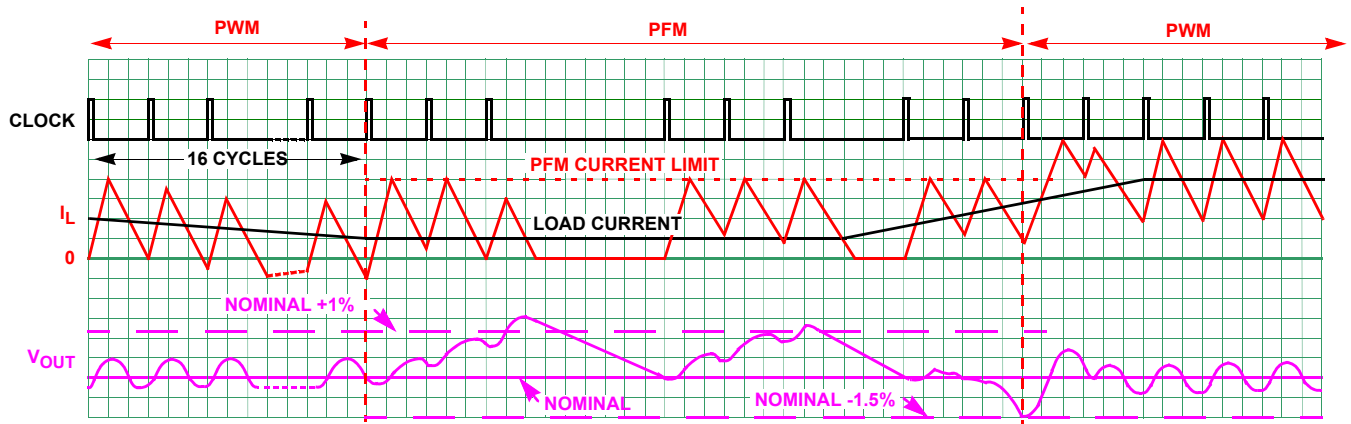


FIGURE 49. SKIP MODE OPERATION WAVEFORMS

## Frequency Adjust

The frequency of operation is fixed at 1MHz when FS is tied to VIN. Adjustable frequency ranges from 500kHz to 4MHz via a simple resistor connecting FS to SGND, according to Equation 2:

$$R_{FS}[\text{k}\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[\text{kHz}]} - 14 \quad (\text{EQ. 2})$$

## Overcurrent Protection

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3. The current sensing circuit has a gain of 200mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the 8<sup>th</sup> soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of 8 soft-start periods, the output will resume back into regulation point after hiccup mode expires.

## Negative Current Protection

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in Figure 3 on page 5. When the valley point of the inductor current reaches -3A for 4 consecutive cycles, both P-FET and N-FET are off. The 100Ω in parallel to the N-FET will activate discharging the output into regulation. The control will begin to switch when output is within regulation. The regulator will be in PFM for 20μs before switching to PWM if necessary.

## PG

PG is an open-drain output of a window comparator that continuously monitors the buck regulator output voltage. PG is actively held low when EN is low and during the buck regulator soft-start period. After 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within nominal regulation voltage set by VFB. When VFB drops 1.5% below or raises 0.8V above the nominal regulation voltage, the ISL8025, ISL8025A pulls PG low. Any fault condition forces PG low until the fault condition is cleared by attempts to soft-start. For logic level output voltages, connect an external pull-up resistor, R<sub>1</sub>, between PG and VIN. A 100kΩ resistor works well in most applications.

## UVLO

When the input voltage is below the undervoltage lock-out (UVLO) threshold, the regulator is disabled.

## Soft Start-Up

The soft-start-up reduces the in-rush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the SKIP mode to support pre-biased output condition.

Tie SS to SGND for internal soft-start is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 1.85μA current source sets the soft-start interval of the converter, t<sub>SS</sub>, as shown by Equation 3.

$$C_{SS}[\mu\text{F}] = 3.1 \cdot t_{SS}[\text{s}] \quad (\text{EQ. 3})$$

C<sub>SS</sub> must be less than 33nF to insure proper soft-start reset after fault condition.

## Enable

The enable (EN) input allows the user to control the turning on or off of the regulator for purposes, such as power-up sequencing. When the regulator is enabled, there is typically a 600μs delay for waking up the bandgap reference and then the soft-start-up begins.

## Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

## Power MOSFETs

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-FET is typically 36mΩ and the ON-resistance for the N-FET is typically 13mΩ.

## 100% Duty Cycle

The ISL8025, ISL8025A features a 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8025, ISL8025A can no longer maintain the regulation at the output, the regulator completely turns on the P-FET. The maximum dropout voltage under the 100% duty-cycle operation is the product of the load current and the ON-resistance of the P-FET.

## Thermal Shut-Down

The ISL8025, ISL8025A has built-in thermal protection. When the internal temperature reaches +150°C, the regulator is completely shut down. As the temperature drops to +125°C, the ISL8025, ISL8025A resumes operation by stepping through the soft-start.

## Application Information

### Output Inductor and Capacitor Selection

To consider steady state and transient operations, the ISL8025 typically uses a 1.0μH output inductor and the ISL8025A uses a 0.47μF. The higher or lower inductor value can be used to optimize the total converter system performance. For example, for higher output voltage 3.3V application, in order to decrease the inductor current ripple and output voltage ripple, the output inductor value can be increased. It is recommended to set the ripple inductor current approximately 30% of the maximum output current for optimized performance. The inductor ripple current can be expressed, as shown in Equation 4:

$$\Delta I = \frac{V_O \cdot \left(1 - \frac{V_O}{V_{IN}}\right)}{L \cdot f_S} \quad (\text{EQ. 4})$$

The inductor's saturation current rating needs to be at least larger than the peak current. The ISL8025, ISL8025A protects the typical peak current 6A. The saturation current needs to be over 7A for maximum output current application.

The ISL8025, ISL8025A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 2.

In Table 2, the minimum output capacitor value is given for the different output voltage to make sure that the whole converter system is stable. Additional output capacitance should be added for better performances in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

## Output Voltage Selection

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage, relative to the internal reference voltage, and feed it back to the inverting input of the error amplifier (refer to Figure 1).

The output voltage programming resistor, R<sub>2</sub>, will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, R<sub>3</sub>, is typically between 10kΩ and 100kΩ, as shown in Equation 5.

$$R_2 = R_3 \left( \frac{V_O}{V_{FB}} - 1 \right) \quad (\text{EQ. 5})$$

If the output voltage desired is 0.6V, then R<sub>3</sub> is left unpopulated and R<sub>2</sub> is shorted. There is a leakage current from V<sub>IN</sub> to PHASE. It is recommended to preload the output with 10μA minimum. For better performance, add 22pF in parallel with R<sub>2</sub> (200kΩ). Check loop analysis before use in application.

## Input Capacitor Selection

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and to provide a filtering function to prevent the switching current flowing back to the battery rail. At least two 22μF X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

## Loop Compensation Design

When COMP is not connected to VDD, the COMP pin is active for external loop compensation. The ISL8025, ISL8025A uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant, and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 50 shows the small signal model of the synchronous buck regulator.

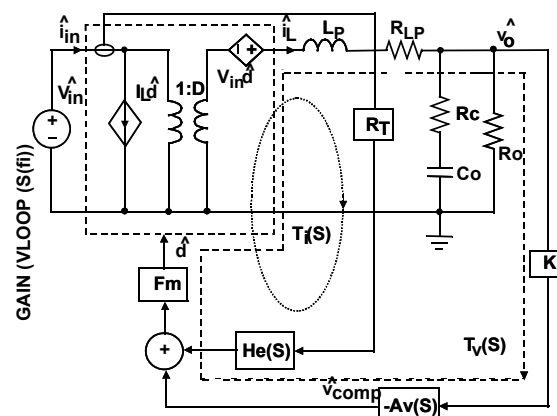


FIGURE 50. SMALL SIGNAL MODEL OF SYNCHRONOUS BUCK REGULATOR

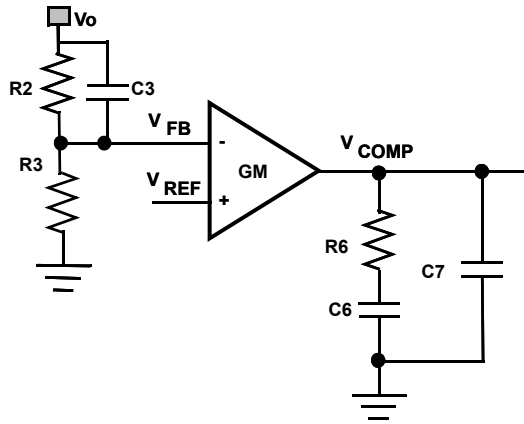


FIGURE 51. TYPE II COMPENSATOR

Figure 51 shows the type II compensator and its transfer function is expressed, as shown in Equation 6:

$$A_V(S) = \frac{\hat{v}_{comp}}{\hat{v}_{FB}} = \frac{GM \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \frac{\left(1 + \frac{S}{\omega_{cz1}}\right) \left(1 + \frac{S}{\omega_{cz2}}\right)}{S \left(1 + \frac{S}{\omega_{cp1}}\right) \left(1 + \frac{S}{\omega_{cp2}}\right)} \quad (EQ. 6)$$

where,

$$\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \quad \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \quad \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}$$

Compensator design goal:

High DC gain

Choose Loop bandwidth  $f_c$  less than 100kHz

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of  $f_c$  has a unity gain. Therefore, the compensator resistance  $R_6$  is determined by Equation 7.

$$R_6 = \frac{2\pi f_c V_o C_o R_t}{GM \cdot V_{FB}} = 15.3 \times 10^3 \cdot f_c V_o C_o \quad (EQ. 7)$$

Where GM is the sum of the trans-conductance,  $g_m$ , of the voltage error amplifier in each phase. Compensator capacitor  $C_6$  is then given by Equation 8.

$$C_6 = \frac{R_o C_o}{R_6} = \frac{V_o C_o}{I_o R_6}, C_7 = \max\left(\frac{R_c C_o}{R_6}, \frac{1}{\pi f_s R_6}\right) \quad (EQ. 8)$$

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 8. An optional zero can boost the phase margin.  $\omega_{cz2}$  is a zero due to  $R_2$  and  $C_3$ .

Put compensator zero 2 to 5 times  $f_c$

$$C_3 = \frac{1}{\pi f_c R_2} \quad (EQ. 9)$$

Example:  $V_{IN} = 5V, V_O = 1.8V, I_O = 5A, f_s = 1MHz, R_2 = 200k\Omega, R_3 = 100k\Omega, C_o = 2 \times 22\mu F / 3m\Omega, L = 1\mu H, f_c = 100kHz$ , then compensator resistance  $R_6$ :

$$R_6 = 15.3 \times 10^3 \cdot 100kHz \cdot 1.8V \cdot 44\mu F = 121k\Omega \quad (EQ. 10)$$

$$C_6 = \frac{1.8V \cdot 44\mu F}{5A \cdot 121k\Omega} = 131pF \quad (EQ. 11)$$

$$C_7 = \max\left(\frac{3m\Omega \cdot 44\mu F}{121k\Omega}, \frac{1}{\pi \cdot 1MHz(121k\Omega)}\right) = (1pF, 2.6pF) \quad (EQ. 12)$$

It is also acceptable to use the closest standard values for  $C_6$  and  $C_7$ . There is approximately 3pF parasitic capacitance from  $V_{COMP}$  to GND; Therefore,  $C_7$  is optional. Use  $C_6 = 150pF$  and  $C_7 = OPEN$ .

$$C_3 = \frac{1}{\pi 100kHz \cdot 200k\Omega} = 16pF \quad (EQ. 13)$$

Use  $C_3 = 15pF$ . Note that  $C_3$  may increase the loop bandwidth from previous estimated value. Figure 52 shows the simulated voltage loop gain. It is shown that it has a 150kHz loop bandwidth with a 42° phase margin and 10dB gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering  $R_6$  by 20% to 30%.

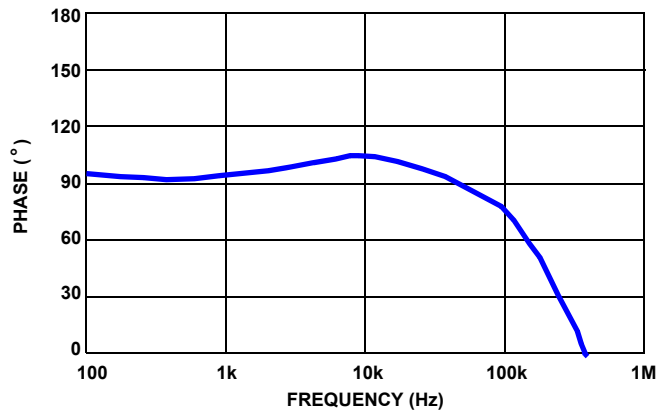
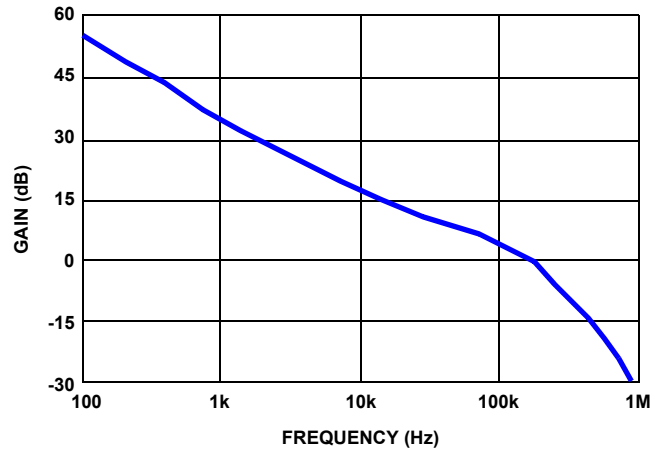


FIGURE 52. SIMULATED LOOP GAIN

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## PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For ISL8025, ISL8025A, the power loop is composed of the output inductor L's, the output capacitor (COUT), the PHASE pins, and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins, and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin. The ground of input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

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## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

DATE	REVISION	CHANGE
December 19, 2013	FN8357.1	<p>Page 1: Left side, line 8 Changed From: P-Channel (45mΩ) high-side FET and N-Channel (19mΩ) To: P-Channel (36mΩ) high-side FET and N-Channel (13mΩ) Left side, line 11 Changed From: 225mV dropout voltage at 5A To: 180mV dropout voltage at 5A Right side, line 2 Changed From: P-channel 45mΩ and N-channel 19mΩ typical values To: P-channel 36mΩ and N-channel 13mΩ typical values</p> <p>Removed 6th Bullet in Features: "Complete BOM with as few as 3 external parts"</p> <p>Page 3 Updated "Pin Descriptions" for COMP pin to include the internal compensation.</p> <p>Electrical Spec Table on page 7 Changed P-Channel and N-Channel from: P-channel (VIN = 5V) TYP = 45mΩ, Max = 55mΩ P-channel (VIN = 2.7V), TYP = 70mΩ, Max = 90mΩ N-channel (VIN = 5V), TYP = 19mΩ, Max = 25mΩ N-channel (VIN = 2.7V), TYP = 28mΩ, Max = 37mΩ To: P-channel (VIN = 5V) TYP = 36mΩ, Max = 41mΩ P-channel (VIN = 2.7V), TYP = 52mΩ, Max = 60mΩ N-channel (VIN = 5V), TYP = 13mΩ, Max = 16mΩ N-channel (VIN = 2.7V), TYP = 17mΩ, Max = 21mΩ</p> <p>Electrical Spec Table on page 7 Compensation Error Amplifier Trans-conductance conditions changed from FSW = VIN to Internal Compensation and FSW with resistor changed to external compensation</p> <p>Resistor load is used in the test was added to conditions in "Typical Operating Performance" on page 8.</p> <p>Page 18 Left side, line 9 Changed From: typically 45mΩ To: typically 36mΩ Left side, line 10 Changed From: typically 19mΩ To: typically 13mΩ Right side, line 16 Changed from: add 15pF to: add 22pF</p> <p>Page 19 Right side, line 5 Changed From: C6 = 164pF To: C6 = 131pF Right side, line 6 Changed From: C7 = (1pF, 2.3pF) To: C7 = (1pF, 2.6pF) Changed the following equations Equation 7 - 17.45 to 15.3 Text above Equation 10 changed 4A to 5A Equation 10 changed 17.45 to 15.3 and 138 to 121 Removed text that followed Equation 10 which read: It is acceptable to use 137kΩ as the closest standard value for R6. Equation 11 changed 4A to 5A, 137 to 121, 144 to 164 Equation 12 changed 137 to 121</p>
February 20, 2013	FN8357.0	Initial Release

## About Intersil

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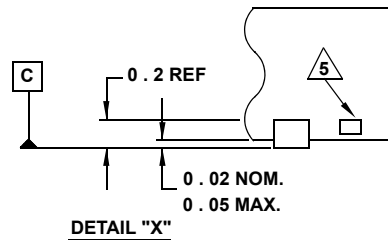
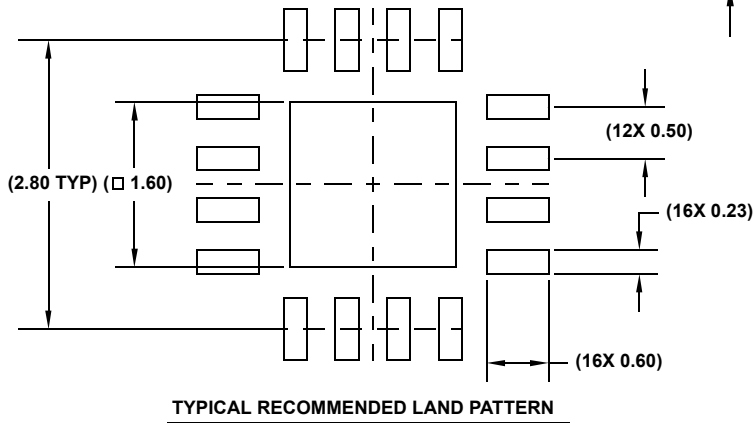
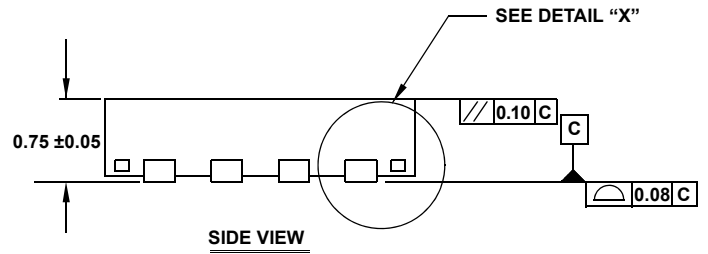
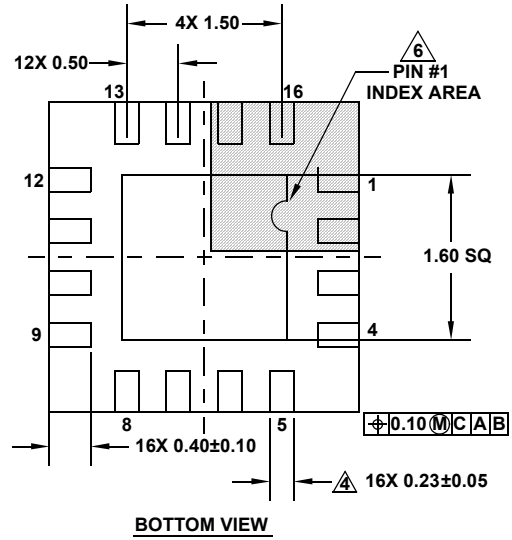
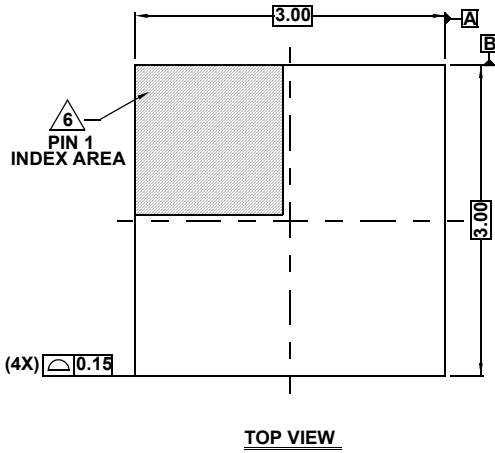
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# Package Outline Drawing

## L16.3x3D

16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE

Rev 0, 3/10




**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. JEDEC reference drawing: MO-220 WEED.

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