THE DATASHEET OF

ISL8240MIRZ

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ISL8240M

Dual 20A/Single 40A Step-Down Power Module

FN8450
Rev 2.00
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The ISL8240M is a fully-encapsulated step-down switching power supply that can deliver up to 100W output power from a small 17mmx17mm PCB footprint. The two 20A outputs may be used independently or combined to deliver a single output of 40A. Designing a high-performance board-mounted power supply has never been simpler – only a few external components are needed to create a very dense and reliable power solution.

1.5% output voltage accuracy, differential remote voltage sensing and fast transient response create a very high-performance power system. Built-in output overvoltage, overcurrent and over-temperature protection enhance system reliability.

The ISL8240M is available in a thermally-enhanced QFN package. Excellent efficiency and low thermal resistance permit full power operation without heat sinks or fans. In addition, the QFN package with external leads permits easy probing and visual solder inspection.

Related Literature

AN1922, "ISL8240MEVAL4Z Dual 20A/Optional 40A Cascadable Evaluation Board Setup Procedure"

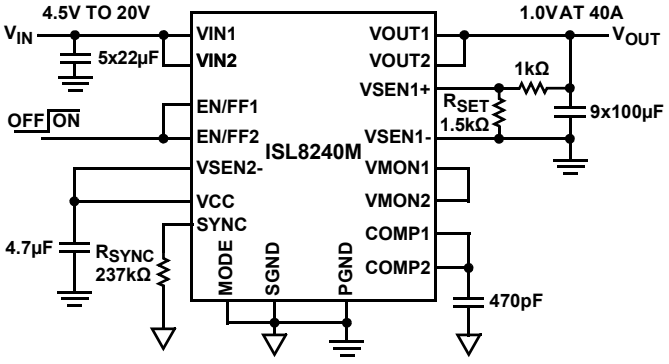
AN1923, "ISL8240MEVAL3Z 40A, Single Output Evaluation Board Setup Procedure"

Features

- Fully-encapsulated dual step-down switching power supply
- Up to 100W output from a 17mmx17mm PCB footprint
- Dual 20A or single 40A output
- Up to 94% conversion efficiency
- 4.5V to 20V input voltage range
- 0.6V to 2.5V output voltage range
- 1.5% output voltage accuracy with differential remote sensing
- Output overvoltage, overcurrent and over-temperature protection
- QFN package with exposed leads permits easy probing and visual solder inspection

Applications

- Computing, networking and telecom infrastructure equipment
- Industrial and medical equipment
- General purpose point-of-load (POL) power



NOTE: All pins not shown are floating

FIGURE 1. COMPLETE 40A STEP-DOWN POWER SUPPLY

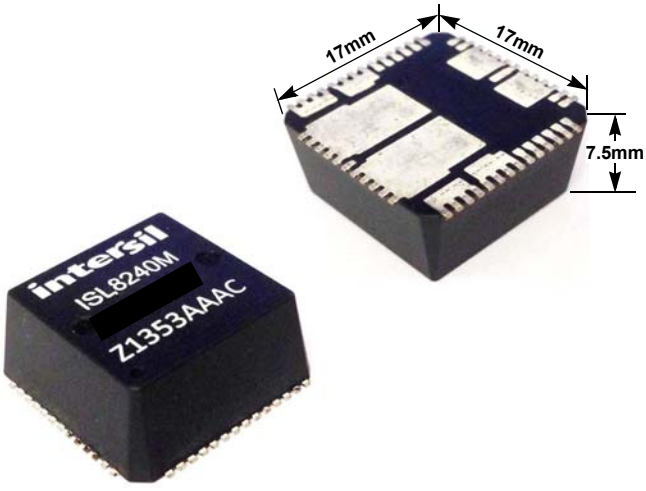


FIGURE 2. SMALL FOOTPRINT WITH HIGH POWER DENSITY

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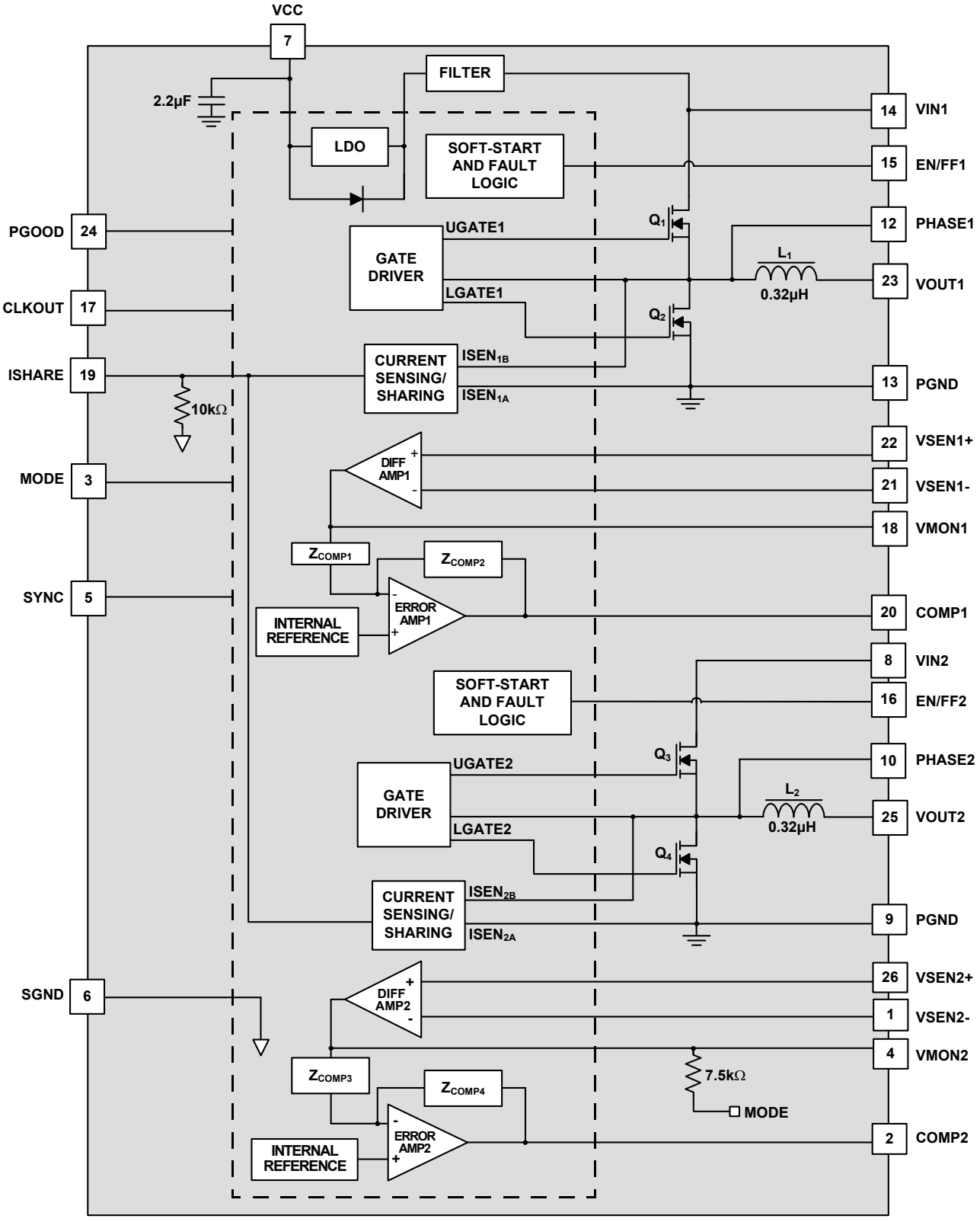
Pinout Internal Circuit



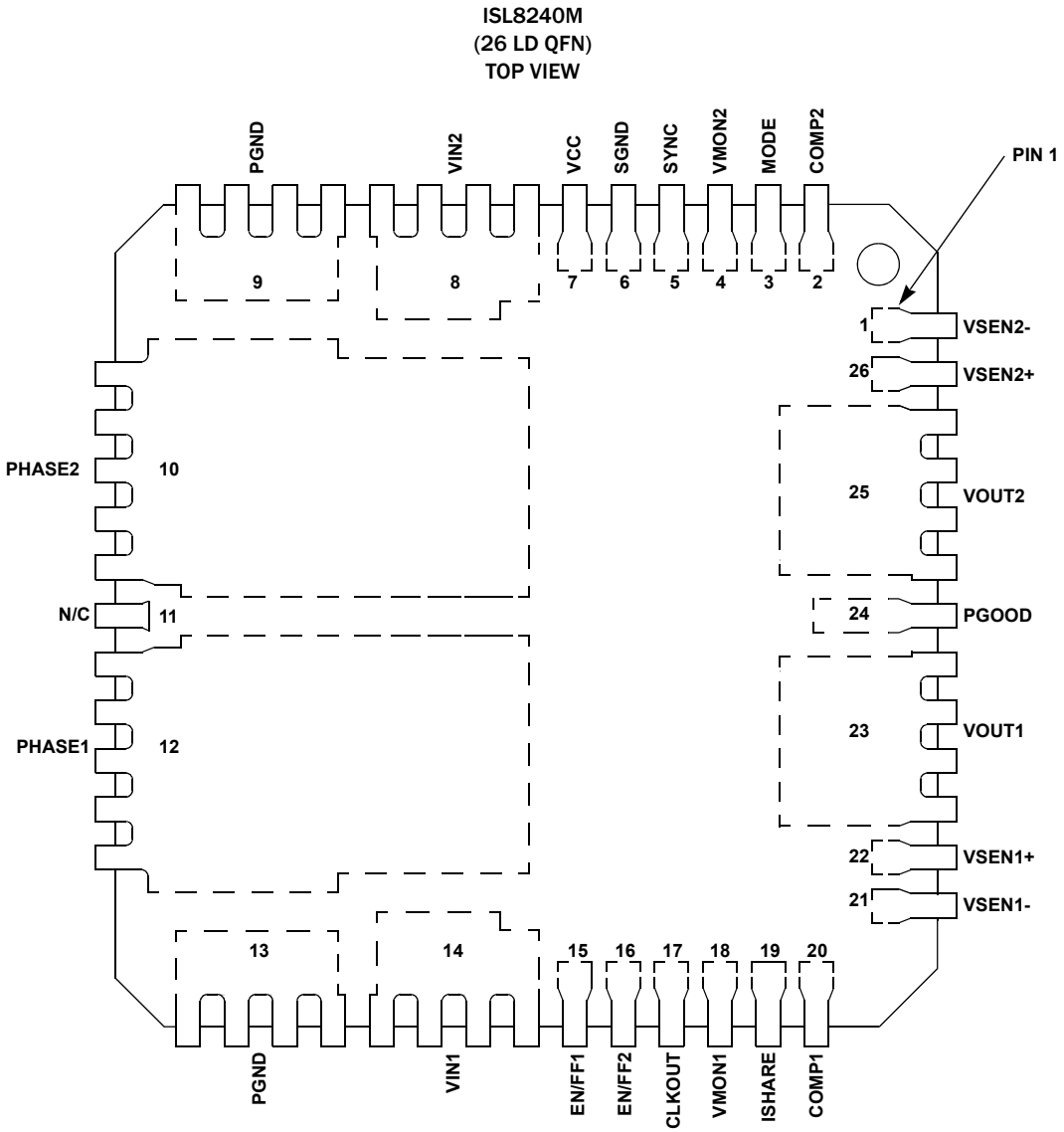
Ordering Information

PART NUMBER (Notes 1, 2, 3)	PART MARKING	TEMP. RANGE (°C) (Note 4)	PACKAGE (RoHS Compliant)	PKG. DWG. #
ISL8240MIRZ	ISL8240M	-40 to +125	26 Ld QFN	L26.17x17
ISL8240MEVAL3Z	Evaluation Board			
ISL8240MEVAL4Z	Evaluation Board			

NOTES:

1. Add “-T*” suffix for tape and reel. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3) termination finish which is compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ISL8240M. For more information on MSL, please see tech brief TB363
4. The ISL8240M is guaranteed over the full -40°C to +125°C internal junction temperature range. Note that the allowed ambient temperature consistent with these specifications is determined by specific operating conditions, including board layout, cooling scheme and other environmental factors.

Pin Configuration



Pin Descriptions

PIN NUMBER	PIN NAME	TYPE	PIN DESCRIPTION
21, 1	VSEN1-, VSEN2-	I	**Output voltage negative feedback.** Negative input of the differential remote sense for the regulator. Connect to the negative rail or ground of the load/processor, as shown in Figure 24. The negative feedback pins can be used to program the module operation conditions. See Tables 3 and 5 for details.
20, 2	COMP1, COMP2	I/O	**Error amplifier outputs.** Typically floating for dual-output use. For parallel use, a 470pF~1nF capacitor is recommended on the COMP pins of each SLAVE phase to eliminate the coupling noise. All COMP pins of SLAVE phases need to tie to MASTER phase COMP1 pin (first phase). Internal compensation networks are implemented for working in the full range of I/O conditions.
3	MODE	I	**Mode setting.** Typically floating for dual-output use; tie to SGND for parallel use. See Tables 3 and 5 for details. When VSEN2- is pulled within 700mV of VCC, the 2nd channel's remote sensing amplifier is disabled. The MODE pin, as well as the VSEN2+ pin, determine relative phase-shift between the two channels and the CLKOUT signal output.
18, 4	VMON1, VMON2	I/O	**Remote sensing amplifier outputs.** These pins are connected internally to OV/UV/PGOOD comparators, so they can't float when the module works in multiphase operation. When VSEN1-, VSEN2- are pulled within 700mV of VCC, the corresponding remote sensing amplifier is disabled; the output (VMON pin) is in high impedance. In this event, the VMON pins can be used as an additional monitor of the output voltage, with a resistor divider to protect the system against single point of failure. The default setting voltage is 0.6V. See Table 3 for details.
5	SYNC	I	**Signal synchronization.** An optional external resistor (R_{SYNC}) connected from this pin to SGND increases oscillator switching frequency (Figure 34 and Table 1). The internal default frequency is 350kHz with this pin floating. Also, the internal oscillator can lock to an external frequency source or the CLKOUT signal from another ISL8240M. Input voltage range for external source: 3V to 5V square wave. No capacitor is recommended on this pin.
6	SGND	PWR	**Control signal ground.** Connect to PGND under the module in the quiet inner layer. Make sure to have the single location for the connection between SGND and PGND to avoid noise coupling. See "Layout Guide" on page 25.
7	VCC	PWR	**5V internal linear regulator output.** Voltage range: 3V to 5.6V. The decoupling ceramic capacitor for the VCC pin is recommended to be 4.7µF.
14, 8	VIN1, VIN2	PWR	**Power inputs.** Input voltage range: 4.5V to 20V. Tie directly to the input rail. VIN1 provides power to the internal linear drive circuitry. When the input is 4.5V to 5.5V, VIN should be tied directly to VCC.
9, 13	PGND	PWR	**Power ground.** Power ground pins for both input and output returns.
12, 10	PHASE1, PHASE2	PWR	**Phase node.** Use for monitoring switching frequency. Phase pins should be floating or used for snubber connections. To achieve better thermal performance, the phase planes can also be used for heat removal with thermal vias connected to large inner layers. See "Layout Guide" on page 25.
11	NC	-	**Non-connection pin.** This pin is floating with no connection inside.
15, 16	EN/FF1, EN/FF2	I/O	**Enable and feed-forward control.** Tie a resistor divider to VIN or use the system enable signal for this pin. The voltage turn-on threshold is 0.8V. With a voltage lower than the threshold, the corresponding channel can be disabled independently. By connecting to VIN with a resistor divider, the input voltage can be monitored for UVLO (undervoltage lockout) function. The voltage on each EN/FF pin is also used to adjust the internal control loop gain independently to realize the feed-forward function. Please set the EN/FF between 1.25V to 5V. A 1nF capacitor is recommended on each EN/FF pin. Please see Table 1 on page 19 to select a resistor divider and application details in "EN/FF Turn ON/OFF" on page 21.
17	CLKOUT	I/O	**Clock out.** Provide the clock signal for the input synchronization signal of other ISL8240Ms. Typically tied to VCC for dual-output use with 180° phase-shift. See Tables 3 and 5 when using more than one ISL8240M. When the module is in dual-output mode, the clock-out signal is disabled. By programming the voltage level of this CLKOUT pin, the module can work for DDR/tracking or as two independent outputs with selectable phase-shift. See Table 6.
19	ISHARE	O	**Current sharing control.** Tie all ISHARE pins together when multiple modules are configured for current sharing and share a common current output. The ISHARE voltage represents the average current of all active and connected channels. A 470pF capacitor is recommended for each ISHARE pin for multiple phase applications. Typically, the ISHARE pin should be floating for dual-output or single module application.
22, 26	VSEN1+, VSEN2+	I	**Output voltage positive feedback.** Positive inputs of differential remote sense for the regulator. A resistor divider can be connected to this pin to program the output voltage. It is recommended to put the resistor divider close to the module and connect the kelvin sensing traces of VOUT and VSEN- to the sensing points of the load/processor; see Figure 24. The VSEN2+ pin can be used to program the module operation conditions. See Tables 3 and 5 for details.
23, 25	VOUT1, VOUT2	PWR	**Power Output.** Apply output load between these pins and PGND pins. Output voltage range: 0.6V to 2.5V.
24	PGOOD	O	**Power-good.** Provide open-drain power-good signal when the output is within 9% of the nominal output regulation point with 4% hysteresis (13%/9%) and soft-start complete. PGOOD monitors the outputs (VMON) of the internal differential amplifiers.

Absolute Maximum Ratings

Input Voltage, V_{IN} . . . . . -0.3V to +25V
Driver Bias Voltage, V_{CC} . . . . . -0.3V to +6.5V
Phase Voltage, V_{PHASE} . . . . . -0.3V to +30V
Input, Output or I/O Control Voltage . . . . . -0.3V to V_{CC} + 0.3V
ESD Rating
Human Body Model (Tested per JESD22-A114E) 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charge Device Model (Tested per JESD22-C101C) 750V
Latch-up (Tested per JESD-78B; Class 2, Level A) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
QFN Package (Notes 5, 6)	8.5	0.9

Maximum Storage Temperature Range . . . . . -55°C to +150°C
Pb-free Reflow Profile . . . . . Refer to Figure 44

Recommended Operating Conditions

Input Voltage, V_{IN1} and V_{IN2} . . . . . 4.5V to 20.0V
Output Voltage, V_{OUT1} and V_{OUT2} . . . . . 0.6V to 2.5V
Junction Temperature Range . . . . . -40°C to +125°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

5. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. See Tech Brief TB379.
6. For θ_{JC}, the "case temp" location is the center of the phase exposed metal pad on the package underside.

Electrical Specifications

T_A = +25°C, V_{IN} = 12V, unless otherwise noted. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C** (Note 4).

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNITS
VCC SUPPLY CURRENT						
Nominal Supply V_{IN} Current	I_{Q_VIN}	V_{IN} = 20V; No Load; EN1 = EN2 = high; V_{OUT1} = V_{OUT2} = 1.5V		140		mA
		V_{IN1} = 20V; No Load; EN1 = high, EN2 = low; V_{OUT1} = 1.5V		80		mA
		V_{IN2} = 20V; No Load; EN1 = low, EN2 = high; V_{OUT2} = 1.5V		76		mA
		V_{IN1} = 12V; No Load; EN1 = high, EN2 = high; V_{OUT1} = V_{OUT2} = 1.5V		159		mA
		V_{IN} = 4.5V; No Load; EN1 = EN2 = high; V_{OUT1} = V_{OUT2} = 1.5V		188		mA
		V_{IN1} = 4.5V; No Load; EN1 = high, EN2 = low; V_{OUT1} = 1.5V		102		mA
		V_{IN2} = 4.5V; No Load; EN1 = low, EN2 = high; V_{OUT2} = 1.5V		94		mA
INTERNAL LINEAR REGULATOR (Note 9)						
Maximum Current	I_{PVCC}	V_{CC} = 4V to 5.6V		250		mA
Saturated Equivalent Impedance	R_{LDO}	P-Channel MOSFET (V_{IN} = 5V)		1		Ω
V_{CC} Voltage Level	V_{CC}	I_{VCC} = 0mA	**5.1**	5.4	**5.6**	V
POWER-ON RESET (Note 9)						
Rising V_{CC} Threshold		0°C to +75°C		2.85	2.97	V
		-40°C to +85°C		2.85	3.05	V
Falling V_{CC} Threshold				2.65	**2.75**	V
System Soft-start Delay	t_{SS_DLY}	After PLL and V_{CC} PORs, and EN above their thresholds		384		Cycles
ENABLE (Note 9)						
Turn-on Threshold Voltage			**0.75**	0.8	**0.86**	V
Hysteresis Sink Current	I_{EN_HYS}		**23**	30	**35**	µA
Undervoltage Lockout Hysteresis	V_{EN_HYS}	V_{EN_RTH} = 10.6V; V_{EN_FTH} = 9V, R_{UP} = 53.6kΩ, R_{DOWN} = 5.23kΩ		1.6		V
Sink Current	I_{EN_SINK}	V_{ENFF} = 1V	**15.4**			mA
Sink Impedance	R_{EN_SINK}	I_{EN_SINK} = 5mA, V_{ENFF} = 1V			**64**	Ω
OSCILLATOR						
Oscillator Frequency	f_{OSC}	SYNC pin is open		350		kHz
Total Variation (Note 9)		V_{CC} = 5V; -40°C < T_A < +85°C	-9		+9	%

Electrical Specifications

T_A = +25°C, V_{IN} = 12V, unless otherwise noted. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C** (Note 4). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNITS
FREQUENCY SYNCHRONIZATION AND PHASE LOCK LOOP (Note 9)						
Synchronization Frequency		V_{CC} = 5V	**350**		**700**	kHz
PLL Locking Time		V_{CC} = 5.4V, f_{SW} = 500kHz		130		µs
Input Signal Duty Cycle Range			**10**		**90**	%
PWM (Note 9)						
Minimum PWM OFF Time	t_{MIN_OFF}		**310**	345	**410**	ns
Current Sampling Blanking Time	$t_{BLANKING}$			175		ns
OUTPUT CHARACTERISTICS						
Output Continuous Current Range	$I_{OUT(DC)}$	V_{IN} = 12V, V_{OUT1} = 1.5V	**0**		**20**	A
		V_{IN} = 12V, V_{OUT2} = 1.5V	**0**		**20**	A
		V_{IN} = 12V, V_{OUT} = 1.5V, in Parallel mode	**0**		**40**	A
Line Regulation Accuracy	$\Delta V_{OUT}/\Delta V_{IN}$	V_{IN} = 4.5V to 20V				
		V_{OUT1} = 1.5V, I_{OUT1} = 0A		0.0065		%
		V_{OUT2} = 1.5V, I_{OUT2} = 0A		0.0065		%
		V_{IN} = 4.5V to 20V				
		V_{OUT1} = 1.5V, I_{OUT1} = 20A		0.01		%
		V_{OUT2} = 1.5V, I_{OUT2} = 20A		0.01		%
Load Regulation Accuracy	$\Delta V_{OUT}/V_{OUT}$	V_{IN} = 5V, 2x47µF ceramic capacitor and 1x330µF POSCAP				
		I_{OUT1} = 0A to 20A, V_{OUT1} = 1V			**1**	%
		I_{OUT2} = 0A to 20A, V_{OUT2} = 1V			**1**	%
Output Ripple Voltage	ΔV_{OUT}	V_{IN} = 12V, 4x100µF +2x10µF ceramic capacitor and 1x330µF POSCAP				
		I_{OUT1} = 0A, V_{OUT1} = 1.5V		16		mV_{P-P}
		I_{OUT2} = 0A, V_{OUT2} = 1.5V		16		mV_{P-P}
		I_{OUT1} = 20A, V_{OUT1} = 1.5V		21		mV_{P-P}
		I_{OUT2} = 20A, V_{OUT2} = 1.5V		21		mV_{P-P}
DYNAMIC CHARACTERISTICS						
Voltage Change for Positive Load Step	ΔV_{OUT-DP}	Current slew rate = 2.5A/µs V_{IN} = 12V, V_{OUT} = 1.5V, 4x100µF + 2x10µF ceramic capacitor and 1x330µF POSCAP				
		I_{OUT1} = 0A to 10A		100		mV_{P-P}
		I_{OUT2} = 0A to 10A		100		mV_{P-P}
Voltage Change for Negative Load Step	ΔV_{OUT-DN}	Current slew rate = 2.5A/µs V_{IN} = 12V, V_{OUT} = 1.5V, 4x100µF + 2x10µF ceramic capacitor, and 1x330µF POSCAP				
		I_{OUT1} = 10A to 0A		80		mV_{P-P}
		I_{OUT2} = 10A to 0A		80		mV_{P-P}
REFERENCE (Note 9)						
Reference Voltage (Include Error and Differential Amplifier Offsets)	V_{REF1}	T_A = -40°C to +85°C	**0.5958**	0.6	**0.6042**	V
			-0.7		**0.7**	%
Reference Voltage (Include Error and Differential Amplifier Offsets)	V_{REF2}	T_A = -40°C to +85°C	**0.5955**	0.6	**0.6057**	V
			-0.75		**0.95**	%

Electrical Specifications T_A = +25°C, V_{IN} = 12V, unless otherwise noted. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C** (Note 4). **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 7)	TYP (Note 8)	MAX (Note 7)	UNITS
DIFFERENTIAL AMPLIFIER (Note 9)						
DC Gain	UG_DA	Unity gain amplifier		0		dB
Unity Gain Bandwidth	UGBW_DA			5		MHz
VSEN+ Pin Sourcing Current	I_{VSEN+}		**0.2**	1	**2.5**	µA
Maximum Source Current for Current Sharing	I_{VSEN1-}	VSEN1- Source Current for Current Sharing when parallel multiple modules, each of which has its own voltage loop		350		µA
Input Impedance	$R_{VSEN+_to_VSEN-}$	V_{VSEN+}/I_{VSEN+}, V_{VSEN+} = 0.6V		-600		kΩ
Output Voltage Swing			**0**		**V_{CC} - 1.8**	V
Input Common Mode Range			**-0.2**		**V_{CC} - 1.8**	V
Disable Threshold	V_{VSEN-}	$V_{MON1,2}$ = tri-state		V_{CC} - 0.4		V
OVERCURRENT PROTECTION (Note 9)						
Channel Overcurrent Limit	I_{limit1}	V_{IN} = 12V, V_{OUT1} = 1.5V, R_{SYNC} = 768k		24.5		A
	I_{limit2}	V_{IN} = 12V, V_{OUT2} = 1.5V, R_{SYNC} = 768k		24		A
Share Pin OC Threshold	V_{OC_SET}	V_{CC} = 5V (comparator offset included)	**1.16**	1.20	**1.22**	V
CURRENT SHARE						
Current Share Accuracy	ΔI/IOUT	V_{IN} = 12V, V_{OUT} = 1.5V I_{OUT} = 40A, VSEN2- = high		±10		%
POWER-GOOD MONITOR (Note 9)						
Undervoltage Falling Trip Point	V_{UVF}	Percentage below reference point	**-15**	-13	**-11**	%
Undervoltage Rising Hysteresis	V_{UVR_HYS}	Percentage above UV trip point		4		%
Overvoltage Rising Trip Point	V_{OVR}	Percentage above reference point	**11**	13	**15**	%
Overvoltage Falling Hysteresis	V_{OVF_HYS}	Percentage below OV trip point		4		%
PGOOD Low Output Voltage		I_{PGOOD} = 2mA			**0.35**	V
Sinking Impedance		I_{PGOOD} = 2mA			**70**	Ω
Maximum Sinking Current		V_{PGOOD} < 0.8V		10		mA
OVERVOLTAGE PROTECTION (Note 9)						
OV Latching-up Trip Point		EN/FF = UGATE = LATCH Low, LGATE = High	**118**	120	**122**	%
OV Non-Latching-up Trip Point		EN = Low, UGATE = Low, LGATE = High		113		%
LGATE Release Trip Point		EN = Low/HIGH, UGATE = Low, LGATE = Low		87		%
OVER-TEMPERATURE PROTECTION (Note 9)						
Over-Temperature Trip (Controller Junction Temperature)				150		°C
Over-Temperature Release Threshold (Controller Junction Temperature)				125		°C

NOTES:

7. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
8. Parameters with TYP limits are not production tested, unless otherwise specified.
9. Parameters are 100% tested for internal IC prior to module assembly.

Typical Performance Characteristics

Efficiency Performance

T_A = +25°C, if not specified, as shown in Figure 23 with 2nd phase disabled. The efficiency equation is as follows:

$$\text{Efficiency} = \frac{\text{Output Power}}{\text{Input Power}} = \frac{P_{OUT}}{P_{IN}} = \frac{(V_{OUT} \times I_{OUT})}{(V_{IN} \times I_{IN})}$$

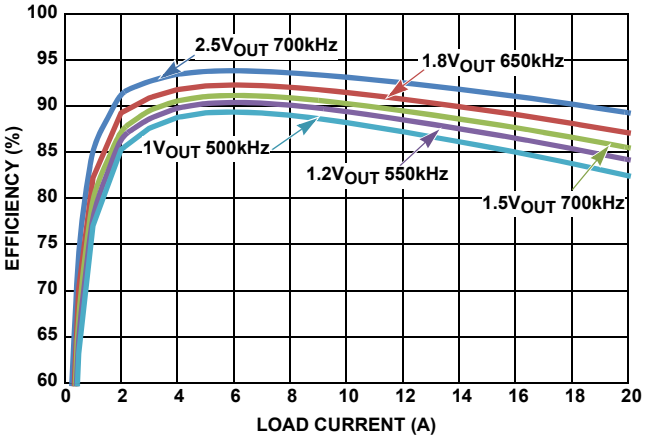


FIGURE 3. EFFICIENCY vs LOAD CURRENT ($5V_{IN}$)

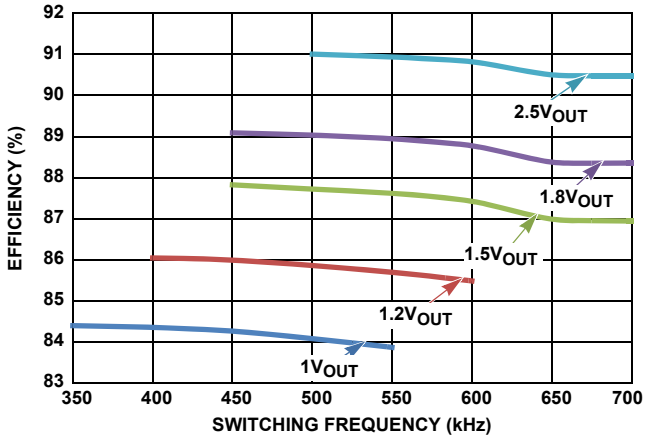


FIGURE 4. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 5V AND I_{OUT} = 18A FOR VARIOUS OUTPUT VOLTAGES

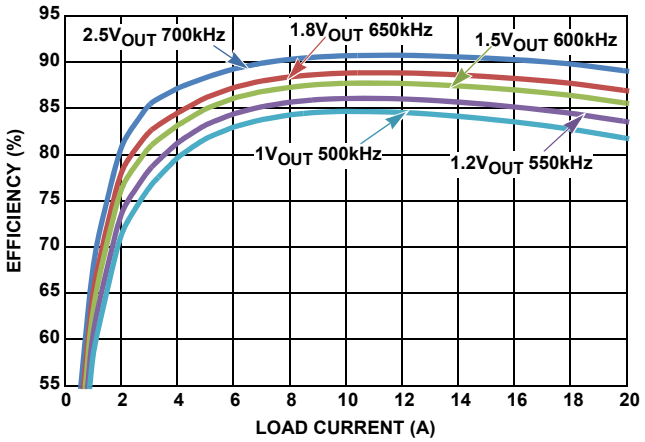


FIGURE 5. EFFICIENCY vs LOAD CURRENT ($12V_{IN}$)

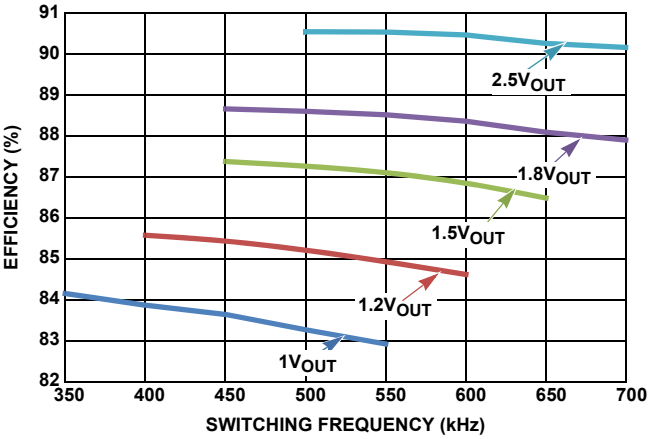


FIGURE 6. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 12V AND I_{OUT} = 18A FOR VARIOUS OUTPUT VOLTAGES

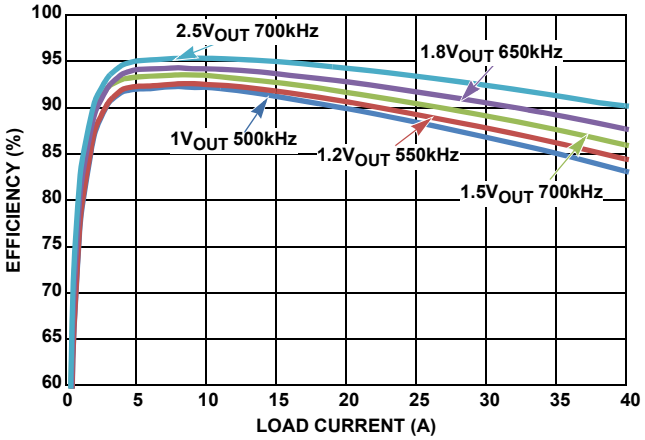


FIGURE 7. EFFICIENCY vs LOAD CURRENT (PARALLEL SINGLE OUTPUT, AS SHOWN IN Figure 24 AT $5V_{IN}$)

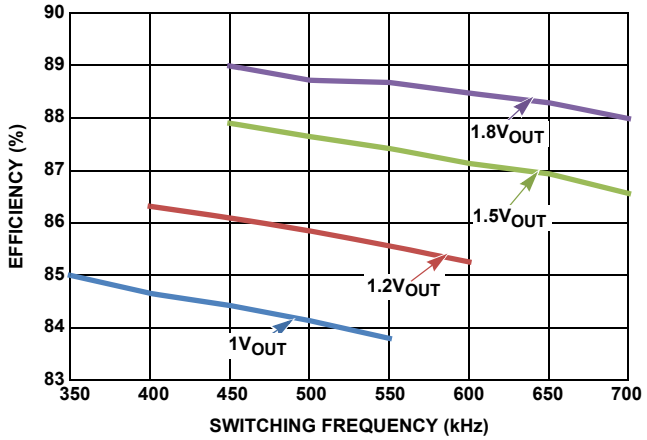


FIGURE 8. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 5V (PARALLEL SINGLE OUTPUT, AS SHOWN IN Figure 24) AND I_{OUT} = 36A FOR VARIOUS OUTPUT VOLTAGES

Typical Performance Characteristics (Continued)

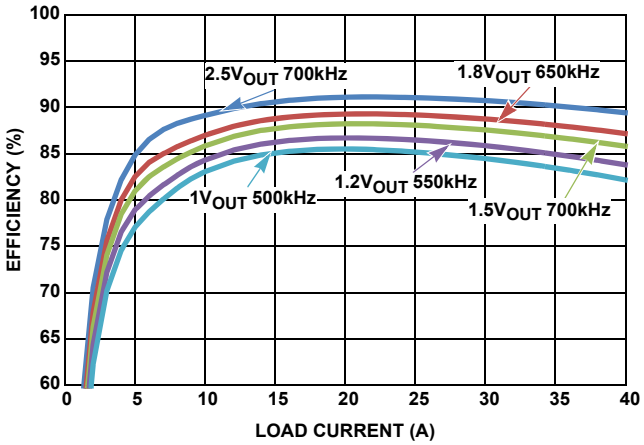


FIGURE 9. EFFICIENCY vs LOAD CURRENT (PARALLEL SINGLE OUTPUT, AS SHOWN IN Figure 24 AT $12V_{IN}$)

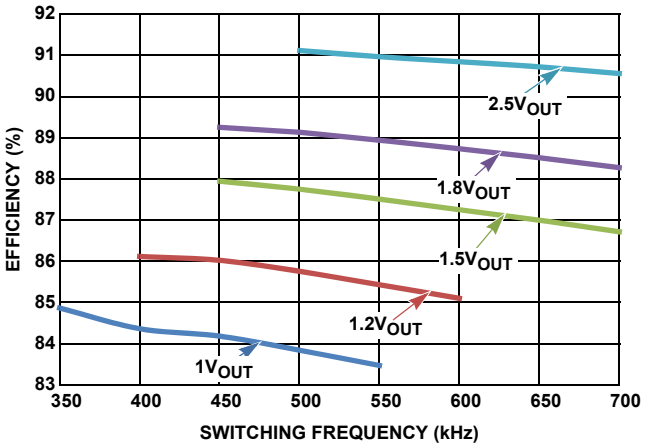


FIGURE 10. EFFICIENCY vs SWITCHING FREQUENCY AT V_{IN} = 12V (PARALLEL SINGLE OUTPUT, AS SHOWN IN Figure 24 AT $12V_{IN}$) AND I_{OUT} = 18A FOR VARIOUS OUTPUT VOLTAGES

Transient Response Performance

V_{IN} = 12V current slew rate = 10A/µs. T_A = +25°C, if not specified, as shown in Figure 23 with 2nd phase disabled.

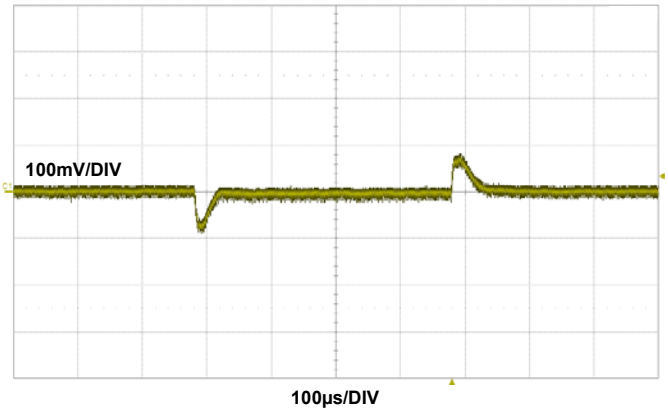


FIGURE 11. $1V_{OUT}$ TRANSIENT RESPONSE, I_{OUT} = 0A TO 10A, f_{SW} = 350kHz, COUT = 2x10µF+7x100µF CERAMIC CAPACITOR, CFF = 6.8nF

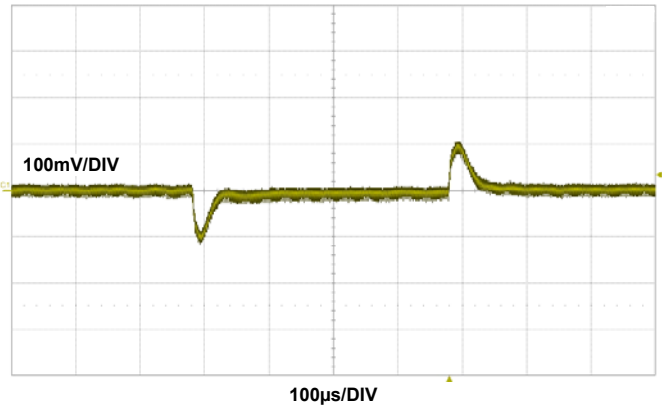


FIGURE 12. $1.5V_{OUT}$ TRANSIENT RESPONSE, I_{OUT} = 0A TO 10A, f_{SW} = 400kHz, COUT = 2x10µF+7x100µF CERAMIC CAPACITOR, CFF = 6.8nF

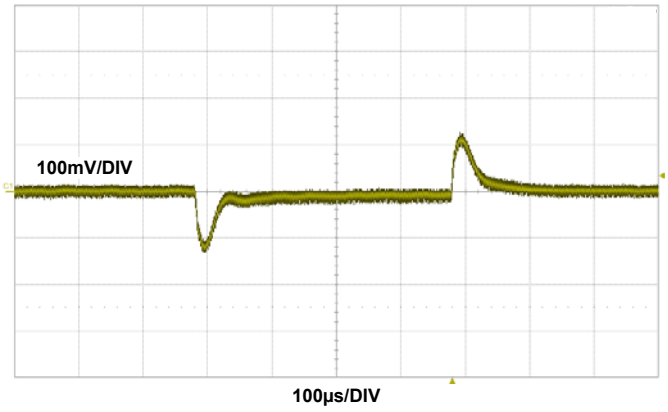


FIGURE 13. $1.8V_{OUT}$ TRANSIENT RESPONSE, I_{OUT} = 0A TO 10A, f_{SW} = 450kHz, COUT = 2x10µF+7x100µF CERAMIC CAPACITOR, CFF = 6.8nF

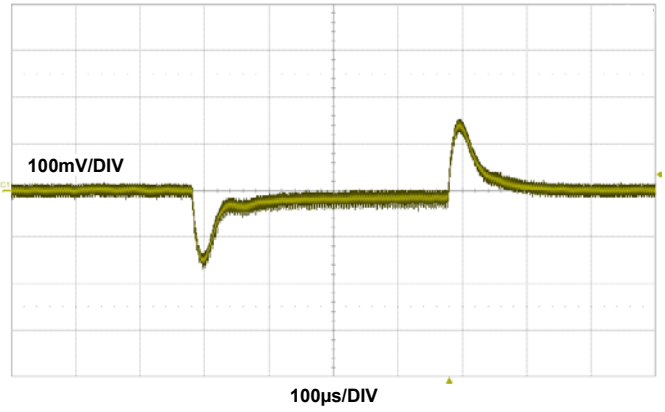


FIGURE 14. $2.5V_{OUT}$ TRANSIENT RESPONSE, I_{OUT} = 0A TO 10A, f_{SW} = 500kHz, COUT = 2x10µF+7x100µF CERAMIC CAPACITOR, CFF = 6.8nF

Typical Performance Characteristics (Continued)

Transient Response Performance

V_{IN} = 12V current slew rate = 10A/µs. T_A = +25°C, if not specified, as shown in Figure 23 with 2nd phase disabled. (Continued)

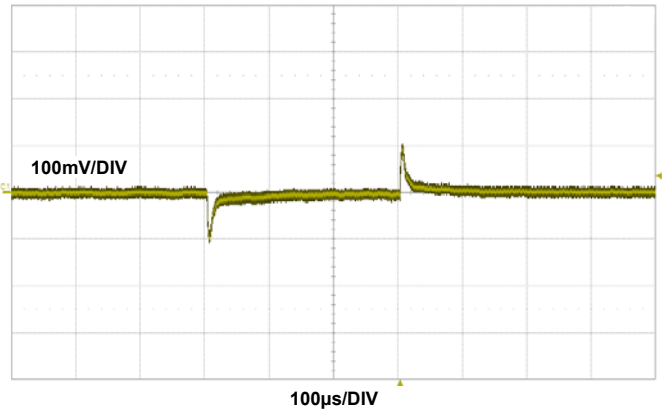


FIGURE 15. $1V_{OUT}$ DUAL PHASE SINGLE OUTPUT TRANSIENT RESPONSE, I_{OUT} = 0A TO 20A, f_{SW} = 350kHz, COUT = 330µF POSCAP+10µF+5x100µF CERAMIC CAPACITOR

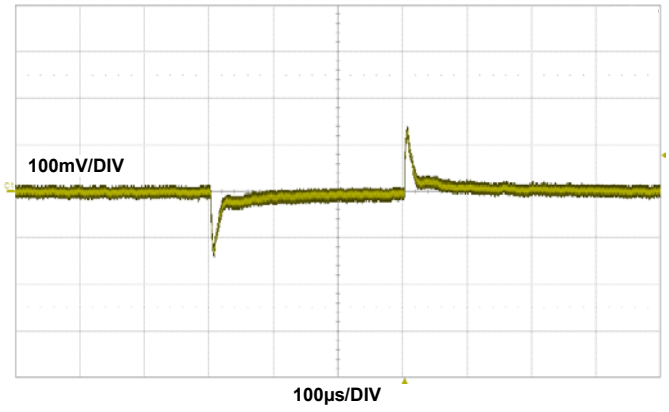


FIGURE 16. $1.5V_{OUT}$ DUAL PHASE SINGLE OUTPUT TRANSIENT RESPONSE, I_{OUT} = 0A TO 20A, f_{SW} = 400kHz, COUT = 330µF POSCAP+10µF+5x100µF CERAMIC CAPACITOR

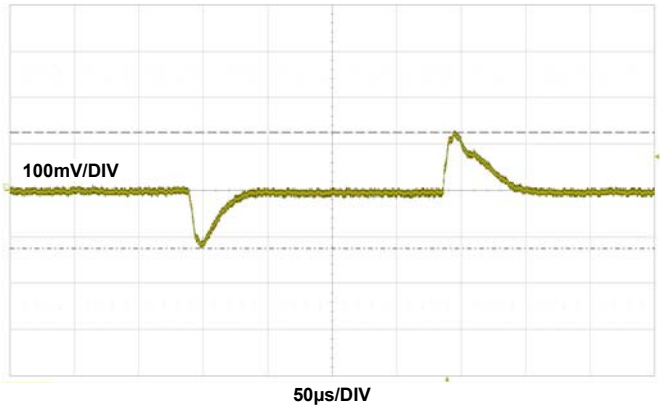


FIGURE 17. $0.9V_{OUT}$ FOUR PHASE SINGLE OUTPUT TRANSIENT RESPONSE, I_{OUT} = 0A TO 40A, f_{SW} = 350kHz, COUT = 6x330µF POSCAP+7x47µF+4x100µF CERAMIC CAPACITOR

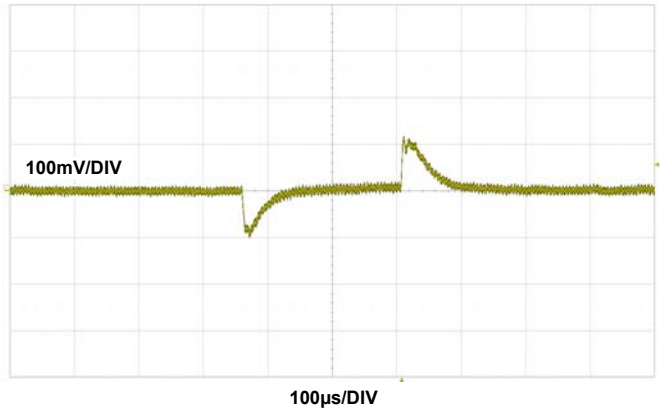


FIGURE 18. $1V_{OUT}$ SIX PHASE SINGLE OUTPUT TRANSIENT RESPONSE, I_{OUT} = 0A TO 60A, f_{SW} = 350kHz, COUT = 6x330µF POSCAP+7x47µF+6x100µF CERAMIC CAPACITOR

Typical Performance Characteristics (Continued)

Start-up and Short Circuit Performance

V_{IN} = 12V, V_{OUT} = 1.5V, CIN = 1x330µF, 3x22µF/Ceramic, COUT = 330µF POSCAP+1x10µF+4x100µF Ceramic. T_A = +25°C, if not specified, as shown in Figure 23 with 2nd phase disabled.

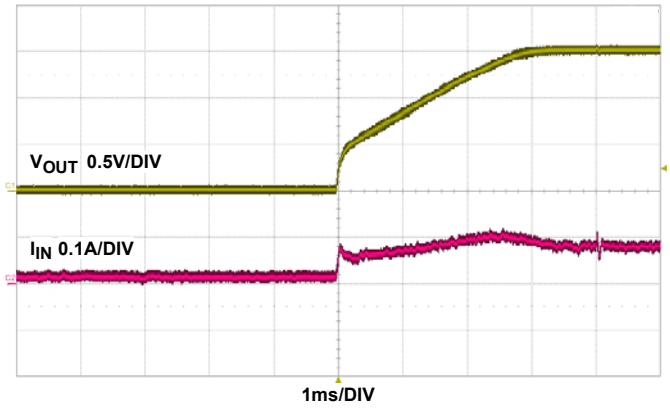


FIGURE 19. START-UP AT 0A

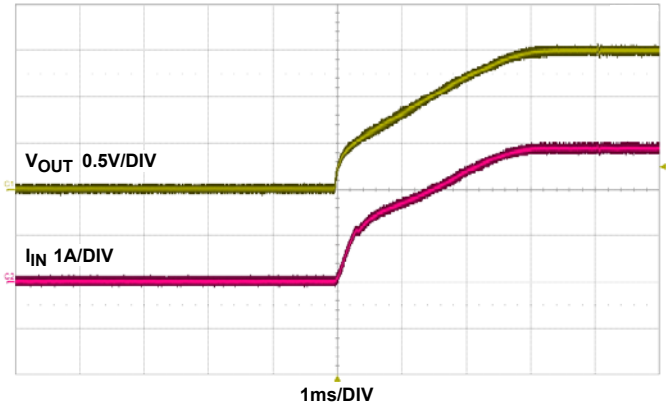


FIGURE 20. START-UP AT 20A

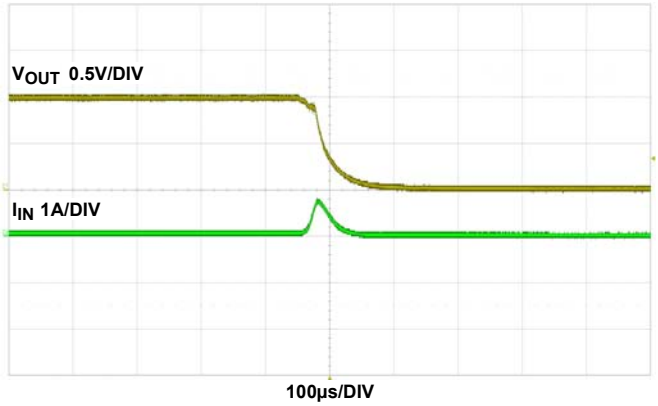


FIGURE 21. SHORT CIRCUIT AT 0A

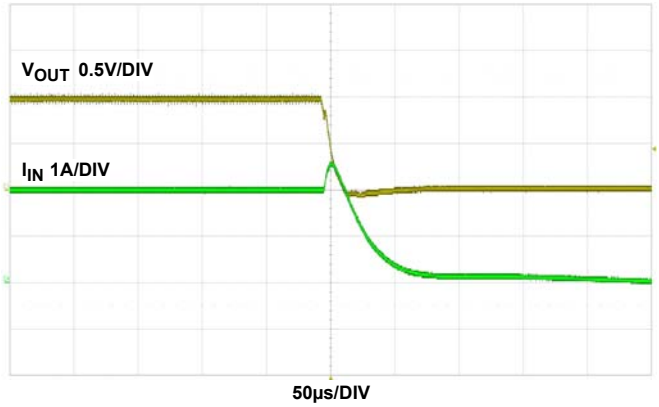
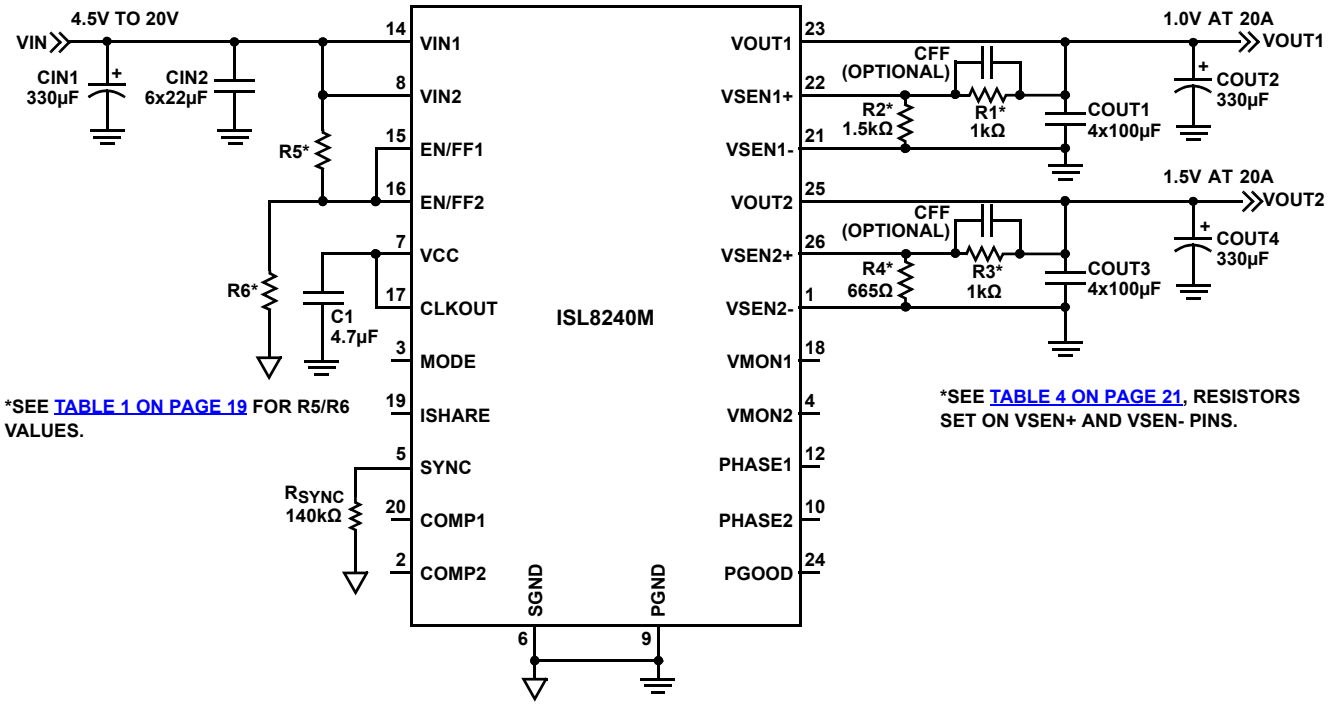


FIGURE 22. SHORT CIRCUIT AT 20A

Typical Application Circuits

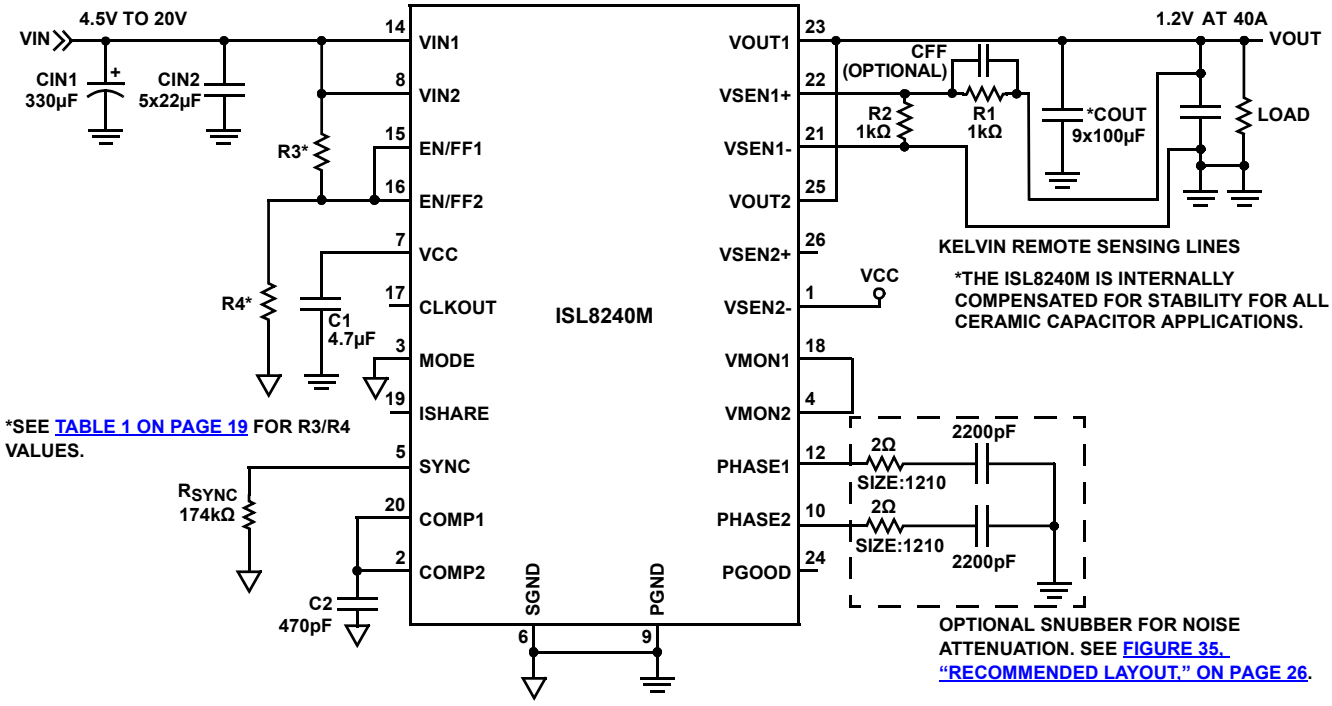


*SEE TABLE 1 ON PAGE 19 FOR R5/R6 VALUES.

*SEE TABLE 4 ON PAGE 21, RESISTORS SET ON VSEN+ AND VSEN- PINS.

SEE "LAYOUT GUIDE" ON PAGE 25 FOR SHORTING SGND TO PGND

FIGURE 23. DUAL OUTPUTS FOR 1.0V/20A AND 1.5V/20A



*SEE TABLE 1 ON PAGE 19 FOR R3/R4 VALUES.

*THE ISL8240M IS INTERNALLY COMPENSATED FOR STABILITY FOR ALL CERAMIC CAPACITOR APPLICATIONS.

OPTIONAL SNUBBER FOR NOISE ATTENUATION. SEE FIGURE 35, "RECOMMENDED LAYOUT," ON PAGE 26.

SEE "LAYOUT GUIDE" ON PAGE 25 FOR SHORTING SGND TO PGND

FIGURE 24. PARALLEL USE FOR SINGLE 1.2V/40A OUTPUT

Typical Application Circuits (Continued)

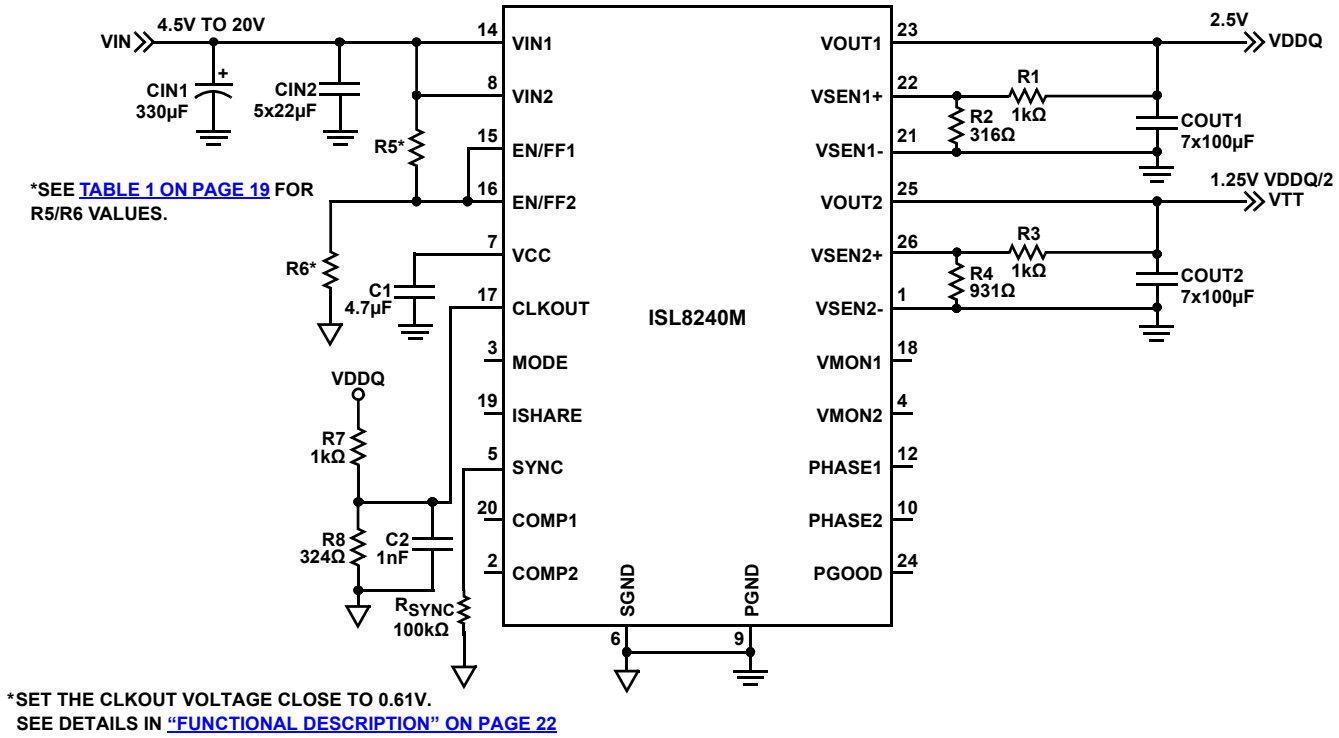


FIGURE 25. DDR/TRACKING USE

Typical Application Circuits (Continued)

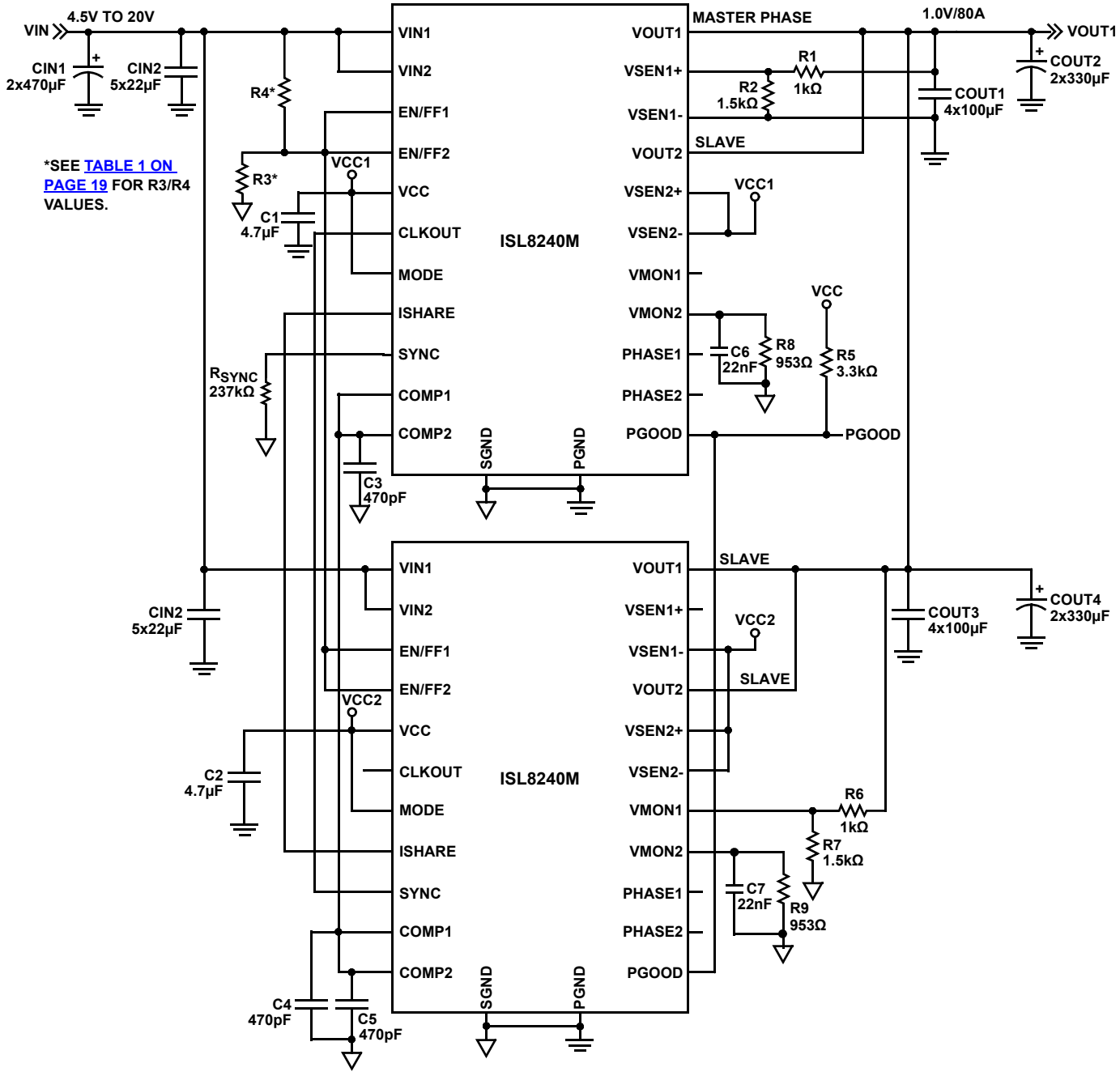


FIGURE 26. 4-PHASE PARALLELED AT 1.0V/80A WITH 90° INTERLEAVING

Typical Application Circuits (Continued)

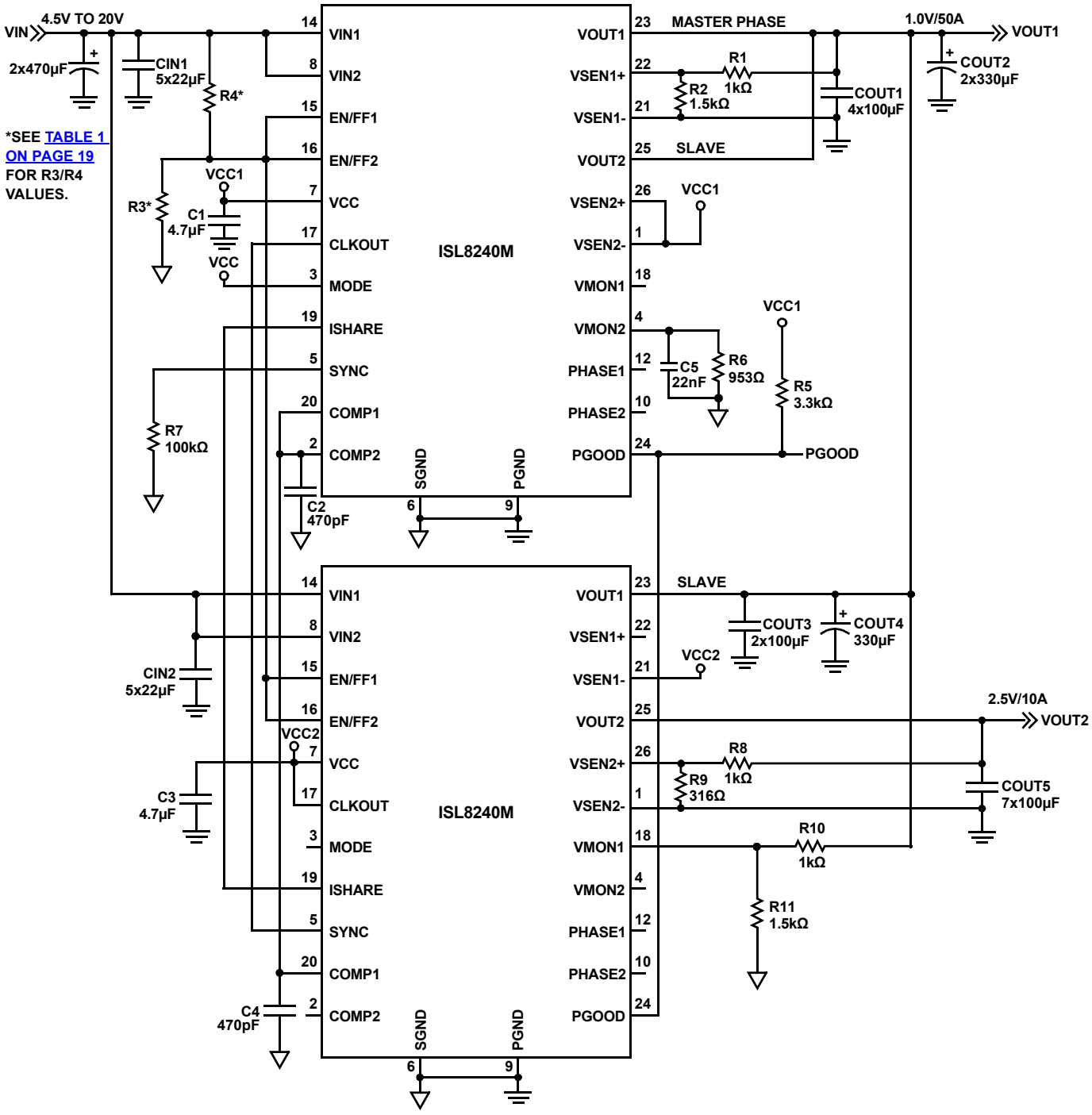


FIGURE 27. 3-PHASE PARALLELED AT 1.0V/50A AND 1-PHASE AT 2.5V/10A OUTPUT WITH 90° INTERLEAVING

Typical Application Circuits (Continued)

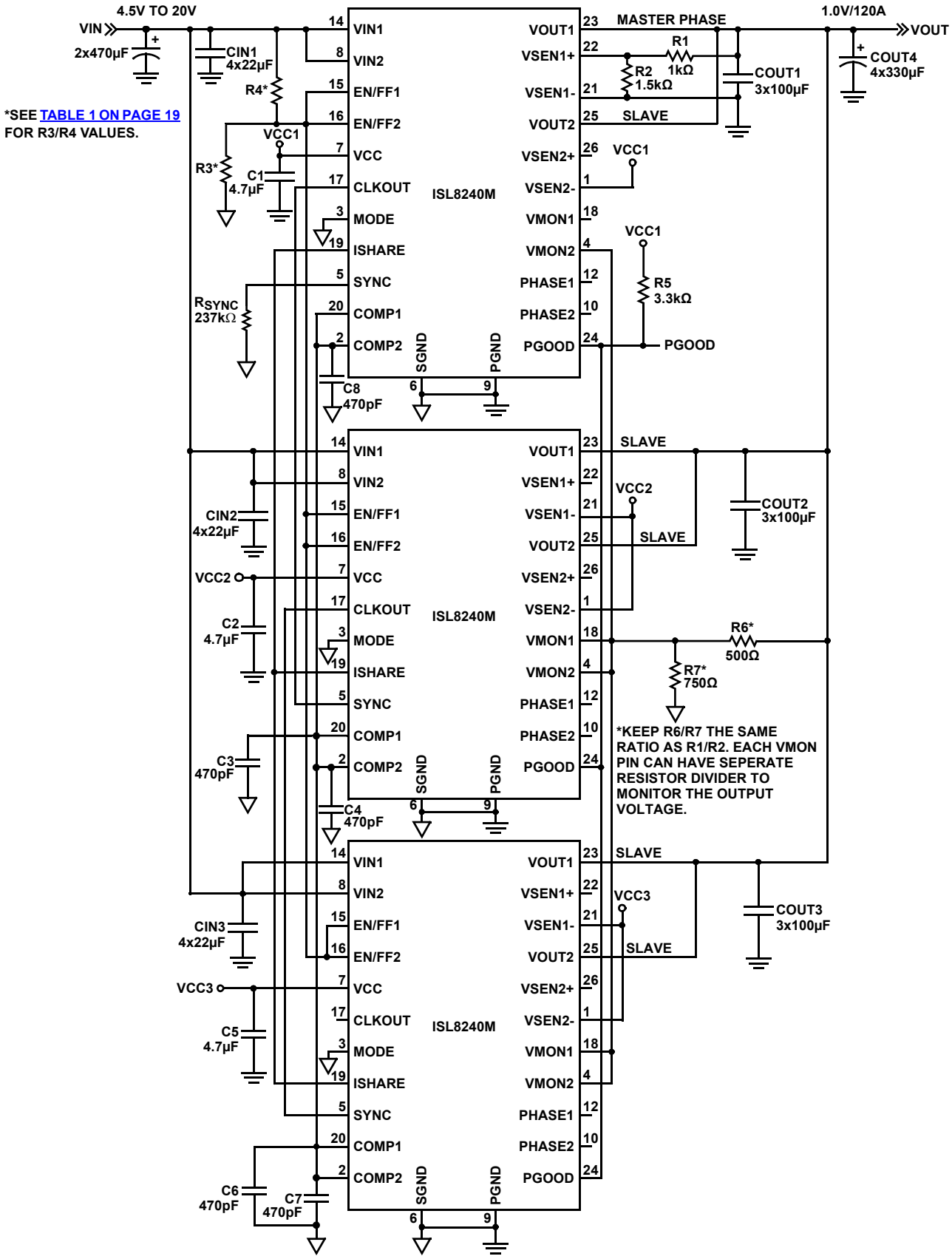


FIGURE 28. SIX-PHASE 120A 1.0V OUTPUT CIRCUIT

TABLE 1. ISL8240M DESIGN GUIDE MATRIX (REFER TO Figure 23)

CASE	V_{IN} (V)	V_{OUT} (V)	R2 or R4 (Ω)	CIN1 (BULK) (µF) (Note 10)	CIN2 (CERAMIC) (µF)	COUT1 (CERAMIC) (µF)	COUT2 (BULK)	CFF (nF)	EN/FF (kΩ) R5/R6 (Note 11)	FREQ. (kHz)	R_{SYNC} (kΩ)	LOAD (A) (Note 12)
1	5	1	1.5k	1x330	1x100	4x100	1x330µF	None	6.04/3.01	500	237	20
2	5	1	1.5k	1x330	1x100	7x100	None	6.8	6.04/3.01	500	237	20
3	12	1	1.5k	1x330	3x22	4x100	1x330µF	None	6.04/1.50	500	237	20
4	12	1	1.5k	1x330	3x22	7x100	None	6.8	6.04/1.50	500	237	20
5	5	1.2	1.0k	1x330	1x100	4x100	1x330µF	None	6.04/3.01	550	174	20
6	5	1.2	1.0k	1x330	1x100	7x100	None	6.8	6.04/3.01	550	174	20
7	12	1.2	1.0k	1x330	3x22	4x100	1x330µF	None	6.04/1.50	550	174	20
8	12	1.2	1.0k	1x330	3x22	7x100	None	6.8	6.04/1.50	550	174	20
9	20	1.2	1.0k	1x330	3x22	4x100	1x330µF	None	6.04/1.50	550	174	19
10	20	1.2	1.0k	1x330	3x22	7x100	None	6.8	6.04/1.50	550	174	19
11	5	1.5	665	1x330	1x100	4x100	1x330µF	None	6.04/3.01	700	100	18
12	5	1.5	665	1x330	1x100	7x100	None	6.8	6.04/3.01	700	100	18
13	12	1.5	665	1x330	3x22	4x100	1x330µF	None	6.04/1.50	600	140	19
14	12	1.5	665	1x330	3x22	7x100	None	6.8	6.04/1.50	600	140	19
15	20	1.5	665	1x330	3x22	4x100	1x330µF	None	6.04/1.50	600	140	18
16	20	1.5	665	1x330	3x22	7x100	None	6.8	6.04/1.50	600	140	18
17	5	2.5	316	1x330	1x100	4x100	1x330µF	None	6.04/3.01	700	100	18
18	5	2.5	316	1x330	1x100	7x100	None	6.8	6.04/3.01	700	100	18
19	12	2.5	316	1x330	3x22	4x100	1x330µF	None	6.04/1.50	700	100	18
20	12	2.5	316	1x330	3x22	7x100	None	6.8	6.04/1.50	700	100	18
21	20	2.5	316	1x330	3x22	4x100	1x330µF	None	6.04/1.50	700	100	16
22	20	2.5	316	1x330	3x22	7x100	None	6.8	6.04/1.50	700	100	16

NOTES:

10. CIN bulk capacitor is optional only for decoupling noise due to the long input cable. CIN2 and COUT1 ceramic capacitors are listed for one phase only. Please increase the capacitor quantity for dual-phase operations.
11. EN/FF resistor divider is tied directly to VIN. The resistors listed here are for two channels' EN/FF pins tied together. If the separate resistor divider is used for each channel, the resistor value needs to be doubled.
12. MAX load current listed in the table is for conditions at +25°C and no air flow on a typical Intersil 4-layer evaluation board.

TABLE 2. RECOMMENDED I/O CAPACITOR IN TABLE 1

VENDOR	VALUE	PART NUMBER
TDK, Input and Output Ceramic	100µF, 6.3V, 1210	C3225X5R0J107M
Murata, Input and Output Ceramic	100µF, 6.3V, 1210	GRM32ER60J107M
AVX, Input and Output Ceramic	100µF, 6.3V, 1210	12106D107MAT2A
Murata, Input Ceramic	22µF, 25V, 1210	GRM32ER61E226KE15L
Taiyo Yuden, Input Ceramic	22µF, 25V, 1210	TMK325BJ226MM-T
AVX, Input Ceramic	22µF, 25V, 1210	12103D226KAT2A
Panasonic POSCAP, Output Bulk	330µF, 6.3V	6TPF330M9L
Panasonic SMT, Input Bulk	330µF, 25V	EEVHA1E331UP

TABLE 3. ISL8240M OPERATION MODES

1ST MODULE (I = INPUT; O = OUTPUT; I/O = INPUT AND OUTPUT, BIDIRECTION)										MODES OF OPERATION		
MODE	EN1/FF1 (I)	EN2/FF2 (I)	VSEN2- (I)	MODE (I)	VSEN2+ (I)	CLKOUT/REFIN WRT 1ST (I OR O)	VMON2 (Note 14)	VMON1 OF 2ND MODULE (Note 14)	2ND CHANNEL WRT 1ST (O) (Note 13)	OPERATION MODE OF 2ND MODULE	OPERATION MODE OF 3RD MODULE	OUTPUT (see Description for details)
1	0	0	-	-	-	-	-	-	-	-	-	Disabled
2A	0	1	Active	Active	Active	-	Active	-	VMON1 = VMON2 to Keep PGOOD Valid	-	-	Single Phase
2B	1	0	-	-	-	-	-	-	VMON1 = VMON2 to Keep PGOOD Valid	-	-	Single Phase
3A	1	1	$<V_{CC}$ -0.7V	Active	Active	29% to 45% of V_{CC} (I)	Active	-	0°	-	-	Dual Regulator
3B	1	1	$<V_{CC}$ -0.7V	Active	Active	45% to 62% of V_{CC} (I)	Active	-	90°	-	-	Dual Regulator
3C	1	1	$<V_{CC}$ -0.7V	Active	Active	>62% of V_{CC} (I)	Active	-	180°	-	-	Dual Regulator
4	1	1	$<V_{CC}$ -0.7V	Active	Active	<29% of V_{CC} (I)	Active	-	-60°	-	-	DDR Mode
5A	1	1	V_{CC}	GND	-	60°	VMON1 or Divider	-	180°	-	-	2-Phase
5B	1	1	V_{CC}	GND	-	60°	Divider	Divider	180°	5B	5B	6-Phase
5C	1	1	V_{CC}	GND	-	60°	VMON1 or Divider	Active	180°	5C	5C	3 Outputs
6	1	1	V_{CC}	V_{CC}	GND	120°	953Ω// 22nF	Active	240°	2B	-	3-Phase
7A	1	1	V_{CC}	V_{CC}	V_{CC}	90°	953Ω// 22nF	Divider	180°	7A	-	4-Phase
7B	1	1	V_{CC}	V_{CC}	V_{CC}	90°	953Ω// 22nF	Active	180°	7B	-	2 Outputs (1st module in Mode 7A)
7C	1	1	V_{CC}	V_{CC}	V_{CC}	90°	953Ω// 22nF	Active	180°	3, 4	-	3 Outputs (1st module in Mode 7A)
8	Cascaded Module Operation MODEs 5B+5B+7A+5B+5B+5B/7A, No External Clock Required											12-Phase
9	External Clock or External Logic Circuits Required for Equal Phase Interval											5, 7, 8, 9, 10, 11, or (PHASE >12)

NOTES:

13. "2ND CHANNEL WRT 1ST" means "second channel with respect to first;" in other words, Channel 2 lags Channel 1 by the degrees specified in this column. For example, 90° means Channel 2 lags Channel 1 by 90°; -60° means Channel 2 leads Channel 1 by 60°.

14. "VMON1" means that the pin is tied to the VMON1 pin of the same module.
"Divider" means that there is a resistor divider from VOUT to SGND; refer to Figure 28.
"953Ω//22nF" means that there is a 953Ω resistor in parallel with a 22nF capacitor connecting the pin to SGND; refer to Figure 26.

Application Information

Programming the Output Voltage

The ISL8240M has an internal 0.6V ±0.7% reference voltage. Programming the output voltage requires a resistor divider (R1 and R2) between the VOUT, VSEN+, and VSEN- pins, as shown in Figure 23 on page 14. Please note that the output voltage accuracy is also dependent on the resistor accuracy of R1 and R2. The user needs to select a high accuracy resistor (i.e., 0.5%) in order to achieve the overall output accuracy. The output voltage can be calculated as shown in Equation 1:

$$V_{OUT} = 0.6 \times \left(1 + \frac{R1}{R2}\right) \quad \text{(EQ. 1)}$$

Note: It is recommended to use a 1kΩ value for the top resistor, R1. The value of the bottom resistor for different output voltages is shown in Table 4.

TABLE 4. VALUE OF BOTTOM RESISTOR FOR DIFFERENT OUTPUT VOLTAGES (V_{OUT} vs R2)

R1 (Ω)	V_{OUT} (V)	R2 (Ω)
1k	0.6	Open
1k	0.8	3.01k
1k	1.0	1.50k
1k	1.2	1.00k
1k	1.5	665
1k	1.8	499
1k	2.0	422
1k	2.5	316

At higher output voltage, the inductor ripple increases, which makes both output ripple and inductor power loss higher. Refer to Figure 34 on page 24 to choose R_{SYNC} which adjusts the switching frequency.

Selection of Input Capacitor

Selection of the input filter capacitor is based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, however, consideration should be given to the higher surge current during power-up. The ISL8240M provides a soft-start function that controls and limits the current surge.

A combination of bulk capacitors and low Equivalent Series Resistance (ESR) ceramic capacitors are recommended as input capacitors. The minimum value of the input ceramic capacitors can be calculated as shown in Equation 2:

$$C_{IN(CER, MIN)} = \frac{I_O \bullet D(1-D)}{V_{P-P} \bullet f_{SW}} \quad \text{(EQ. 2)}$$

where:

- $C_{IN(CER, MIN)}$ is the minimum required input ceramic capacitance (µF)
- I_O is the output current (A)
- D is the duty cycle
- V_{P-P} is the allowable peak-to-peak voltage (V)
- f_{SW} is the switching frequency (Hz)

The low Equivalent Series Resistance (ESR) ceramic capacitance is recommended to decouple between the VIN and PGND of each channel. See Table 2 for some recommended capacitors. This capacitance reduces voltage ringing created by the switching current across parasitic circuit elements. All these ceramic capacitors should be placed as closely as possible to the module pins. The estimated RMS current should be considered in choosing ceramic capacitors.

$$I_{IN(RMS)} = \frac{Io\sqrt{D(1-D)}}{\eta} \quad \text{(EQ. 3)}$$

Each 10µF X5R or X7R ceramic capacitor is typically good for 2A to 3A of RMS ripple current. Refer to the capacitor vendor to check the RMS current ratings. In a typical 15A output application for one channel, if the duty cycle is 0.5, it needs at least three 10µF X5R or X7R ceramic input capacitors.

Selection of Output Capacitors

The ISL8240M is designed for low-output voltage ripple. The output voltage ripple and transient requirements can be met with bulk output capacitors (COUT) that have adequately low ESR. COUT can be a low ESR tantalum capacitor, a low ESR polymer capacitor or a ceramic capacitor. The typical capacitance is 330µF, and decoupling ceramic output capacitors are used for each phase. See Tables 1 and 2 for more capacitor information. Internally optimized loop compensation provides sufficient stability margins for all ceramic capacitor applications, with a recommended total value of 700µF per phase. Additional output filtering may be needed if further reduction of output ripple or dynamic transient spike is required.

EN/FF Turn ON/OFF

Each output of the ISL8240M can be turned on/off independently through the EN/FF pins. For parallel use, tie all EN/FF pins together. Since this pin has the feed-forward function, the voltage on this pin can actively adjust the loop gain to be constant for variable input voltage. Please refer to Table 1 on page 19 to select the resistor divider for commonly used conditions. Otherwise, use the following procedures to finish the EN/FF design:

1. A resistor divider from V_{IN} to GND is recommended to set the EN/FF voltage between 1.25V to 5.0V. The resistor divider ratio is recommended to be between 3/1 to 4/1 with a resistor divider at 7.15kΩ/2.05kΩ.
2. Check EN turn-on hysteresis (recommend V_{EN_HYS} > 0.3V) :

$$V_{EN-HYS} = N \bullet R_{UP} \bullet 3x10^{-5} \quad \text{(EQ. 4)}$$

where:

- R_{UP} is the top resistor of the resistor divider
- N is the total number of the EN/FF pins tied to the resistor divider

3. Set the maximum current flowing through the top pull-up resistor R_{UP} to below 7mA (considering EN/FF is pulled to ground ($V_{EN/FF}$ = 0)). Refer to Figure 27 on page 17; a 3.01kΩ/1kΩ resistor is used to allow for the input voltage from 5V to 20V operation. In addition, the maximum current flowing through R5 is 6.6mA (<7mA).
4. If the EN/FF is controlled by system EN signal instead of the input voltage, we recommend setting the fixed EN/FF voltage to about 1/3.5 of the input voltage. If the input voltage is 12V, a 3.3V system EN signal can be tied to EN/FF pin directly.
5. If the input voltage is below 5.5V, it is recommended to have EN/FF voltage >1.5V to have better stability. The input voltage can be directly tied to the VCC pin to disable the internal LDO.
6. A 1nF capacitor is recommended on the EN/FF pin to avoid the noise injecting into the feed-forward loop.

Thermal Considerations

The ISL8240M QFN package offers typical junction to ambient thermal resistance θ_{JA} of approximately 8.5°C/W at natural convection (~5.0°C/W at 400LFM) with a typical 4-layer PCB. Therefore, use Equation 5 to estimate the module junction temperature:

$$T_{junction} = P \times \Theta_{jA} + T_{ambient} \quad \text{(EQ. 5)}$$

where:

- $T_{junction}$ is the module internal maximum temperature (°C)
- $T_{ambient}$ is the system ambient temperature (°C)
- P is the total power loss of the module package (W)
- θ_{JA} is the thermal resistance of module junction to ambient

If the calculated temperature, $T_{junction}$, is over the required design target, the extra cooling scheme is required. Please refer to "Current Derating" on page 26 for adding air flow.

Functional Description

Initialization

Initially, the Power-On Reset (POR) circuits continuously monitor bias voltages (V_{CC}) and voltage at the EN/FF pin. The POR function initiates soft-start operation 384 clock cycles after: (1) the EN pin voltage is pulled above 0.8V, (2) all input supplies exceed their POR thresholds, and (3) the PLL locking time expires. The Enable pin can be used as a voltage monitor and to set the desired hysteresis, with an internal 30µA sinking current going through an external resistor divider. The sinking current is disengaged after the system is enabled. This feature is specially designed for applications that require higher input rail POR for better undervoltage protection. For example, in 12V applications, R_{UP} = 53.6kΩ and R_{DOWN} = 5.23kΩ sets the turn-on threshold (V_{EN_RTH}) to 10.6V and the turn-off threshold (V_{EN_FTH}) to 9V, with 1.6V hysteresis (V_{EN_HYS}).

During shutdown or fault conditions, soft-start is quickly reset, and the gate driver immediately changes state (<100ns) when input drops below POR.

Enable and Voltage Feed-forward

Voltage applied to the EN/FF pin is fed to adjust the sawtooth amplitude of the channel. Sawtooth amplitude is set to 1.25 times the corresponding FF voltage when the module is enabled. This configuration helps maintain a constant gain. This configuration also helps maintain input voltage to achieve optimum loop response over a wide input voltage range.

A 384-cycle delay is added after the system reaches its rising POR and prior to soft-start. The RC timing at the FF pin should be small enough to ensure that the input bus reaches its static state and that the internal ramp circuitry stabilizes before soft-start. A large RC could cause the internal ramp amplitude not to synchronize with the input bus voltage during output start-up or when recovering from faults. A 1nF capacitor is recommended as a starting value for typical applications.

In a multi-module system, with the EN pins wired together, all modules can immediately turn off, at one time, when a fault condition occurs in one or more modules. A fault pulls the EN pin low, disabling all modules, and does not create current bounce; thus, no single channel is overstressed when a fault occurs.

Because the EN pins are pulled down under fault conditions, the pull-up resistor (R_{UP}) should be scaled to sink no more than 7mA current from the EN pin. Essentially, the EN pins cannot be directly connected to VCC.

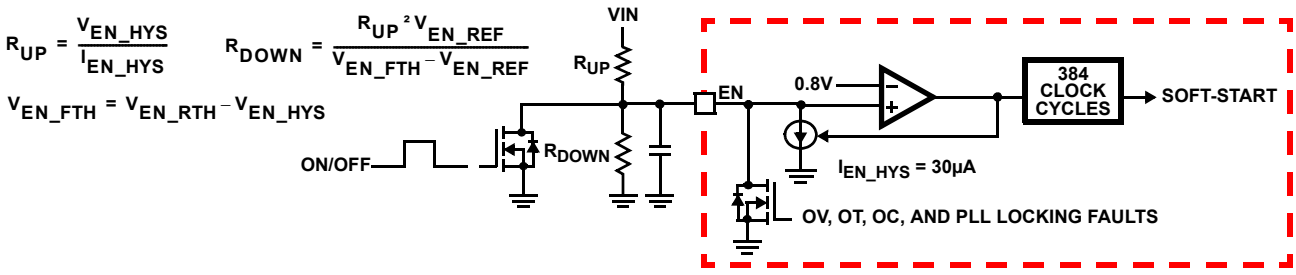


FIGURE 29. SIMPLIFIED ENABLE AND VOLTAGE FEED-FORWARD CIRCUIT

Soft-Start

The ISL8240M has an internal, digital, precharged soft-start circuitry (Figures 30 through 32). The circuitry has a rise time inversely proportional to the switching frequency. Rise time is determined by a digital counter that increments with every pulse of the phase clock. The full soft-start time from 0V to 0.6V can be estimated as shown in Equation 6. The typical soft-start time is ~2.5ms.

$$t_{SS} = \frac{1280}{f_{SW}} \quad \text{(EQ. 6)}$$

The ISL8240M is able to work under a precharged output. The PWM outputs do not feed to the drivers until the first PWM pulse is seen. The low-side MOSFET is on for the first clock cycle, to provide charge for the bootstrap capacitor. If the precharged output voltage is greater than the final target level but less than the 113% set point, switching does not start until the output voltage is reduced to the target voltage and the first PWM pulse is generated. The maximum allowable precharged level is 113%. If the precharged level is above 113% but below 120%, the output hiccups between 113% (LGATE turns on) and 87% (LGATE turns off), while EN is pulled low. If the precharged load voltage is above 120% of the targeted output voltage, then the controller is latched off and cannot power up.

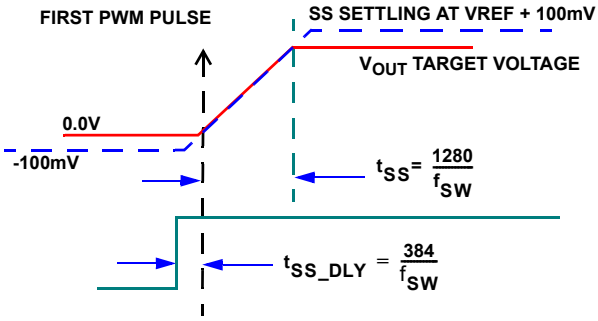


FIGURE 30. SOFT-START WITH V_{OUT} = 0V

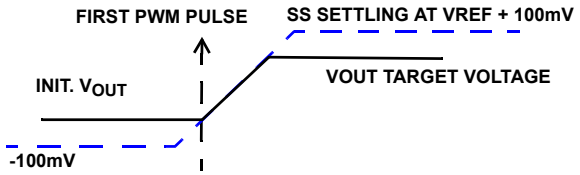


FIGURE 31. SOFT-START WITH V_{OUT} < TARGET VOLTAGE

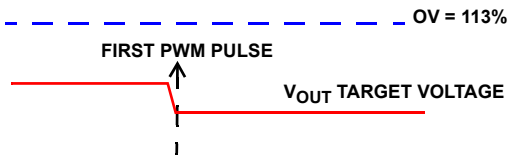
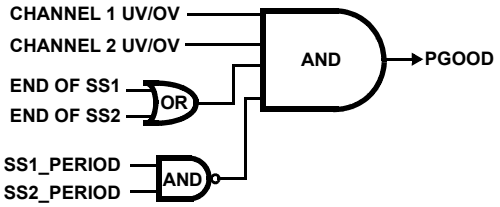


FIGURE 32. SOFT-START WITH V_{OUT} BELOW 113% BUT ABOVE FINAL TARGET VOLTAGE

Power-Good

Power-good comparators monitor voltage on the VMON pin. Trip points are shown in Figure 33. PGOOD is not asserted until the soft-start cycle is complete. PGOOD pulls low upon both ENs disabling it or when the VMON voltage is out of the threshold window. PGOOD does not pull low until the fault presents for three consecutive clock cycles.

UV indication is not enabled until the end of soft-start. In a UV event, if the output drops below -13% of the target level due to a reason other than OV, OC, OT, or PLL faults (cases when EN is not pulled low), PGOOD is pulled low.



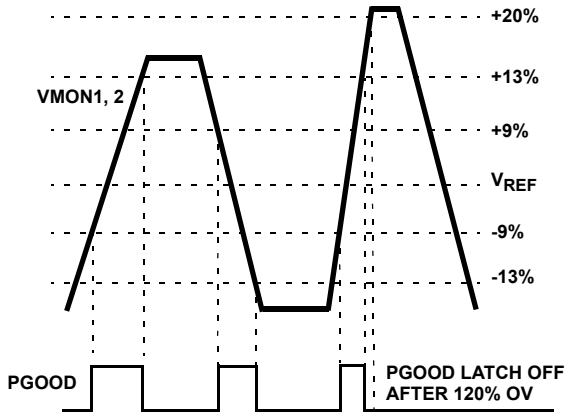


FIGURE 33. POWER-GOOD THRESHOLD WINDOW

Current Share

In parallel operations, the share bus voltages (I_{SHARE}) of different modules must tie together. The ISHARE pin voltage is set by an internal resistor and represents the average current of all active modules. The average current signal is compared with the local module current, and the current share error signal is fed into the current correction block to adjust each module's PWM pulse accordingly. The current share function provides at least 10% overall accuracy between modules. The current share bus works for up to 12 phases without requiring an external clock. A 470pF ~1nF capacitor is recommended for each ISHARE pin.

In current sharing scheme, all slave channels have the feedback loops disabled with the VSEN- pin tied to VCC. The master channel can control all modules with COMP and ISHARE pins tied together. For phase-shift setting, all VMON pins of slave channels are needed to set 0.6V for monitoring use only. Typically, the slaved VMON pins can be tied together with a resistor divider to VOUT. However, if the MODE pin is tied to VCC for mode setting, the related VMON2 pin is needed to tie to SGND with a 953Ω resistor and a 22nF capacitor, as shown in Figure 27 on page 17.

If there are multiple modules paralleled with the MODE pins tied to VCC, each VMON2 pin of the slave modules needs to have a 953Ω resistor to GND while all VMON1 pins of the slave modules can be tied together with a resistor divider from VOUT to GND, as shown in Figure 28 on page 18. Also see Table 3 on page 20 for VMON settings.

Because of the typical 5.4V VCC and the internal 7.5kΩ resistor between MODE pin and VMON2 pin, the 953Ω resistor maintains VMON2 pin voltage close to 0.6V, thus output OVP/UVP (caused by VMON2 voltage too high or too low) will not be falsely triggered due to part to part variation at mass production. The 22nF capacitor is used to avoid output UVP/OVP triggered during input start-up.

Overvoltage Protection (OVP)

The overvoltage (OV) protection indication circuitry monitors voltage on the VMON pin. OV protection is active from the beginning of soft-start. An OV condition (>120%) would latch the IC off. In this condition, the high-side MOSFET (Q1 or Q3) latches off permanently. The low-side MOSFET (Q2 or Q4) turns on immediately at the time of OV trip and then turns off permanently after the output voltage drops below 87%. EN and PGOOD are also latched low in an OV event. The latch condition can be reset only by recycling V_{CC}.

There is another non-latch OV protection (113% of target level). When EN is low and output is over 113% OV, the low-side MOSFET turns on until output drops below 87%. This action protects the power trains when even a single channel of a multi-module system detects OV. The low-side MOSFET always turns on when EN = LOW and the output voltage rises above 113% (all EN pins are tied together) and turns off after the output drops below 87%. Thus, in a high phase count application (multi-module mode), all cascaded modules can latch off simultaneously via the EN pins (EN pins are tied together in multi-phase mode). Each channel shares the same sink current to reduce stress and eliminate bouncing among phases.

Over-Temperature Protection (OTP)

When the junction temperature of the internal controller is greater than +150°C (typically), the EN pin is pulled low to inform other cascaded channels via their EN pins. All connected ENs stay low and then release after the module's junction temperature drops below +125°C (typically), a +25°C hysteresis (typically).

Overcurrent Protection (OCP)

The OCP maximum load current level is set to about 24A for each channel, but the OC trip point can vary, due mainly to MOSFET $r_{DS(ON)}$ variations (over process, current, and temperature). The OCP can be increased by increasing the switching frequency since the inductor ripple is reduced. However, the module efficiency drops accordingly with more switching loss. When OCP is triggered, the controller pulls EN low immediately to turn off all switches. The OCP function is enabled at start-up and has a 7-cycle delay before it triggers.

In multi-module operation, ISHARE pins can be connected to create V_{ISHARE}, which represents the average current of all active channels. Total system currents are compared with a precision threshold to determine the overcurrent condition. Each channel also has an additional overcurrent set point with a 7-cycle delay. This scheme helps protect modules from damage in multi-module mode by having each module carry less current than the set point.

For overload and hard short conditions, overcurrent protection reduces the regulator RMS output current to much less than full load by putting the controller into hiccup mode. A delay equal to three soft-start intervals is entered to allow time to clear the disturbance. After the delay time, the controller initiates a soft-start interval. If the output voltage comes up and returns to regulation, PGOOD transitions high. If the OC trip is exceeded during the soft-start interval, the controller pulls EN low again. The PGOOD signal remains low, and the soft-start interval is allowed to expire. Another soft-start interval is initiated after the delay interval. If an overcurrent trip occurs again, this same cycle repeats until the fault is removed. Since the output voltage may trigger the OVP if the output current changes too fast, the module can go into latch-off mode. In this case, the module needs to be restarted.

Frequency Synchronization and Phase Lock Loop

The SYNC pin has two primary capabilities: fixed frequency operation and synchronized frequency operation. The ISL8240M has an internally set fixed frequency of 350kHz. By tying a resistor (R_{SYNC}) to SGND from the SYNC pin, the switching frequency can be set to higher than 350kHz. To increase the switching frequency, select an externally connected resistor, R_{SYNC}, from SYNC to SGND according to the frequency setting curve shown in Figure 34. See Table 1 on page 19 for R_{SYNC} at commonly used frequency.

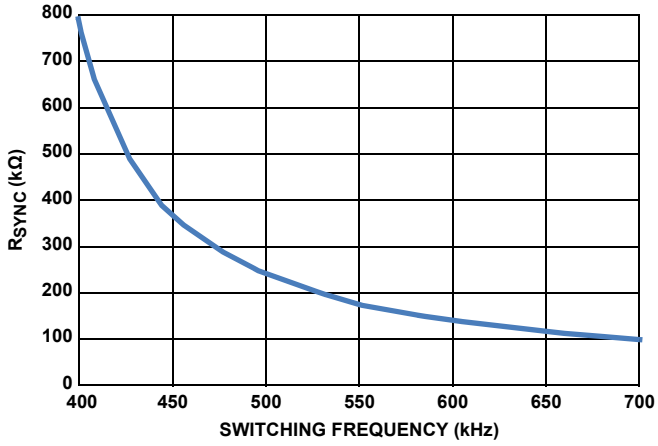


FIGURE 34. R_{SYNC} vs SWITCHING FREQUENCY

Connecting the SYNC pin to an external square-pulse waveform (such as the CLKOUT signal, typically 50% duty cycle from another ISL8240M) synchronizes the ISL8240M switching frequency to the fundamental frequency of the input waveform. The synchronized frequency can be from 350kHz to 700kHz. The applied square-pulse recommended high level voltage range is 3V to V_{CC}+0.3V. The frequency synchronization feature synchronizes the leading edge of the CLKOUT signal with the falling edge of Channel 1's PWM signal. CLKOUT is not available until PLL locks. No capacitor is recommended on the SYNC pin.

For 18A or less load current (or 36A for parallel single output configuration), the ISL8240M's efficiency can be improved by adjusting the switching frequency. Please refer to Figures 4, 6, 8 and 10 for the efficiency at different switching frequencies at various output voltages. For higher than 18A load current (or 36A for parallel single output configuration), please refer to Table 1 on page 19 for the recommended switching frequencies for various conditions

Locking time is typically 130µs for f_{SW} = 500kHz. EN is not released for a soft-start cycle until SYNC is stabilized and PLL is locking. Connecting all EN pins together in a multiphase configuration is recommended.

Loss of a synchronization signal for 13 clock cycles causes the module to be disabled until PLL returns locking, at which point a soft-start cycle is initiated and normal operation resumes. Holding SYNC low disables the module. **Please note that the quick change of the synchronization signal can cause module shutdown.**

Tracking Function

If CLKOUT is less than 800mV, an external soft-start ramp (0.6V) can be in parallel with the Channel 2 internal soft-start ramp for tracking applications. Therefore, the output voltage of Channel 2 can track the output voltage of Channel 1.

The tracking function can be applied to a typical Double Data Rate (DDR) memory application, as shown in Figure 25 on page 15. The output voltage (typical VTT output) of Channel 2 tracks with the input voltage [typical VDDQ/(1+k) from Channel 1] at the CLKOUT pin. As for the external input signal and the internal reference signal (ramp and 0.6V), the one with the lowest voltage is used as the reference for comparing with the FB signal. In DDR configuration, VTT channel should start up later, after its internal soft-start ramp, such that VTT tracks the voltage on the CLKOUT pin derived from VDDQ. This configuration can be achieved by adding more filtering at EN/FF1 than at EN/FF2.

It is recommended to scale the target CLKOUT voltage to 0.612V (2% above 0.6V reference) with an external resistor divider from VDDQ. After start-up, the internal reference takes over to maintain the good regulation of VTT.

The resistor divider ratio k of R7/R8 in Figure 20 is based on the feedback divider of VDDQ (R1 and R2 values) and the 0.612V target CLKOUT voltage as shown in Equation 7:

$$k = \frac{R7}{R8} = \frac{(1 + R1/R2)}{1.02} - 1 \quad \text{(EQ. 7)}$$

Mode Programming

ISL8240M can be programmed for dual-output, paralleled single-output or mixed outputs (Channel 1 in parallel and Channel 2 in dual-output). With multiple ISL8240Ms, up to 6 modules using its internal cascaded clock signal control, the modules can supply large current up to 240A. For complete operation, please refer to Table 3 on page 20. Commonly used settings are listed in Table 5.

TABLE 5. PHASE-SHIFT SETTING

OPERATION	PHASE-SHIFT BETWEEN PHASES	VSEN2-	VSEN2+	CLKOUT	MODE
Dual Output (Figure 23)	180°	N/C	N/C	VCC	N/C
40A (Figure 24)	180°	VCC	N/C	N/C	SGND
80A (Figure 26)	90°	VCC	VCC	N/C	VCC
120A (Figure 28)	60°	VCC	N/C	N/C	SGND

When the module is in the dual-output condition, depending upon the voltage level at CLKOUT (which is set by the VCC resistor divider output), ISL8240M operates with phase shifted as the CLKOUT voltage shown in Table 6. The phase shift is latched as V_{CC} rises above POR; it cannot be changed on the fly.

TABLE 6. CLKOUT TO PROGRAM PHASE SHIFT AT DUAL-OUTPUT

CLKOUT VOLTAGE SETTING	PHASE FOR CLKOUT WRT CHANNEL 1	RECOMMENDED CLKOUT VOLTAGE
<29% of V_{CC}	-60°	15% V_{CC}
29% to 45% of V_{CC}	0°	37% V_{CC}
45% to 62% of V_{CC}	90°	53% V_{CC}
62% of V_{CC}	180°	V_{CC}

Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary (Figure 35).

- VOUT1, VOUT2, PHASE1, PHASE2, PGND, VIN1 and VIN2 should have large, solid planes. Place enough thermal vias to connect the power planes in different layers under or around the module.
- Place high-frequency ceramic capacitors between VIN, VOUT, and PGND, as closely to the module as possible in order to minimize high-frequency noise.
- Use remote sensed traces to the regulation point to achieve tight output voltage regulation, and keep the sensing traces close to each other in parallel.
- PHASE1 and PHASE2 pads are switching nodes that generate switching noise. Keep these pads under the module. For noise-sensitive applications, it is recommended to keep phase pads only on the top and inner layers of the PCB. Also, do not place phase pads exposed to the outside on the bottom layer of the PCB.
- Avoid routing any noise-sensitive signal traces, such as the VSEN+, VSEN-, ISHARE, COMP and VMON sensing points, near the PHASE pins.
- Use a separated SGND ground copper area for components connected to signal ground pins. Connect SGND to PGND with multiple vias underneath the unit in one location to avoid the noise coupling, as shown in Figure 35. Don't ground vias surrounded by the noisy planes of VIN, PHASE and VOUT. For dual output applications, the SGND to PGND vias are preferred to be as close as possible to SGND pin.

- Optional snubbers can be put on the bottom side of the board layout, connecting the PHASE to PGND planes, as shown in Figure 35.

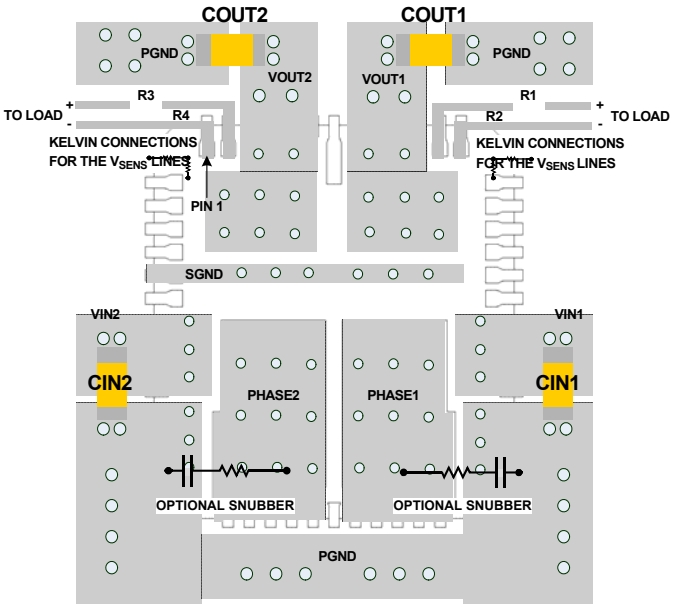


FIGURE 35. RECOMMENDED LAYOUT

Current Derating

Experimental power loss curves (Figures 36 and 37), along with θ_{JA} from thermal modeling analysis, can be used to evaluate the thermal consideration for the module. Derating curves are derived from the maximum power allowed while maintaining temperature below the maximum junction temperature of +120°C (Figures 38 through 43). The maximum +120°C junction temperature is considered for the module to load the current consistently and it provides the 5°C margin of safety from the rated junction temperature of +125°C. If necessary, customers can adjust the margin of safety according to the real applications. All derating curves are obtained from the tests on the ISL8240MEVAL4Z evaluation board. In the actual application, other heat sources and design margins should be considered.

Package Description

The ISL8240M is integrated into a quad flat no-lead package (QFN). This package has such advantages as good thermal and electrical conductivity, low weight, and small size. The QFN package is applicable for surface mounting technology and is becoming more common in the industry. The ISL8240M contains several types of devices, including resistors, capacitors, inductors, and control ICs. The ISL8240M is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi-component assembly are over-molded with polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern, and typical stencil pattern design are shown in the L26.17x17 package outline drawing on page 31. Figure 44 shows typical reflow profile parameters. These guidelines are general design rules. Users can modify parameters according to specific applications.

PCB Layout Pattern Design

The bottom of ISL8240M is a lead-frame footprint, which is attached to the PCB by surface mounting. The PCB layout pattern is shown in the L26.17x17 package outline drawing on page 31. The PCB layout pattern is essentially 1:1 with the QFN exposed pad and the I/O termination dimensions, except that the PCB lands are slightly longer than the QFN terminations by about 0.2mm (0.4mm max). This extension allows for solder filleting around the package periphery and ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

Thermal Vias

A grid of 1.0mm to 1.2mm pitched thermal vias, which drops down and connects to buried copper planes, should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 2.0 ounce copper. Although adding more vias (by decreasing pitch) improves thermal performance, it also diminishes results as more vias are added. Use only as many vias as are needed for the thermal land size and as your board design rules allow.

Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. The stencil aperture size to land size ratio should typically be 1:1. Aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands.

To reduce solder paste volume on the larger thermal lands, an array of smaller apertures instead of one large aperture is recommended. The stencil printing area should cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown in the L26.17x17 package outline drawing on page 31. The gap width between pads is 0.6mm. Consider the symmetry of the whole stencil pattern when designing the pads.

A laser-cut, stainless-steel stencil with electropolished trapezoidal walls is recommended. Electropolishing smooths the aperture walls, resulting in reduced surface friction and better paste release, which reduces voids. Using a trapezoidal section aperture (TSA) also promotes paste release and forms a brick-like paste deposit, which assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large-pitch (1.0mm) QFN.

Power Loss Curves

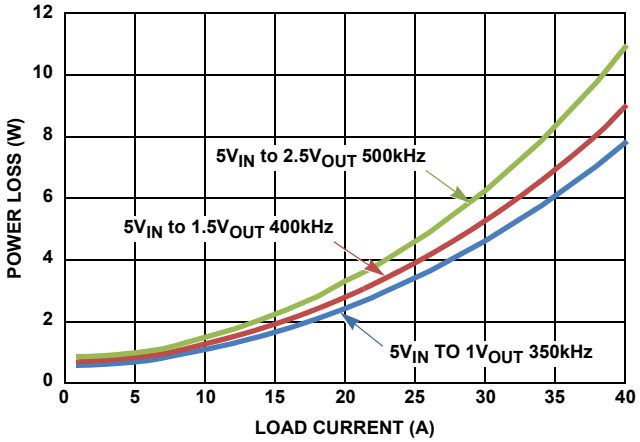


FIGURE 36. POWER LOSS CURVES OF $5V_{IN}$

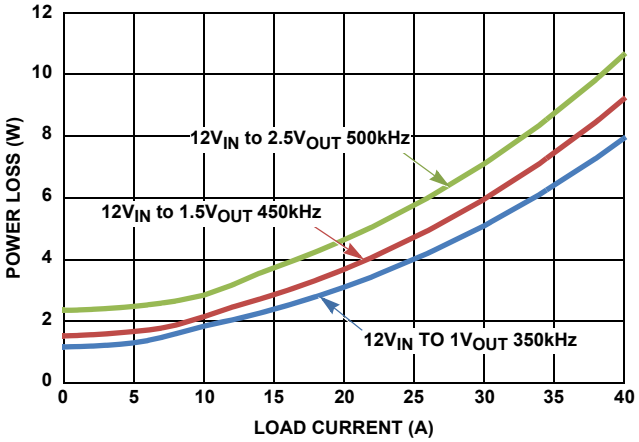


FIGURE 37. POWER LOSS CURVES OF $12V_{IN}$

Derating Curves

All of the following curves were plotted at T_J = +120°C.

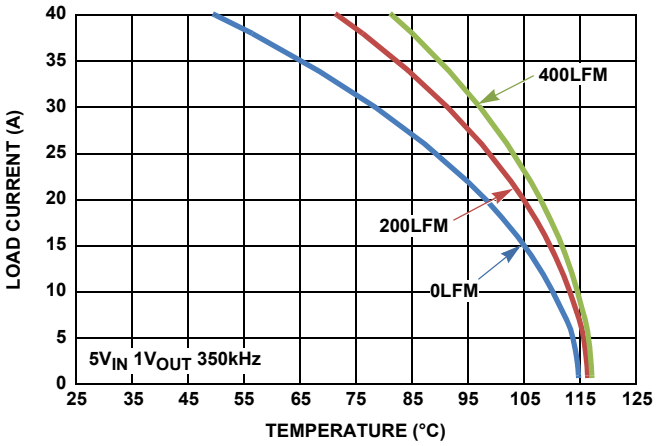


FIGURE 38. DERATING CURVE $5V_{IN}$ TO $1V_{OUT}$

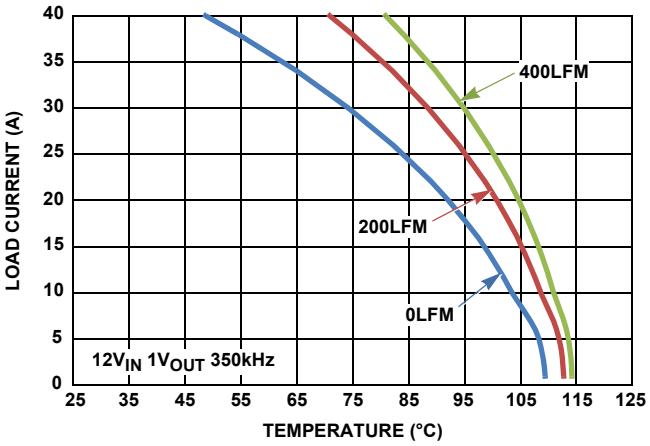


FIGURE 39. DERATING CURVE $12V_{IN}$ TO $1V_{OUT}$

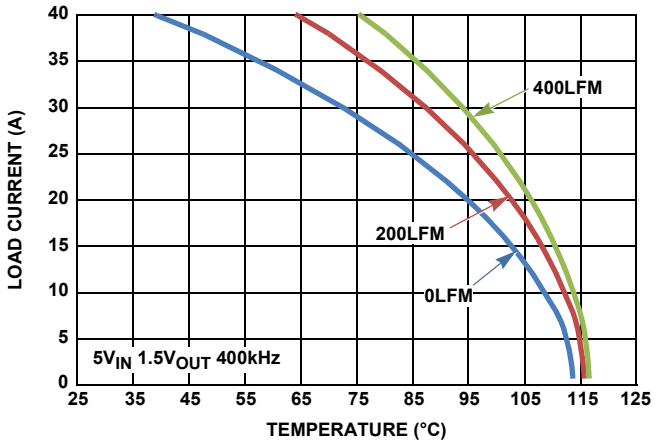


FIGURE 40. DERATING CURVE $5V_{IN}$ TO $1.5V_{OUT}$

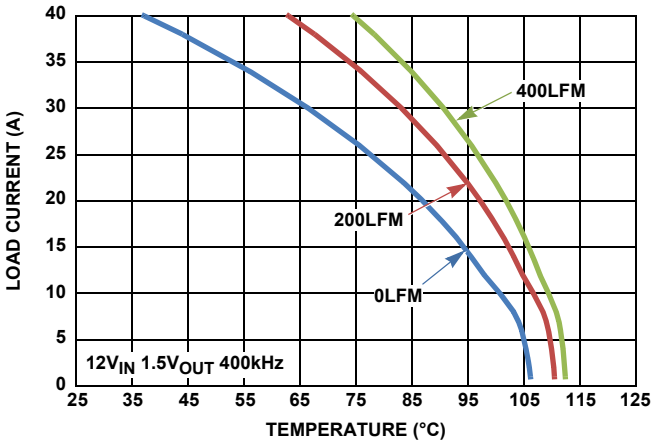


FIGURE 41. DERATING CURVE $12V_{IN}$ TO $1.5V_{OUT}$

Derating Curves

All of the following curves were plotted at T_J = +120°C. **(Continued)**

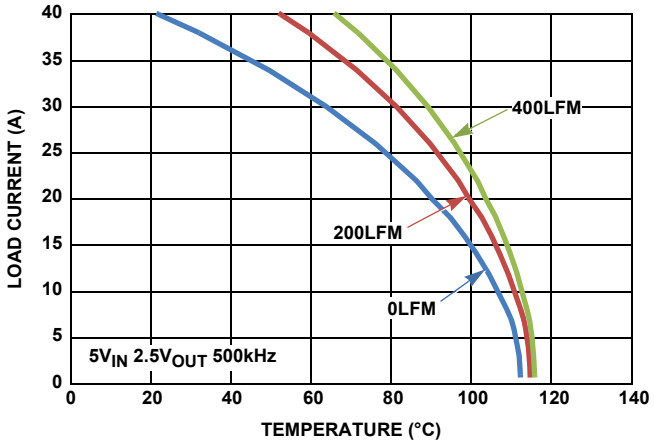


FIGURE 42. DERATING CURVE $5V_{IN}$ TO $2.5V_{OUT}$

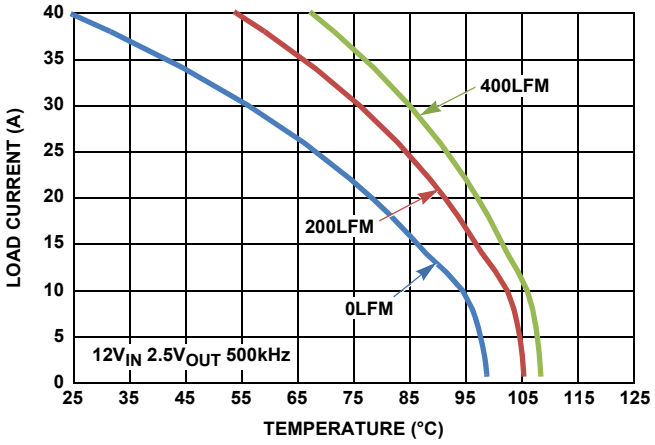


FIGURE 43. DERATING CURVE $12V_{IN}$ TO $2.5V_{OUT}$

Reflow Parameters

Due to the low mount height of the QFN, "No Clean" Type 3 solder paste, per ANSI/J-STD-005, is recommended. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the QFN. The profile given in Figure 44 is provided as a guideline to customize for varying manufacturing practices and applications.

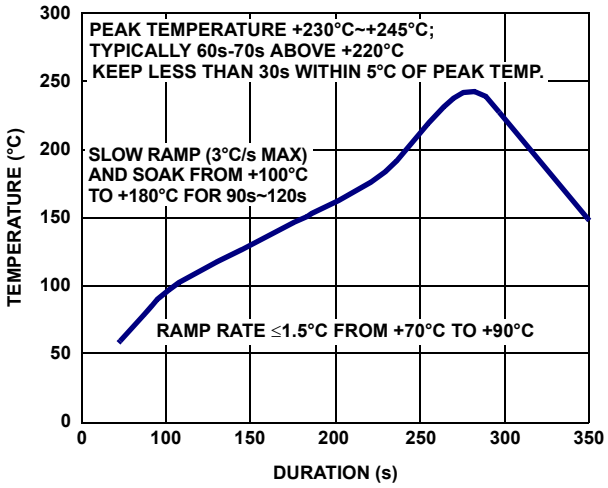


FIGURE 44. TYPICAL REFLOW PROFILE

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Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
January 7, 2015	FN8450.2	On page 7, Electrical Specifications table, Vcc voltage level updated min from 5.15V to 5.1V and max from 5.95V to 5.6V. On page 8, Electrical Specifications table, VREF1 and VREF2, added absolute values for MIN and MAX corresponding to the percentages. On page 16, Figure 26, R8 value changed from 1kΩ to 953Ω, added a capacitor C6, value of 22nF, in parallel with R8, R9 value changed from 1kΩ to 953Ω, added a capacitor C7, value of 22nF, in parallel with R9. On page 17, Figure 27, R6 value changed from 1kΩ to 953Ω, added a capacitor C5, value of 22nF, in parallel with R6. On page 20, Table 3, updated VMON2 from 1kΩ to "953Ω//22nF" for MODE 6, MODE 7A, MODE 7B, and MODE 7C. On page 20, Note 14, changed the sentence "1kΩ means..." to "953Ω//22nF" means that there are a 953Ω resistor in parallel with a 22nF capacitor connecting the pin to SGND; refer to Figure 26. On page 23, Current Share; 2nd paragraph, changed the text "with a 1.0kΩ resistor" to "with a 953Ω resistor and a 22nF capacitor". On page 24, "Current share" 2nd paragraph, changed "1kΩ" to "953Ω"; added a new paragraph "Because of the typical 5.4V VCC and the internal 7.5kΩ resistor between MODE pin and VMON2 pin, the 953Ω resistor maintains VMON2 pin voltage close to 0.6V, thus output OVP/UVP (caused by VMON2 voltage too high or too low) will not be falsely triggered due to part to part variation at mass production. The 22nF capacitor is used to avoid output UVP/OVP triggered during input start-up." On page 25, "Tracking Function", 2nd paragraph, changed "VDDQ*(1+k)" to "VDDQ/(1+k)"; updated the 3rd paragraph "It is recommended to scale the target CLKOUT voltage to 0.612V (2% above 0.6V reference) with an external resistor divider from VDDQ. After start-up, the internal reference takes over to maintain the good regulation of VTT. The resistor divider ratio k of R7/R8 in Figure 20 is based on the feedback divider of VDDQ (R1 and R2 values) and the 0.612V target CLKOUT voltage as shown in Equation 7:"; updated Equation 7.
May 23, 2014	FN8450.1	Replaced Figures 3 through 9 with figures showing efficiency up to a switching speed of 700kHz. Figure 1 on page 1: added SYNC pin and RSYNC resistor of 237kΩ. Electrical Specifications Table, "Synchronization Frequency" on page 8, changed MAX from 500kHz to 700kHz. Figure 23 on page 14: added RSYNC resistor of 140kΩ. Figure 24 on page 14: added RSYNC resistor of 174kΩ. Figure 25 on page 15: added RSYNC resistor of 100kΩ. Figure 26 on page 16: added RSYNC resistor of 237kΩ. Figure 28 on page 18: added RSYNC resistor of 237kΩ. Table 1 on page 19: updated the three columns of FREQ., RSYNC, LOAD, to give more accurate information about optimum settings. Figure 34 on page 24: updated the graph to include a wider switching frequency range. "Frequency Synchronization and Phase Lock Loop" on page 24: changed "The synchronized frequency can be from 350kHz to 500kHz" to "The synchronized frequency can be from 350kHz to 700kHz".
March 12, 2014	FN8450.0	Initial Release

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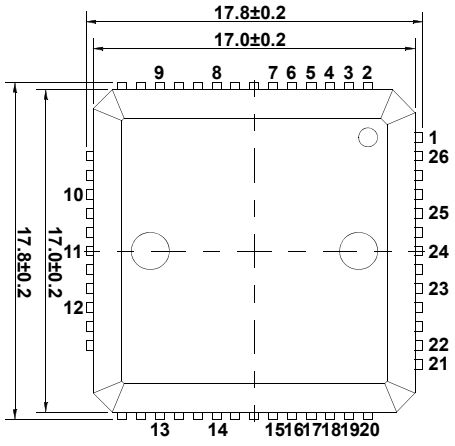
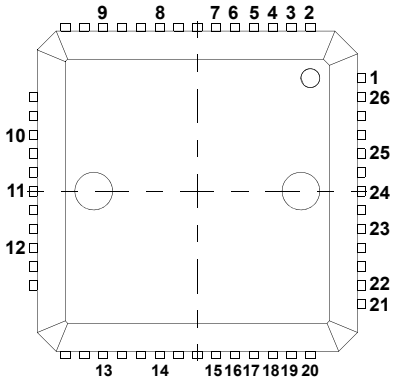
Package Outline Drawing

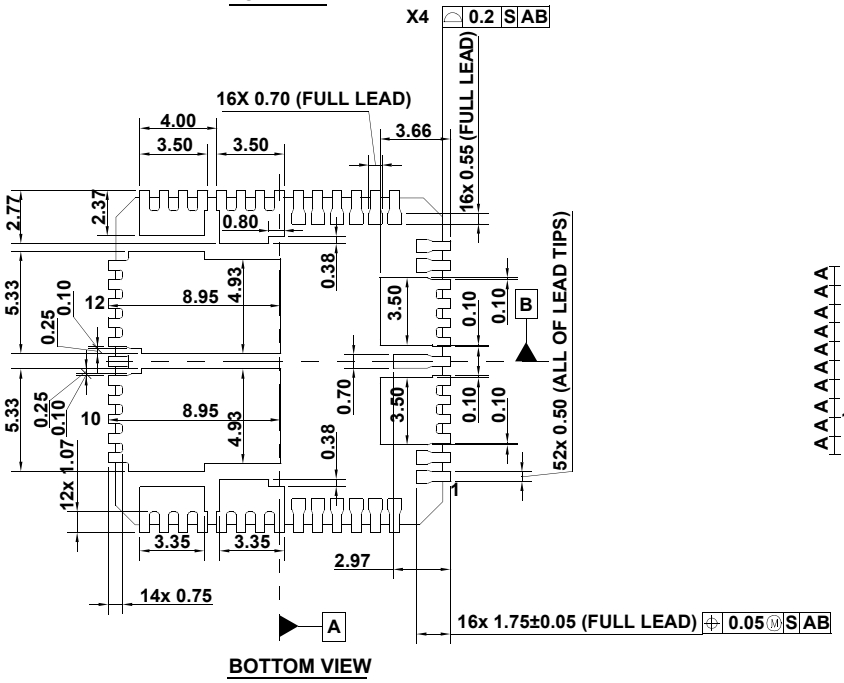
L26.17x17

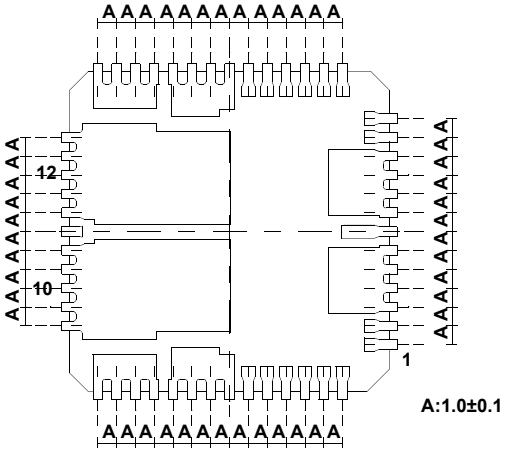
26 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (PUNCH QFN)

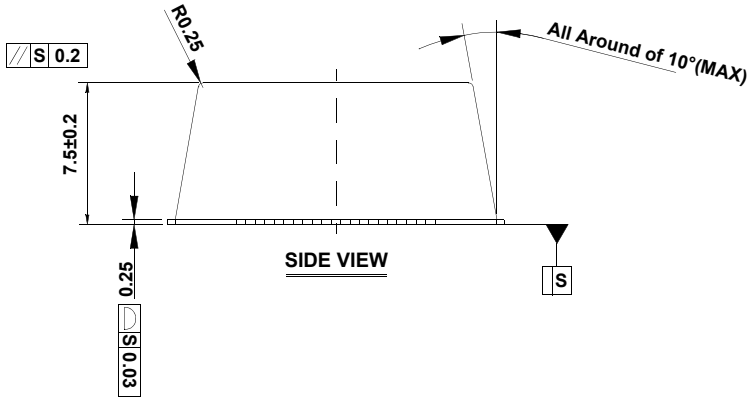
Rev 4, 10/12

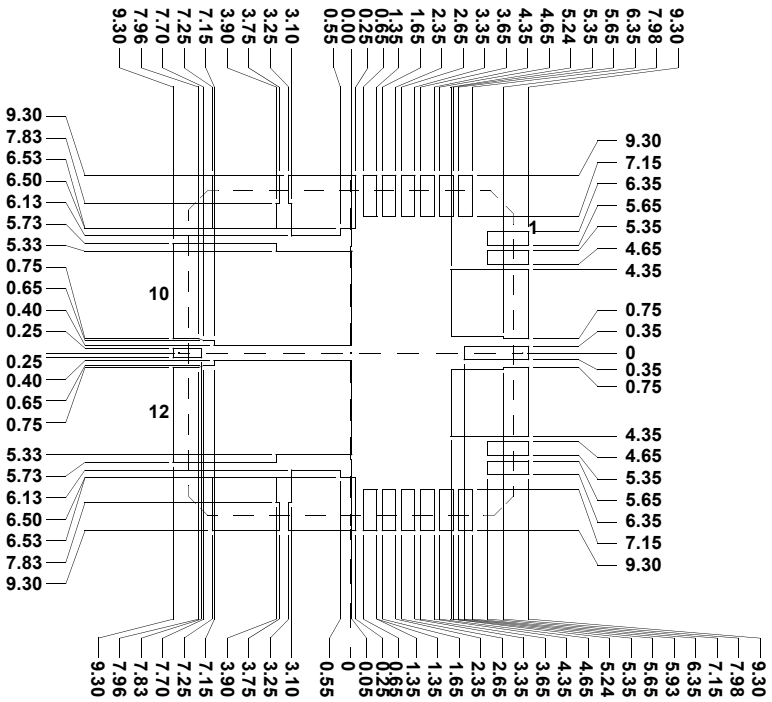




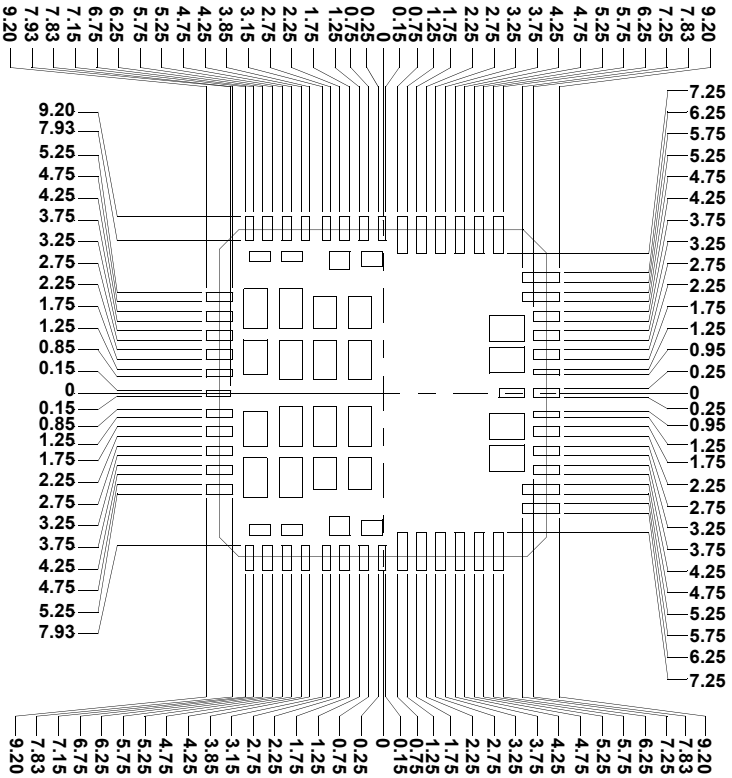




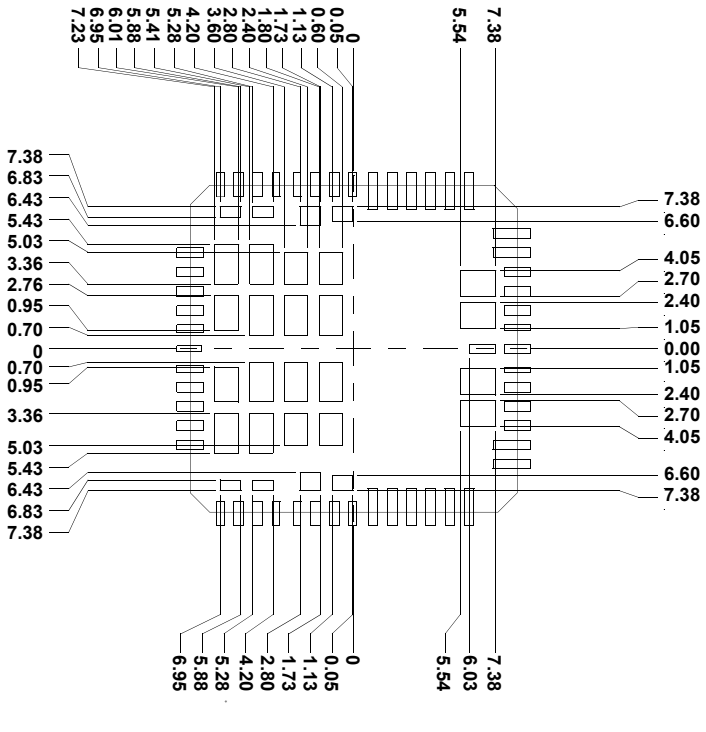




TYPICAL RECOMMENDED LAND PATTERN (TOP VIEW)



SOLDER STENCIL PATTERN WITH SQUARE PADS 1 OF 2 (TOP VIEW)



SOLDER STENCIL PATTERN WITH SQUARE PADS 2 OF 2 (TOP VIEW)

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