THE DATASHEET OF

LM3209TLE-G3/NOPB

LM3209-G3 Seamless-Transition Buck-Boost Converter for Battery-Powered 3G/4G RF Power Amplifiers

Check for Samples: LM3209-G3

FEATURES

- **Operates From a Single Li-Ion Cell: 2.7V to 5.5V**
- **Adjustable Output Voltage: 0.6V to 4.2V**
- **1A Maximum Load Capability for V_{IN} ≥ 3.2V, V_{OUT} = 3.6V**
- **2.4 MHz (typ.) Switching Frequency**
- **Seamless Buck-Boost Mode Transition**
- **Fast Output Voltage Transition: 0.8V to 4.0V in 20 µs**
- **High-Efficiency: 95% typ. at 3.7 V_{IN}, 3.5 V_{OUT}, at 300 mA**
- **Cycle-by-cycle Over-Current Limit**
- **Output Over-Voltage Clamp**
- **Internal Compensation**
- **12-bump DSBGA Package**

APPLICATIONS

- **Battery-Powered 3G/4G RF PAs**
- **Cellular Phones**
- **Portable Hard Disk Drives**
- **PDAs**

DESCRIPTION

The LM3209-G3 is buck-boost DC/DC converter designed to generate output voltages above or below a given input voltage. It is particularly suitable for single-cell Li-ion batteries for portable applications.

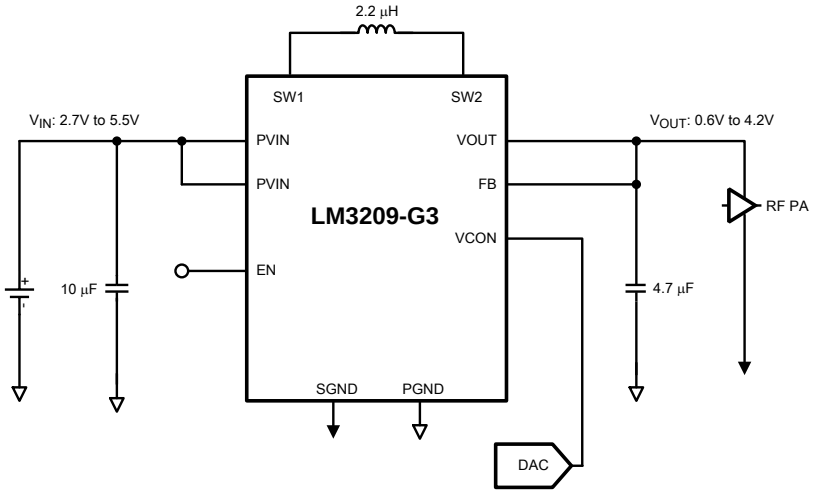
The LM3209-G3 operates at a 2.4 MHz typical switching frequency in full synchronous operation providing seamless transitions between buck and boost operating modes.

The power converter topology needs only one external inductor and two capacitors. Five internal power switches enable high overall efficiency.

The LM3209-G3 is internally compensated for buck and boost modes of operation, thus providing an optimal transient response.

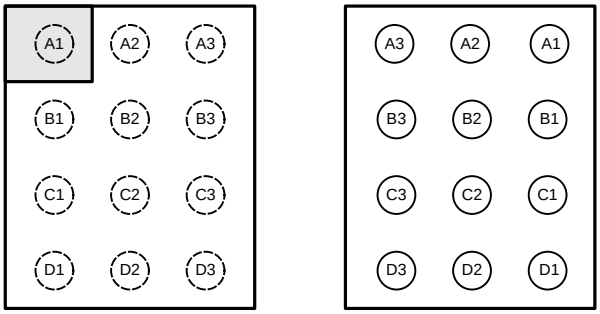
The LM3209-G3 is available in an 12-bump lead-free DSBGA package of size 2.0 mm x 2.5 mm x 0.6 mm.

TYPICAL APPLICATION CIRCUIT



CONNECTION DIAGRAMS AND PACKAGE MARK INFORMATION

Figure 1. 12–Bump Thin DSBGA Package, Large Bump



Top View Bottom View

PIN DESCRIPTIONS

Pin #	Name	Description
A1	NC	This pin is shorted to ground internally. Leave this pin floating.
B1	VCON	Output voltage program pin. Analog voltage from DAC/controller to set VOUT.
C1	FB	Feedback input to inverting input of error amplifier. Connect output voltage directly to this node at load point.
D1	VOUT	Regulated output voltage of LM3209-G3. Connect this to a 4.7 µF ceramic output filter capacitor to GND.
A2	NC	Supply voltage for analog circuits of LM3209-G3. This pin is connected to PVIN via a 36Ω resistor internally. Leave this pin floating.
B2	EN	Enable Pin. Pulling this pin higher than 1.2V enables part to function.
C2	SGND	Signal Ground for analog circuits.
D2	SW2	Switch pin for Internal Power Switches M3 and M4. Connect inductor between SW1 and SW2.
A3	PVIN	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
B3	PVIN	Power MOSFET input and power current input pin. Optional low-pass filtering may help buck and buck-boost modes for radiated EMI and noise reduction.
C3	SW1	Switch pin for Internal Power Switches M1 and M2. Connect inductor between SW1 and SW2.
D3	PGND	Power Ground for Power MOSFETs and gate drive circuitry.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

PVIN pin: Voltage to GND	−0.2V to +6.0V
EN, FB, VCON, VOUT pin: Voltage to GND	−0.2V) to (V_{IN} +0.2V) w/6.0V max.
PGND to SGND	−0.2V to +0.2V
SW1, SW2	(PGND −0.2V) to (PV_{IN} +0.2V) w/6.0V
Continuous Power Dissipation(4)	Internally Limited
Junction Temperature (T_{J-MAX})	+150°C
Storage Temperature Range	−65°C to +150°C
Maximum Lead Temperature (Soldering 10 sec.)	+260°C
ESD Rating, Human Body Model(5)(6)	2kV

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
(4) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T_J = 150°C (typ.) and disengages at T_J = 120°C (typ.).
(5) The Human body model is a 100 pF capacitor discharged through a 1.5 kΩ resistor into each pin. (MIL-STD-883 3015.7)
(6) Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper ESD handling procedure can result in damage.

OPERATING RATINGS(1)(2)

Input Voltage Range	2.7V to 5.5V
Recommended Load Current	0 to 650 mA
Junction Temperature (T_J) Range	−30°C to +125°C
Ambient Temperature (T_A) Range(3)	−30°C to +85°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to the potential at the GND pins.
(3) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be de-rated. Maximum ambient temperature (T_{A-MAX}) is dependent on the maximum operating junction temperature ($T_{J-MAX-OP}$ = 125°C), the maximum power dissipation of the device in the application (P_{D-MAX}), and the junction-to ambient thermal resistance of the part/package in the application (θ_{JA}), as given by the following equation: $T_{A-MAX} = T_{J-MAX-OP} – (\theta_{JA} \times P_{D-MAX})$.

THERMAL PROPERTIES

Junction-to-Ambient Thermal, Resistance (θ_{JA}), YZR Package	85°C/W

ELECTRICAL CHARACTERISTICS[1][2]

Limits in standard typeface are for $T_A = T_J = 25°C$. Limits in **boldface** type apply over the full operating ambient temperature range ($-30°C \le T_J = T_A \le +85°C$). Unless otherwise noted, specifications apply to the LM3209-G3 Typical Application Circuit with: PVIN = EN = 3.6V.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
$V_{FB,\ min}$	Min FB voltage	VCON = 0.2V	**0.530**	0.600	**0.670**	V
$V_{FB,\ max}$	Max FB voltage	VCON = 1.4V	**4.130**	4.200	**4.270**	V
I_Q	Quiescent current	No switching[3], VCON = 0.1V, FB = PVIN		0.8	**2.0**	mA
I_{SHDN}	Shutdown supply current	EN = 0V, VCON = 0V, SW1 = SW2 = V_{OUT} = 0V		0.02	**2**	µA
R_{DSON} PMOS	Buck PMOS switch on resistance (Small PFET)	M1, I_{SW1} = 200 mA		415		mΩ
R_{DSON} PMOS	Buck PMOS switch on resistance (Large+Small PFET)	M1, I_{SW1} = 200 mA		120	140 **165**	mΩ
R_{DSON} PMOS	Buck PMOS switch on resistance during boost operation	M1, I_{SW1} = 200 mA		80	90 **110**	mΩ
R_{DSON} NMOS	Buck and Boost NMOS switch on resistance	M2, I_{SW1} = -200 mA M4, I_{SW2} = −200 mA		215	230 **285**	mΩ
R_{DSON} PMOS	Boost PMOS switch on resistance (between SW2 and V_{OUT})	M3, I_{SW2} = 200 mA, V_{OUT} = 3.4V		90	105 **135**	mΩ
R_{DSON} NMOS	NMOS output switch on resistance (between SW2 and V_{OUT})	M5, I_{SW2} = 200 mA V_{OUT} = 0.8V		100	110 **135**	mΩ
I_{LIM_L}	Input Current Limit (Large)	Open Loop[4]	**1500**	1700	**1900**	mA
I_{LIM_S}	Input Current Limit (Small)	Open Loop[4]	**750**	850		mA
I_{SHRT}	Output Short Current	FB ≤ 0.35V		850		mA
F_{OSC}	Internal Oscillator Frequency		**2.1**	2.4	**2.7**	MHz
Gain	Internal Gain[5]	0.2V ≤ VCON ≤ 1.4V		3		V/V
I_{EN}	EN pin pull down current			5	10	µA
I_{CON}	VCON pin input current			0.02	2	µA
V_{IH}	Logic High Input Threshold for EN		**1.2**			V
V_{IL}	Logic Low Input Threshold for EN				**0.6**	V

(1) All voltages are with respect to the potential at the GND pins.
(2) Min and Max limits are verified by design, test, or statistical analysis.
(3) I_Q specified here is when the part is not switching.
(4) Current limit is built-in, fixed, and not adjustable.
(5) To calculate V_{OUT}, use the following equation: V_{OUT} = VCON × 3

Dissipation Rating Table

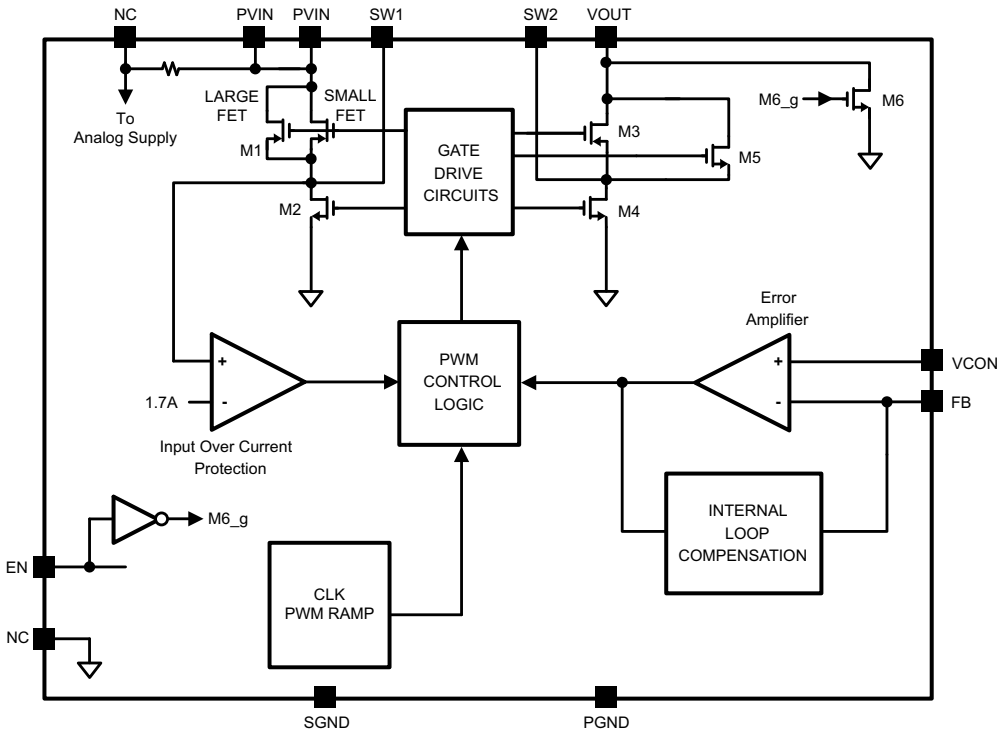
Ambient Temperature	T_A = 25°C	T_A = 55°C	T_A = 85°C
Power Dissipation	1.176 (W)	0.82 (W)	0.47 (W)

SYSTEM CHARACTERISTICS

The following spec table entries are specified by design and verifications providing the component values in the typical application circuit are used (L = 2.2 µH, DCR = 110 mΩ, MIPSZ2520D2R2/FDK; C_{IN} = 10 µF 6.3V, C1608X5R0J106K/TDK; C_{OUT} = 4.7 µF, 6.3V, ECJ1VB0J475K/Panasonic). **These parameters are not verified by production testing.** Min and Max limits in apply over the full operating ambient temperature range (−30°C ≤ T_A ≤ 85°C) and over the VIN range (= PVIN = EN) = 2.7V to 5.5V unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Units
T_{ON}	Turn on time (time for output to reach 0V→90% × 3.5V)	EN = L to H, V_{IN} = 3.7V, I_{OUT} = 0 mA		35	50	µs
T_{OFF}	Turn off time (time output to reach 3.5V→10% × 3.5V)	EN = H to L, V_{IN} = 3.7V, I_{OUT} = 0 mA		50	100	µs
I_{OUT_MAX}	Max output current	V_{IN} ≥ 3.2V, V_{OUT} = 4.2V	500			mA
D_{MAX}	Maximum Duty Cycle	Boost (% M4 on)			50	%
		Buck (% M1 on)			100	
C_{CON}	VCON input capacitance	VCON = 1V, Test frequency = 100 kHz			10	pF
V_{CON_LIN}	VCON linearity	0.2V ≤ VCON ≤ 1.4V	−70		+70	mV
V_{O_RIPPLE}	Ripple voltage	V_{IN} ≥ 3.2V, 0.6 ≤ V_{OUT} ≤ 4.2V, 0 mA ≤ I_{OUT} ≤ 430 mA, T_A = 25°C		15	50	mV
	Ripple voltage in mode transition	V_{IN} = 3.0V to 5.0V, V_{IN} = T_R = T_F = 30s 3.3V ≤ V_{OUT} ≤ 4.2V			50	mV
V_{OUT}	Output Voltage Accuracy	VCON = 0.2V, I_{OUT} = 70 mA	0.530	0.600	0.670	V
		VCON = 0.4V, I_{OUT} = 70 mA	1.130	1.200	1.270	
		VCON = 0.833V, I_{OUT} = 200 mA	2.430	2.50	2.57	
		VCON = 1.167V, I_{OUT} = 300 mA	3.431	3.50	3.57	
		VCON = 1.333V, I_{OUT} = 350 mA	3.930	4.000	4.070	
		VCON = 1.4V, I_{OUT} = 500 mA, V_{IN} ≥ 3.2V	4.13	4.20	4.27	
ΔV_{OUT}	Line Regulation	V_{IN} = 3.2V to 4.9V, V_{IN} T_R = T_F = 10 µs, V_{OUT} = 3.5V			10	mV
	Load Regulation	I_{OUT} = 0 mA to 500 mA, I_{OUT} = T_R = T_F = 1 µs, V_{IN} = 3.2V to 4.9V			20	mV
V_{CON_TR}	VCON transient response overshoot	V_{IN} = 3.2V to 4.2V, V_{OUT} = 0.8V to 4.0V, VCON Tr = Tf = 1 µs, R_{LOAD} = 11.4Ω			200	mV
	VCON transient response rise time				20	µs
	VCON transient response fall time				50	
η	Efficiency	V_{IN} = 3.7V, V_{OUT} = 1.2V, I_{OUT} = 70 mA	80	85		%
		V_{IN} = 3.7V, V_{OUT} = 2.5V, I_{OUT} = 200 mA	90	95		
		V_{IN} = 3.7V, V_{OUT} = 3.5V, I_{OUT} = 300 mA	90	95		
		V_{IN} = 3.7V, V_{OUT} = 4.1V, I_{OUT} = 350 mA	85	95		

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE CHARACTERISTICS

(V_{IN} = PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Quiescent Current vs Supply Voltage (VCON = 0.5, PVIN = VOUT = FB, No Switching)

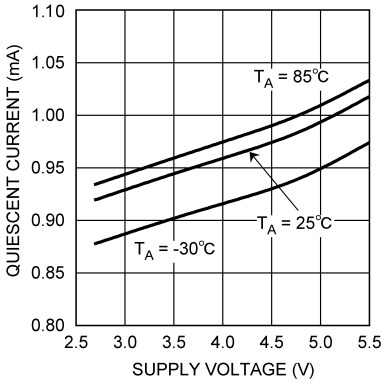


Figure 2.

Shutdown Current vs Temperature (VCON = VOUT = SW1 = SW2 = EN = 0V)

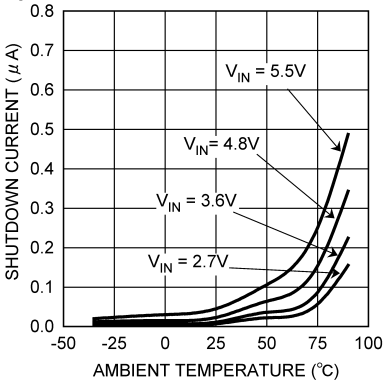


Figure 3.

Closed Loop Supply Current vs Output Voltage (No load)

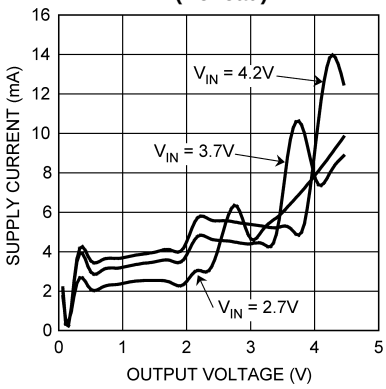


Figure 4.

Switching Frequency vs Temperature (V_{OUT} = 3.5V, I_{OUT} = 300 mA)

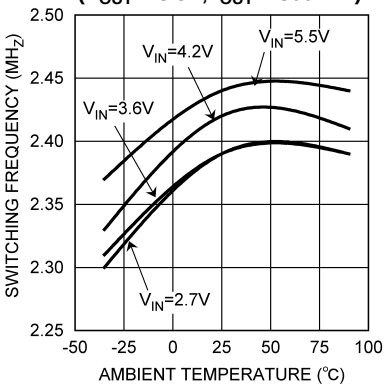


Figure 5.

Current Limit vs Temperature (Large PFET, V_{OUT} = 3.5V)

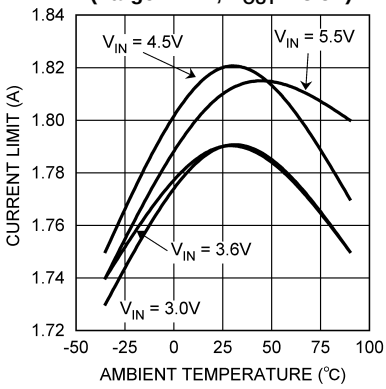


Figure 6.

Current Limit vs Temperature (Small PFET, V_{OUT} = 1.2V)

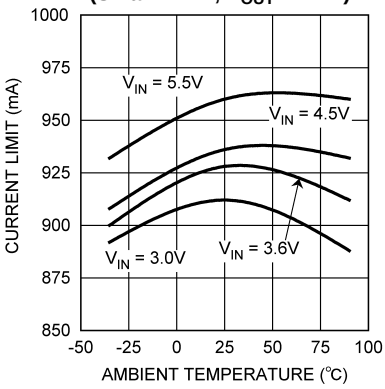


Figure 7.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(V_{IN} = PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Load Capability vs Output Voltage

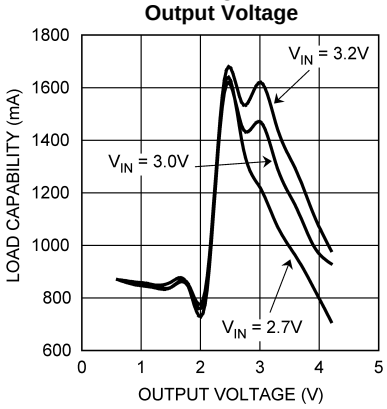


Figure 8.

VCON Voltage vs Output Voltage (No load)

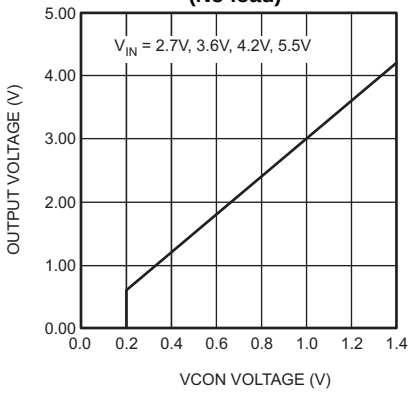


Figure 9.

EN High Threshold vs Supply Voltage

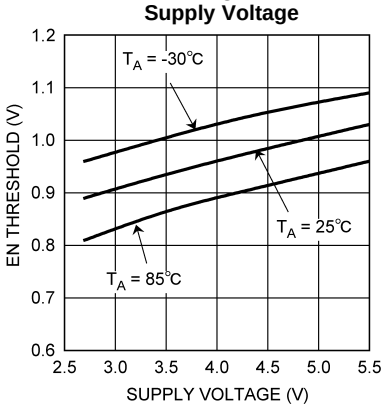


Figure 10.

Efficiency vs Output Voltage (V_{IN} = 3.7V, R_{LOAD} = 15Ω)

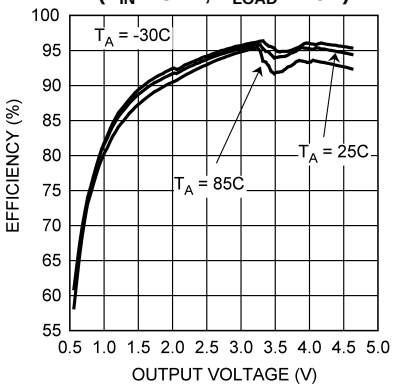


Figure 11.

Efficiency vs Output Current (V_{OUT} = 1.2V)

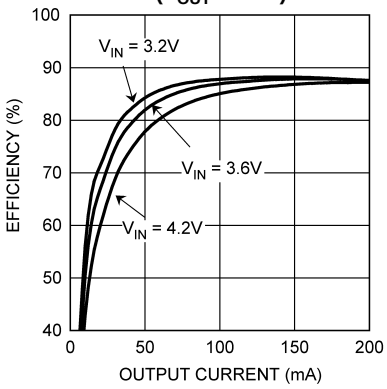


Figure 12.

Efficiency vs Output Current (V_{OUT} = 2.5V)

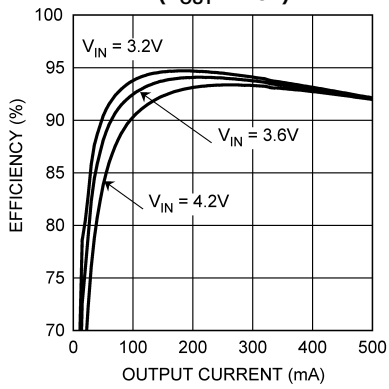


Figure 13.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(V_{IN} = PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Efficiency vs Output Current (V_{OUT} = 3.5V)

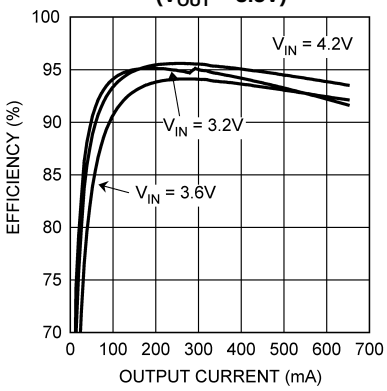


Figure 14.

Efficiency vs Output Current (V_{OUT} = 4.1V)

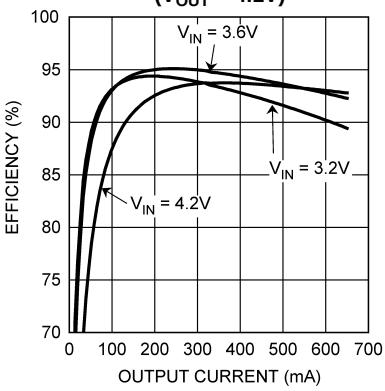


Figure 15.

R_{DSON} vs Temperature (M1 PFET, I_{SW} = 200 mA)

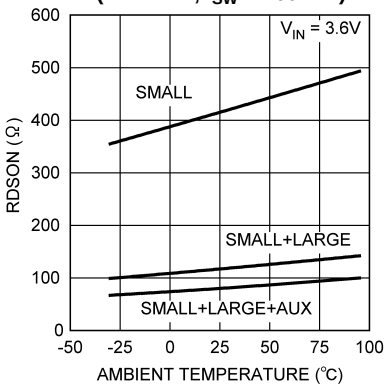


Figure 16.

R_{DSON} vs Supply Voltage (M1 Small PFET, I_{SW} = 200 mA)

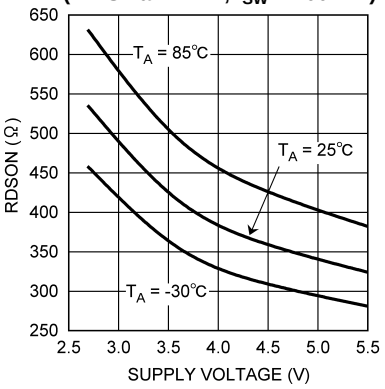


Figure 17.

R_{DSON} vs Supply Voltage (M2, M4 NFET, I_{SW} = -200 mA)

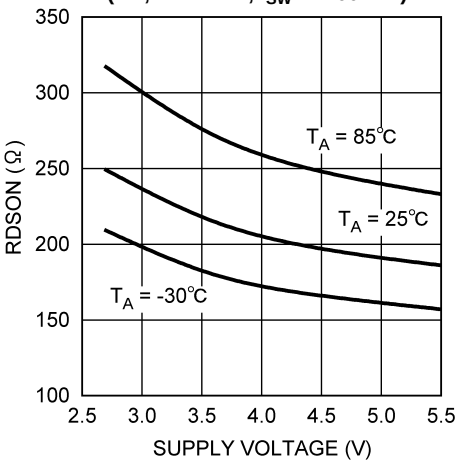


Figure 18.

R_{DSON} vs Supply Voltage (M3 and M5 FET, I_{SW} = 200 mA)

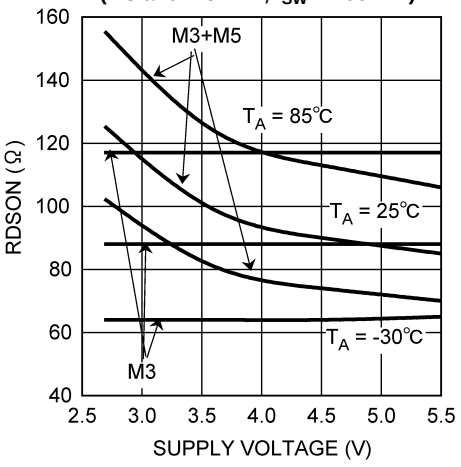


Figure 19.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(V_{IN} = PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

VCON Transient Response
(V_{IN} = 3.7V, V_{OUT} = 0.8V/4.0V, R_{LOAD} = 15Ω)

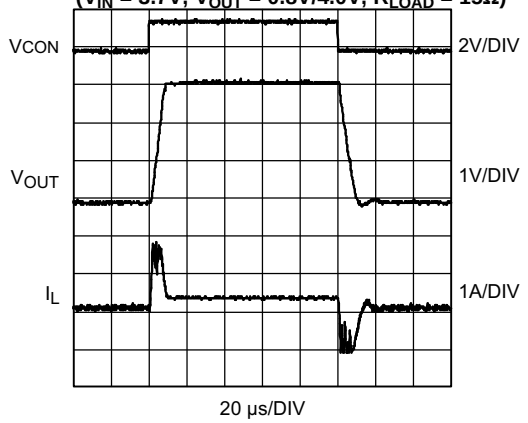


Figure 20.

Output Voltage Ripple in Buck Mode
(V_{OUT} = 1.2V, I_{OUT} = 70 mA)

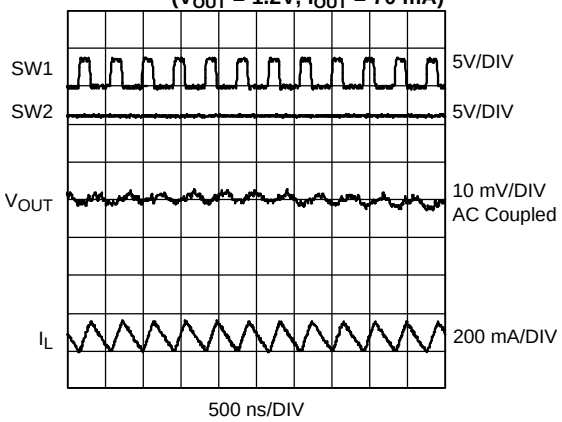


Figure 21.

Output Voltage Ripple in Buck-Boost Mode
(V_{IN} = 3.598V, V_{OUT} = 3.5V, I_{OUT} = 300 mA)

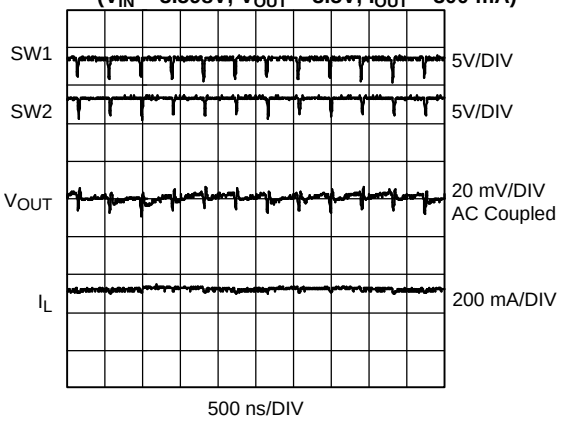


Figure 22.

Output Voltage Ripple in Boost Mode
(V_{IN} = 3.2V, V_{OUT} = 4.0V, I_{OUT} = 350 mA)

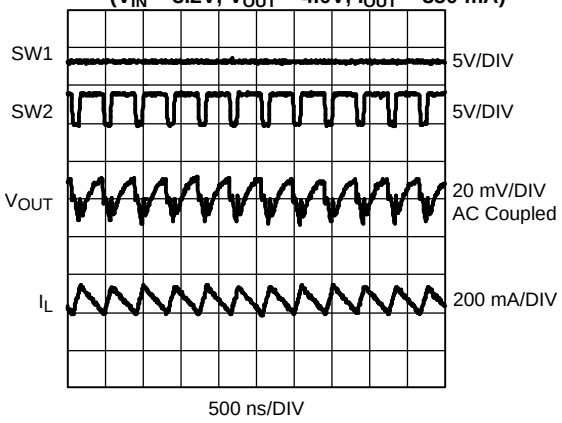


Figure 23.

Startup
(V_{OUT} = 0V to 3.5V)

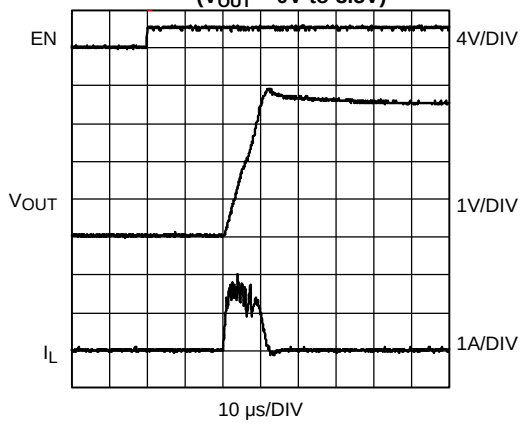


Figure 24.

Shutdown
(V_{OUT} = 3.5V to 0V)

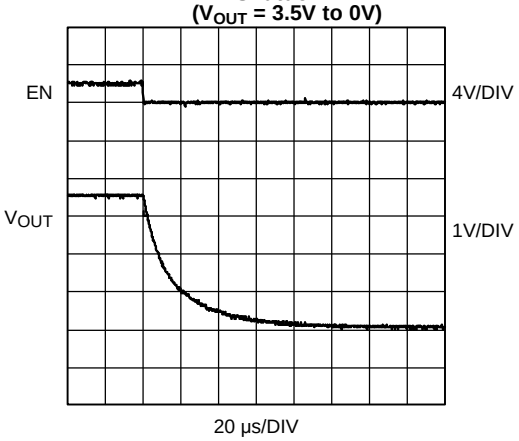


Figure 25.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

(V_{IN} = PVIN = EN = 3.6V and T_A = 25°C, unless otherwise noted)

Time Current Limit
(V_{OUT} = 2.5V to Ground shorted, R_{LOAD} = 15Ω)

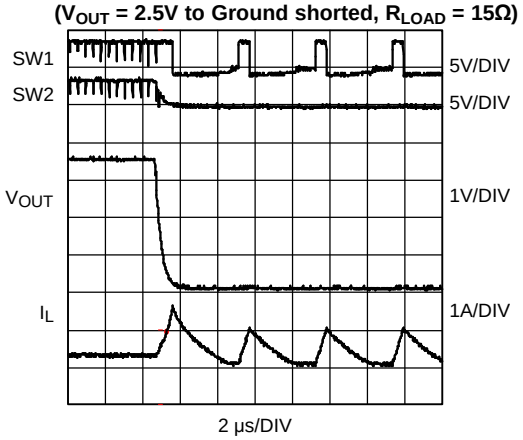


Figure 26.

Load Transient
(V_{IN} = 3.3V, V_{OUT} = 4.2V, R_{LOAD} = 11Ω/22Ω)

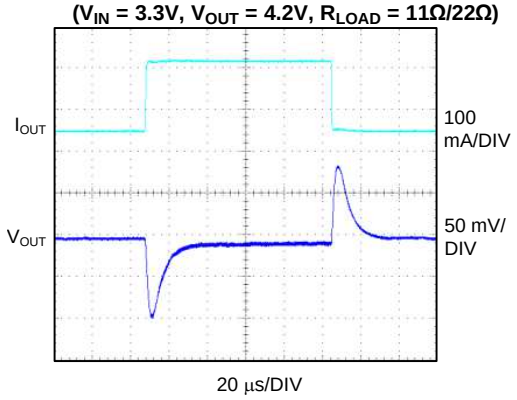


Figure 27.

Load Transient
(V_{IN} = 4.2V, V_{OUT} = 3.6V, R_{LOAD} = 11Ω/22Ω)

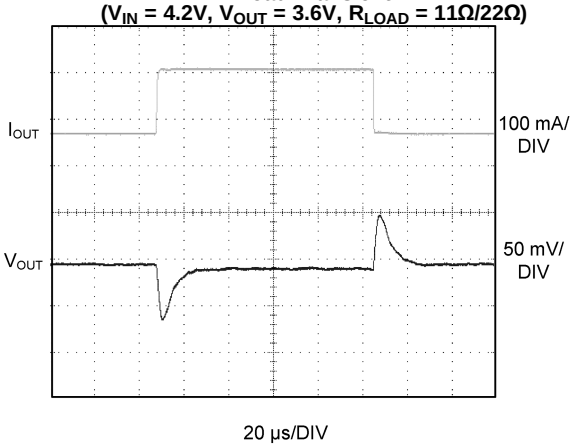


Figure 28.

Line Transient
(V_{IN} = 3.6V-4.2, V_{OUT} = 3.9V, R_{LOAD} = 11.4Ω)

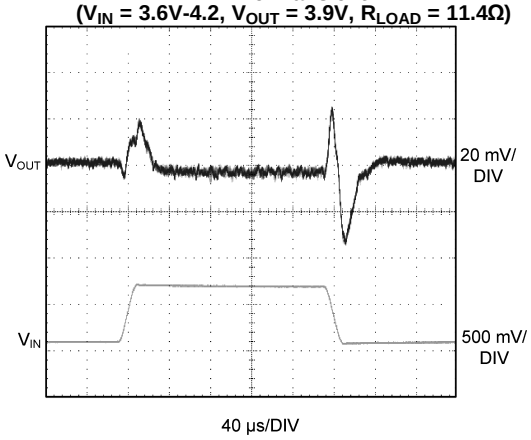


Figure 29.

Line Transient
(V_{IN} = 2.7V-3.3V, V_{OUT} = 3.9V, R_{LOAD} = 11.4Ω)

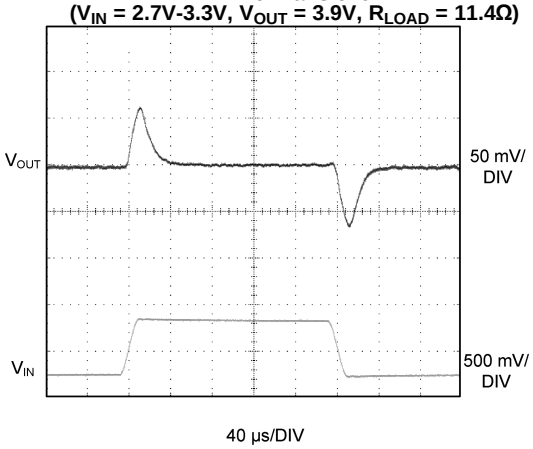


Figure 30.

OPERATION DESCRIPTION

The LM3209-G3 buck-boost converter provides high-efficiency, low-noise power for RF power amplifiers (PAs) in mobile phones, portable communicators and similar battery-powered RF devices. It is designed to allow the RF PA to operate at maximum efficiency for a wide range of power levels from a single Li-Ion battery cell. The capability of LM3209-G3 to provide an output voltage lower than as well as higher than the input battery voltage also enables the PA to operate with high linearity for a wide range of battery voltages thereby extending the usable voltage range of the battery. The converter feedback loop is internally compensated for both buck and boost operation and the architecture is such that it provides seamless transition between buck and boost mode of operation.

The efficiency of LM3209-G3 is typically around 95% for a 300 mA load with 3.5V output, 3.7V input. The LM3209-G3 has an R_{DSON} management scheme for low as well as high output voltage. This achieves high efficiency for a wide range of output voltage. The output voltage is dynamically programmable from 0.6V to 4.2V by adjusting the voltage on the control pin, VCON , without the need for external feedback resistors. The fast output voltage transient response of LM3209-G3 makes it suitable for adaptively adjusting the PA supply voltage depending on its transmitting power which prolongs battery life.

Additional features include current overload protection, output over voltage clamp and thermal overload shutdown.

The LM3209-G3 is constructed using a chip-scale 12-bump DSBGA package that offers the smallest possible size for space-critical applications such as cell phones where board area is an important design consideration. Use of high switching frequency (2.4 MHz, typ.) reduces the size of the external components. As shown in Typical Application Circuit, only three external power components are required for circuit operation. Use of the DSBGA package requires special design considerations for implementation. (See DSBGA PACKAGE ASSEMBLY AND USE in the APPLICATION INFORMATION section.) Its fine bump-pitch requires careful board design and precision assembly equipment. Use of this package is best suited for opaque-case applications, where its edges are not subjected to high-intensity ambient red or infrared light.

SHUTDOWN MODE

Setting the EN digital pin low (< 0.6V) places the LM3209-G3 in shutdown mode (0.01 µA I_{SHDN} typ.). During shutdown, the output of LM3209-G3 is pulled to ground enabling complete discharge of the output capacitor. Setting EN high (>1.2V) enables normal operation. EN should be set low to turn off the LM3209-G3 during power-up and under voltage conditions when the power supply is less than the 2.7V minimum operating voltage.

$V_{CON,ON}$

The output is disabled when VCON is below 125 mV (typ.). It is enabled when VCON is above 150 mV (typ.). The threshold has approximately 25 mV (typ.) of hysteresis.

R_{DSON} MANAGEMENT

The LM3209-G3 has a unique R_{DSON} management function to improve efficiency in low output voltage as well as high output voltage conditions. When VCON < 0.775V (typ.) the device uses only a small part of the PMOS M1 to minimize drive loss. When VCON > 0.775V, a large PMOS is also used along with the small PMOS. For RF PAs, the current consumption typically increases with its supply voltage and hence higher supply voltage for the PA also means higher current delivered to it. Adding a large PMOS for VCON > 1.124V reduces the conduction losses thereby achieving higher efficiency. The LM3209-G3 can also provide output voltages higher than the battery voltage. This boost mode of operation is typically used when the battery voltage has discharged to a low voltage that is not sufficient to provide the required linearity in the PA. A special R_{DSON} management scheme is designed for operation well into boost mode such that an auxiliary PMOS switch is also turned on along with the large and small PMOS switches. This effectively reduces the R_{DSON} of M1 to a very low value in order to keep the efficiency maximized. Since M1 conducts all the time in boost mode, reducing the R_{DSON} of M1 achieves a significant improvement in efficiency.

SUPPLY CURRENT LIMIT

A current limit feature allows the LM3209-G3 to protect itself and external components during overload conditions. In PWM mode, a 1700 mA (typ.) cycle-by-cycle current limit is normally used when VCON is above 0.775V (typ.) and an 850 mA (typ.) limit is used when VCON is below 0.775V (typ.). If an excessive load pulls the output voltage down to approximately 0.35V, then the device switches to a timed current limit mode. The current limit in this mode is 850 mA (typ.) independent of the set VCON voltage. In timed current limit mode, the internal PMOS M1 is turned off after the current limit is hit and the beginning of the next cycle is inhibited for 3.5 µs to force the inductor current to ramp down to a safe value.

REVERSE CURRENT LIMIT

Since LM3209-G3 features dynamically adjustable output voltage, the inductor current can build up to high values in either direction depending on the output voltage transient. For a low to high output voltage transient, the inductor current flows from SW1 pin to SW2 pin, and this current is limited by the current limit feature monitoring PMOS M1. For a high to low output voltage transient, the inductor current flows from SW2 pin to SW1 pin, and this current needs to be limited to protect the LM3209-G3 as well as the external components. A reverse current limit feature allows monitoring the reverse inductor current that also flows through NMOS M2. A -1.2A (typ.) cycle-by-cycle current limit is used to limit the reverse current. When the reverse current hits the reverse current limit during a PWM cycle, NMOS M2 is turned off and MOSFET M1 and M4 are turned on for the rest of that switching cycle. This allows the inductor to build current in the opposite direction thereby limiting the reverse current. It should be noted that the power MOSFET switches M3 and M4 do not have their own current limiting circuits and are dependent on the current limit operation implemented for power MOSFETs M1 and M2 to protect them. The implication of this is that any external forcing of voltage/current on SW2 pin or misuse of SW2 pin may be detrimental to the part and may damage the internal circuits.

DYNAMICALLY ADJUSTABLE OUTPUT VOLTAGE

The LM3209-G3 features dynamically adjustable output voltage which eliminates the need for external feedback resistors. The output can be set from 0.6V to 4.2V by changing the voltage on the analog VCON pin. This feature is useful in cell phone RF PA applications where peak power is needed only when the handset is far away from the base station or when data is being transmitted. In other instances, the transmitting power can be reduced. Hence the supply voltage to the PA can be reduced, promoting longer battery life. In order to adaptively adjust the supply voltage to the PA in real time in a cell phone application, the output voltage transition should be fast enough in order to meet the RF transmit signal specifications. LM3209-G3 offers ultra fast output voltage transitions without drawing very large currents from the battery supply. With a current limit of 1700 mA (typ.), the output voltage can transition from 0.8V to 4.0V in less than 20 µs with a load resistance of 11.4Ω.

SEAMLESS MODE TRANSITION

In a typical non-inverting buck-boost converter, all four power switches, M1 through M4, are switched every cycle. This operation increases MOSFET drive losses and lowers the converter efficiency. The LM3209-G3 switches only two power switches every cycle to improve converter efficiency. Hence it operates either as a buck converter or a boost converter depending upon the input and output voltage conditions. This creates a boundary between the buck and boost modes of operation. When the input battery voltage is close to the set output voltage, the converter automatically switches to four-switch operation seamlessly such that the output voltage does not see any perturbations at the mode boundary. The excellent mode transition capability of LM3209-G3 enables low noise output with the highest efficiency. Internal feedback loop compensation ensures stable operation in buck, boost, as well as the buck-boost mode transition region.

VCON OVER-VOLTAGE CLAMP

The LM3209-G3 features an internal clamp on the analog VCON pin voltage to limit the output voltage to a maximum safe value. The VCON voltage is internally switched to a reference voltage of approximately 1.6V when the VCON in voltage exceeds 1.6V. This limits the output voltage to approximately 4.8V and protects the part from over voltage stress.

THERMAL OVERLOAD PROTECTION

The LM3209-G3 has a thermal overload protection function that operates to protect itself from short-term misuse and over-load conditions. When the junction temperature exceeds approximately 150°C, the device inhibits operation. All power MOSFET switches are turned off. When the temperature drops below 120°C, normal operation resumes. Prolonged operation in thermal overload conditions may damage the device and is considered bad practice.

APPLICATION INFORMATION

SETTING THE OUTPUT VOLTAGE

The LM3209-G3 features a pin-controlled variable output voltage which eliminates the need for external feedback resistors. It can be programmed for an output voltage from 0.6V to 4.2V by setting the voltage on the VCON pin, as in the following formula.

$$V_{OUT} = 3 \times VCON \quad (1)$$

When VCON is between 0.2V and 1.4V, the output voltage will follow this formula.

Internally, VCON is clamped to avoid exceeding the maximum output voltage. When the VCON voltage is greater than 1.6V, the output voltage is regulated at approximately 4.8V.

OUTPUT CURRENT CAPABILITY

The LM3209-G3 is designed for a maximum load capability of 650 mA when $V_{IN} \geq 3.0V$ and 500 mA when $V_{IN} < 3.0V$.

Table 1. Output Voltage vs. Maximum Output Current

V_{OUT}	V_{IN}	Maximum I_{OUT}
4.2V	> 3.0V	650 mA
4.2V	≤ 3.0V	500 mA
3.6V	≥ 3.2V	1000 mA

RECOMMENDED EXTERNAL COMPONENTS

INDUCTOR SELECTION

A 2.2 µH inductor with a saturation current rating over 1900 mA and low inductance drop at the full DC bias condition is recommended for almost all applications. An inductor with a DC resistance of less than 0.1Ω and lower ESR should be used to get good efficiency for the entire output current range.

If an inductance with a lower I_{SAT} rating is used in the application, the VCON Transient Response time will be affected. The rise time of the output voltage will be increased because the inductor will saturate and cannot charge the output capacitor quickly enough. If a winding type inductor is selected, the efficiency in light load conditions may be degraded due to higher ESR losses.

Table 2. Suggested Inductors (2.2 µH)

Vendor	Part Number	Dimensions (mm)	I_{SAT} (30%)	I_{RATING}(Δ40°C)	DCR (mΩ)
FDK	MIPSZ2520D2R2 (2.2 µH)	2.5 x 2.0 x 1.0	1.5A	1.1A	110
Murata	LQH2HPN1R0NG0	2.5 x 2.0 x 1.2	1.8A	1.1A	115
Samsung	CIG22H2R2MNE	2.5 x 2.0 x 1.2	1.9A	1.6A	116

INPUT CAPACITOR SELECTION

A ceramic input capacitor of 10 µF, 6.3V or higher is sufficient for most applications. Place the input capacitor as close as possible to the PV_{IN} and PGND pins of the device. A larger value or higher voltage rating may be used to improve input filtering. Use X7R, X5R, or B types; do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered when selecting case sizes like 0603(1608), 0805(2012), or smaller profile. The input filter capacitor supplies current to the PMOS switch in the first half of each cycle and reduces the voltage ripple imposed on the input power source. A ceramic capacitor's low ESR provides the best noise filtering of input voltage spikes caused by this rapidly changing current.

OUTPUT CAPACITOR SELECTION

Use a 4.7 µF, 6.3V, X7R, X5R, or B types; do not use Y5V or F. DC bias characteristics of ceramic capacitors must be considered. DC bias characteristics vary from manufacturer to manufacturer, and DC bias curves should be requested from them as part of the capacitor selection process.

The output filter capacitor smooths out current flow from the inductor to the load, helps maintain a steady output voltage during transient load changes and reduces output voltage ripple. These capacitors must be selected with sufficiency capacitance and low ESR to perform these functions. Note that the output voltage ripple is dependent on the inductor current ripple and the Equivalent Series Resistance of the output capacitor (ESR). The ESR is frequency dependent (as well as temperature dependent); make sure the value used for calculations is at the switching frequency of the part.

Table 3. SUGGESTED CAPACITORS

Model	Vendor
10 µF for C_{IN}	
C1608X5R0J106K	TDK
4.7 µF for C_{OUT}	
ECJ1VB0J475K	Panasonic
GRM188R60J475ME84D	Murata
GRM219R61A475KE19	Murata

RECOMMENDED EXTERNAL COMPONENT COMBINATIONS FOR VCON TRANSIENT

Achieving optimum Output Voltage (VCON) Transient is expected to require both an inductor with smaller inductance degradation and an output capacitor with modest capacitance. FDK MIPSZ2520D2R2 and Panasonic ECJ1VB0J475K are one sample of the external component combination.

An inductor with a large inductance drop at high DC bias causes slower charging current to the output capacitor. An output capacitor with less capacitance drop at high voltage will cause a big overshoot. However, an output capacitor with a large capacitance drop generates bigger output voltage ripple.

DSBGA PACKAGE ASSEMBLY AND USE

Use of the DSBGA package requires specialized board layout, precision mounting and careful re-flow techniques, as detailed in Texas Instruments Application Note 1112. Refer to the section *Surface Mount Technology (SMD) Assembly Considerations*. For best results in assembly, alignment ordinals on the PC board should be used to facilitate placement of the device. The pad style used with DSBGA package must be the NSMD (non-solder mask defined) type. This means that the solder-mask opening is larger than the pad size. This prevents a lip that otherwise forms if the solder-mask and pad overlap, from holding the device off the surface of the board and interfering with mounting. See Application Note 1112 for specific instructions how to do this.

The 12-bump package used for LM3209-G3 has 300 micron solder balls and requires 10.82 mil pads for mounting on the circuit board. The trace to each pad should enter the pad with a 90° entry angle to prevent debris from being caught in deep corners. Initially, the trace to each pad should be 7 mil wide, for a section approximately 7 mil long, as a thermal relief. Then each trance should neck up or down to its optimal width. The important criterion is symmetry. This ensures the solder bumps on the LM3209-G3 re-flow evenly and that the device solders level to the board. In particular, special attention must be paid to the pads for bumps A3, B3, and D3. Because PVIN and PGND are typically connected to large copper planes, inadequate thermal relief can result in late or inadequate re-flow of these bumps.

The DSBGA package is optimized for the smallest possible size in applications with red or infrared opaque cases. Because the DSBGA package lacks the plastic encapsulation characteristic of larger devices, it is vulnerable to light. Backside metallization and/or epoxy coating, along with front-side shading by the printed circuit board, reduce this sensitivity. However, the package has exposed die edges. In particular, DSBGA devices are sensitive to light (in the red and infrared range) shining on the package's exposed die edges.

BOARD LAYOUT CONSIDERATIONS

PC board layout is an important part of DC-DC converter design. Poor board layout can disrupt the performance of a DC-DC converter and surrounding circuitry by contributing to EMI, ground bounce, and resistive voltage loss in the traces.

1. Place the LM3209-G3, inductor and filter capacitors close together and make the traces short. The traces between these components carry relatively high switching currents and act as antennas. Following this rule reduces radiated noise. Special care must be given to place the input filter capacitor very close to the PV_{IN} and PGND pins.
2. Connect the ground pins of the LM3209-G3 and filter capacitors together using a generous component-side copper fill as a pseudo-ground plane. Then connect this to the ground-plane (if one is used) with several vias. This reduces ground-plane noise by preventing the switching currents from circulating through the ground plane. It also reduces ground bounce at the LM3209-G3 by giving it a low-impedance ground connection.
3. Use wide traces between the power components and for power connections to the DC-DC converter circuit. This reduces voltage errors caused by resistive losses across the traces.
4. Route noise sensitive traces such as the voltage feedback path away from noisy traces between the power components. The voltage feedback trace must remain close to the LM3209-G3 circuit and should be routed directly from FB to V_{OUT} at the output capacitor and should be routed opposite to noisy components. This reduces EMI radiated onto the DC-DC converter's own voltage feedback trace.
5. Place noise sensitive circuitry, such as radio IF blocks, away from the DC-DC converter, CMOS digital blocks, and other noisy circuitry. Interference with noise-sensitive circuitry in the system can be reduced through distance.

In mobile phones, for example, a common practice is to place the DC-DC converter on one corner of the board, arrange the CMOS digital circuitry around it (since this also generates noise), and then place sensitive preamplifiers and IF stages on the diagonally opposing corner. Often, the sensitive circuitry is shielded with a metal pan and power to it is post-regulated to reduce conducted noise, using low-dropout linear regulators.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3209TLE-G3/NOPB	ACTIVE	DSBGA	YZR	12	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	09G3	Samples
LM3209TLX-G3/NOPB	ACTIVE	DSBGA	YZR	12	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM	-30 to 85	09G3	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

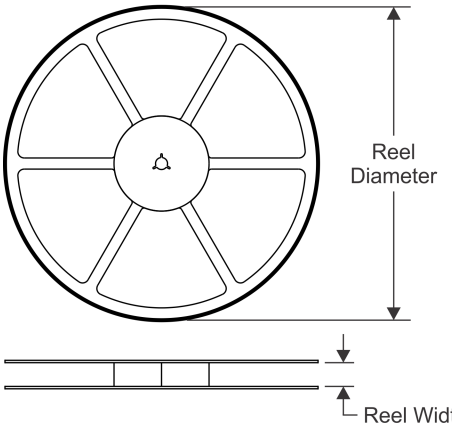
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

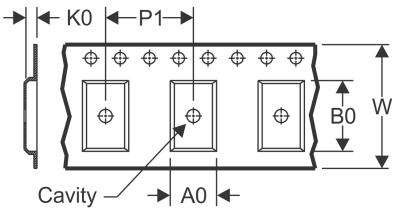
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

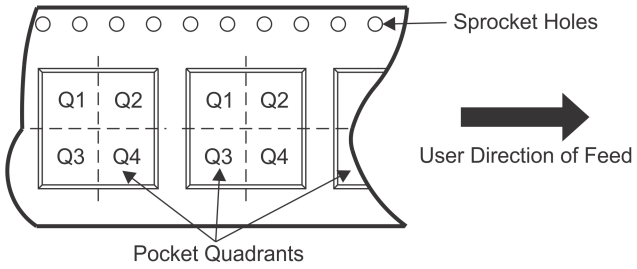


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

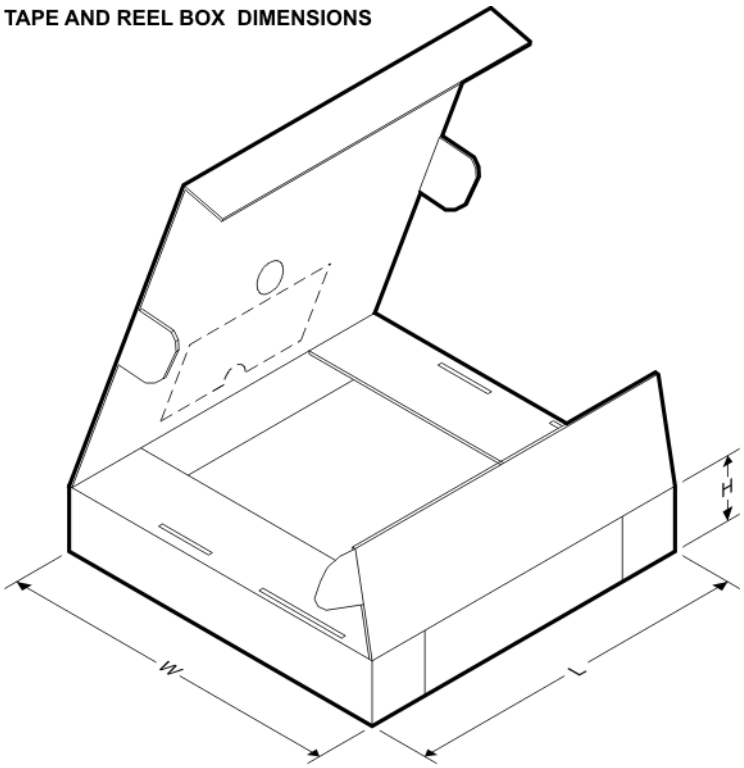
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3209TLE-G3/NOPB	DSBGA	YZR	12	250	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1
LM3209TLX-G3/NOPB	DSBGA	YZR	12	3000	178.0	8.4	2.18	2.69	0.76	4.0	8.0	Q1

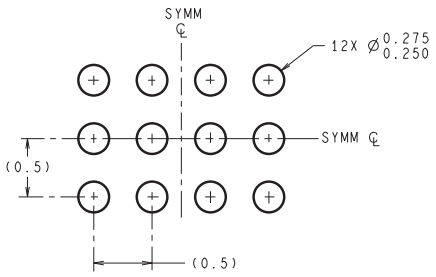
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

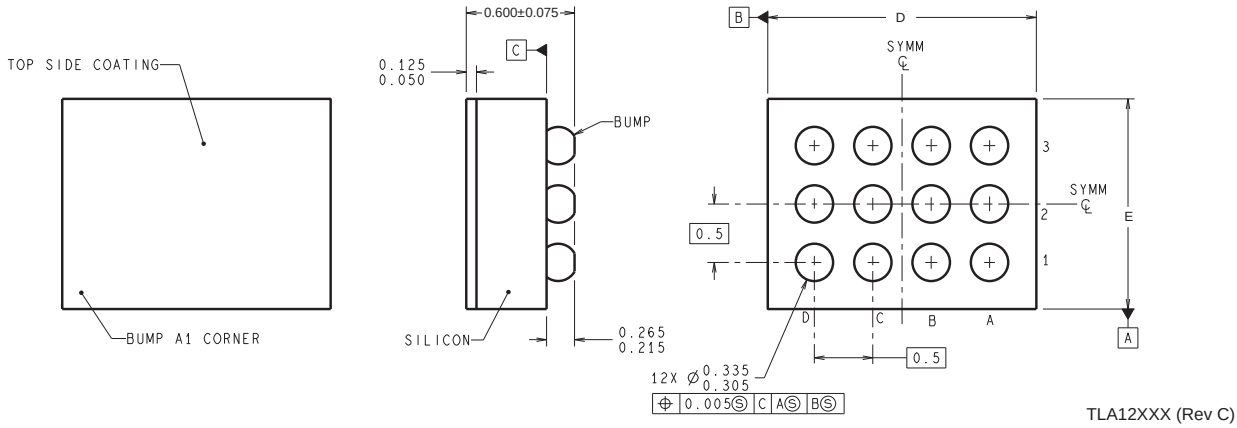
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3209TLE-G3/NOPB	DSBGA	YZR	12	250	210.0	185.0	35.0
LM3209TLX-G3/NOPB	DSBGA	YZR	12	3000	210.0	185.0	35.0

YZR0012



DIMENSIONS ARE IN MILLIMETERS
DIMENSIONS IN ( ) FOR REFERENCE ONLY

LAND PATTERN RECOMMENDATION



TLA12XXX (Rev C)

D: Max = 2.529 mm, Min =2.469 mm

E: Max = 2.022 mm, Min =1.961 mm

4215049/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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